

FEATURES

Latch-up proof
3.5 pF off source capacitance
Off drain capacitance
ADG5206: 64 pF
ADG5207: 33 pF
0.35 pC typical charge injection
 ± 0.02 nA on channel leakage
Low on resistance: 155 Ω typical
 ± 9 V to ± 22 V dual-supply operation
9 V to 40 V single-supply operation
 V_{SS} to V_{DD} analog signal range
Human body model (HBM) ESD rating
ADG5206: 8 kV all pins
ADG5207: 8 kV I/O port to supplies

APPLICATIONS

Automatic test equipment
Data acquisition
Instrumentation
Avionics
Battery monitoring
Communication systems

GENERAL DESCRIPTION

The **ADG5206** and **ADG5207** are monolithic CMOS analog multiplexers comprising 16 single channels and 8 differential channels, respectively. The **ADG5206** switches one of sixteen inputs to a common output, as determined by the 4-bit binary address lines, A0, A1, A2, and A3. The **ADG5207** switches one of eight differential inputs to a common differential output, as determined by the 3-bit binary address lines, A0, A1, and A2.

An EN input on both devices enables or disables the device. When EN is low, the device is disabled and all channels switch off. The ultralow capacitance and charge injection of these switches make them ideal solutions for data acquisition and sample-and-hold applications, where low glitch and fast settling are required. Fast switching speed coupled with high signal bandwidth make these devices suitable for video signal switching.

Each switch conducts equally well in both directions when on, and each switch has an input signal range that extends to the power supplies. In the off condition, signal levels up to the supplies are blocked.

FUNCTIONAL BLOCK DIAGRAMS

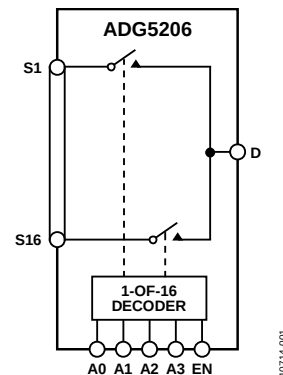


Figure 1.

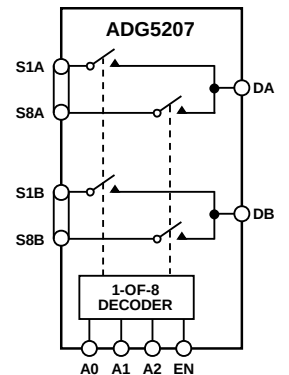


Figure 2.

The **ADG5206/ADG5207** do not have V_L pins; instead, an on-chip voltage generator generates the logic power supply internally.

PRODUCT HIGHLIGHTS

1. Trench Isolation Guards Against Latch-Up. A dielectric trench separates the P and N channel transistors to prevent latch-up even under severe overvoltage conditions.
2. Optimal switch design for low charge injection, low switch capacitance, and low leakage currents.
3. The **ADG5206** achieves 8 kV HBM ESD specification on all external pins, while the **ADG5207** achieves 8 kV on the I/O port to supply pins, 2 kV on the I/O port to I/O port pins, and 8 kV on all other pins.
4. Dual-Supply Operation. For applications where the analog signal is bipolar, the **ADG5206/ADG5207** can be operated from dual supplies of up to ± 22 V.
5. Single-Supply Operation. For applications where the analog signal is unipolar, the **ADG5206/ADG5207** can be operated from a single rail power supply of up to 40 V.

Rev. A

Document Feedback

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REVISION HISTORY

5/13—Rev. 0 to Rev. A

Added 32-Lead LFCSP	Universal
Changes to Features Section and Product Highlights Section	1
Moved Continuous Current per Channel, Sx, D, or Dx Section, Table 5, and Table 6	10
Changes to Table 7	11
Changes to Figure 3	12
Changes to Figure 5	13
Changes to Figure 30, Figure 32, and Figure 33	22

7/12—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

$V_{DD} = +15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	−40°C to +60°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range				V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	155				Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -1\text{ mA}$; see Figure 32
	200	225	250	285	Ω max	$V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$
On Resistance Match Between Channels, ΔR_{ON}	4				Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -1\text{ mA}$
	12	13	14	15	Ω max	
On Resistance Flatness, $R_{FLAT(ON)}$	48				Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -1\text{ mA}$
	65	73	80	90	Ω max	
LEAKAGE CURRENTS						
Source Off Leakage, I_S (Off)	±0.005				nA typ	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$ $V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$; see Figure 33
	±0.1	±0.15	±0.2	±0.4	nA max	
Match Between Channels, Δ Leakage, I_S (Off) ¹	0.01			0.015	nA typ	$V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$
Drain Off Leakage, I_D (Off)						$V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$; see Figure 33
ADG5206	±0.02				nA typ	
	±0.1	±0.25	±0.6	±3.3	nA max	
ADG5207	±0.02				nA typ	
	±0.1	±0.25	±0.4	±1.7	nA max	
Match Between Channels, Δ Leakage, I_D (Off), ADG5207 Only	0.015			0.015	nA typ	$V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$
Channel On Leakage, I_D (On), I_S (On)						$V_S = V_D = \pm 10\text{ V}$; see Figure 34
ADG5206	±0.02				nA typ	
	±0.1	±0.25	±0.6	±3.3	nA max	
ADG5207	±0.02				nA typ	
	±0.1	±0.2	±0.4	±1.7	nA max	
Match Between Channels, Δ Leakage, I_D (On), I_S (On) ²	0.01			0.03	nA typ	$V_S = V_D = \pm 10\text{ V}$
DIGITAL INPUTS						
Input High Voltage, V_{INH}				2.0	V min	
Input Low Voltage, V_{INL}				0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002				μA typ	$V_{IN} = V_{GND}$ or V_{DD}
				±0.1	μA max	
Digital Input Capacitance, C_{IN}	3				pF typ	
DYNAMIC CHARACTERISTICS³						
Transition Time, $t_{TRANSITION}$	200				ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	260	300	320	360	ns max	$V_S = 10\text{ V}$; see Figure 35
t_{ON} (EN)	180				ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	245	260	270	285	ns max	$V_S = 10\text{ V}$; see Figure 36
t_{OFF} (EN)	140				ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	200	220	240	270	ns max	$V_S = 10\text{ V}$; see Figure 36
Break-Before-Make Time Delay, t_D	85				ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
				27	ns min	$V_{S1} = V_{S2} = 10\text{ V}$; see Figure 37

Parameter	25°C	–40°C to +60°C	–40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/Comments
Charge Injection, Q_{INJ}	0.35				pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 38
Off Isolation	± 1.8 –90			± 2	pC typ dB typ	$V_S = \pm 10\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 39
Channel-to-Channel Crosstalk	–76				dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 40
–3 dB Bandwidth						$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 41
ADG5206	60				MHz typ	
ADG5207	140				MHz typ	
Insertion Loss	6.4				dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 41
C_S (Off)	3.5				pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
C_D (Off)						
ADG5206	64				pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
ADG5207	33				pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
C_D (On), C_S (On)						
ADG5206	68				pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
ADG5207	36				pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
POWER REQUIREMENTS						$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$
I_{DD}	45 55			70	$\mu\text{A typ}$ $\mu\text{A max}$	Digital inputs = 0 V or V_{DD}
I_{SS}	0.001			1	$\mu\text{A typ}$ $\mu\text{A max}$	Digital inputs = 0 V or V_{DD}
V_{DD}/V_{SS}				$\pm 9/\pm 22$	V min/V max	GND = 0 V

¹ The off channel leakage delta is calculated using the maximum of $V_S = +10\text{ V}$ and $V_D = -10\text{ V}$, or $V_S = -10\text{ V}$ and $V_D = +10\text{ V}$.

² The on channel leakage delta is calculated using the maximum of $V_S = V_D = +10\text{ V}$, or $V_S = V_D = -10\text{ V}$.

³ Guaranteed by design; not subject to production test.

±20 V DUAL SUPPLY

$V_{DD} = +20\text{ V} \pm 10\%$, $V_{SS} = -20\text{ V} \pm 10\%$, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	–40°C to +60°C	–40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range				V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	130				Ω typ	$V_S = \pm 15\text{ V}$, $I_S = -1\text{ mA}$; see Figure 32
	160	180	200	230	Ω max	$V_{DD} = +18\text{ V}$, $V_{SS} = -18\text{ V}$
On-Resistance Match Between Channels, ΔR_{ON}	4				Ω typ	$V_S = \pm 15\text{ V}$, $I_S = -1\text{ mA}$
	12	13	14	15	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	35				Ω typ	$V_S = \pm 15\text{ V}$, $I_S = -1\text{ mA}$
	50	58	65	75	Ω max	

Parameter	25°C	−40°C to +60°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
LEAKAGE CURRENTS						
Source Off Leakage, I _S (Off)	±0.005				nA typ	V _{DD} = +22 V, V _{SS} = −22 V V _S = ±15 V, V _D = ∓ 15 V; see Figure 33
Match Between Channels, ΔLeakage, I _S (Off) ¹	±0.1 0.01	±0.15	±0.2	±0.4 0.015	nA max nA typ	V _S = ±15 V, V _D = ∓ 15 V; see Figure 33
Drain Off Leakage, I _D (Off)						
ADG5206	±0.02				nA typ	V _S = V _D = ±15 V; see Figure 34
ADG5207	±0.1 ±0.02	±0.25	±0.6	±3.3	nA max nA typ	
Match Between Channels, ΔLeakage, I _D (Off), ADG5207 Only	±0.1 0.015	±0.25	±0.4	±1.7 0.015	nA max nA typ	
Channel On Leakage, I _D (On), I _S (On)						
ADG5206	±0.02				nA typ	
ADG5207	±0.1 ±0.02	±0.25	±0.6	±3.3	nA max nA typ	
Match Between Channels, ΔLeakage, I _D (On), I _S (On) ²	±0.1 0.01	±0.2	±0.4	±1.7 0.03	nA max nA typ	
DIGITAL INPUTS						
Input High Voltage, V _{INH}				2.0	V min	V _{IN} = V _{GND} or V _{DD}
Input Low Voltage, V _{INL}				0.8	V max	
Input Current, I _{INL} or I _{INH}	±0.002			±0.1	μA typ μA max	
Digital Input Capacitance, C _{IN}	3				pF typ	
DYNAMIC CHARACTERISTICS ³						
Transition Time, t _{TRANSITION}	185				ns typ	R _L = 300 Ω, C _L = 35 pF
t _{ON} (EN)	240 175	270	290	320	ns max ns typ	V _S = 10 V; see Figure 35 R _L = 300 Ω, C _L = 35 pF
t _{OFF} (EN)	230 135	245	255	270	ns max ns typ	V _S = 10 V; see Figure 36 R _L = 300 Ω, C _L = 35 pF
Break-Before-Make Time Delay, t _D	185 75	205	220	245	ns max ns typ	V _S = 10 V; see Figure 36 R _L = 300 Ω, C _L = 35 pF
Charge Injection, Q _{INJ}	0.45			27	ns min pC typ	V _{S1} = V _{S2} = 10 V; see Figure 37 V _S = 0 V, R _S = 0 Ω, C _L = 1 nF; see Figure 38
Off Isolation	±4 −90			±4	pC typ dB typ	V _S = ±10 V, R _S = 0 Ω, C _L = 1 nF R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 39
Channel-to-Channel Crosstalk	−76				dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 40
−3 dB Bandwidth						R _L = 50 Ω, C _L = 5 pF; see Figure 41
ADG5206	65				MHz typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 41
ADG5207	145				MHz typ	
Insertion Loss	5.6				dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 41
C _S (Off)	3.3				pF typ	V _S = 0 V, f = 1 MHz

Parameter	25°C	−40°C to +60°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
C _D (Off)						
ADG5206	62				pF typ	V _S = 0 V, f = 1 MHz
ADG5207	32				pF typ	V _S = 0 V, f = 1 MHz
C _D (On), C _S (On)						
ADG5206	67				pF typ	V _S = 0 V, f = 1 MHz
ADG5207	35				pF typ	V _S = 0 V, f = 1 MHz
POWER REQUIREMENTS						V _{DD} = +22 V, V _{SS} = −22 V
I _{DD}	50				μA typ	Digital inputs = 0 V or V _{DD}
	70			110	μA max	
I _{SS}	0.001				μA typ	Digital inputs = 0 V or V _{DD}
				1	μA max	
V _{DD} /V _{SS}				±9/±22	V min/V max	GND = 0 V

¹ The off channel leakage delta is calculated using the maximum of V_S = +15 V and V_D = −15 V, or V_S = −15 V and V_D = +15 V.

² The on channel leakage delta is calculated using the maximum of V_S = V_D = +15 V, or V_S = V_D = −15 V.

³ Guaranteed by design; not subject to production test.

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	25°C	−40°C to +60°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range				0 V to V _{DD}	V	
On Resistance, R _{ON}	350				Ω typ	V _S = 0 V to 10 V, I _S = −1 mA; see Figure 32
	500	560	610	700	Ω max	V _{DD} = 10.8 V, V _{SS} = 0 V
On-Resistance Match Between Channels, ΔR _{ON}	5				Ω typ	V _S = 0 V to 10 V, I _S = −1 mA
	20	21	22	24	Ω max	
On-Resistance Flatness, R _{FLAT} (ON)	170				Ω typ	V _S = 0 V to 10 V, I _S = −1 mA
	280	310	335	370	Ω max	
LEAKAGE CURRENTS						V _{DD} = +13.2 V, V _{SS} = 0 V
Source Off Leakage, I _S (Off)	±0.005				nA typ	V _S = 1 V/10 V, V _D = 10 V/1 V; see Figure 33
	±0.1	±0.15	±0.2	±0.4	nA max	
Match Between Channels, ΔLeakage, I _S (Off) ¹	0.01			0.015	nA typ	
Drain Off Leakage, I _D (Off)						V _S = 1 V/10 V, V _D = 1 V/10 V; see Figure 33
ADG5206	±0.02				nA typ	
	±0.1	±0.25	±0.6	±3.3	nA max	
ADG5207	±0.02				nA typ	
	±0.1	±0.25	±0.4	±1.7	nA max	
Match Between Channels, ΔLeakage, I _D (Off), ADG5207 Only	0.015			0.015	nA typ	
Channel On Leakage, I _D (On), I _S (On)						V _S = V _D = 1 V/10 V; see Figure 34
ADG5206	±0.02				nA typ	
	±0.1	±0.25	±0.6	±3.3	nA max	
ADG5207	±0.02				nA typ	
	±0.1	±0.2	±0.4	±1.7	nA max	
Match Between Channels, ΔLeakage, I _D (On), I _S (On) ²	0.01			0.03	nA typ	

Parameter	25°C	–40°C to +60°C	–40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/Comments
DIGITAL INPUTS						
Input High Voltage, V_{INH}				2.0	V min	$V_{IN} = V_{GND}$ or V_{DD}
Input Low Voltage, V_{INL}				0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			±0.1	μA typ μA max	
Digital Input Capacitance, C_{IN}	3				pF typ	
DYNAMIC CHARACTERISTICS ³						
Transition Time, $t_{TRANSITION}$	290				ns typ	$R_L = 300\ \Omega$, $C_L = 35\ \text{pF}$
	290	440	480	550	ns max	$V_S = 8\ \text{V}$; see Figure 35
t_{ON} (EN)	230				ns typ	$R_L = 300\ \Omega$, $C_L = 35\ \text{pF}$
	290	320	340	370	ns max	$V_S = 8\ \text{V}$; see Figure 36
t_{OFF} (EN)	230				ns typ	$R_L = 300\ \Omega$, $C_L = 35\ \text{pF}$
	315	360	390	450	ns max	$V_S = 8\ \text{V}$; see Figure 36
Break-Before-Make Time Delay, t_D	170				ns typ	$R_L = 300\ \Omega$, $C_L = 35\ \text{pF}$
				45	ns min	$V_{S1} = V_{S2} = 8\ \text{V}$; see Figure 37
Charge Injection, Q_{INJ}	0.25				pC typ	$V_S = 6\ \text{V}$, $R_S = 0\ \Omega$, $C_L = 1\ \text{nF}$; see Figure 38
	±0.6			±0.7	pC typ	$V_S = 0\ \text{V}$ to $10\ \text{V}$, $R_S = 0\ \Omega$, $C_L = 1\ \text{nF}$
Off Isolation	–90				dB typ	$R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$, $f = 1\ \text{MHz}$; see Figure 39
Channel-to-Channel Crosstalk	–76				dB typ	$R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$, $f = 1\ \text{MHz}$; see Figure 40
–3 dB Bandwidth						$R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$; see Figure 41
ADG5206	50				MHz typ	
ADG5207	105				MHz typ	
Insertion Loss	8.55				dB typ	$R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$, $f = 1\ \text{MHz}$; see Figure 41
C_S (Off)	3.6				pF typ	$V_S = 6\ \text{V}$, $f = 1\ \text{MHz}$
C_D (Off)						
ADG5206	71				pF typ	$V_S = 6\ \text{V}$, $f = 1\ \text{MHz}$
ADG5207	36				pF typ	$V_S = 6\ \text{V}$, $f = 1\ \text{MHz}$
C_D (On), C_S (On)						
ADG5206	75				pF typ	$V_S = 6\ \text{V}$, $f = 1\ \text{MHz}$
ADG5207	40				pF typ	$V_S = 6\ \text{V}$, $f = 1\ \text{MHz}$
POWER REQUIREMENTS						
I_{DD}	40				μA typ	$V_{DD} = 13.2\ \text{V}$
	50			65	μA max	Digital inputs = 0 V or V_{DD}
V_{DD}				9/40	V min/V max	$GND = 0\ \text{V}$, $V_{SS} = 0\ \text{V}$

¹ The off channel leakage delta is calculated using the maximum of $V_S = 1\ \text{V}$ and $V_D = 10\ \text{V}$, or $V_S = 10\ \text{V}$ and $V_D = 1\ \text{V}$.

² The on channel leakage delta is calculated using the maximum of $V_S = V_D = 1\ \text{V}$, or $V_S = V_D = 10\ \text{V}$.

³ Guaranteed by design; not subject to production test.

36 V SINGLE SUPPLY

$V_{DD} = 36\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 4.

Parameter	25°C	−40°C to +60°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range				0 V to V _{DD}	V	V _S = 0 V to 30 V, I _S = −1 mA; see Figure 32
On Resistance, R _{ON}	140				Ω typ	
	170	195	215	245	Ω max	V _{DD} = 32.4 V, V _{SS} = 0 V V _S = 0 V to 30 V, I _S = −1 mA
On-Resistance Match Between Channels, ΔR _{ON}	4				Ω typ	
	12	13	14	15	Ω max	V _S = 0 V to 30 V, I _S = −1 mA
On-Resistance Flatness, R _{FLAT} (ON)	40				Ω typ	
	55	63	70	80	Ω max	
LEAKAGE CURRENTS						
Source Off Leakage, I _S (Off)	±0.005				nA typ	V _{DD} = 39.6 V, V _{SS} = 0 V V _S = 1 V/30 V, V _D = 30 V/1 V; see Figure 33
	±0.1	±0.15	±0.2	±0.4	nA max	
Match Between Channels, ΔLeakage, I _S (Off) ¹	0.01			0.015	nA typ	V _S = 1 V/30 V, V _D = 30 V/1 V; see Figure 33
Drain Off Leakage, I _D (Off)						
ADG5206	±0.02				nA typ	V _S = 1 V/30 V, V _D = 30 V/1 V; see Figure 33
	±0.1	±0.25	±0.6	±3.3	nA max	
ADG5207	±0.02				nA typ	V _S = 1 V/30 V, V _D = 30 V/1 V; see Figure 33
	±0.1	±0.25	±0.4	±1.7	nA max	
Match Between Channels, ΔLeakage, I _D (Off), ADG5207 Only	0.015			0.015	nA typ	V _S = V _D = 1 V/30 V; see Figure 34
Channel On Leakage, I _D (On), I _S (On)						
ADG5206	±0.02				nA typ	V _S = V _D = 1 V/30 V; see Figure 34
	±0.1	±0.25	±0.6	±3.3	nA max	
ADG5207	±0.02				nA typ	V _S = V _D = 1 V/30 V; see Figure 34
	±0.1	±0.2	±0.4	±1.7	nA max	
Match Between Channels, ΔLeakage, I _D (On), I _S (On) ²	0.01			0.03	nA typ	
DIGITAL INPUTS						
Input High Voltage, V _{INH}				2.0	V min	V _{IN} = V _{GND} or V _{DD}
Input Low Voltage, V _{INL}				0.8	V max	
Input Current, I _{INL} or I _{INH}	0.002				μA typ	
				±0.1	μA max	
Digital Input Capacitance, C _{IN}	3				pF typ	
DYNAMIC CHARACTERISTICS ³						
Transition Time, t _{TRANSITION}	225				ns typ	R _L = 300 Ω, C _L = 35 pF V _S = 18 V; see Figure 35
	290	310	320	350	ns max	
t _{ON} (EN)	215				ns typ	R _L = 300 Ω, C _L = 35 pF V _S = 18 V; see Figure 36
	265	285	285	295	ns max	
t _{OFF} (EN)	170				ns typ	R _L = 300 Ω, C _L = 35 pF V _S = 18 V; see Figure 36
	215	230	245	270	ns max	
Break-Before-Make Time Delay, t _D	90				ns typ	R _L = 300 Ω, C _L = 35 pF V _{S1} = V _{S2} = 18 V; see Figure 37
				28	ns min	
Charge Injection, Q _{INJ}	0.7				pC typ	V _S = 18 V, R _S = 0 Ω, C _L = 1 nF; see Figure 38
	±3			±3	pC typ	
						V _S = 0 V to 30 V, R _S = 0 Ω, C _L = 1 nF

Parameter	25°C	–40°C to +60°C	–40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/Comments
Off Isolation	–90				dB typ	$R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$, $f = 1\ \text{MHz}$; see Figure 39
Channel-to-Channel Crosstalk	–76				dB typ	$R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$, $f = 1\ \text{MHz}$; see Figure 40
–3 dB Bandwidth						$R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$; see Figure 41
ADG5206	55				MHz typ	
ADG5207	115				MHz typ	
Insertion Loss	5.65				dB typ	$R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$, $f = 1\ \text{MHz}$; see Figure 41
C_S (Off)	3.4				pF typ	$V_S = 18\ \text{V}$, $f = 1\ \text{MHz}$
C_D (Off)						
ADG5206	62				pF typ	$V_S = 18\ \text{V}$, $f = 1\ \text{MHz}$
ADG5207	32				pF typ	$V_S = 18\ \text{V}$, $f = 1\ \text{MHz}$
C_D (On), C_S (On)						
ADG5206	66				pF typ	$V_S = 18\ \text{V}$, $f = 1\ \text{MHz}$
ADG5207	35				pF typ	$V_S = 18\ \text{V}$, $f = 1\ \text{MHz}$
POWER REQUIREMENTS						$V_{DD} = 3.9.6\ \text{V}$
I_{DD}	80				$\mu\text{A typ}$	Digital inputs = 0 V or V_{DD}
	100			130	$\mu\text{A max}$	
V_{DD}				9/40	V min/V max	GND = 0 V, $V_{SS} = 0\ \text{V}$

¹ The off channel leakage delta is calculated using the maximum of $V_S = 1\ \text{V}$ and $V_D = 30\ \text{V}$, or $V_S = 30\ \text{V}$ and $V_D = 1\ \text{V}$.

² The on channel leakage delta is calculated using the maximum of $V_S = V_D = 1\ \text{V}$, or $V_S = V_D = 30\ \text{V}$.

³ Guaranteed by design; not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, Sx, D, OR Dx**Table 5. ADG5206**

Parameter	25°C	60°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR D					
$V_{DD} = +15\text{ V}$, $V_{SS} = -15\text{ V}$					
TSSOP ($\theta_{JA} = 67.7^\circ\text{C/W}$)	44	32	23	12	mA maximum
LFCSP ($\theta_{JA} = 27.27^\circ\text{C/W}$)	62	42	28	13	mA maximum
$V_{DD} = +20\text{ V}$, $V_{SS} = -20\text{ V}$					
TSSOP ($\theta_{JA} = 67.7^\circ\text{C/W}$)	47	33	24	12	mA maximum
LFCSP ($\theta_{JA} = 27.27^\circ\text{C/W}$)	66	44	29	13	mA maximum
$V_{DD} = 12\text{ V}$, $V_{SS} = 0\text{ V}$					
TSSOP ($\theta_{JA} = 67.7^\circ\text{C/W}$)	31	24	19	11	mA maximum
LFCSP ($\theta_{JA} = 27.27^\circ\text{C/W}$)	45	33	24	12	mA maximum
$V_{DD} = 36\text{ V}$, $V_{SS} = 0\text{ V}$					
TSSOP ($\theta_{JA} = 67.7^\circ\text{C/W}$)	46	33	24	12	mA maximum
LFCSP ($\theta_{JA} = 27.27^\circ\text{C/W}$)	65	43	28	13	mA maximum

Table 6. ADG5207

Parameter	25°C	60°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR Dx					
$V_{DD} = +15\text{ V}$, $V_{SS} = -15\text{ V}$					
TSSOP ($\theta_{JA} = 67.7^\circ\text{C/W}$)	33	25	19	11	mA maximum
LFCSP ($\theta_{JA} = 27.27^\circ\text{C/W}$)	48	34	24	12	mA maximum
$V_{DD} = +20\text{ V}$, $V_{SS} = -20\text{ V}$					
TSSOP ($\theta_{JA} = 67.7^\circ\text{C/W}$)	35	27	20	11	mA maximum
LFCSP ($\theta_{JA} = 27.27^\circ\text{C/W}$)	51	36	25	12	mA maximum
$V_{DD} = 12\text{ V}$, $V_{SS} = 0\text{ V}$					
TSSOP ($\theta_{JA} = 67.7^\circ\text{C/W}$)	23	19	15	12	mA maximum
LFCSP ($\theta_{JA} = 27.27^\circ\text{C/W}$)	34	26	20	12	mA maximum
$V_{DD} = 36\text{ V}$, $V_{SS} = 0\text{ V}$					
TSSOP ($\theta_{JA} = 67.7^\circ\text{C/W}$)	34	26	20	11	mA maximum
LFCSP ($\theta_{JA} = 27.27^\circ\text{C/W}$)	50	35	25	12	mA maximum

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 7.

Parameter	Rating
V_{DD} to V_{SS}	48 V
V_{DD} to GND	−0.3 V to +48 V
V_{SS} to GND	+0.3 V to −48 V
Analog Inputs ¹	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Digital Inputs ¹	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Peak Current, Sx, D, or Dx Pins ADG5206	140 mA (pulsed at 1 ms, 10% duty cycle maximum)
ADG5207	105 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx, D, or Dx Pins ²	Data + 15%
Temperature Range	
Operating	−40°C to +125°C
Storage	−65°C to +150°C
Junction Temperature	150°C
Thermal Impedance, θ_{JA}	
28-Lead TSSOP (4-Layer Board)	67.7°C/W
32-Lead LFCSP (4-Layer Board)	27.27°C/W
Reflow Soldering Peak Temperature, Pb Free	As per JEDEC J-STD-020
HBM ESD (ESDA/JEDEC JS-001-2011)	
ADG5206	
All Pins	8 kV
ADG5207	
I/O Port to Supplies	8 kV
I/O Port to I/O Port	2 kV
All Other Pins	8 kV

¹ Overvoltages at the Ax, EN, Sx, D, and Dx pins are clamped by internal diodes. Limit current to the maximum ratings given.

² See Table 5 and Table 6.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

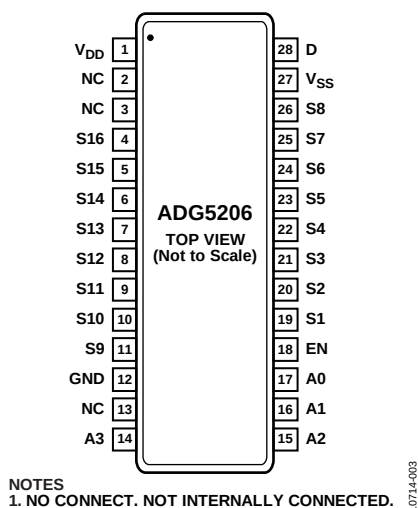


Figure 3. ADG5206 Pin Configuration (TSSOP)

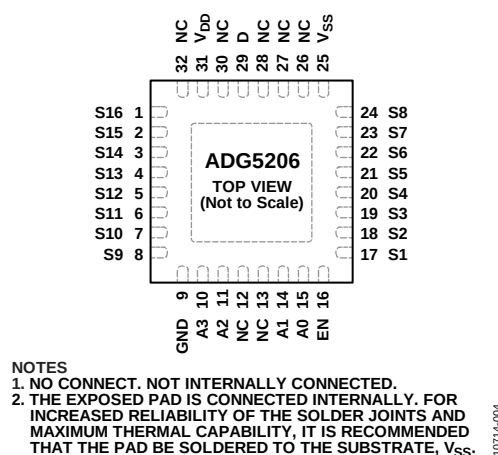


Figure 4. ADG5206 Pin Configuration (LFCSP)

Table 8. ADG5206 Pin Function Descriptions

Pin No.		Mnemonic	Description
TSSOP	LFCSP		
1	31	V _{DD}	Most Positive Power Supply Potential.
2, 3, 13	12, 13, 26, 27, 28, 30, 32	NC	No Connect. Not internally connected.
4	1	S16	Source Terminal 16. This pin can be an input or an output.
5	2	S15	Source Terminal 15. This pin can be an input or an output.
6	3	S14	Source Terminal 14. This pin can be an input or an output.
7	4	S13	Source Terminal 13. This pin can be an input or an output.
8	5	S12	Source Terminal 12. This pin can be an input or an output.
9	6	S11	Source Terminal 11. This pin can be an input or an output.
10	7	S10	Source Terminal 10. This pin can be an input or an output.
11	8	S9	Source Terminal 9. This pin can be an input or an output.
12	9	GND	Ground (0 V) Reference.
14	10	A3	Logic Control Input.
15	11	A2	Logic Control Input.
16	14	A1	Logic Control Input.
17	15	A0	Logic Control Input.
18	16	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are turned off. When this pin is high, the Ax logic inputs determine which switch is turned on.
19	17	S1	Source Terminal 1. This pin can be an input or an output.
20	18	S2	Source Terminal 2. This pin can be an input or an output.
21	19	S3	Source Terminal 3. This pin can be an input or an output.
22	20	S4	Source Terminal 4. This pin can be an input or an output.
23	21	S5	Source Terminal 5. This pin can be an input or an output.
24	22	S6	Source Terminal 6. This pin can be an input or an output.
25	23	S7	Source Terminal 7. This pin can be an input or an output.
26	24	S8	Source Terminal 8. This pin can be an input or an output.
27	25	V _{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
28	29	D	Drain Terminal. This pin can be an input or an output.
NA	Exposed Pad		The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V _{SS} .

Table 9. [ADG5206](#) Truth Table

A3	A2	A1	A0	EN	On Switch
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

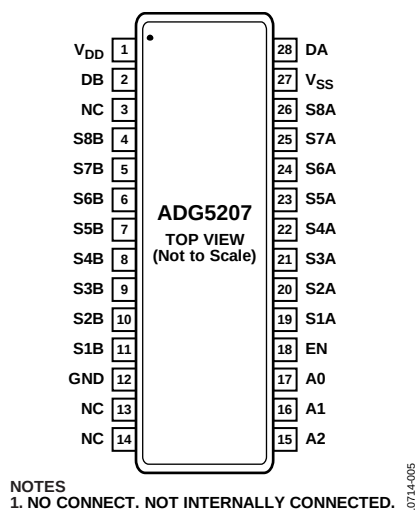


Figure 5. ADG5207 Pin Configuration (TSSOP)

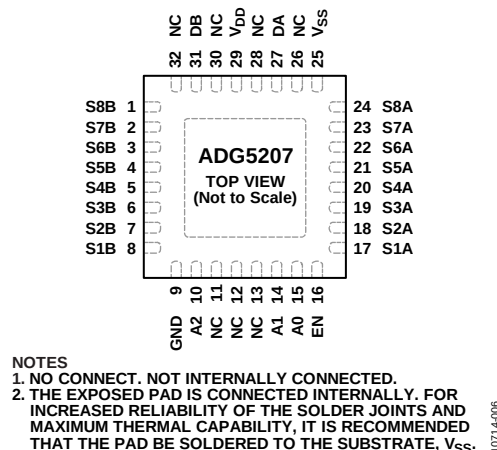


Figure 6. ADG5207 Pin Configuration (LFCSP)

Table 10. ADG5207 Pin Function Descriptions

Pin No.		Mnemonic	Description
TSSOP	LFCSP		
1	29	V _{DD}	Most Positive Power Supply Potential.
2	31	DB	Drain Terminal B. This pin can be an input or an output.
3, 13, 14	11, 12, 12, 26, 28, 30, 32	NC	No Connect. Not internally connected.
4	1	S8B	Source Terminal 8B. This pin can be an input or an output.
5	2	S7B	Source Terminal 7B. This pin can be an input or an output.
6	3	S6B	Source Terminal 6B. This pin can be an input or an output.
7	4	S5B	Source Terminal 5B. This pin can be an input or an output.
8	5	S4B	Source Terminal 4B. This pin can be an input or an output.
9	6	S3B	Source Terminal 3B. This pin can be an input or an output.
10	7	S2B	Source Terminal 2B. This pin can be an input or an output.
11	8	S1B	Source Terminal 1B. This pin can be an input or an output.
12	9	GND	Ground (0 V) Reference.
15	10	A2	Logic Control Input.
16	14	A1	Logic Control Input.
17	15	A0	Logic Control Input.
18	16	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are turned off. When this pin is high, the Ax logic inputs determine which switch is turned on.
19	17	S1A	Source Terminal 1A. This pin can be an input or an output.
20	18	S2A	Source Terminal 2A. This pin can be an input or an output.
21	19	S3A	Source Terminal 3A. This pin can be an input or an output.
22	20	S4A	Source Terminal 4A. This pin can be an input or an output.
23	21	S5A	Source Terminal 5A. This pin can be an input or an output.
24	22	S6A	Source Terminal 6A. This pin can be an input or an output.
25	23	S7A	Source Terminal 7A. This pin can be an input or an output.
26	24	S8A	Source Terminal 8A. This pin can be an input or an output.
27	25	V _{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
28	27	DA	Drain Terminal A. This pin can be an input or an output.
NA	Exposed Pad		The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V _{SS} .

Table 11. [ADG5207](#) Truth Table

A2	A1	A0	EN	On Switch Pair
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

TYPICAL PERFORMANCE CHARACTERISTICS

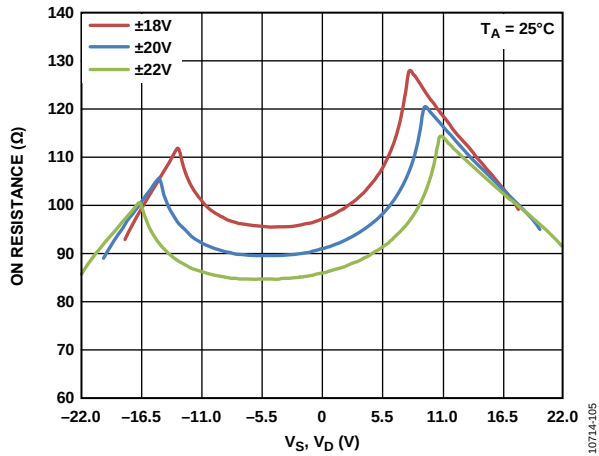


Figure 7. R_{ON} as a Function of V_S , V_D (± 20 V Dual Supply)

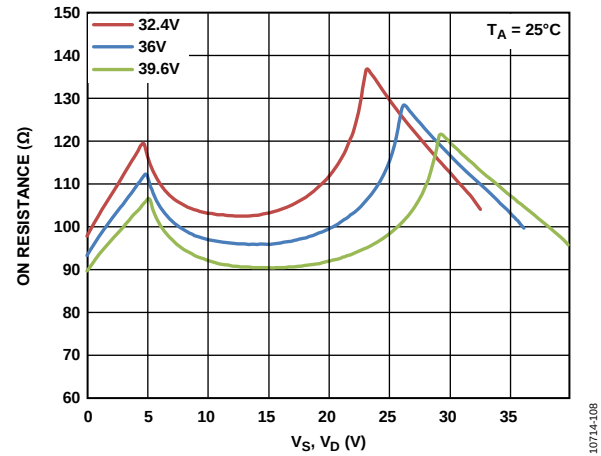


Figure 10. R_{ON} as a Function of V_S , V_D (36 V Single Supply)

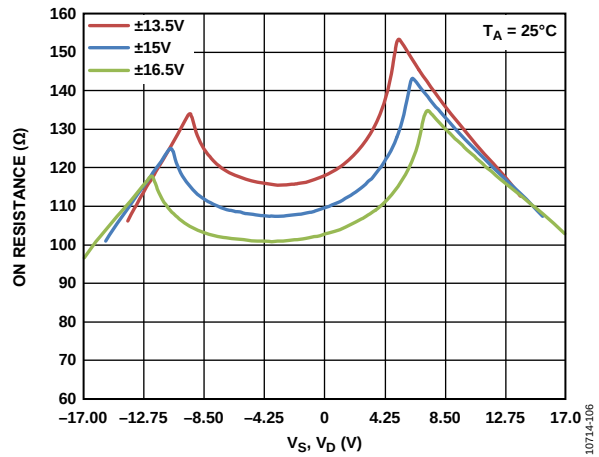


Figure 8. R_{ON} as a Function of V_S , V_D (± 15 V Dual Supply)

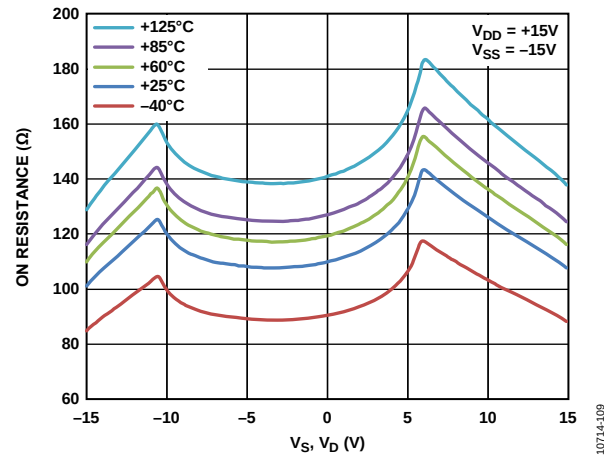


Figure 11. R_{ON} as a Function of V_S , V_D for Different Temperatures, ± 15 V Dual Supply

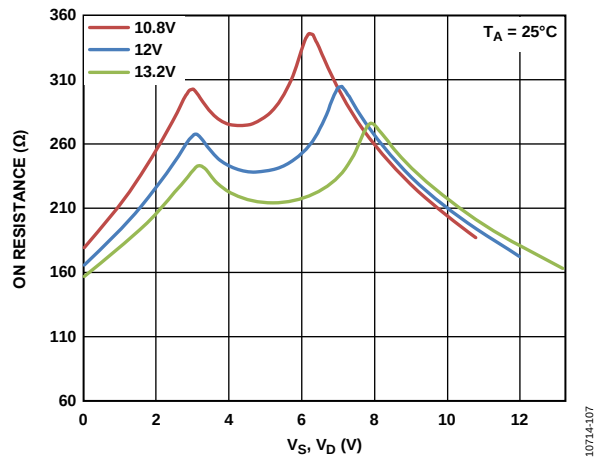


Figure 9. R_{ON} as a Function of V_S , V_D (12 V Single Supply)

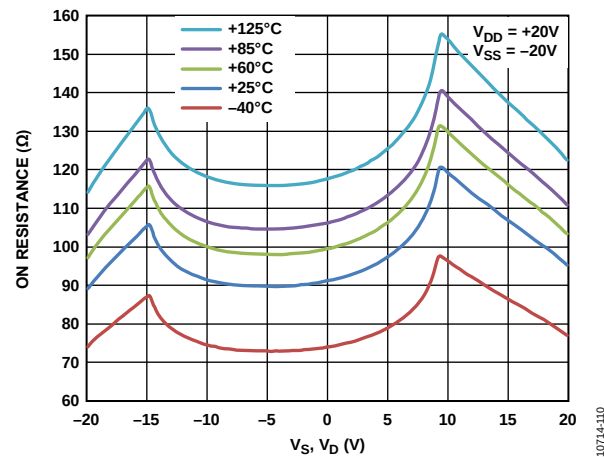


Figure 12. R_{ON} as a Function of V_S , V_D for Different Temperatures, ± 20 V Dual Supply

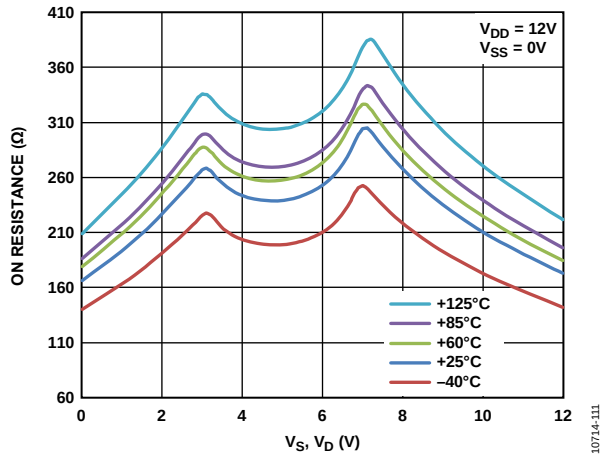


Figure 13. R_{ON} as a Function of V_S , V_D for Different Temperatures, 12 V Single Supply

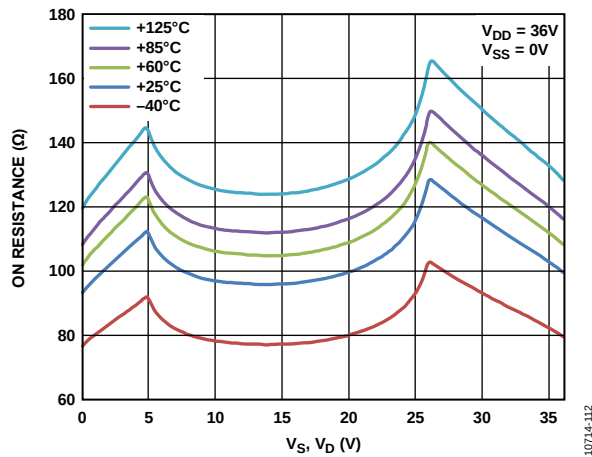


Figure 14. R_{ON} as a Function of V_S , V_D for Different Temperatures, 36 V Single Supply

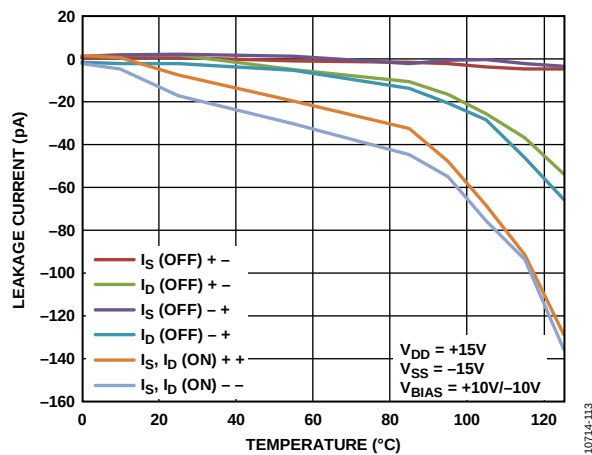


Figure 15. Leakage Currents vs. Temperature, $\pm 15V$ Dual Supply

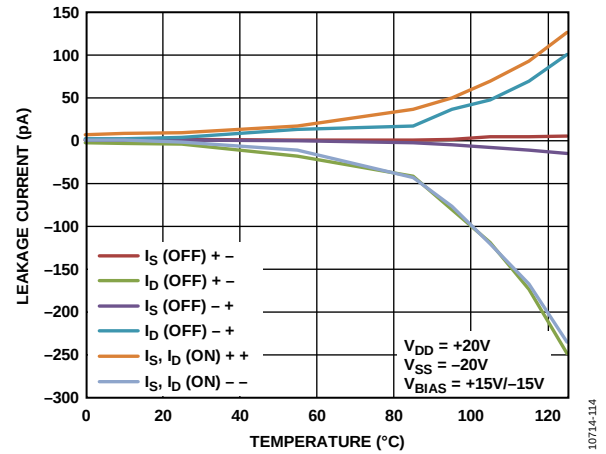


Figure 16. Leakage Currents vs. Temperature, $\pm 20V$ Dual Supply

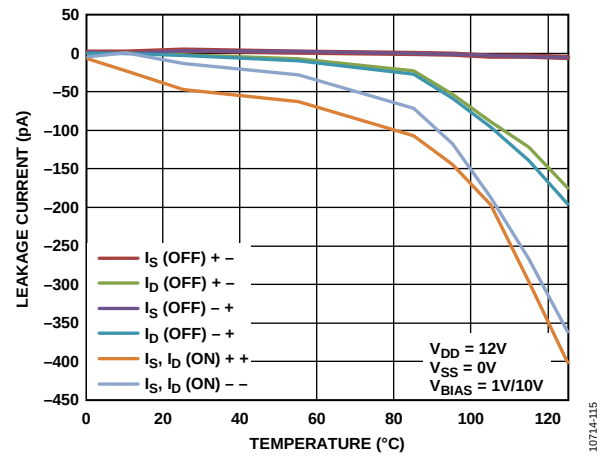


Figure 17. Leakage Currents vs. Temperature, 12 V Single Supply

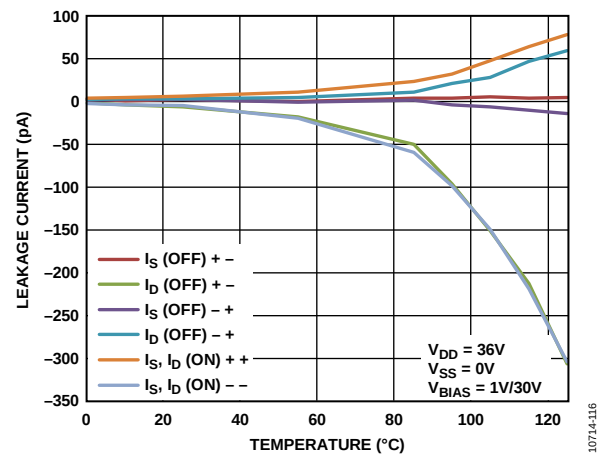


Figure 18. Leakage Currents vs. Temperature, 36 V Single Supply

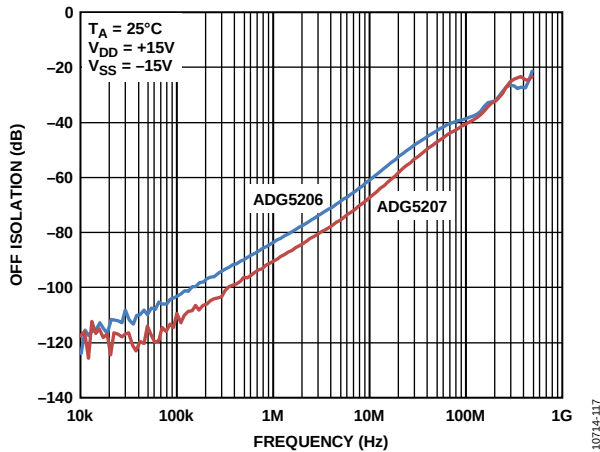


Figure 19. Off Isolation vs. Frequency, ± 15 V Dual Supply

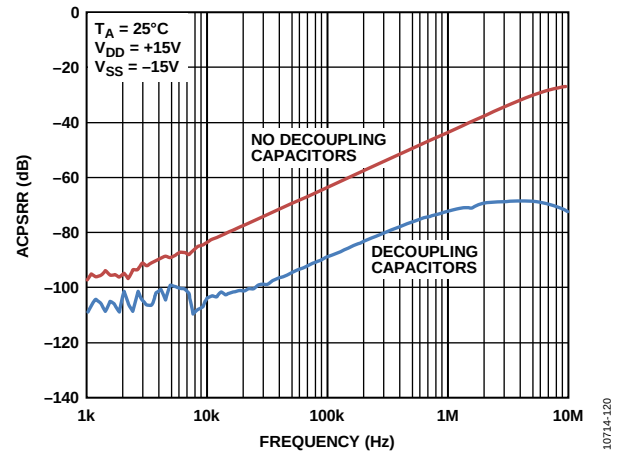


Figure 22. ACPSRR vs. Frequency, ± 15 V Dual Supply

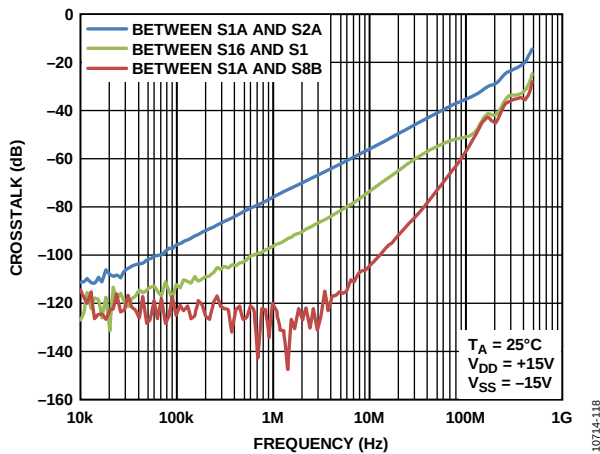


Figure 20. Crosstalk vs. Frequency, ± 15 V Dual Supply

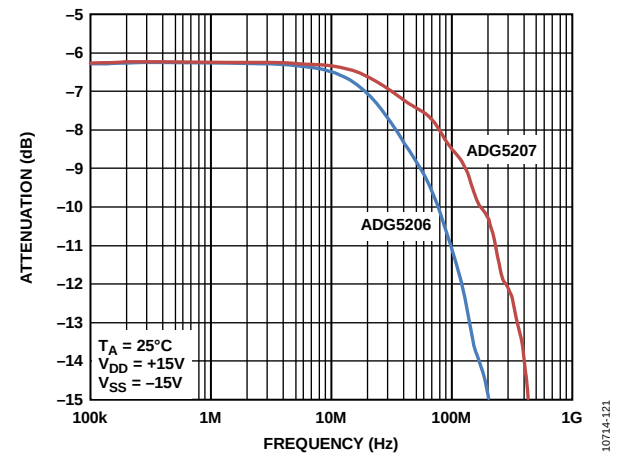


Figure 23. Bandwidth

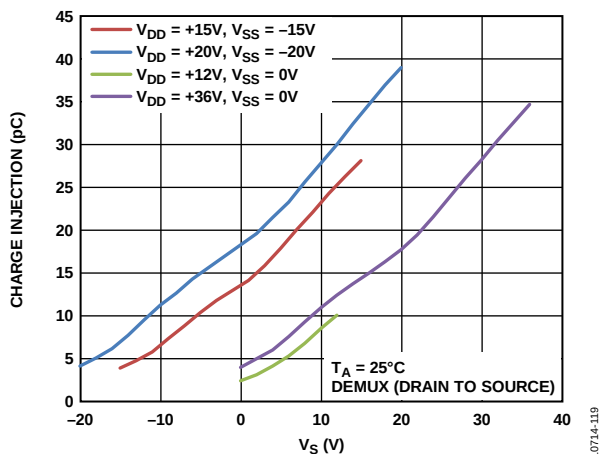


Figure 21. Charge Injection vs. Source Voltage, Drain to Source

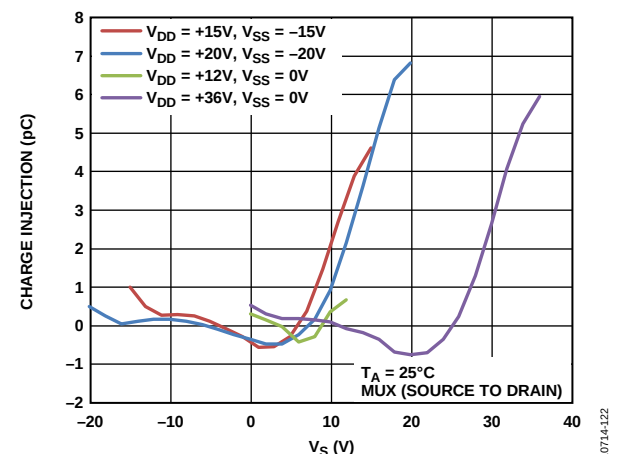
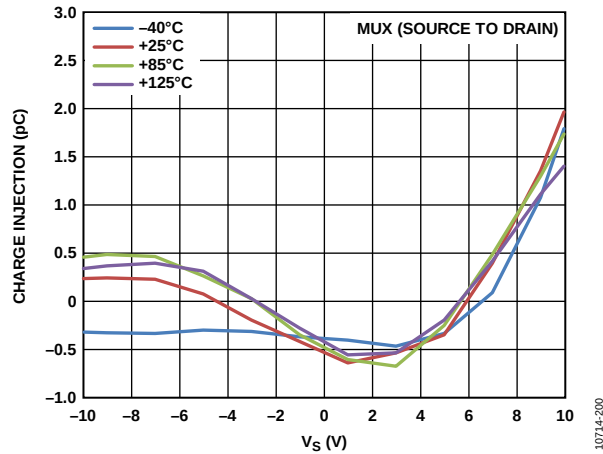
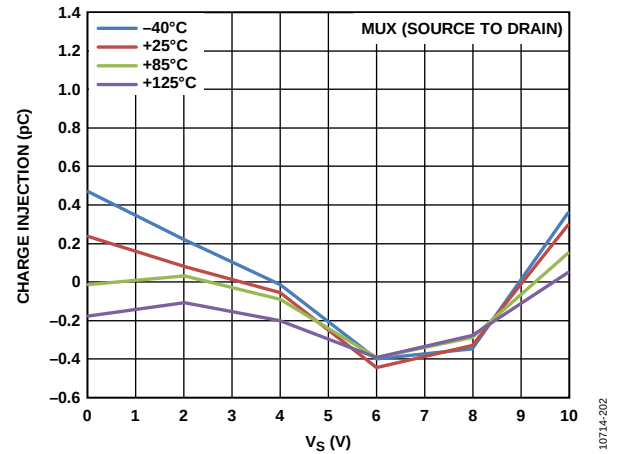
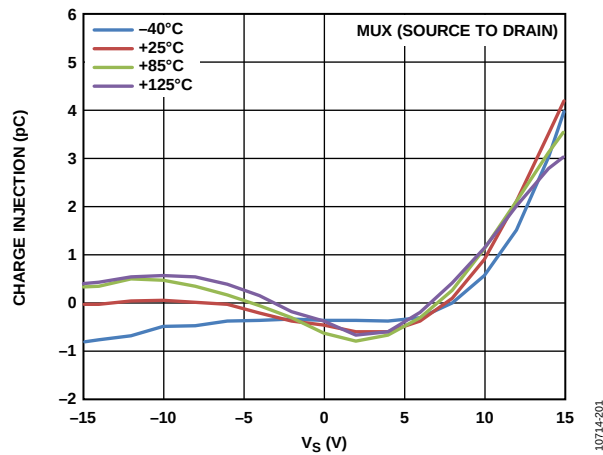
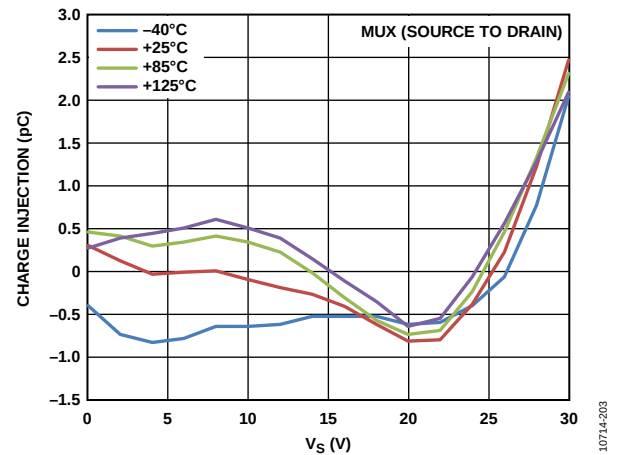
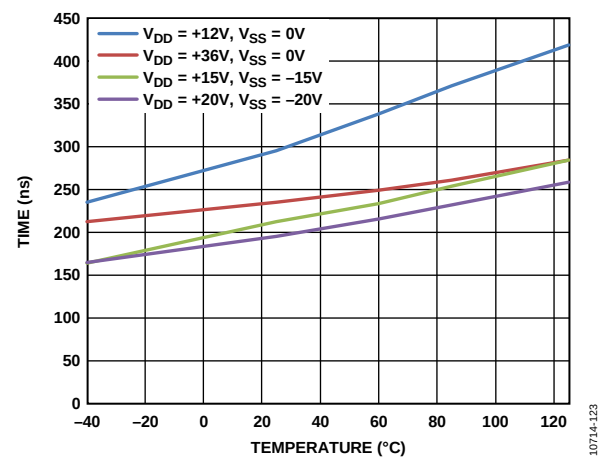
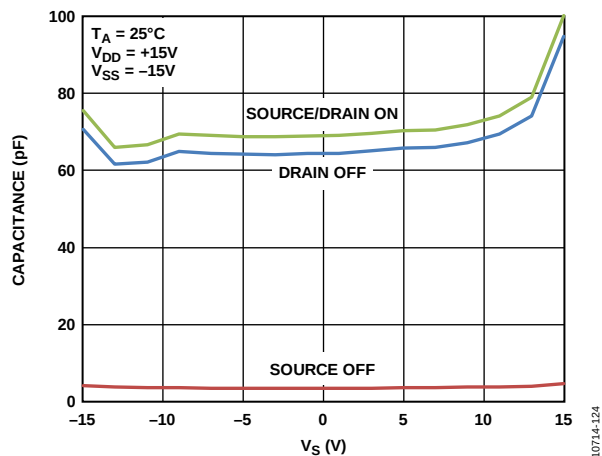
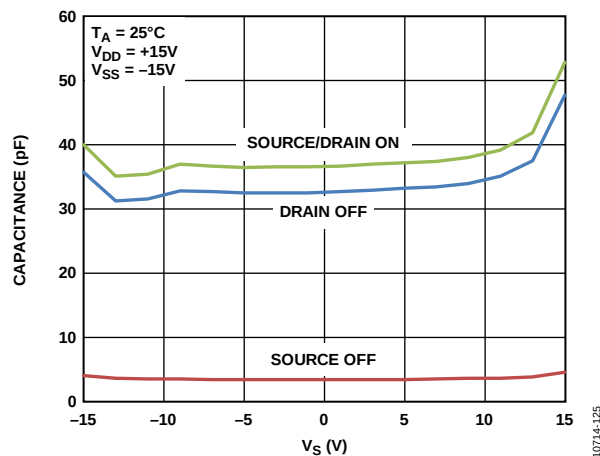


Figure 24. Charge Injection vs. Source Voltage, Source to Drain

Figure 25. Q_{INJ} as a Function of V_S for Different Temperatures, ± 15 V Dual SupplyFigure 28. Q_{INJ} as a Function of V_S for Different Temperatures, 12 V Single SupplyFigure 26. Q_{INJ} as a Function of V_S for Different Temperatures, ± 20 V Dual SupplyFigure 29. Q_{INJ} as a Function of V_S for Different Temperatures, 36 V Single SupplyFigure 27. $t_{TRANSITION}$ Time vs. Temperature

Figure 30. ADG5206 Capacitance vs. Source Voltage, $\pm 15\text{ V}$ Dual SupplyFigure 31. ADG5207 Capacitance vs. Source Voltage, $\pm 15\text{ V}$ Dual Supply

The diagram shows a two-port network. The input port is connected to a voltage source V_S and a diode. The input current is I_S (OFF). The output port is connected to a load resistor R_L and a diode. The output current is I_D (OFF). The network contains two switches, S_1 and S_{16} , and a central component labeled D .

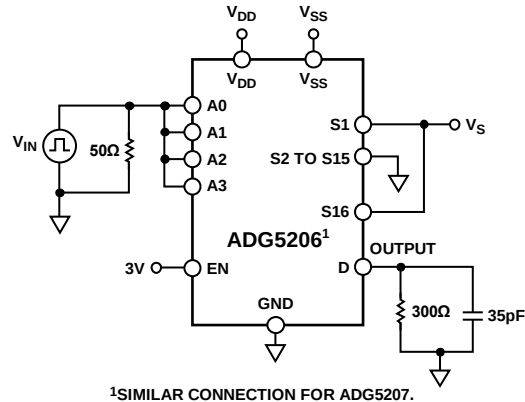
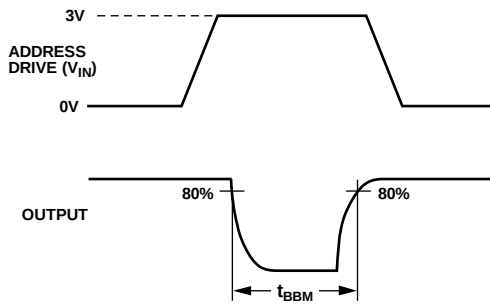
Timing diagram for the 74VHC04 inverter. The diagram shows the ADDRESS DRIVE (V_{IN}) and OUTPUT signals. The input signal transitions from 0V to 3V and back to 0V. The output signal transitions from 0V to 3V and back to 0V. The transition time t_r is specified as less than 20ns. The output signal is shown with 50% and 90% voltage levels. The transition time $t_{TRANSITION}$ is indicated for the output signal.

1SIMILAR CONNECTION FOR ADG5207.

0714-034

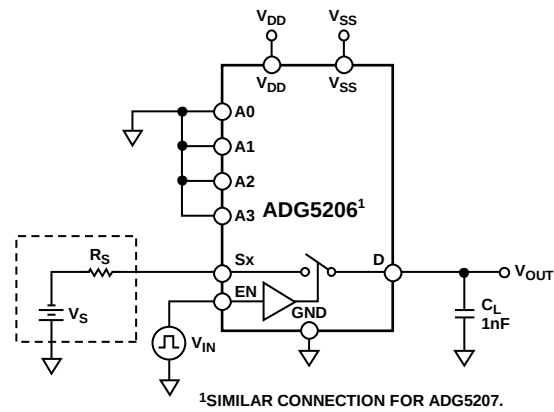
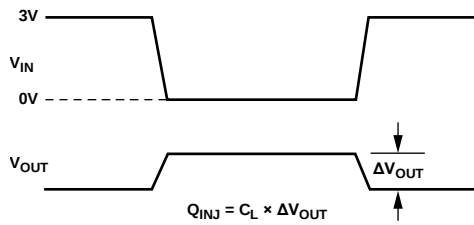
The diagram shows the relationship between the enable input and the output. The enable signal (V_{IN}) is a pulse from 0V to 3V. The output (V_{OUT}) transitions from 0V to 0.9V_{OUT} during the enable pulse. The output signal is labeled 0.1V_{OUT} during the fall time. The output signal returns to 0V after the enable signal returns to 0V. The output signal is labeled 0.1V_{OUT} during the fall time.

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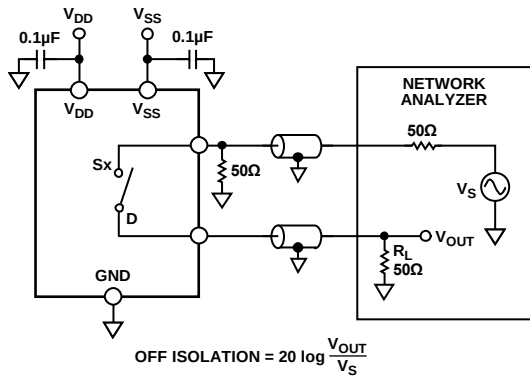
10714-035

Figure 37. Break-Before-Make Time Delay, t_D



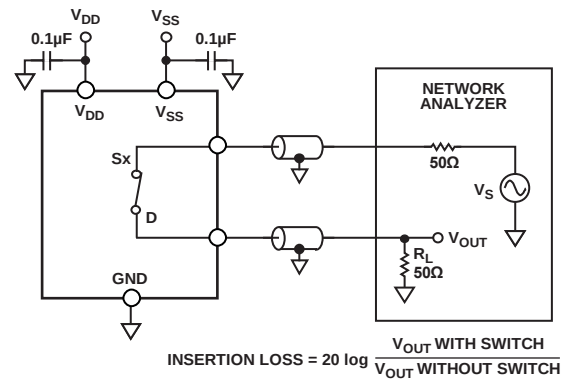
10714-037

Figure 38. Charge Injection



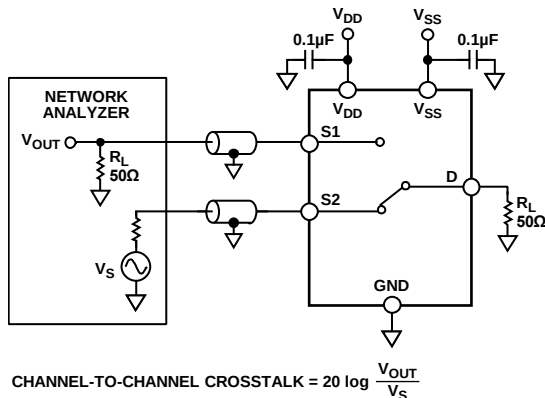
10714-032

Figure 39. Off Isolation



10714-033

Figure 41. Bandwidth



10714-030

Figure 40. Channel-to-Channel Crosstalk

TERMINOLOGY

I_{DD}

I_{DD} represents the positive supply current.

I_{SS}

I_{SS} represents the negative supply current.

V_D, V_S

V_D and V_S represent the analog voltage on Terminal D and Terminal S, respectively.

R_{ON}

R_{ON} is the ohmic resistance between Terminal D and Terminal S.

ΔR_{ON}

ΔR_{ON} represents the difference between the R_{ON} of any two channels.

R_{FLAT (ON)}

R_{FLAT (ON)} is the flatness defined as the difference between the maximum and the minimum value of on resistance measured over the specified analog signal range.

I_S (Off)

I_S (Off) is the source leakage current with the switch off.

I_D (Off)

I_D (Off) is the drain leakage current with the switch off.

I_D (On), I_S (On)

I_D (On) and I_S (On) represent the channel leakage currents with the switch on.

V_{INL}

V_{INL} is the maximum input voltage for Logic 0.

V_{INH}

V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}

I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

C_D (Off)

C_D (Off) represents the off switch drain capacitance, which is measured with reference to ground.

C_S (Off)

C_S (Off) represents the off switch source capacitance, which is measured with reference to ground.

C_D (On), C_S (On)

C_D (On) and C_S (On) represent on switch capacitances, which are measured with reference to ground.

C_{IN}

C_{IN} represents digital input capacitance.

t_{ON} (EN)

t_{ON} (EN) represents the delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF} (EN)

t_{OFF} (EN) represents the delay time between the 50% and 90% points of the digital input and switch off condition.

t_{TRANSITION}

t_{TRANSITION} represents the delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

Break-Before-Make Time Delay (t_D)

t_D represents the off time measured between the 80% point of both switches when switching from one address state to another.

Off Isolation

Off isolation is a measure of unwanted signal coupling through an off channel.

Charge Injection

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

Crosstalk

Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth

Bandwidth is the frequency at which the output is attenuated by 3 dB.

On Response

On response is the frequency response of the on switch.

AC Power Supply Rejection Ratio (ACPSRR)

ACPSRR is a measure of the ability of a device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the ACPSRR.

APPLICATIONS INFORMATION

The ADG52xx family of switches and multiplexers provides a robust solution for instrumentation, industrial, automotive, aerospace, and other harsh environments that are prone to latch-up, which is an undesirable high current state that can lead to device failure and persist until the power supply is turned off. The [ADG5206/ADG5207](#) high voltage switches allow single-supply operation from 9 V to 40 V and dual-supply operation from ± 9 V to ± 22 V.

TRENCH ISOLATION

In the [ADG5206/ADG5207](#), an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, and the result is a completely latch-up proof switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors form a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode can become forward-biased. A silicon controlled rectifier (SCR) type circuit is formed by the two transistors, causing a significant amplification of the current that, in turn, leads to latch-up. With trench isolation, this diode is removed and the result is a latch-up proof switch.

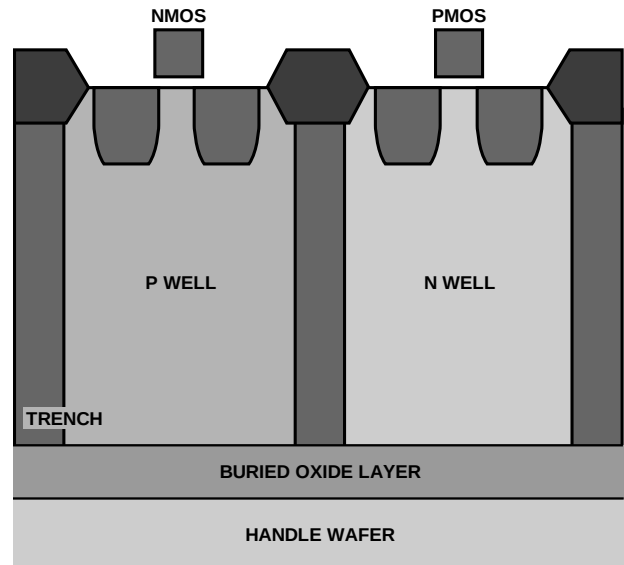


Figure 42. Trench Isolation

10714-038

OUTLINE DIMENSIONS

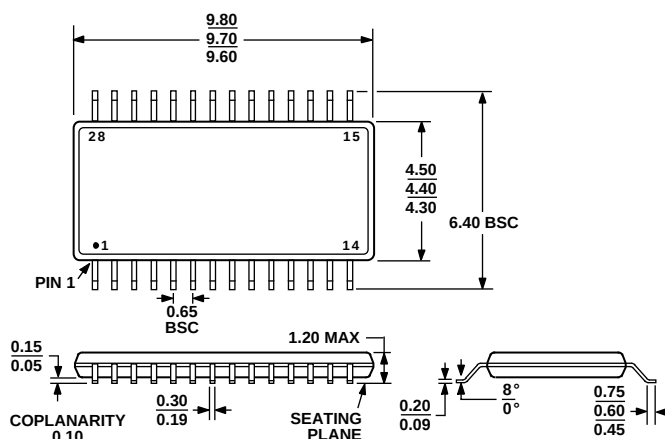
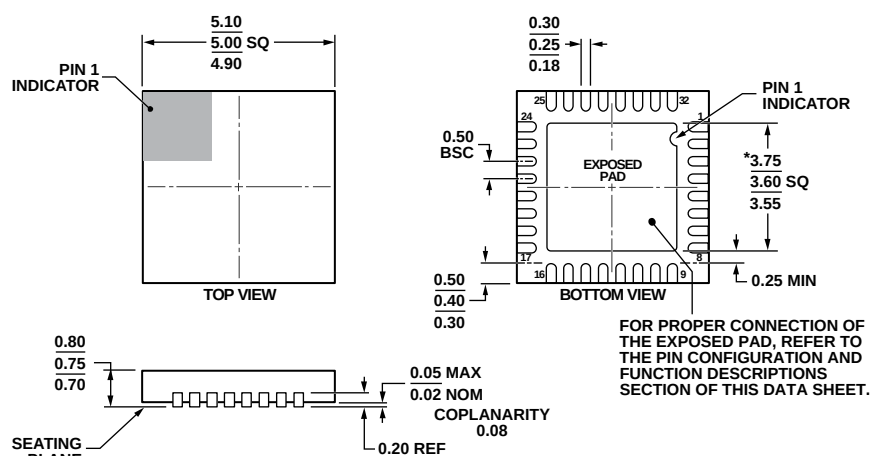


Figure 43. 28-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-28)

Dimensions shown in millimeters



*COMPLIANT TO JEDEC STANDARDS MO-220-WHHD-5
WITH EXCEPTION TO EXPOSED PAD DIMENSION.

Figure 44. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]

5 × 5 mm Body, Very Very Thin Quad (CP-32-12)

Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADG5206BRUZ	−40°C to +125°C	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28
ADG5206BRUZ-RL7	−40°C to +125°C	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28
ADG5206BCPZ-RL7	−40°C to +125°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
ADG5207BRUZ	−40°C to +125°C	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28
ADG5207BRUZ-RL7	−40°C to +125°C	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28
ADG5207BCPZ-RL7	−40°C to +125°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12

¹ Z = RoHS Compliant Part.

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