512 Mb NAND Flash
H27U518S2C

Document Title

512 Mbit (64 M × 8 bit) NAND Flash Memory

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial Draft	Jul. 29. 2008	Preliminary
0.1	Correct Partnumber	Nov. 25. 2008	Preliminary
1.0	Preliminary removed	Dec. 10. 2008	

FEATURES SUMMARY

HIGH DENSITY NAND FLASH MEMORIES
- Cost effective solutions for mass storage applications

NAND INTERFACE
- x8 bus width
- Address/ Data Multiplexing
- Pinout compatiblity for all densities

SUPPLY VOLTAGE
- 3.3 V device : Vcc = 2.7 V ~ 3.6 V

MEMORY CELL ARRAY
- (512 + 16) bytes x 32 pages x 4096 blocks

PAGE SIZE
- (512 + 16 spare) Bytes

BLOCK SIZE
- (16 K + 512 spare) Bytes

PAGE READ / PROGRAM
- Random access : 12 us (max.)
- Sequential access : 30 ns (min.)
- Page program time : 200 us (typ.)

COPY BACK PROGRAM
- Automatic block download without latency time

FAST BLOCK ERASE
- Block erase time : 1.5 ms (typ.)

STATUS REGISTER
- Normal Status Register (Read/Program/Erase)
- Extended Status Register (EDC)

ELECTRONIC SIGNATURE
- 1st cycle : Manufacturer Code
- 2nd cycle : Device Code

CHIP ENABLE DON'T CARE
- Simple interface with microcontroller

HARDWARE DATA PROTECTION
- Program/Erase locked during Power transitions.

DATA RETENTION
- 100,000 Program/Erase cycles (with 1bit/528byte ECC)
- 10 years Data Retention

PACKAGE
- H27U518S2CTR-Bx
  : 48-Pin TSOP1 (12 × 20 × 1.2 mm)
  - H27U518S2CTR-Bx (Lead & Halogen Free)

1. SUMMARY DESCRIPTION

Hynix NAND H27U518S2C Series have 64 M × 8 bit with spare 2 M × 8 bit capacity. The device is offered in 3.3 V Vcc Power Supply, and with x8 I/O interface.

Its NAND cell provides the most cost-effective solution for the solid state mass storage market.

The device is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.

The device contains 4096 blocks, composed by 32 pages consisting in two NAND sturctures of 16 series connected Flash cells. A program operation allows to write the 512-byte page in typical 200 us and an erase operation can be performed in typical 1.5 ms on a 16 K-byte block.

Data in the page can be read out at 30 ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of footprint.

Commands, Data and Addresses are synchronously introduced using $\overline{CE}$, $\overline{WE}$, $\overline{RE}$, ALE and CLE input pin. The on-chip Program/Erase Controller automates all read, program and erase functions including pulse repetition, where required, and internal verification and margining of data. The modify operations can be locked using the $\overline{WP}$ input. The output pin R/$\overline{B}$ (open drain buffer) signals the status of the device during each operation. In a system with multiple memories the R/$\overline{B}$ pins can be connected all together to provide a global status signal.

The copy back function allows the optimization of defective blocks management. When a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase.

Even the write-intensive systems can take advantage of the H27U518S2C Series extended reliability of 100K program/ erase cycles by supporting ECC (Error Correcting Code) with real time mapping-out algorithm. The chip supports $\overline{CE}$ don't care function. This function allows the direct download of the code from the NAND Flash memory device by a microcontroller, since the $\overline{CE}$ transitions do not stop the read operation.

This device includes also extra features like OTP/Unique ID area, Read ID2 extension.

The H27U518S2C is available in 48-TSOP1 12 x 20 mm.

1.1 Product List

PART NUMBER	ORGANIZATION	VCC RANGE	PACKAGE
H27U518S2C	x8	2.7 ~ 3.6 Volt	48 TSOP 1

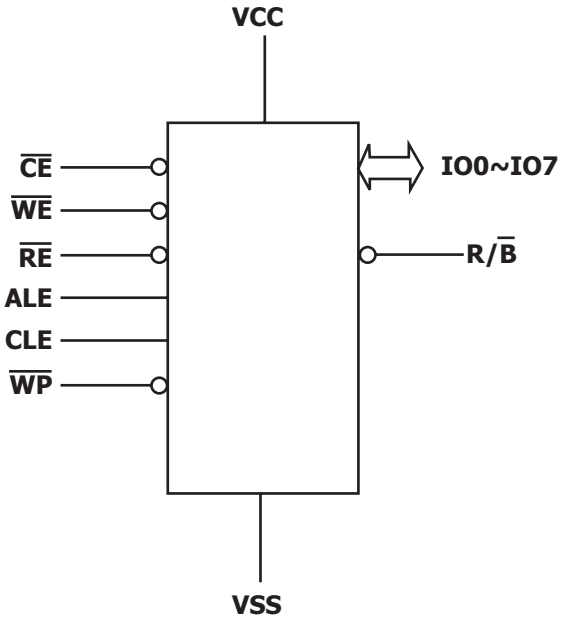


Figure 1 : Logic Diagram

IO7 - IO0	Data Input / Outputs
CLE	Command latch enable
ALE	Address latch enable
$\overline{CE}$	Chip Enable
$\overline{RE}$	Read Enable
$\overline{WE}$	Write Enable
$\overline{WP}$	Write Protect
R/$\overline{B}$	Ready / Busy
Vcc	Power Supply
Vss	Ground
NC	No Connection

Table 1 : Signal Names

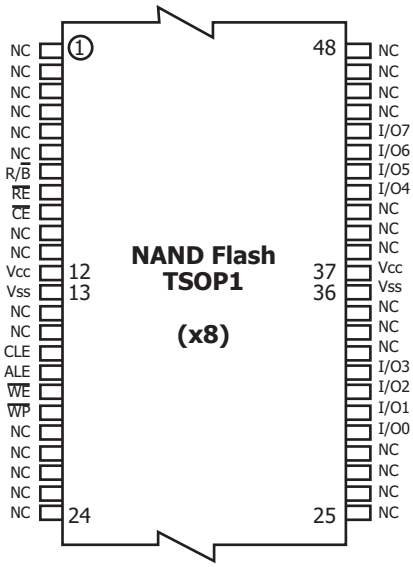


Figure 2 : 48 TSOP 1 Contact, x8 Device

1.2 Pin Description

Pin Name	Description
IO0-IO7	**DATA INPUTS/OUTPUTS** The IO pins allow to input command, address and data and to output data during read / program operations. The inputs are latched on the rising edge of Write Enable ($\overline{WE}$). The I/O buffer float to High-Z when the device is deselected or the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** This input activates the latching of the IO inputs inside the Command Register on the Rising edge of Write Enable ($\overline{WE}$).
ALE	**ADDRESS LATCH ENABLE** This input activates the latching of the IO inputs inside the Address Register on the Rising edge of Write Enable ($\overline{WE}$).
$\overline{CE}$	**CHIP ENABLE** This input controls the selection of the device.
$\overline{WE}$	**WRITE ENABLE** This input acts as clock to latch Command, Address and Data. The IO inputs are latched on the rise edge of $\overline{WE}$.
$\overline{RE}$	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.
$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin, when Low, provides an Hardware protection against undesired modify (program / erase) operations.
R/$\overline{B}$	**READY BUSY** The Ready/Busy output is an Open Drain pin that signals the state of the memory.
Vcc [1]	**SUPPLY VOLTAGE** The Vcc supplies the power for all the operations (Read, Write, Erase).
Vss	**GROUND**
NC	**NO CONNECTION**

Table 2 : Pin Description

NOTE

1. A 0.1uF capacitor should be connected between the Vcc Supply Voltage pin and the Vss Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.

	IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A9	A10	A11	A12	A13	A14	A15	A16
3rd Cycle	A17	A18	A19	A20	A21	A22	A23	A24
4th Cycle	A25	L [1]	L [1]	L [1]	L [1]	L [1]	L [1]	L [1]

Table 3 : Address Cycle Map

NOTE

1. L must be set to Low
2. A8 is set to LOW or High by the Read 1 Command(00h or 01h).

Density	Plane Address	Block Address	Page Address	Column Address
1 Gbit	A25	A24 ~ A14	A13 ~ A9	A7 ~ A0

Table 4 : Address Role

FUNCTION	1st CYCLE	2nd CYCLE	3rd CYCLE	4th CYCLE	Acceptable command during busy
READ 1	00h / 01h	-	-	-	
READ 2	50 h	-	-	-	
READ ID	90h	-	-	-	
RESET	FFh	-	-	-	Yes
PAGE PROGRAM	80h	10h	-	-	
COPY BACK PROGRAM [1]	00h	8Ah	(10h)	-	
BLOCK ERASE	60h	D0h	-	-	
READ STATUS REGISTER	70h	-	-	-	Yes

Table 5 : Command Set

NOTE

1. The program confirm command (10h) can either be excuted or ignored during copy back program

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	MODE	
H	L	L	Rising	H	X	Read Mode	Command Input
L	H	L	Rising	H	X		Address Input
H	L	L	Rising	H	H	Write Mode	Command Input
L	H	L	Rising	H	H		Address Input
L	L	L	Rising	H	H	Data Input	
L	L	L [1]	H	Falling	X	Sequential Read and Data Output	
X	X	X	H	H	X	During Read (Busy)	
X	X	X	X	X	H	During Program (Busy)	
X	X	X	X	X	H	During Erase (Busy)	
X	X	X	X	X	L	Write Protect	
X	X	H	X	X	0 V / Vcc	Stand By	

Table 6 : Mode Selection

NOTE

1. With the $\overline{CE}$ high during latency time does not stop the read operation.

2. Bus Opeation

There are six standard bus operations that control the device. These are Command Input, Address Input, Data Input, Data Output, Write Protect, and Standby.

Typically glitches less than 5 ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations.

2.1 Command Set

Command Input bus operation is used to give a command to the memory device. Command are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See Figure 4 and Table 13 for details of the timings requirements.

2.2 Address Input

Address Input bus operation allows the insertion of the memory address. Four bus cycles are required to input the addresses. Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modifying operation (write/erase) the Write Protect pin must be high. See Figure 5 and Table 13 for details of the timings requirements. In addition, addresses over the addressable space are disregarded even if the user sets them during command insertion.

2.3 Data Input

Data Input bus operation allows to feed to the device the data to be programmed. The data insertion is serial and timed by the Write Enable cycles. Data are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable. See Figure 6 and Table 13 for details of the timings requirements.

2.4 Data Output

Data Output bus operation allows to read data from the memory array and to check the status register content, the EDC register content and the ID data. Data can be serially shifted out by toggling the Read Enable pin with Chip Enable low, Write Enable High, Address Latch Enable low, and Command Latch Enable low. See Figure 7, 8, 9, 10, 11 and Table 13 for details of the timings requirements.

2.5 Write Protect

Hardware Write Protection is activated when the Write Protect pin is low. In this condition modifying operation does not start and the content of the memory is not altered. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up.

2.6 Standby

In Standby mode the device is deselected, outputs are disabled and Power Consumption is reduced.

3. DEVICE OPERATION

3.1 Page Read.

Upon initial device power up, the device defaults to Read1(00h/01h) mode. This operation is also initiated by writing 00h to the command register along with followed by the four address input cycles. Once the command is latched, it does not need to be written for the following page read operation.

Three types of operations are available: random read, serial page read and sequential row read.

The random read mode is enabled when the page address is changed. The 528 bytes (x8 device) of data within the selected page are transferred to the data registers in less than access random read time tR. The system controller can detect the completion of this data transfer tR by analyzing the output of R/$\overline{B}$ pin. Once the data in a page is loaded into the registers, they may be read out in 30 ns cycle time by sequentially pulsing $\overline{RE}$. High to low transitions of the $\overline{RE}$ clock output the data stating from the selected column address up to the last column address.

After the data of last column address is clocked out, the next page is automatically selected for sequential row read.

Waiting tR again allows reading the selected page. The sequential row read operation is terminated by bringing $\overline{CE}$ high.

The way the Read1 and Read2 commands work is like a pointer set to either the main area or the spare area (Refer to Figure 19) . Writing the Read2 command user may selectively access the spare area of bytes 512 to 527. Addresses A0 to A3 set the starting address of the spare area while addresses A4 to A7 are ignored.

Unless the operation is aborted, the page address is automatically incremented for sequential row

Read as in Read1 operation and spare sixteen bytes of each page may be sequentially read. The Read1 command (00h/01h) is needed to move the pointer back to the main area. Figure 9 to 11 show typical sequence and timings for each read operation.

3.2 Page Program.

The device is programmed basically on a page basis, but it does allow multiple partial page programming of a byte or consecutive bytes up to 528, in a single page program cycle. The number of consecutive partial page programming operations within the same page without an intervening erase operation must not exceed 1 for main array and 2 for spare array. The addressing may be done in any random order in a block. A page program cycle consists of a serial data loading period in which up to 528 bytes of data may be loaded into the page register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. Serial data loading can be started from 2nd half array by moving pointer. About the pointer operation, please refer to Figure 20.

The data-loading sequence begins by inputting the Serial Data Input command (80h), followed by the four address input cycles (Refer to Table 3 for details) and then serial data loading. The Page Program confirm command (10h) starts the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal Program Erase Controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered, with $\overline{RE}$ and $\overline{CE}$ low, to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked as specified in Figure 12.

The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

3.3 Block Erase.

The Erase operation is done on a block (16K Byte) basis. It consists of an Erase Setup command (60h), a Block address loading and an Erase Confirm Command (D0h). The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

The block address loading is accomplished three cycles. Only block addresses(Refer to Table 4 for further info) are needed while A9 to A13 is ignored.

At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal Program Erase Controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked. Figure 13 details the sequence.

3.4 Copy-Back Program.

The copy-back program is provided to quickly and efficiently rewrite data stored in one page within the plane to another page within the same plane without using an external memory. Since the time-consuming sequential-reading and its reloading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also need to be copied to the newly assigned free block. The operation for performing a copy-back program is a sequential execution of page-read without burst-reading cycle and copying-program with the address of destination page. A normal read operation with "00h" command and the address of the source page moves the whole 528byte data into the internal buffer. As soon as the device returns to Ready state, Page-Copy Data-input command (8Ah) with the address cycles of destination page followed may be written. The Program Confirm command (10h) is not needed to actually begin the programming operation. For backward-compatibility, issuing Program Confirm command during copy-back does not prevent correct device operation.

Copy-Back Program operation is allowed only within the same memory plane. Once the Copy-Back Program is finished, any additional partial page programming into the copied pages is prohibited before erase. Plane address must be the same between source and target page(Refer to Table 4 for details).

When there is a program-failure at Copy-Back operation, error is reported by pass/fail status. But, if Copy-Back operations are accumulated over time, bit error due to charge loss is not checked by external error detection/correction scheme. For this reason, two bit error correction is recommended for the use of Copy-Back operation.

Figure 14 shows the command sequence for the copy-back operation.

3.5 Read Status Register.

The device contains a Status Register which may be read to find out whether read, program or erase operation is completed, and whether the read, program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last (see figure Figure 8). This two-line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to Table 14 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command (00h or 50h) should be given before sequential page read cycle.

3.6 Read ID.

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Two read cycles sequentially output the manufacturer code (ADh), the device code(76h). The command register remains in Read ID mode until further commands are issued to it. Figure 15 shows the operation sequence, while Tables 15 to 16 explain the byte meaning.

3.7 Reset.

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when $\overline{WP}$ is high. Refer to table 14 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The R/$\overline{B}$ pin transitions to low for tRST after the Reset command is written. Refer to Figure 16 below.

4. OTHER FEATURES

4.1 Power Up Sequence.

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below V_{LKO} (1.8 V for 3.3 V version) . $\overline{WP}$ pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down. A recovery time of minimum 10 us is required before internal circuit gets ready for any command sequences as shown in Figure 17. The two-step command sequence for program/erase provides additional software protection.

4.2 Ready/Busy.

The device has a Ready/Busy output that provides method of indicating the completion of a page program, erase, copy-back and random read completion. The R/$\overline{B}$ pin is normally high and goes to low when the device is busy (after a reset, read, program, erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. Because pull-up resistor value is related to tr(R/$\overline{B}$) and current drain during busy (I_{busy}), an appropriate value can be obtained with the following reference chart in Figure 18. Its value can be determined by the following guidance.

4.3 Data Protection

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below VLKO (V_{LKO}=1.8V). The situation is described in Figure 21. The two-step command sequence for program/erase provides additional software protection.

Parameter	Symbol	Min	Max	Unit
Valid Block Number	NVB	4016	4096	Blocks

Table 7 : Valid Block Numbers

NOTE
1. The 1st block is guaranteed to be a valid block at the time of shipment.

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature (Commercial Temperature Range)	0 to 70	℃
	Ambient Operating Temperature (Industrial Temperature Range)	-40 to 85	℃
T_{BIAS}	Temperature Under Bias	-50 to 125	℃
T_{STG}	Storage Temperature	-65 to 150	V
VIO(2)	Input or Output Voltage	-0.6 to 4.6	V
Vcc	Supply Voltage	-0.6 to 4.6	V

Table 8 : Absolute maximum ratings

Note
1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the Hynix SURE Program and other relevant quality documents.
2. Minimum Voltage may undershoot to -2 V during transition and for less than 20 ns during transitions.

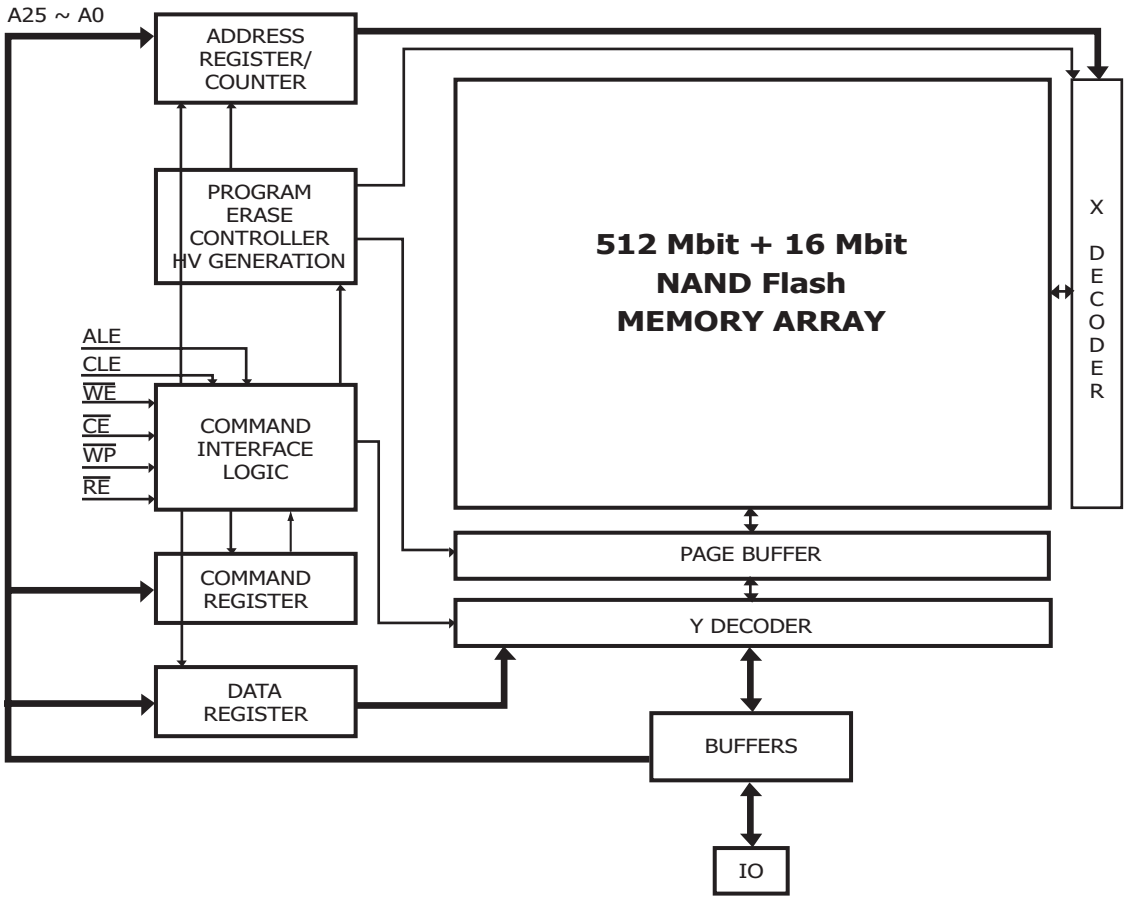


Figure 3 : Block Diagram

Parameter		Symbol	Test Conditions	3.3Volt			Unit
				Min	Typ	Max	
Operating Current	Sequential Read	I_{CC1}	t_{RC} = 50 ns $\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA	-	15	30	mA
	Program	I_{CC2}	-	-	15	30	mA
	Erase	I_{CC3}	-	-	15	30	mA
Stand-by Current (TTL)		I_{CC4}	$\overline{CE}$=V_{IH}, $\overline{WP}$ = 0 V / Vcc	-		1	mA
Stand-by Current (CMOS)		I_{CC5}	$\overline{CE}$ = Vcc-0.2, $\overline{WP}$ = 0V/Vcc	-	10	50	uA
Input Leakage Current		I_{LI}	V_{IN} = 0 to Vcc (max)	-	-	± 10	uA
Output Leakage Current		I_{LO}	V_{OUT} = 0 to Vcc (max)	-	-	± 10	uA
Input High Voltage		V_{IH}	-	0.8xVcc	-	Vcc+0.3	V
Input Low Voltage		V_{IL}	-	-0.3	-	0.2xVcc	V
Output High Voltage Level		V_{OH}	I_{OH} = - 400 uA	2.4	-	-	V
Output Low Voltage Level		V_{OL}	I_{OL} = 2.1 mA	-	-	0.4	V
Output Low Current (R/$\overline{B}$)		I_{OL} (R/$\overline{B}$)	V_{OL} = 0.4 V	8	10	-	mA
Vcc supply voltage (erase and program) lockout		V_{LKO}	-	-	1.8	-	V

Table 9 : DC and Operation Characteristics

Parameter	Value
Input Pulse Levels	0 V to VCC
Input Rise and Fall Times	5 ns
Input and Output Timing Levels	V_{CC} / 2
Output Load (1.7 V - 1.95 V)	1 TTL GATE and CL = 50pF

Table 10 : AC Conditions

Item	Symbol	Test Condition	Min	Max	Unit
Input / Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF

Table 11 : Pin Capacitance (T_A = 25 ℃, Frequency = 1 MHz)

Parameter		Symbol	Min	Typ	Max	Unit
Program Time		t_{PROG}	-	200	700	us
Number of partial Program Cycles in the same page	Main Array	NOP	-	-	1	Cycles
	Spare Array				2	
Block Erase Time		t_{BERS}	-	1.5	3	ms

Table 12 : Program / Erase Characteristics

Parameter	Symbol	Min	Max	Unit
CLE Setup time	t_{CLS}	15		ns
CLE Hold time	t_{CLH}	5		ns
$\overline{CE}$ setup time	t_{CS}	20		ns
$\overline{CE}$ hold time	t_{CH}	5		ns
$\overline{WE}$ pulse width	t_{WP}	15		ns
ALE setup time	t_{ALS}	15		ns
ALE hold time	t_{ALH}	5		ns
Data setup time	t_{DS}	15		ns
Data hold time	t_{DH}	5		ns
Write Cycle time	t_{WC}	30		ns
$\overline{WE}$ High hold time	t_{WH}	10		ns
Data Transfer from Cell to register	t_{R}		12	us
ALE to $\overline{RE}$ Delay (ID Read)	t_{AR1}	10		ns
CLE to $\overline{RE}$ Delay	t_{CLR}	10		ns
Ready to $\overline{RE}$ Low	t_{RR}	20		ns
$\overline{RE}$ Pulse Width	t_{RP}	15		ns
$\overline{WE}$ High to Busy	t_{WB}		100	ns
Read Cycle Time	t_{RC}	30		ns
$\overline{RE}$ Access Time	t_{REA}		18	ns
$\overline{RE}$ High to Output High Z	t_{RHZ}		30	ns
$\overline{CE}$ High to Output High Z	t_{CHZ}		20	ns
$\overline{RE}$ or $\overline{CE}$ high to Output hold	T_{OH}	10		
$\overline{RE}$ High Hold Time	T_{REH}	10		ns
Output High Z to $\overline{RE}$ low	t_{IR}	0		ns
$\overline{WE}$ High to $\overline{RE}$ low	t_{WHR}	60		ns
Device Resetting Time (Read / Program / Erase)	t_{RST}		5/10/500 (1,2)	us
Last RE High to BUSY (at sequential read)	t_{RB}		100	ns
$\overline{CE}$ High to Ready (in case of interception by $\overline{CE}$)	t_{CRY}		60+tr(1)	ns
$\overline{CE}$ High hold time (at the last serial read)	t_{CEH}	100(3)		ns

Table 13 : AC Timing Characteristics

NOTE
1. The time to Ready depends on the value of the pull-up resistor tied to R/$\overline{B}$ pin.
2. If Reset Command (FFh) is issued at Ready state, the device goes into Busy for maximum 5 us.
3. To break the sequential read cycle. $\overline{CE}$ must be held high for a time longer than t_{CEH}

IO	Page Program	Block Erase	Read	Cache Read	CODING
0	Pass / Fail	Pass / Fail	NA	NA	Pass: '0' Fail: '1'
1	NA	NA	NA	NA	Pass: '0' Fail: '1' (Only for Cache Program, else Don't care)
2	NA	NA	NA	NA	-
3	NA	NA	NA	NA	-
4	NA	NA	NA	NA	-
5	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Busy: '0' Ready:'1'
6	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Busy: '0' Ready:'1'
7	Write Protect	Write Protect	Write Protect	NA	Protected: '0' Not Protected: '1'

Table 14 : Status Register Coding

DEVIIDENTIFIER CYCLE	DESCRIPTION
1st	Manufacturer Code
2nd	Device Identifier

Table 15 : Device Identifier Coding

Part Number	Voltage	Bus Width	1st cycle (Manufacture Code)	2nd cycle (Device Code)
H27U518S2C	3.3V	x8	ADh	76h

Table 16 : Read ID Data Table

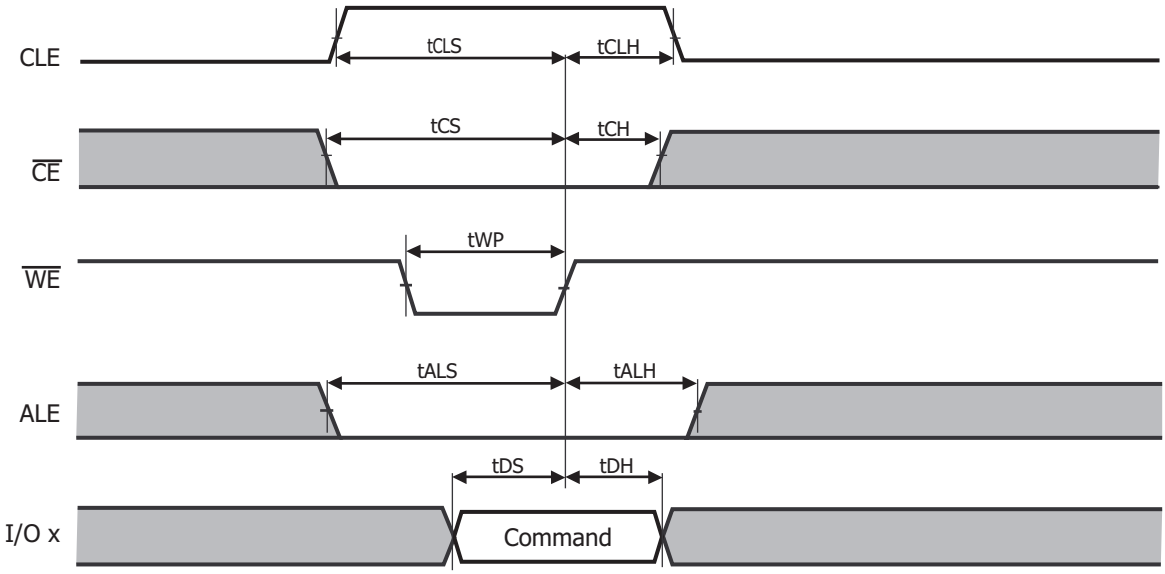


Figure 4 : Command Latch Cycle

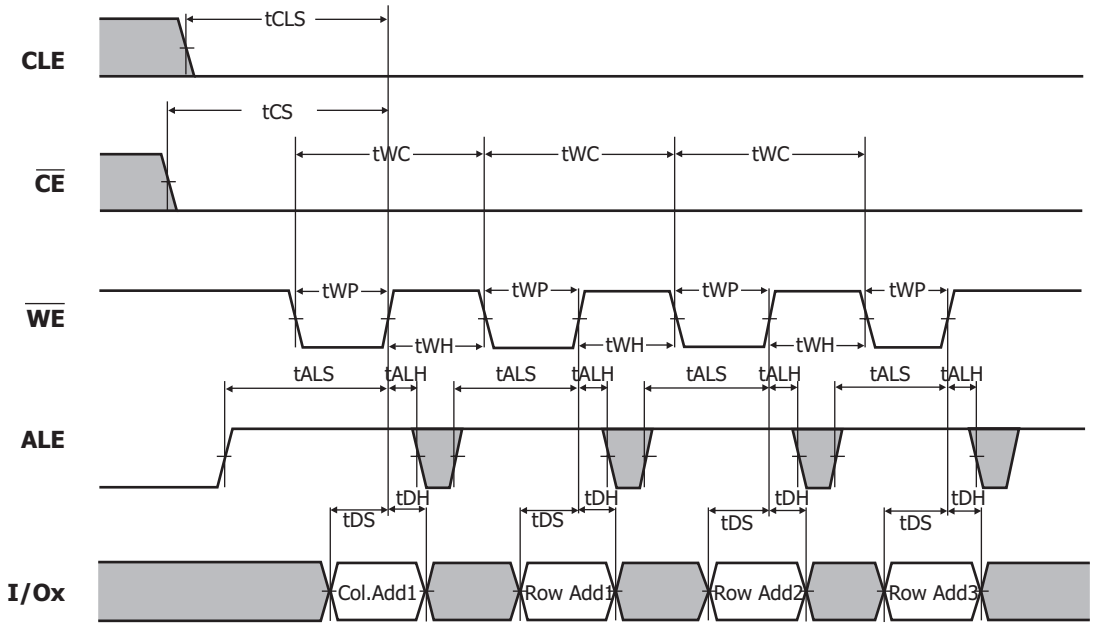
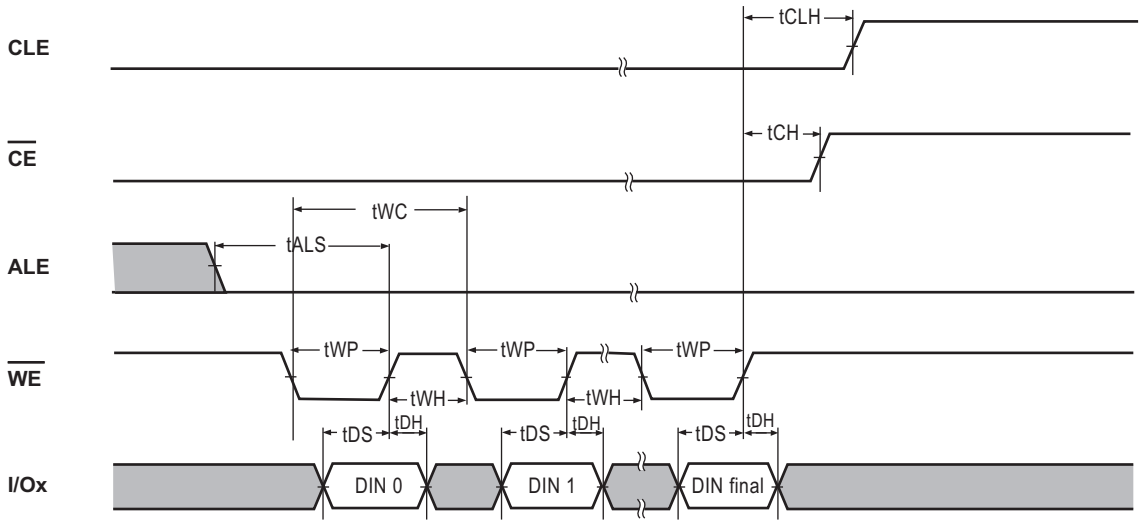
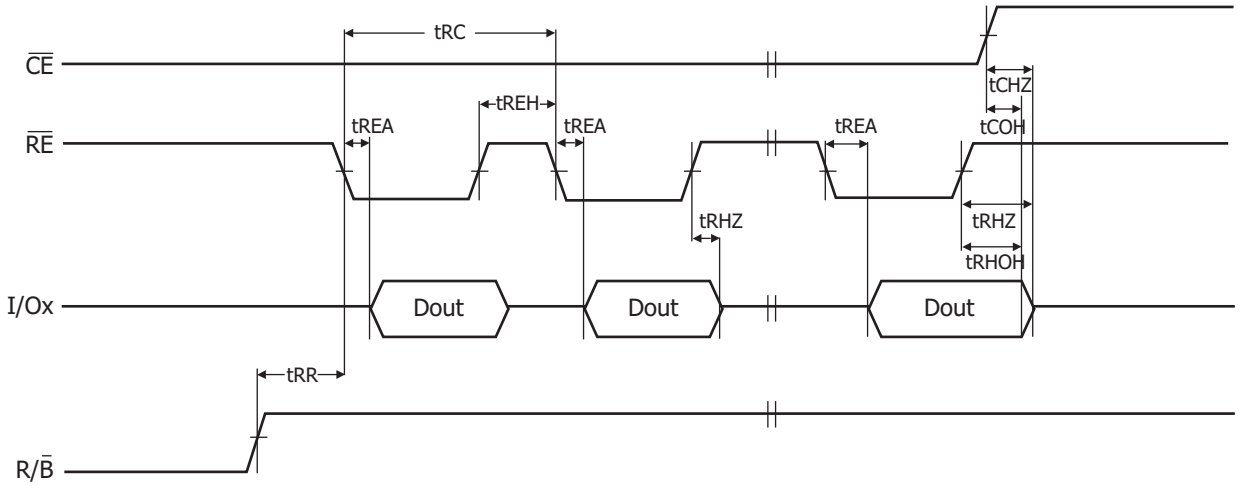


Figure 5 : Address Latch Cycle



Notes: DIN final means 2,112Bytes (x8)

Figure 6 : Input Data Latch Cycle



Notes: Transition is measured at +/-200mV from steady state voltage with load
This parameter is sampled and not 100% tested. (tCHZ, tRHZ)
tRHOH starts to be valid when frequency is lower than 33MHz.
tRLOH is valid when frequency is higher than 33MHz

Figure 7 : Sequential Out Cycle after Read (CLE = L, $\overline{WE}$ = H, ALE = L)

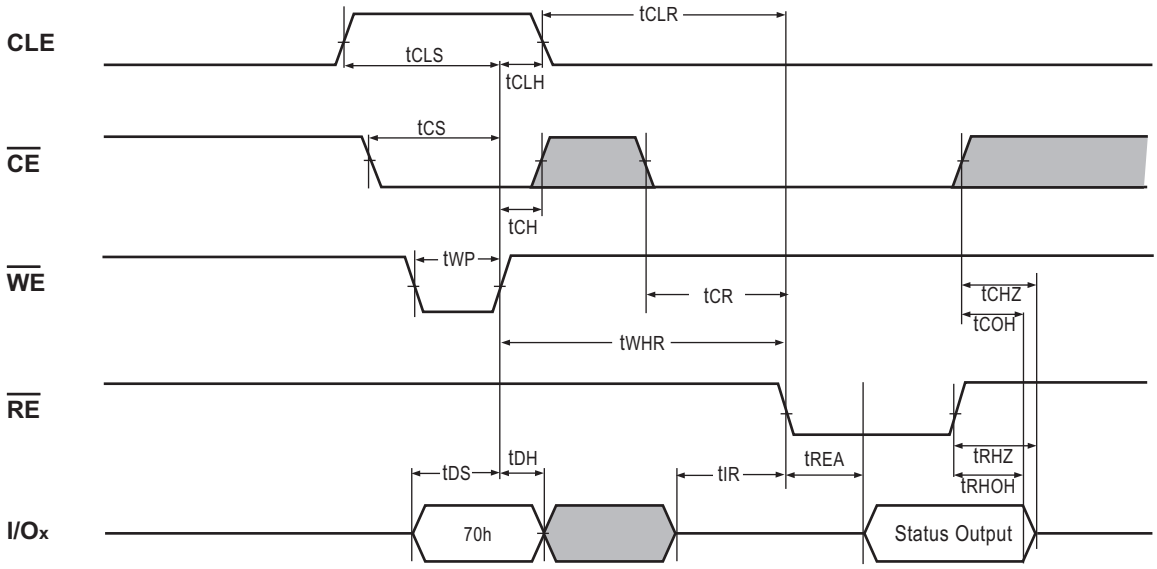


Figure 8 : Read Status Register Command Sequence and Reading

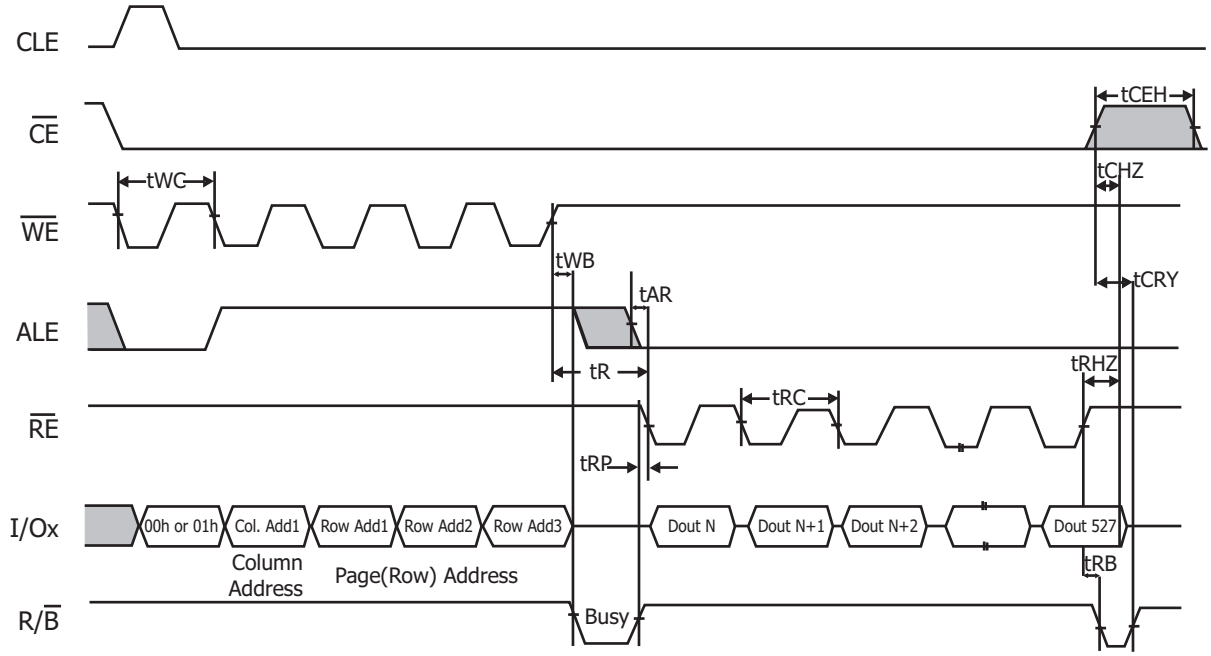


Figure 9 : Read 1 Operation (Read One Page)

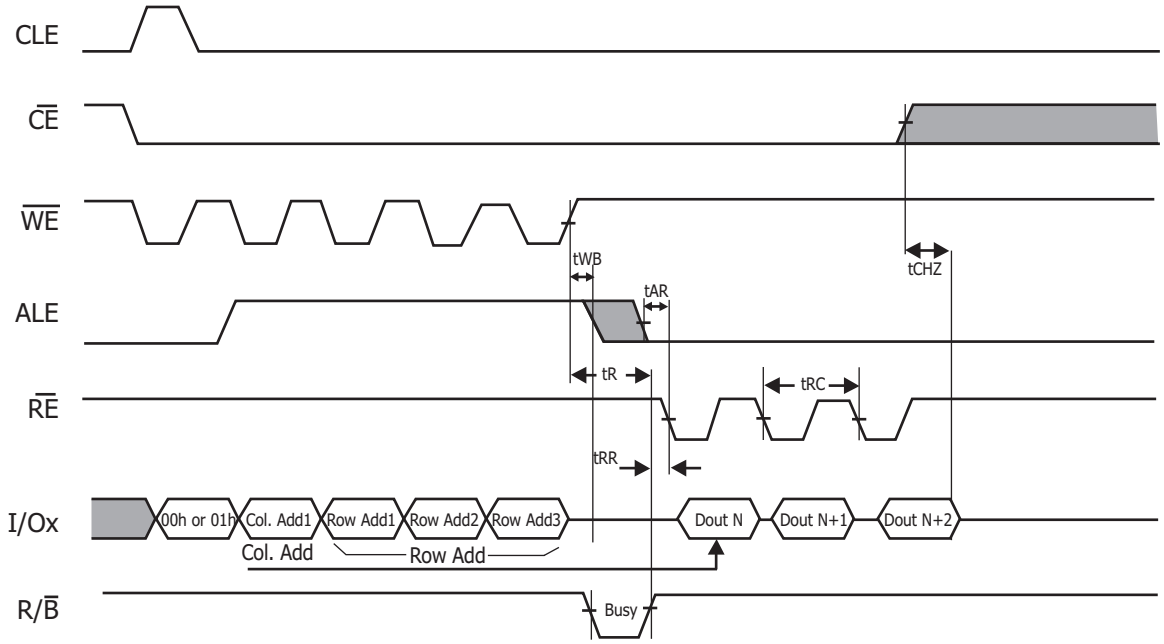


Figure 10 : Read 1 Operation Intercepted by $\overline{CE}$

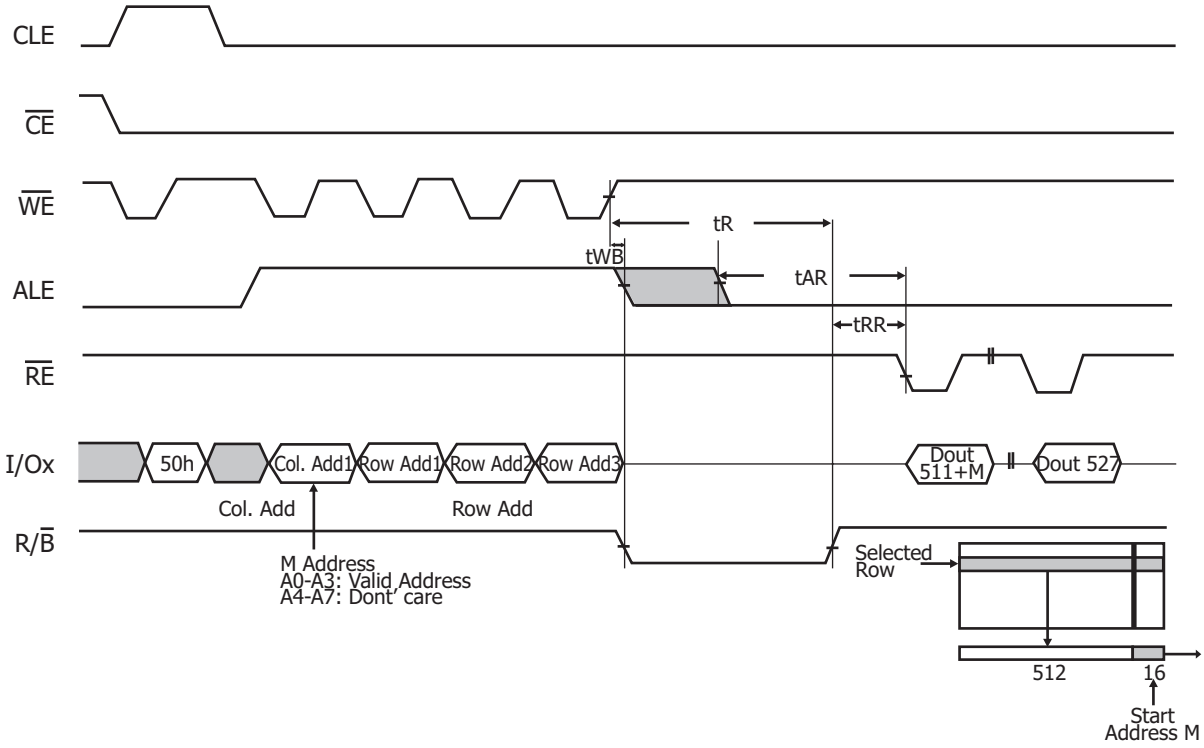
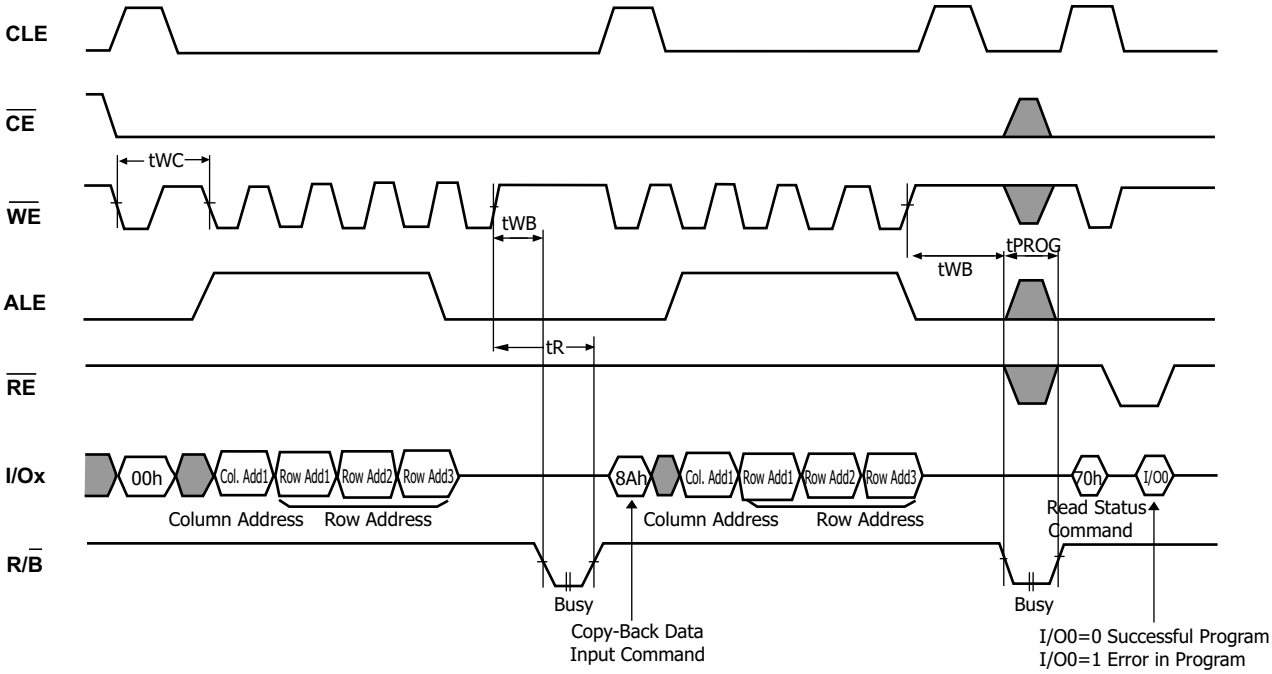


Figure 11 : Read 2 Operation (Read One Page)



Note : tADL is the time from the WE# rising edge of final address cycle to the WE# rising edge fo first data cycle.

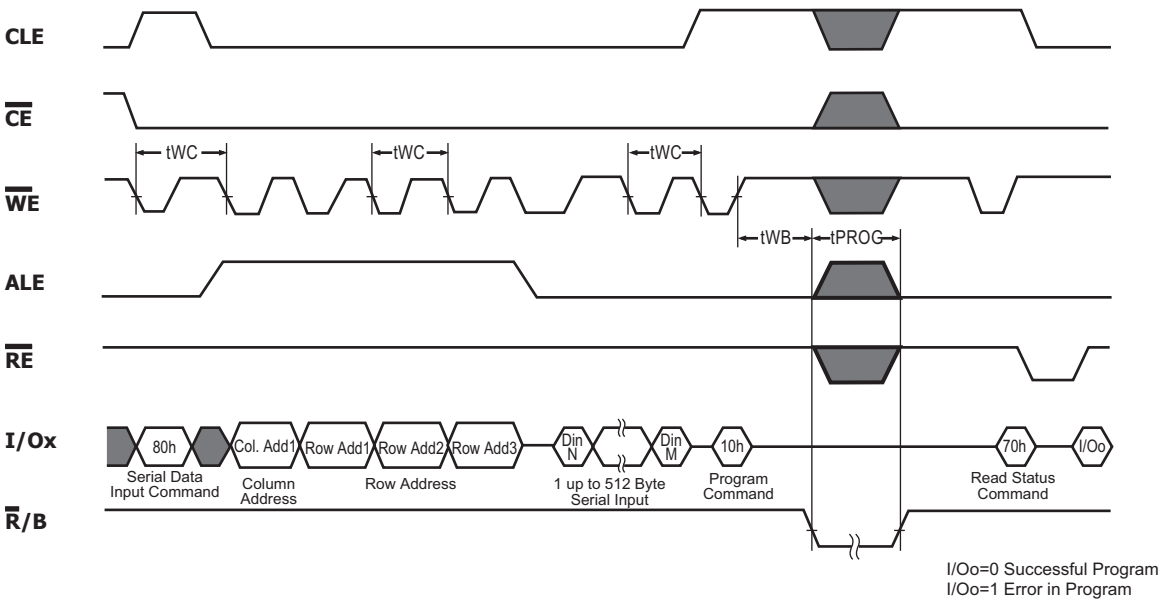


Figure 12 : Page Program Operation

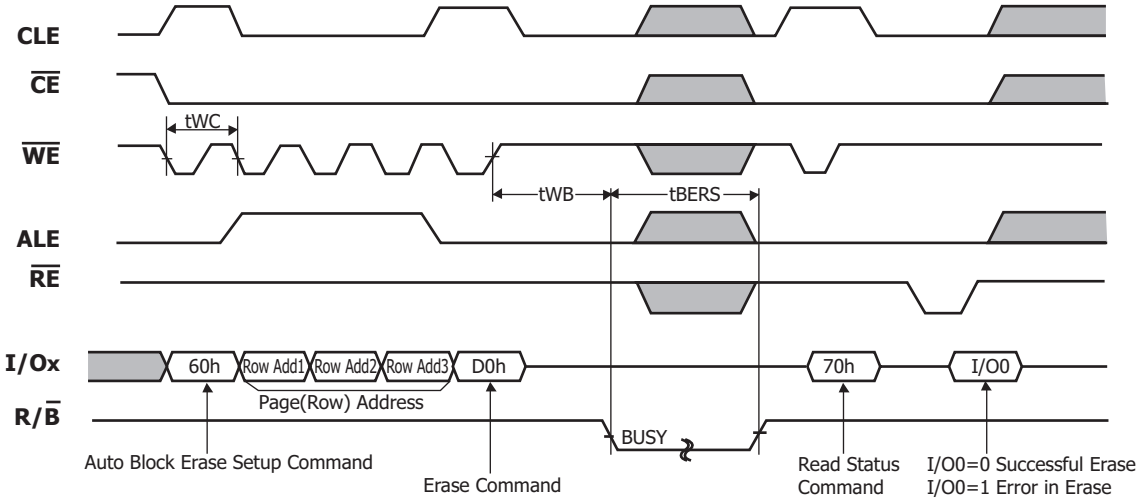
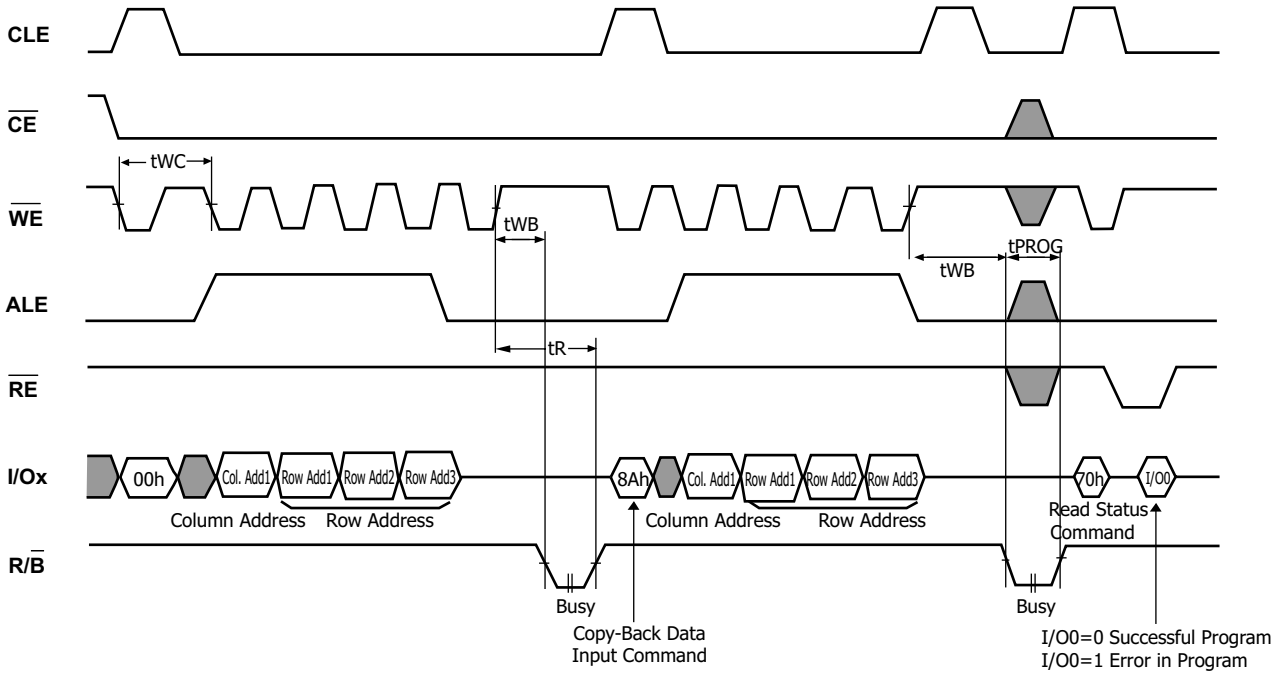


Figure 13 : Block Erase Operation (Erase One Block)



Note : tADL is the time from the WE# rising edge of final address cycle to the WE# rising edge fo first data cycle.

Figure 14 : Copy Back Program

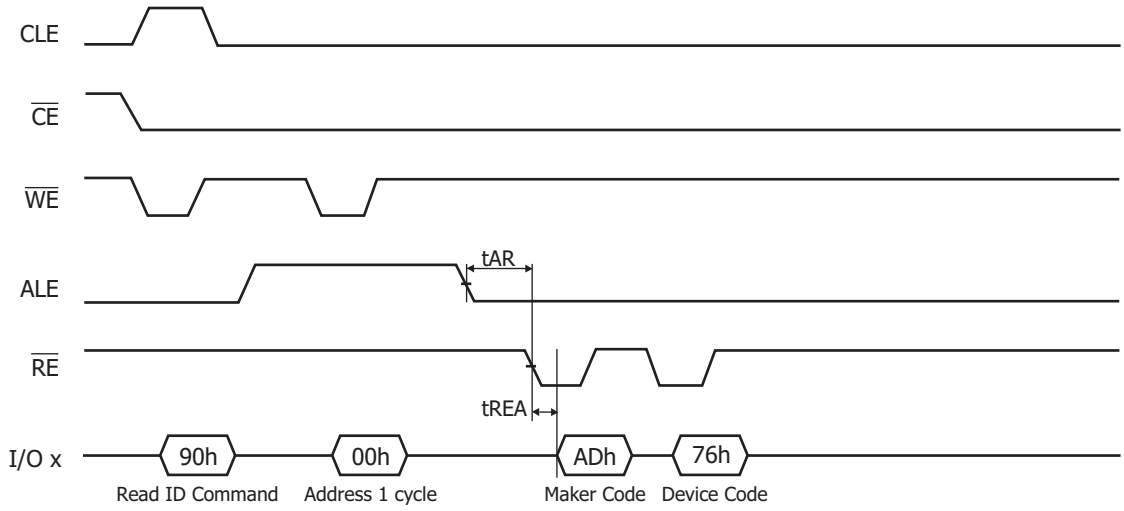


Figure 15 : Read ID Operation

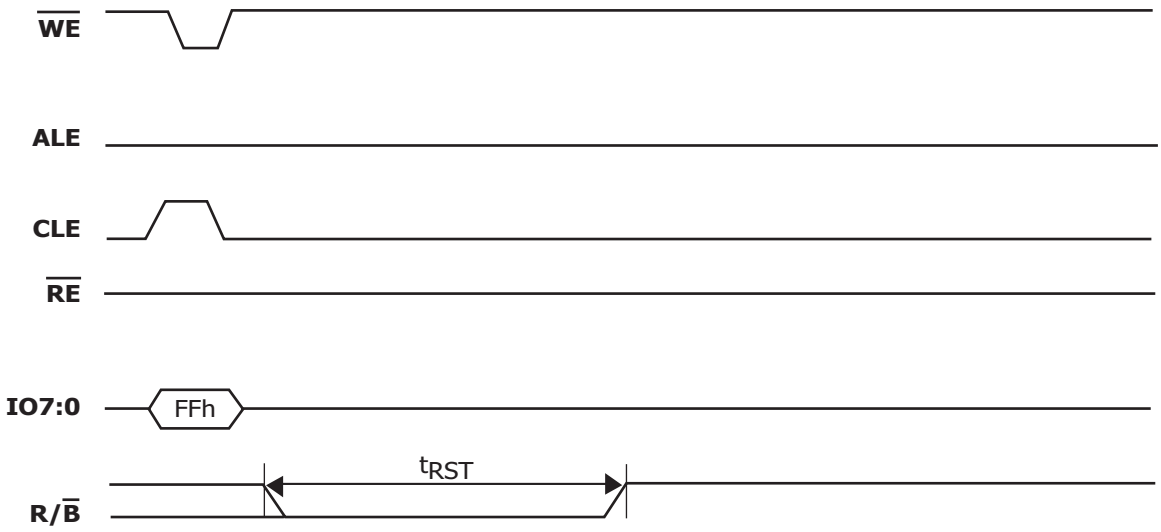


Figure 16 : Reset Operation

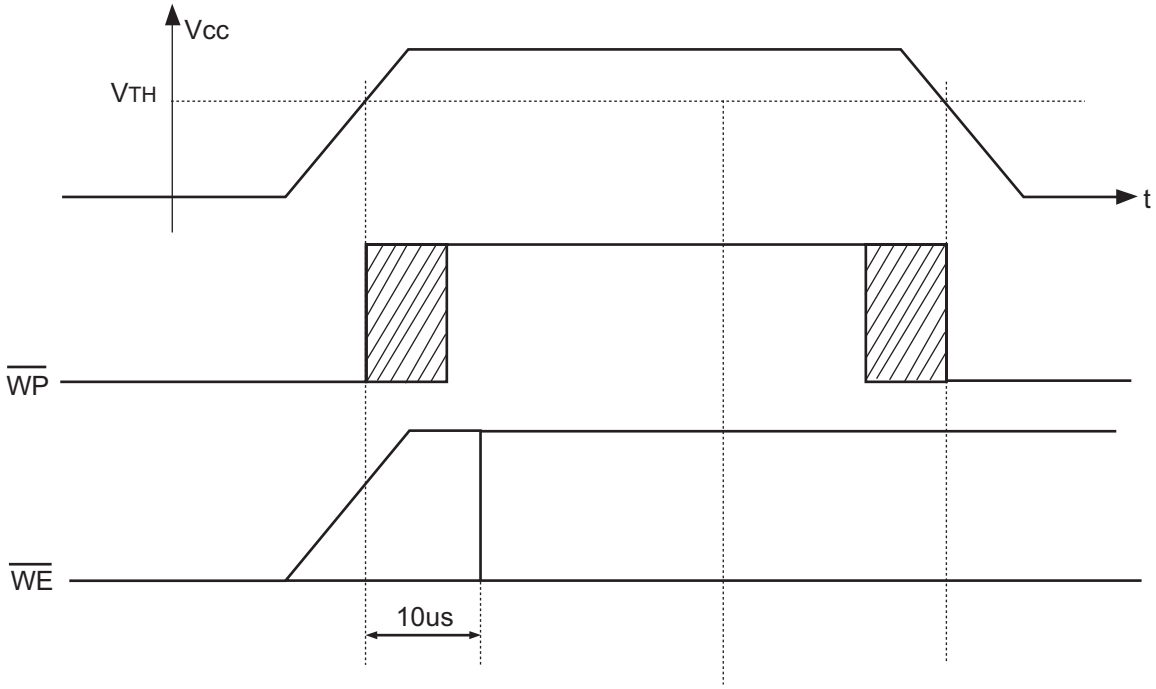


Figure 17 : Power On and Data Protection Timing

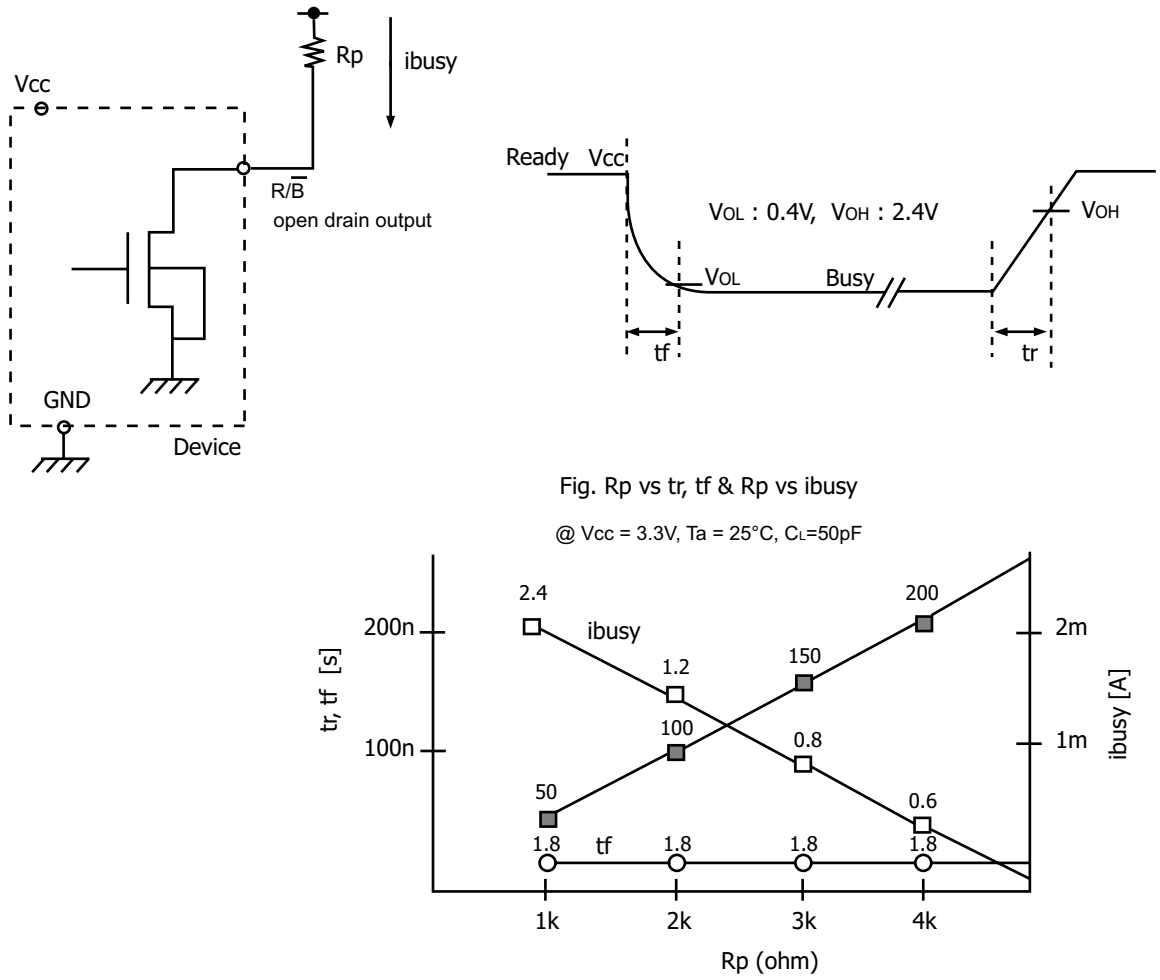


Fig. Rp vs tr, tf & Rp vs ibusy

Rp value guidence

$$Rp\ (min) = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \sum I_L} = \frac{3.2V}{8mA + \sum I_L}$$

where IL is the sum of the input currents of all devices tied to the R/B pin.

Rp(max) is determined by maximum permissible limit of tr

Figure 18 : Ready / Busy Pin Electrical Specifications

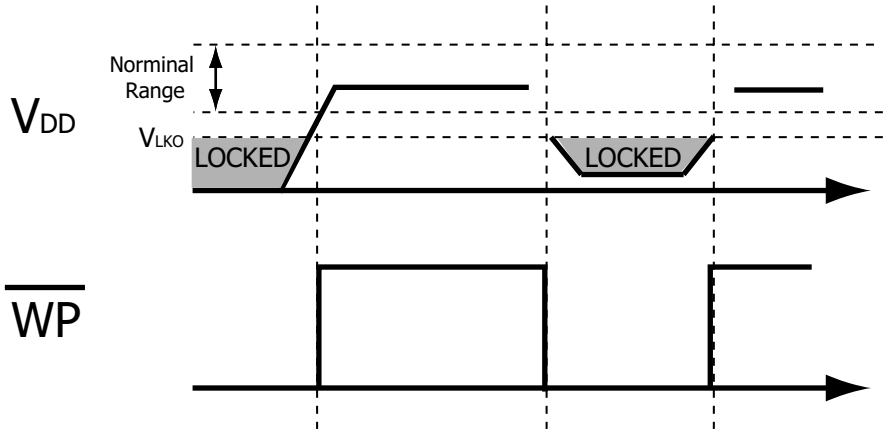


Figure 21 : Data Protection in relation to V_{DD} value

NOTE : V_{LKO} = 1.8 V

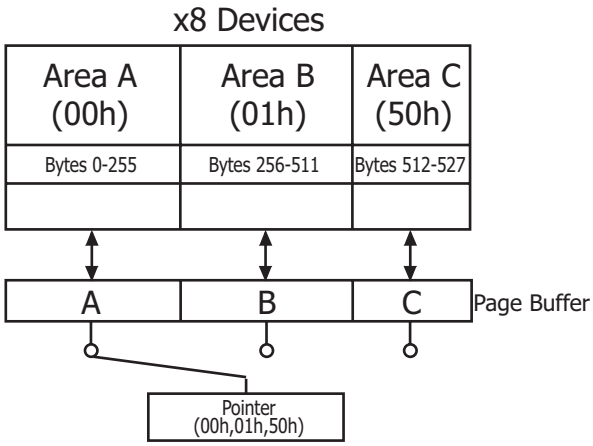


Figure 19 : Pointer Operations

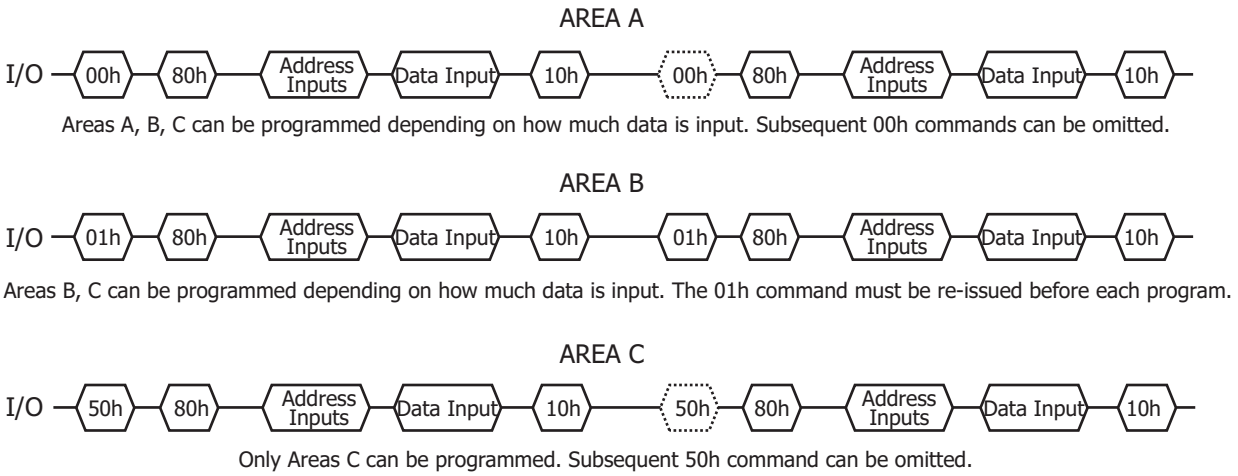


Figure 20 : Pointer Operation for Programming

Bad Block Management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased(FFh). The Bad Block Information is written prior to shipping. Any block where the 1st Byte in the spare area of the 1st or 2nd th page (if the 1st page is Bad) does not contain FFh is a Bad Block. The Bad Block Information must be read before any erase is attempted as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information it is recommended to create a Bad Block table following the flowchart shown in Figure 22. The 1st block, which is placed on 00h block address is guaranteed to be a valid block.

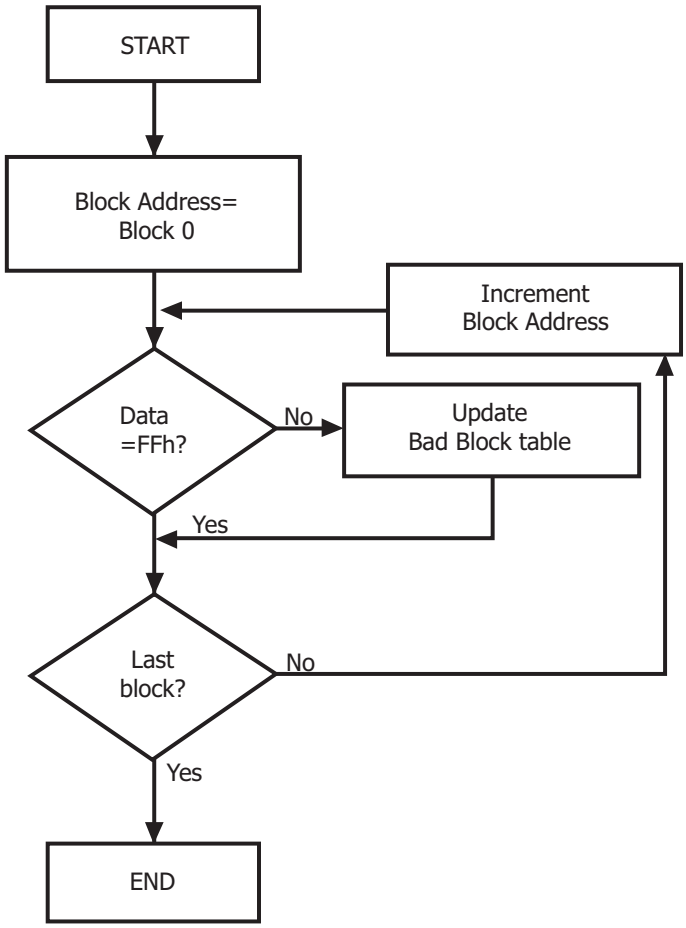


Figure 22 : Bad Block Management Flowchart

Bad Block Replacement

Over the lifetime of the device additional Bad Blocks may develop. In this case the block has to be replaced by copying the data to a valid block. These additional Bad Blocks can be identified as attempts to program or erase them will give errors in the Status Register.

Unlike the case of odd page which carries a possibility of affecting previous page, the failure of a page program operation does not affect the data in other pages in the same block, the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block.

Refer to Table 17 and Figure 23 for the recommended procedure to follow if an error occurs during an operation.

Operation	Recommended Procedure
Erase	Block Replacement
Program	Block Replacement
Read	ECC (with 1bit/528byte)

Table 17 : Block Failure

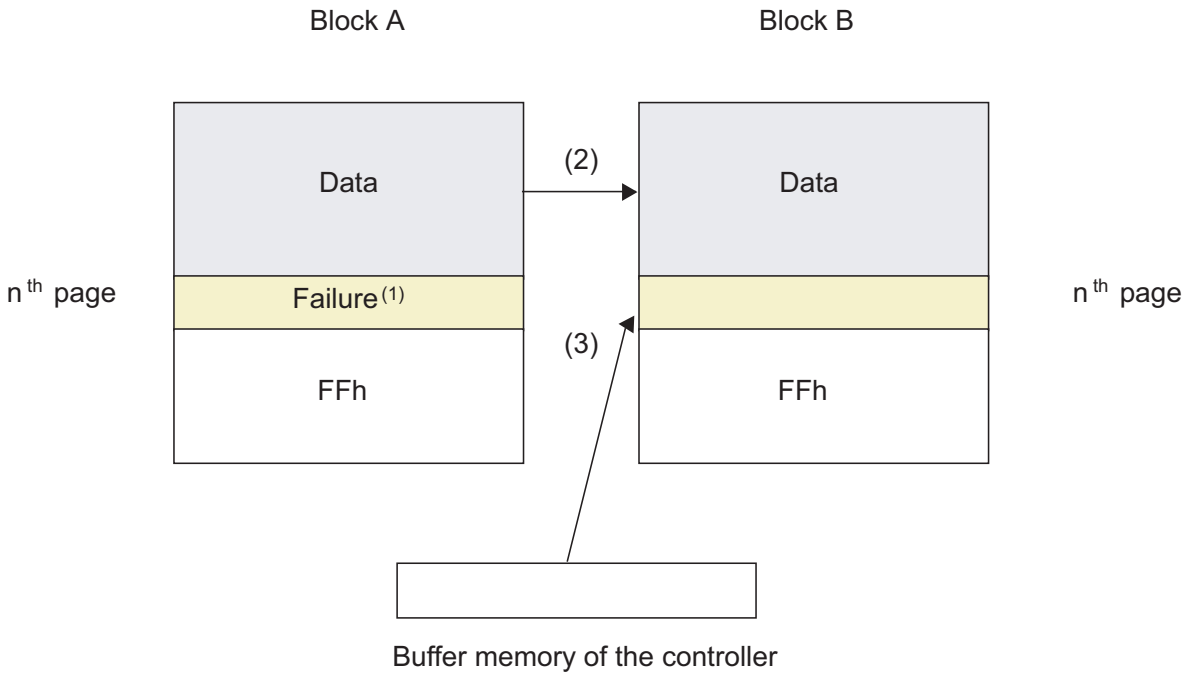


Figure 23 : Bad Block Replacement

NOTE :
1. An error occurs on n^{th} page of the Block A during program or erase operation.
2. Data in Block A is copied to same location in Block B which is valid block.
3. N^{th} data of block A which is in controller buffer memory is copied into n^{th} page of Block B
4. Bad block table should be updated to prevent from eraseing or programming Block A

Write Protect Operation

The Erase and Program Operations are automatically reset when $\overline{WP}$ goes Low (t_{WW} = 100 ns, min). The operations are enabled and disabled as follows (Figure 24 ~ 27)

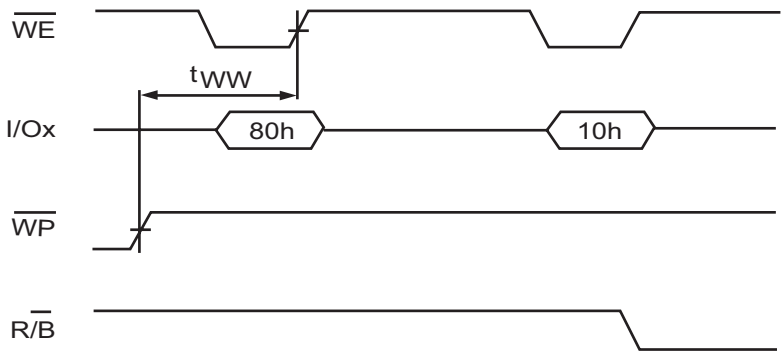


Figure 24 : Enable Programming

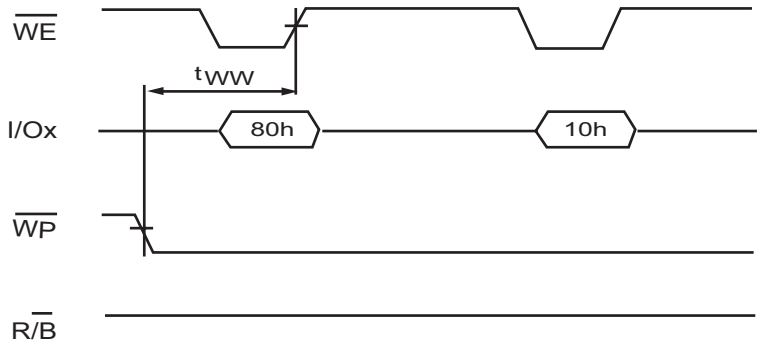


Figure 25 : Disable Programming

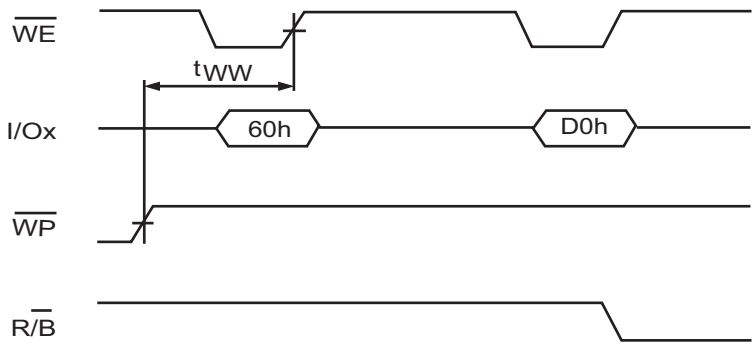


Figure 26 : Enable Erasing

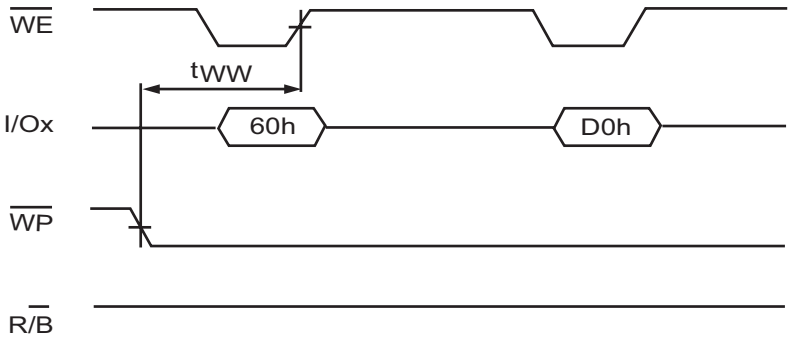


Figure 27 : Disable Erasing

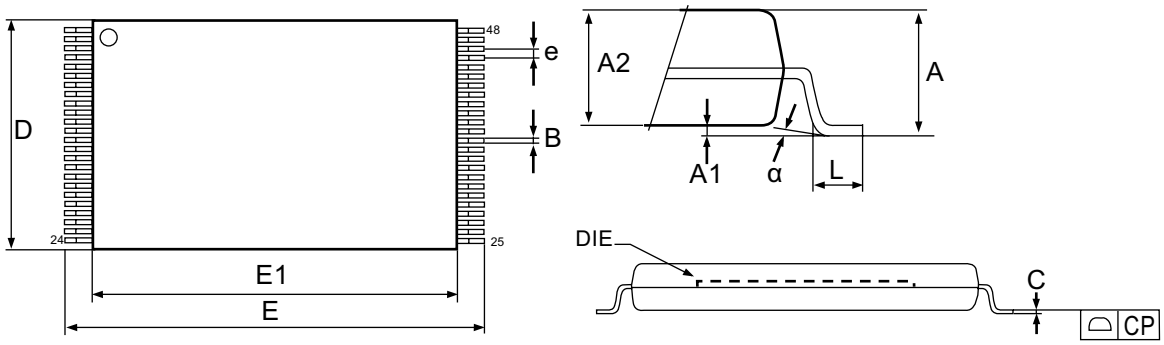


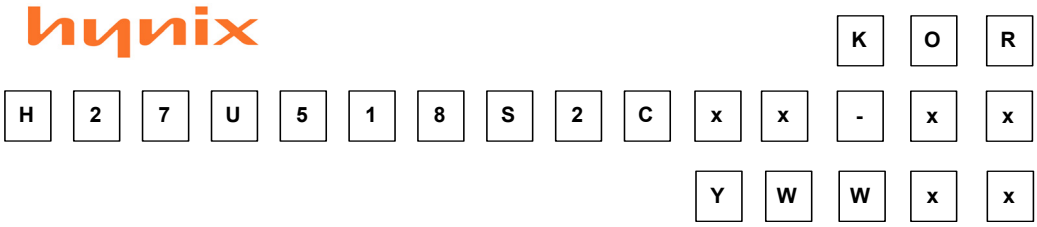
Figure 28 : 48-TSOP1 - 48-lead Plastic Thin Small Outline, 12 x 20mm, Package Outline

Symbol	millimeters		
	Min	Typ	Max
A			1.200
A1	0.050		0.150
A2	0.980		1.030
B	0.170		0.250
C	0.100		0.200
CP			0.100
D	11.910	12.000	12.120
E	19.900	20.000	20.100
E1	18.300	18.400	18.500
e		0.500	
L	0.500		0.680
alpha	0		5

Table 18 : 48-TSOP1 - 48-lead Plastic Thin Small Outline, 12 × 20 mm Package Mechanical Data

MARKING INFORMATION - TSOP1

Marking Example



- hynix	: Hynix Symbol
- KOR	: Origin Country
- H27U518S2Cxx-xx	: Part Number
H: Hynix	
27: NAND Flash	
U: Power Supply	: U (2.7 V ~ 3.6 V)
51: Density	: 512 Mbit
8 : Bit Organization	: 8(x8)
S: Classification	: Single Level Cell + Single Die + Small Block
2: Mode	: 2(1nCE & 1R/nB; Sequential Row Read Disable)
C: Version	: 3rd Generation
x: Package Type	: T(48-TSOP1)
x: Package Material	: Blank(Normal), R(Lead & Halogen Free)
x: Bad Block	: B(Included Bad Block), S(1~5 Bad Block), P(All Good Block)
x: Operating Temperature	: C(0℃ ~70℃), I(-40℃ ~85℃)

- **Y:** Year (ex: 8=year 2008, 9= year 2009)
- **ww:** Work Week (ex: 12= work week 12)
- **xx:** Process Code

Note

- Capital Letter	: Fixed Item
- Small Letter	: Non-fixed Item