CY8CMBR2010

CapSense® Express™ 10-Button Controller

Features

- Easy to use capacitive button controller
  - Ten-button solution configurable through Hardware straps
  - No software tools or programming required
  - Ten general-purpose outputs (GPO)
  - GPOs linked to CapSense buttons
  - GPOs support direct LED drive
- SmartSense™ Auto-Tuning
  - Maintains optimal button performance even in noisy environment
  - CapSense parameters dynamically set in runtime
  - Saves time and effort in device tuning
  - Wide parasitic capacitance (C_P) range (5 pF - 40 pF)
- Noise Immunity
  - Specifically designed for superior noise immunity to external radiated and conducted noise
  - Low radiated noise emission
- System Diagnostics of CapSense buttons - reports faults at device power up
  - Button shorts
  - Improper value of modulator capacitor (C_{MOD})
  - Out of range $C_P$value
- Advanced features
  - Robust sensing even with closely spaced buttons - flanking sensor suppression (FSS)
  - User-configurable LED Effects
    - On-system power-on
    - LED ON Time after button release
  - Supports analog voltage output (requires external resistors)
  - Serial Debug Data output
    - Simplifies production-line testing and system debug
- Wide operating voltage range
  - 1.71 V to 5.5 V – ideal for both regulated and unregulated battery applications
- Low power consumption
  - Average current consumption of 21 µA [1] per button
  - Deep sleep current: 100 nA
- Industrial temperature range: –40 °C to +85 °C
- 32-pin Quad Flat No leads (QFN) package (5 mm × 5 mm × 0.6 mm)

Overview

The CY8CMBR2010 CapSense Express™ capacitive touch sensing controller saves time and money, quickly enabling a capacitive touch sensing user interface in your design. It is a hardware-configurable device and does not require any software tools, firmware coding, or device programming. This device is enabled with Cypress's revolutionary SmartSense™ Auto-Tuning algorithm. SmartSense™ Auto-Tuning ends the need to manually tune the user interface during development and production ramp. This speeds the time to volume and saves valuable engineering time, test time and production yield loss.

The CY8CMBR2010 CapSense controller supports up to ten capacitive touch sensing buttons and ten General Purpose Outputs (GPO). The GPO is an active low output controlled directly by the CapSense input making it ideal for a wide variety of consumer, industrial, and medical applications. The wide operating range of 1.71 V to 5.5 V enables unregulated battery operation, further saving component cost. The same device can also be used in different applications with varying power supplies.

This device supports ultra low-power consumption in both run mode and deep sleep modes to stretch battery life. In addition, this device also supports many advanced features which enhance the robustness and user interface of the end solution. Some of the key advanced features include Noise Immunity and FSS. Noise Immunity improves the immunity of the device against radiated and conducted noise, such as audio and radio frequency (RF) noise. FSS provides robust sensing even with closely spaced buttons. FSS is a critical requirement in small form factor applications.

Power-on LED effects provide a visual feedback to the design at power-on. This improves the aesthetic value of the end product. System Diagnostics test for design faults at power-on and report any failures. This simplifies production line testing and reduces manufacturing costs. Serial Debug data output gives the critical information about the design, such as button C_P and signal-to-noise ratio (SNR). This further helps in production line testing.

Note

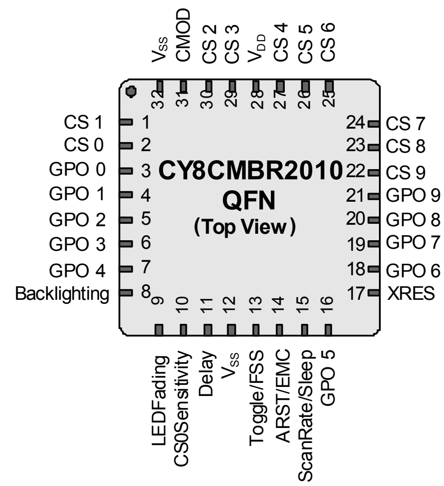
1. 21 µA per button (4-buttons used, 3% touch time, 10 pF < Cp of all buttons < 20 pF, Button Scan Rate = 556 ms, with power consumption optimized, Noise Immunity level "Normal", CS0 sensitivity "High").

Contents

Pinout

Table 1. Pin Diagram and Definitions – CY8CMBR2010

Pin	Label	Type [2]	Description	If Unused
1	CS1	AI	CapSense button input, controls GPO1	Ground
2	CS0	AI	CapSense button input, controls GPO0	Ground
3	GPO0	DO	GPO activated by CS0	Leave open
4	GPO1	DO	GPO activated by CS1	Leave open
5	GPO2	DO	GPO activated by CS2	Leave open
6	GPO3	DO	GPO activated by CS3	Leave open
7	GPO4	DO	GPO activated by CS4	Leave open
8	Backlighting	DO	GPO controlled by CS0–CS9 when analog output voltage is enabled	Leave open
9	LEDFading	AI	Controls the Power-on LED effects and Analog Voltage Output	Leave open
10	CS0Sensitivity	AI	Controls the Sensitivity and Debounce values of CS0	Ground
11	Delay	AI	Controls the LED ON time and serial debug data out	Ground
12	V_{SS}	P	Ground	N/A
13	Toggle/FSS	AI	Controls the enabling/disabling of Toggle ON/OFF and FSS	Ground
14	ARST/EMC	AI	Controls the Button Auto Reset period, enabling / disabling Noise Immunity technique	Ground
15	ScanRate/Sleep	DI	Controls the button scan rate	Ground
16	GPO5	DO	GPO activated by CS5	Leave open
17	XRES	DI	Device reset, active high input, with internal pull down	Leave open
18	GPO6	DO	GPO activated by CS6	Leave open
19	GPO7	DO	GPO activated by CS7	Leave open
20	GPO8	DO	GPO activated by CS8	Leave open
21	GPO9	DO	GPO activated by CS9	Leave open
22	CS9	AI	CapSense button input, controls GPO9	Ground
23	CS8	AI	CapSense button input, controls GPO8	Ground
24	CS7	AI	CapSense button input, controls GPO7	Ground
25	CS6	AI	CapSense button input, controls GPO6	Ground
26	CS5	AI	CapSense button input, controls GPO5	Ground
27	CS4	AI	CapSense button input, controls GPO4	Ground
28	V_{DD}	P	Power	N/A
29	CS3	AI	CapSense button input, controls GPO3	Ground
30	CS2	AI	CapSense button input, controls GPO2	Ground
31	C_{MOD}	AI	External modulator capacitor, recommended value 2.2 nF (±10%)	N/A
32	V_{SS}	P	Ground	N/A

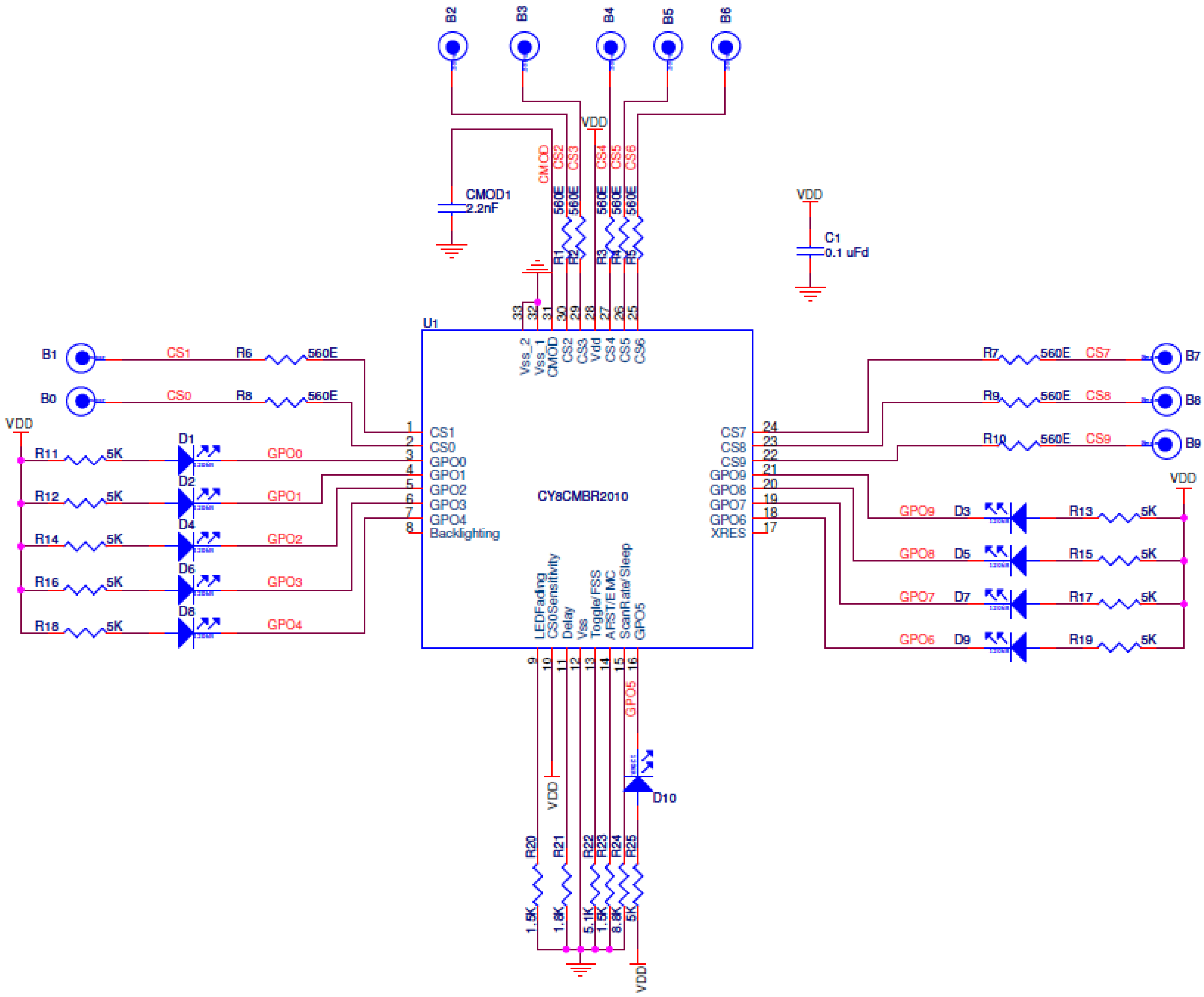


Note
2. AI – Analog Input; DI – Digital Input; DO – Digital Output; P – Power

Typical Circuits

Schematic #1: Ten Buttons with Ten GPOs

Figure 1. CY8CMBR2010 Schematic 1

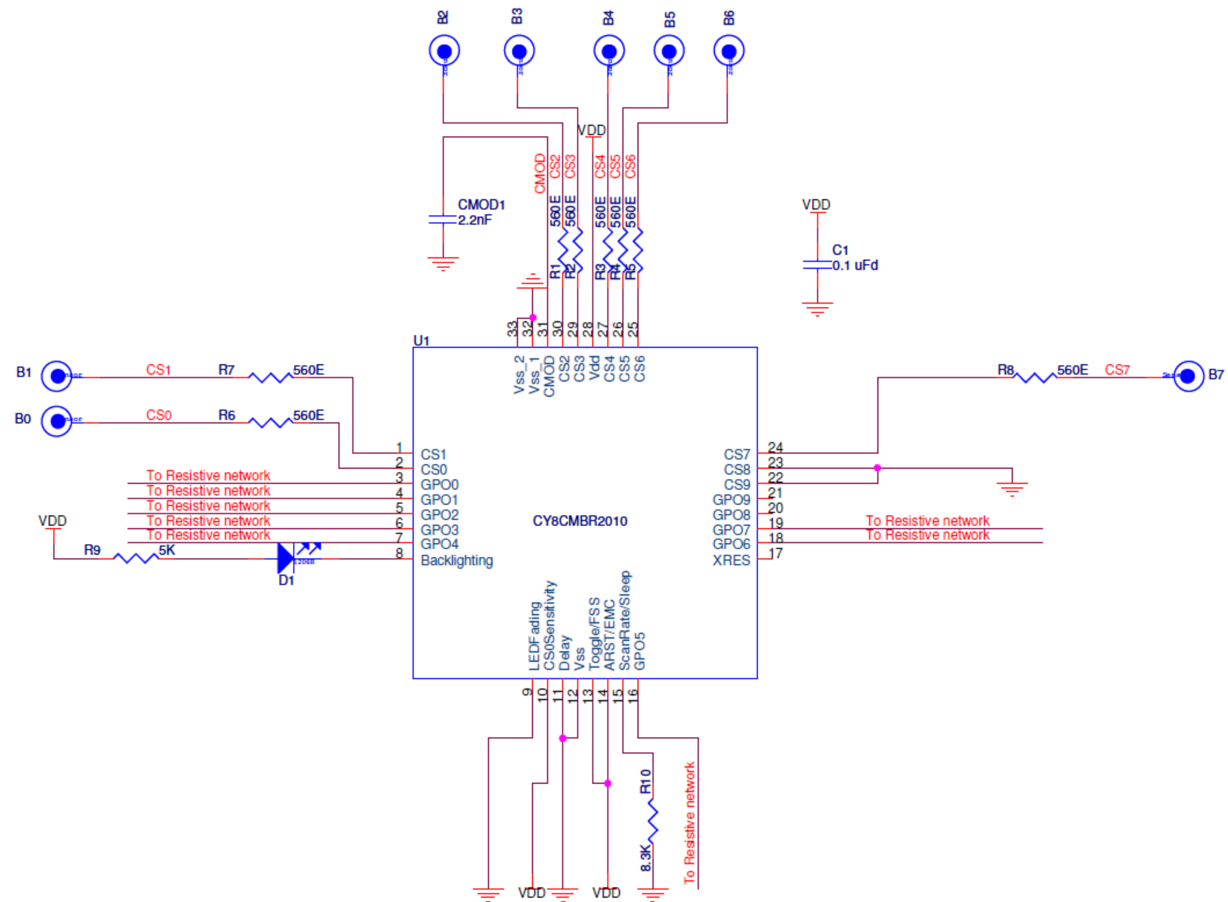


In Figure 1, the device is configured in the following manner:

- CS0-CS9 pins: 560 Ω to CapSense buttons
  - Ten CapSense buttons (CS0 - CS9)
- GPO0-GPO9 pins: LED and 5 kΩ to V_{DD}
  - CapSense buttons driving 10 LEDs (GPO0-GPO9)
- C_{MOD} pin: 2.2 nF to Ground
  - Modulator capacitor
- XRES pin: Floating
  - For external reset
- Toggle/FSS pin: 5.1 kΩ to Ground
  - Toggle ON/OFF disabled
  - Flanking sensor suppression (FSS) enabled
- ARST/EMC pin: 1.5 kΩ to Ground
  - Button Auto Reset enabled
  - Noise Immunity level “Normal”
- LEDFading pin: 1.5 kΩ to Ground
  - Analog Voltage Support disabled
  - Power-on LED effects sequence 1
- Backlighting pin: Floating
  - No LED Backlighting output, as Analog Voltage Support disabled
- Delay pin: 1.8 kΩ to Ground
  - LED ON Time of 1000 ms
  - Serial Debug Data out disabled
- CS0Sensitivity pin: V_{DD}
  - CS0 Sensitivity “Low”
  - CS0 Debounce = 99
- ScanRate/Sleep pin: 8.8 kΩ to Ground
  - Power consumption optimization
  - User configured scan rate = 298 ms

Schematic #2: Eight Buttons with Analog Voltage Output

Figure 2. CY8CMBR2010 Schematic 2



In Figure 2, the device is configured in the following manner:

- CS0 - CS7 pins: 560 Ω to CapSense buttons; CS8, CS9 pins: Ground
  - Eight CapSense buttons (CS0 - CS7)
  - CS8, CS9 buttons not used in design
- GPO0-GPO9 pins: Connect to external resistive network
  - Eight GPOs (GPO0 - GPO7) used for Analog Voltage Output
  - GPO8, GPO9 not used in design
- C_{MOD} pin: 2.2 nF to Ground
  - Modulator capacitor
- XRES pin: Floating
  - For external reset
- Toggle/FSS pin: V_{DD}
  - Toggle ON/OFF enabled
  - Flanking sensor suppression (FSS) enabled
- ARST/EMC pin: V_{DD}
  - Button Auto Reset enabled
  - Noise Immunity level "High"
- LEDFading pin: Ground
  - Analog Voltage Support enabled
  - Power-on LED effects disabled
- Backlighting pin: LED and 5 kΩ to V_{DD}
  - LED Backlighting output, as Analog Voltage Support enabled
- Delay pin: Ground
  - LED ON Time disabled
  - Serial Debug Data out disabled
- CS0Sensitivity pin: V_{DD}
  - CS0 Sensitivity "Low"
  - CS0 Debounce = 99
- ScanRate/Sleep pin: 8.3 kΩ to Ground
  - Power consumption optimization
  - User configured scan rate = 210 ms

Configuring the CY8CMBR2010

The CY8CMBR2010 device features are configured using external resistors.

The resistors on the hardware configurable pins are determined by the device upon power-on.

The Appendix on page 28 gives the matrix of features enabled using different external resistor configurations.

To know more about the required settings for your design, refer to the CY8CMBR2010 Design Guide.

Device Features

CapSense Buttons

- Supports up to ten CapSense buttons.
- Ground the CSx pin to disable CapSense button input.
- A 2.2 nF (±10%) capacitor must be connected on the C_{MOD} pin for proper CapSense operation.
- For proper CapSense operation, ensure C_P of each button is less than 40 pF.

SmartSense™ Auto-Tuning

- Supports auto-tuning of CapSense parameters
- No manual tuning required; all parameters are automatically tuned by the device.
- Reduces the design cycle time.
  - No manual tuning.
- Ensures portability of the user interface design.
- Compensates Printed Circuit Board (PCB) variations, Device process variations, and PCB vendor changes.

General-Purpose Outputs

- GPOx pin outputs are strong drive[3]
- The GPOx is controlled by the corresponding CSx
- Active low output – supports sinking configuration for LEDs (see Figure 3)
- If CSx is disabled (grounded), then the corresponding GPOx must be left floating
- A 5-ms pulse is sent after 350 ms (if Noise Immunity level is “Normal”) / 1000 ms (if Noise Immunity level is “High”) after power-up on the GPOx if the CSx fails the System Diagnostics

Figure 3. Example of GPO0 Driven by CS0

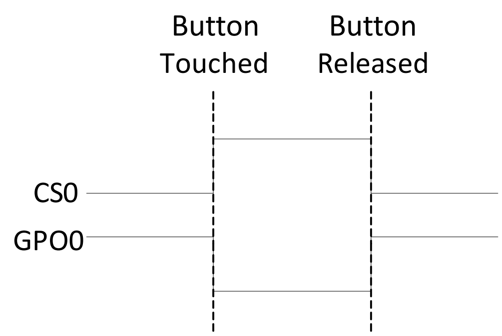


Table 2. Advanced Features Supported by CY8CMBR2010

Feature	Benefit
Toggle ON/OFF	Button retains state on touch (ON/OFF)
Flanking Sensor Suppression (FSS)	Helps in distinguishing closely spaced buttons
Noise Immunity	Improves device immunity to external noise (such as RF noise)
LED ON Time	Gives an LED effect on button release
Button Auto Reset	Disables false output trigger, due to conducting object placed close to button
Power-on LED Effects	Provides visual effects to design at power-on
Analog Voltage Support	External resistors can be used with GPOs to generate analog voltage output
LED Backlighting	Common GPO available for LED drive if Analog Voltage Support enabled
Sensitivity Control for CS0 Button and Debounce Control for CS0 Button	Useful for special function buttons such as power button
System Diagnostics	Support for production testing and debugging
Serial Debug Data	Support for production testing and validating design
Low Power Sleep Mode and Deep Sleep Mode	Low power consumption

Note

3. When a pin is in strong drive mode, it is pulled up to V_{DD} when the output is HIGH and pulled down to Ground when the output is LOW.

Toggle ON/OFF

- Toggles the GPO state at each button touch (see Figure 4).
- Used for mechanical button replacement. For example, wall switch.

Flanking Sensor Suppression (FSS)

- Helps in distinguishing closely spaced buttons.
- Also used in situations with buttons having opposite functions. For example, an interface with two buttons for brightness control (UP or DOWN).
- FSS action can be explained for following different scenarios:

1. When only one button is touched, it is reported as ON. See Figure 5.
2. When more than one button is detected as ON and previously one of those buttons was touched, then the previously touched button is reported as ON. See Figure 6.

Noise Immunity

- Improves the immunity of the device against external radiated and conducted noise.
- Reduces the radiated noise emission.
- Possible Noise Immunity levels are “Normal” and “High”.

LED ON Time

- Provides better visual feedback when a button is released and improves the design’s aesthetic value.
- The GPOx is driven low for a specified interval after the corresponding CSx button is released (see Figure 7).
- When a button gets reset (refer to Button Auto Reset on page 8), LED ON Time is not applied on the corresponding GPO.
- Applicable to the GPO of the last button released.
- In Figure 8 on page 8, GPO0 goes high prematurely (prior to LED ON Time expiration) because CS1 button is released. Therefore, the LED ON Time counter is reset. Now, GPO1 remains low for LED ON Time after releasing CS1.
- LED ON time can range from 0–2000 ms.
- LED ON time resolution is 20 ms.

Figure 4. Example of Toggle ON/OFF Feature on GPO0

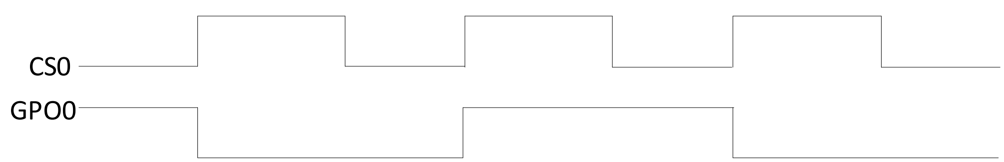
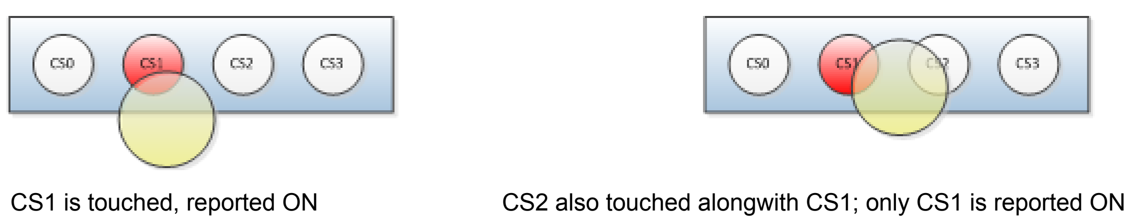


Figure 5. FSS when only one button is touched

Figure 6. FSS when multiple buttons are touched with one button ON previously



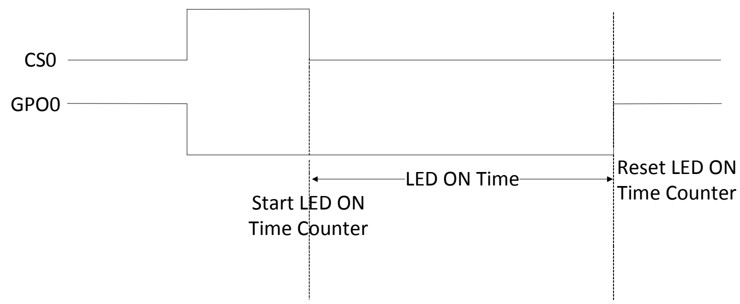


Figure 7. Example LED ON timing diagram on GPO0

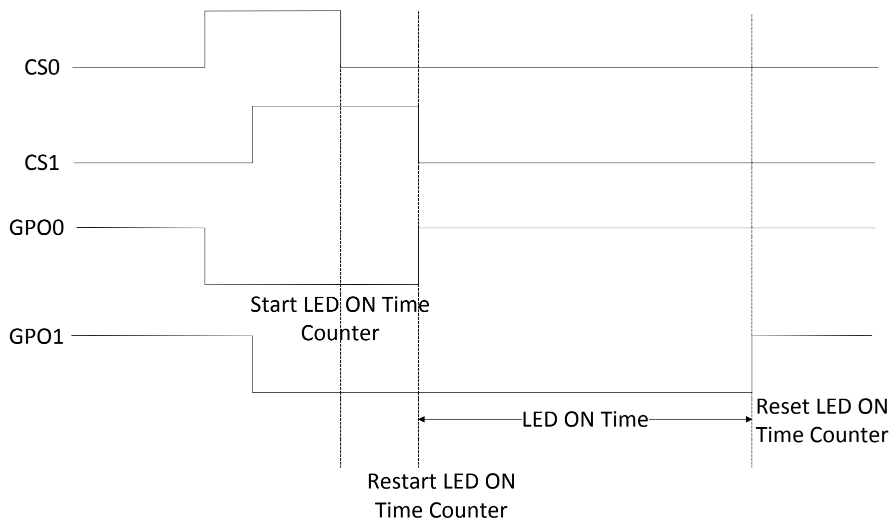


Figure 8. Example LED ON Timing Diagram on GPO0 and GPO1

Button Auto Reset

- Prevents button stuck, due to metal object placed close to button.
- Useful when GPO output to be kept on only for a specific time.
- If enabled, the GPOx is driven for a maximum of ARST time when CSx is continuously touched. See Figure 9.
- Auto reset period is 20 s.

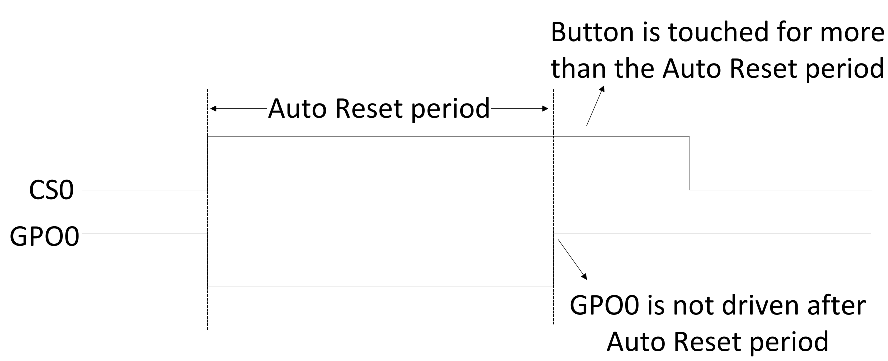


Figure 9. Example of Button Auto Reset on GPO0

Power-on LED Effects

- Provides a visual effect at device power up.
- After power on, all the LEDs show dimming and fading effects for an initial time.
- Seen on GPOx when CSx is enabled.
- All CapSense buttons are disabled during this time.
- If any CapSense button, CSx fails the Power-on Self Test then these effects are not seen on the corresponding GPOx.
- To know more about Power-on Self Test, refer System Diagnostics.
- The following parameters are set for LED effects:
  - Low brightness – Minimum intensity of LED brightness.
  - Low brightness time – Time for which the LED stays in the Low Brightness state.
  - Ramp up time – Time taken by the LED to go from Low Brightness state to High Brightness state.
  - High brightness – Maximum intensity of LED brightness.
  - High brightness time – Time for which the LED stays in the High Brightness state.
  - Ramp down time – Time taken by the LED to go from High Brightness state to Low Brightness state.
  - Repeat Rate – The number of times the effect cycle is repeated.
- The effects are seen after the device initialization time from power-on. This time is less than 350 ms (if Noise Immunity level is "Normal") and less than 1000 ms (if Noise Immunity level is "High").
- The device responds to any button touch only after the effects are complete.
- There are three different predefined Power-on LED effects available.
- The different effects are as follows –
  - All the LEDs concurrently go to high brightness state and come back to low brightness state. See Figure 10.
  - All the LEDs concurrently go to high brightness state and come back to low brightness state. This is repeated once (repeat rate = 2). See Figure 11.
  - All the LEDs sequentially go to high brightness state and come back to low brightness state. See Figure 12 on page 10.

Figure 10. Power-on LED Effect Sequence 1

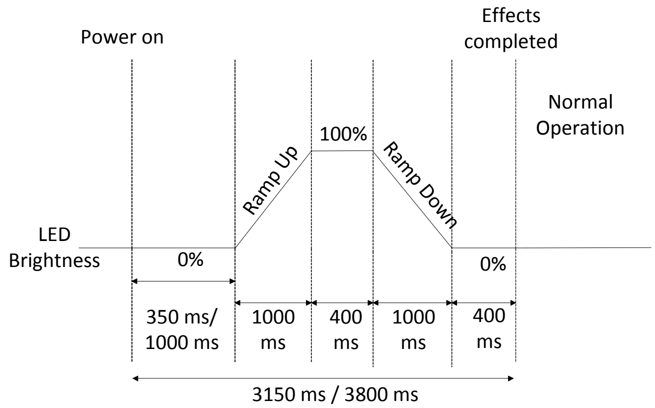


Figure 11. Power-on LED Effect Sequence 2

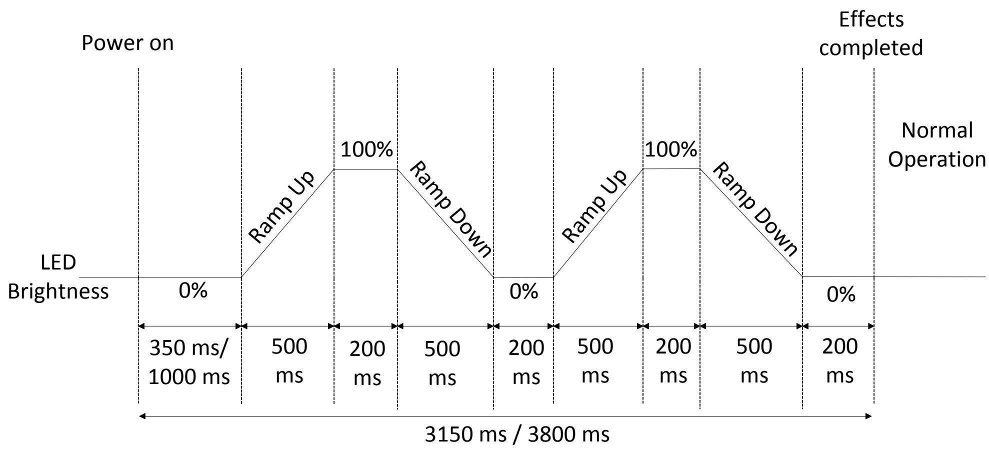
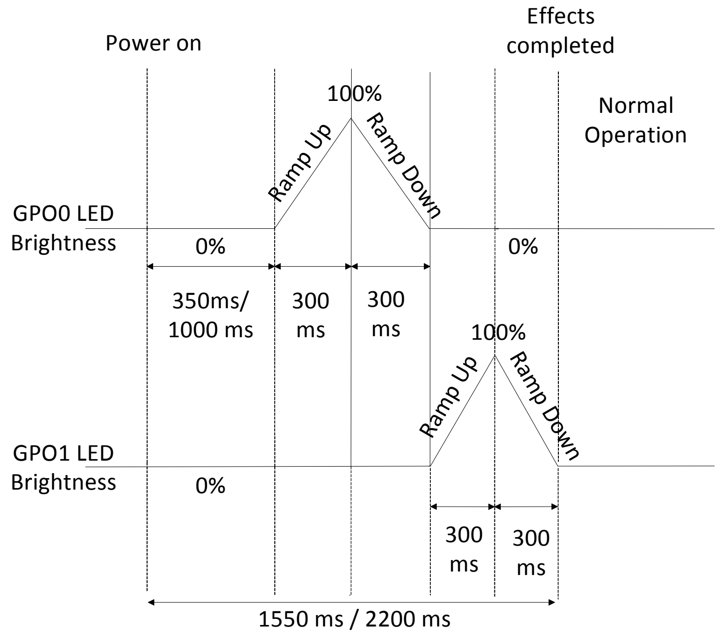


Figure 12. Power-on LED Effect Sequence 3 with Two Button Design



Analog Voltage Support

- A general external resistive network with a host processor is shown in Figure 13.
- Host can be configured to perform different functions based on the voltage level at input pins. This is controlled by switches.
- These switches can be controlled by CapSense buttons.
- If enabled, GPOs replace these switches in the network.
- GPOs are in Open Drain Low drive mode.
- GPOs cannot be used for the resistive network and LED drive simultaneously. Instead, the Backlighting pin acts as a GPO for LED drive, controlled by all the CSx buttons.
- If only one button needs to be ON for analog voltage support, FSS should be enabled.
- For CY8CMBR2010, a simple external resistive network is shown in Figure 14.

Figure 13. A General External Resistive Network

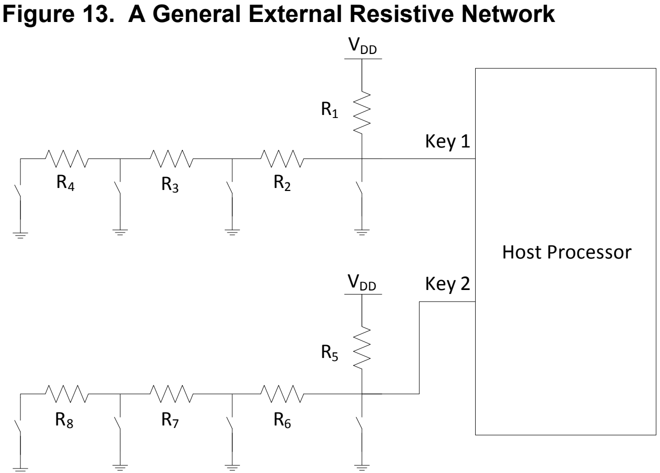
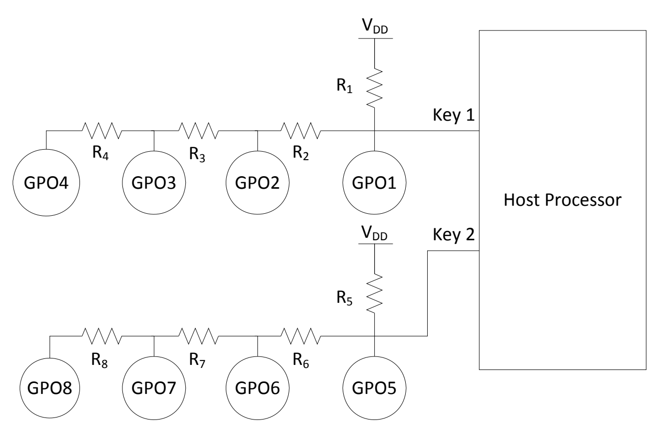


Figure 14. Analog Voltage Support for CY8CMBR2010



LED Backlighting

- Acts as a GPO for LED drive; controlled by all the CapSense buttons CSx.
- Can be used when Analog Voltage Support is enabled.
- Backlighting is a strong drive, active low output. It goes low if one or more CapSense button is touched.

Sensitivity Control for CS0 Button

- Sensitivity of all buttons except CS0 is “High”.
- CS0 can have “Low” sensitivity as well for special purpose, such as a power button.
- Use higher sensitivity setting when the overlay thickness is higher.

Debounce Control for CS0 Button

- Avoids false triggering of button due to noise spike or any other glitches in the system.
- Specifies the minimum time for which CS0 has to be touched, for an output trigger.
- Useful for added functionalities. Example, linking system reset to touch time corresponding to CS0 Debounce.

System Diagnostics

- A built-in Power-on Self Test (POST) mechanism performs some tests at power-on reset (POR), which can be useful in production testing.
- If any button fails these tests, a 5 ms pulse is sent out on the corresponding GPO within 350 ms (if Noise Immunity level is “Normal”) / 1000 ms (if Noise Immunity level is “High”) after POR.
- Following tests are performed on all the buttons –

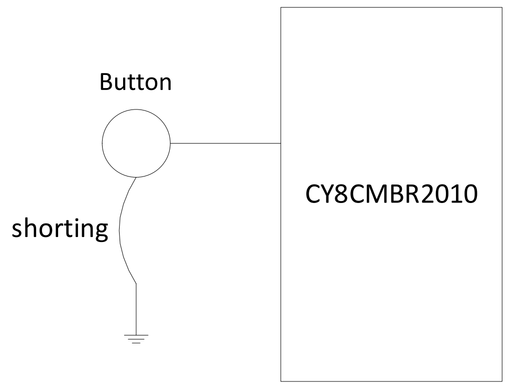
Button Shorted to Ground

If any button is found to be shorted to ground, it is disabled. For an accurate detection of Button shorted to ground, the resistance between the CSx pin and ground should be less than the limits specified in Table 3. See Figure 15.

Table 3. Maximum Resistance between CSx and GND for Proper System Diagnostics Operation

Power Supply (V_{DD}) (V)	Max Resistance between CSx and GND (Ω)
5.5	680
5	760
1.8	1700

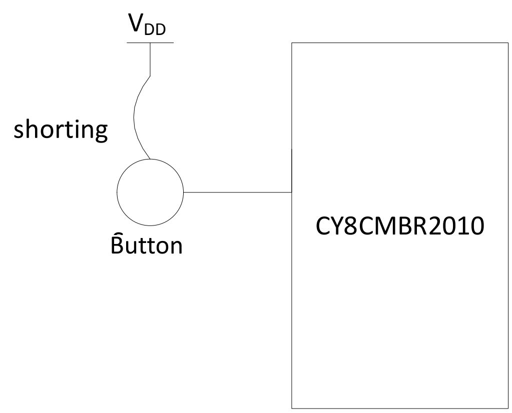
Figure 15. Button Shorted to Ground



Button Shorted to V_{DD}

If any button is found to be shorted to V_{DD}, it is disabled. See Figure 16.

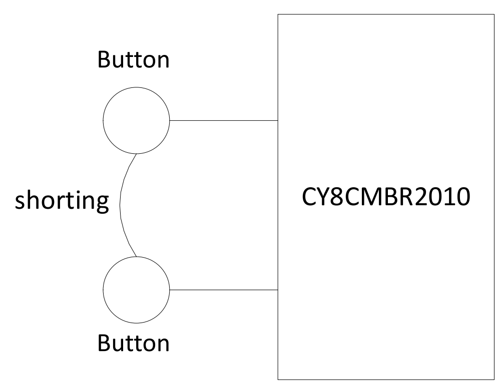
Figure 16. Button Shorted to V_{DD}



Button to Button Short

If two or more buttons are found to be shorted to each other, all of these buttons are disabled. See Figure 17.

Figure 17. Button to Button Short



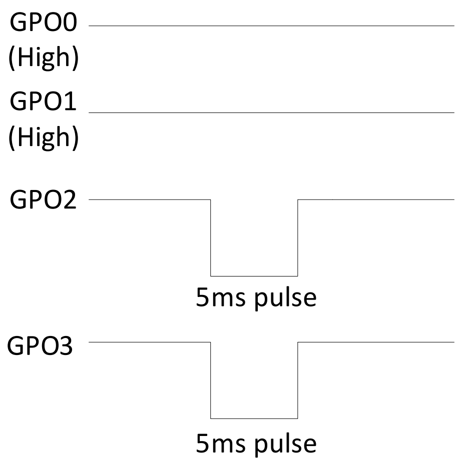
Improper Value of C_{MOD}

- Recommended value of C_{MOD} is 2 nF to 2.4 nF.
- If the value of C_{MOD} is found to be less than 1 nF or greater than 4 nF, all the buttons are disabled.

Button C_P > 40 pF

If the parasitic capacitance (C_P) of any button is found to be more than 40 pF, that button is disabled.

Figure 18. Example Showing CS0 and CS1 Passing the POST and CS2 and CS3 Failing



In Figure 18, CS0 and CS1 buttons are enabled; CS2 and CS3 buttons are disabled because they failed the Power-on Self Test. A 5 ms pulse is observed on GPO2 and GPO3.

Serial Debug Data

- Used to see CapSense data through the Delay pin.
- If enabled, debug data is transmitted on Delay pin using UART communication protocol.
- Serial data is sent out with ~115,200 baud rate.
- The Cypress MultiChart tool can be used to view the data as a graph.
- The following data is sent out by the device for all the buttons enabled –
  - Firmware revision
  - CapSense button status
  - GPO status
  - Raw Counts of all buttons
  - Baseline of all buttons
  - Difference Counts of all buttons
  - Parasitic capacitance of all buttons
  - SNR of all buttons
  - System Diagnostics data
  - Compensated IDAC value

For more information on Raw Count, Baseline, Difference count, Parasitic capacitance and SNR, refer Getting Started with CapSense section 2. For more information on MultiChart tool, refer AN2397 CapSense Data Viewing Tools Method 2.

- The MultiChart tool arranges the data in the format as shown in Table 4.
- The serial debug data is sent by the device in the order as per Table 5.

Table 4. Serial Debug Data arranged in MultiChart

#	Raw count array		Baseline Array		Signal Array	
	MSB	LSB	MSB	LSB	MSB	LSB
0	0x80	FW Revision	0x00	CS_status_MSB	IDAC_Comp	GPO_Status_MSB
1	CS0_Cp	CS1_Cp	0x00	CS_status_LSB	0x00	GPO_Status_LSB
2	CS0_RawCount		CS0_Baseline		CS0_DiffCount	
3	CS1_RawCount		CS1_Baseline		CS1_DiffCount	
4	CS2_RawCount		CS2_Baseline		CS2_DiffCount	
5	CS3_RawCount		CS3_Baseline		CS3_DiffCount	
6	CS4_RawCount		CS4_Baseline		CS4_DiffCount	
7	CS5_RawCount		CS5_Baseline		CS5_DiffCount	
8	CS6_RawCount		CS6_Baseline		CS6_DiffCount	
9	CS7_RawCount		CS7_Baseline		CS7_DiffCount	
10	CS8_RawCount		CS8_Baseline		CS8_DiffCount	
11	CS9_RawCount		CS9_Baseline		CS9_DiffCount	
12	CS2_Cp	CS3_Cp	CS4_Cp	CS5_Cp	CS7_Cp	CS8_Cp
13	0x00	CS0_CS1_SNR	CS6_Cp	CS4_CS5_SNR	CS9_Cp	CS8_CS9_SNR
14	0x00	CS2_CS3_SNR	0x00	CS6_CS7_SNR	0x00	CMOD_Mask

Table 4. Serial Debug Data arranged in MultiChart *(continued)*

#	Raw count array		Baseline Array		Signal Array	
	MSB	LSB	MSB	LSB	MSB	LSB
15	VDD_Short_Mask		GND_Short_Mask		Pin_to_pin_short_Mask	
16	0x00	0x01	0x00	0x02	Cp_High_Mask	

Table 5. Serial Debug Data Output sent by CY8CMBR2010

Byte	Data	Notes
0	0x0D	Dummy data for multi chart
1	0x0A	
2	0x80	–
3	FW Revision	Firmware Revision
4	CS0_Cp	CS0 parasitic capacitance (pF) in Hex
5	CS1_Cp	CS1 parasitic capacitance (pF) in Hex
6	CS0_RawCount_MSB	Unsigned 16-bit integer
7	CS0_RawCount_LSB	
8	CS1_RawCount_MSB	Unsigned 16-bit integer
9	CS1_RawCount_LSB	
. .	. .	. .
24	CS9_RawCount_MSB	Unsigned 16-bit integer
25	CS9_RawCount_LSB	
26	CS2_Cp	CS2 parasitic capacitance (pF) in Hex
27	CS3_Cp	CS3 parasitic capacitance (pF) in Hex
28	0x00	–
29	CS0_CS1_SNR	CS0 and CS1 SNR
30	0x00	–
31	CS2_CS3_SNR	CS2 and CS3 SNR
32	VDD_Short_Mask_MSB	System Diagnostics data for CS pins shorted to V_{DD}
33	VDD_Short_Mask_LSB	
34	0x00	–
35	0x01	
36	0x00	–
37	CS_status_MSB	Gives CS status for CS8–CS9
38	0x00	–
39	CS_status_LSB	Gives CS status for CS0–CS7
40	CS0_Baseline_MSB	Unsigned 16-bit integer
41	CS0_Baseline_LSB	
42	CS1_Baseline_MSB	Unsigned 16-bit integer
43	CS1_Baseline_LSB	
. .	. .	. .
58	CS9_Baseline_MSB	Unsigned 16-bit integer
59	CS9_Baseline_LSB	

Table 5. Serial Debug Data Output sent by CY8CMBR2010 *(continued)*

Byte	Data	Notes
60	CS4_Cp	CS4 parasitic capacitance (pF) in Hex
61	CS5_Cp	CS5 parasitic capacitance (pF) in Hex
62	CS6_Cp	CS6 parasitic capacitance (pF) in Hex
63	CS4_CS5_SNR	CS4 and CS5 SNR
64	0x00	–
65	CS6_CS7_SNR	CS6 and CS7 SNR
66	GND_Short_Mask_MSB	System Diagnostics data for CS pins shorted to GND
67	GND_Short_Mask_LSB	
68	0x00	–
69	0x02	
70	IDAC_Comp	Compensated IDAC
71	GPO_Status_Mask_MSB	Gives GPO status for GPO8–GPO9
72	0x00	–
73	GPO_Status_Mask_LSB	Gives GPO status for GPO0–GPO7
74	CS0_DiffCount_MSB	Unsigned 16-bit integer
75	CS0_DiffCount_LSB	
76	CS1_DiffCount_MSB	Unsigned 16-bit integer
77	CS1_DiffCount_LSB	
. .	. .	. .
92	CS9_DiffCount_MSB	Unsigned 16-bit integer
93	CS9_DiffCount_LSB	
94	CS7_Cp	CS7 parasitic capacitance (pF) in Hex
95	CS8_Cp	CS8 parasitic capacitance (pF) in Hex
96	CS9_Cp	CS9 parasitic capacitance (pF) in Hex
97	CS8_CS9_SNR	CS8 and CS9 SNR
98	0x00	–
99	CMOD_Mask	System Diagnostics data for C_{MOD} out of range
100	Pin_to_Pin_shorted_Mask_MSB	System Diagnostics data for CS pin to pin short
101	Pin_to_Pin_shorted_Mask_LSB	
102	Cp_High_Mask_MSB	System Diagnositcs data for CS button Cp > 40 pF
103	Cp_High_Mask_LSB	
104	0x00	Dummy data for MultiChart
105	0xFF	
106	0xFF	

System Diagnostics data contains the POST results. This is as follows:

- VDD_Short_Mask – This contains the information about any button short to V_{DD}. The MSB and LSB of this data contain the following.

Table 6. VDD_Short_Mask

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VDD_Short_Mask_LSB	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0
VDD_Short_Mask_MSB							CS9	CS8

For CSx, the corresponding bit is written as:

0 ....If the CSx is not shorted to V_{DD}

1 ....If the CSx is shorted to V_{DD}

- GND_Short_Mask – This contains the information about any button short to Ground. The MSB and LSB of this data contain the following.

Table 7. GND_Short_Mask

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GND_Short_Mask_LSB	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0
GND_Short_Mask_MSB							CS9	CS8

For CSx, the corresponding bit is written as:

0 ....If the CSx is not shorted to ground

1 ....If the CSx is shorted to ground

- CMOD_Mask – This contains the information about the C_{MOD} value within range. This byte is written as:

0 ...... If the C_{MOD} value is within range (between 1 nF–4 nF)

1 .... If the C_{MOD} value > 4 nF

2 .... If the C_{MOD} value < 1 nF

- Pin_to_Pin_Short_Mask – This contains the information about any button to button short. The MSB and LSB of this data contain the following.

Table 8. Pin_to_Pin_Short_Mask

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Pin_to_Pin_Short_Mask_LSB	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0
Pin_to_Pin_Short_Mask_MSB							CS9	CS8

For CSx, the corresponding bit is written as:

0................If the CSx pin is not shorted to any other CSy pin

1........................ If the CSx pin is shorted to another CSy pin

- Cp_High_Mask – This contains the information about the CSx button C_P value within range. The MSB and LSB of this data contain the following

Table 9. Cp_High_Mask

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Cp_High_Mask_LSB	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0
Cp_High_Mask_MSB							CS9	CS8

For CSx, the corresponding bit is written as:

0... If the CSx C_P value < 40 pF

1... If the CSx C_P value > 40 pF

Power Consumption and Operating Modes

The CY8CMBR2010 is designed to meet the low power requirements of battery powered applications. To design for the lowest operating current –

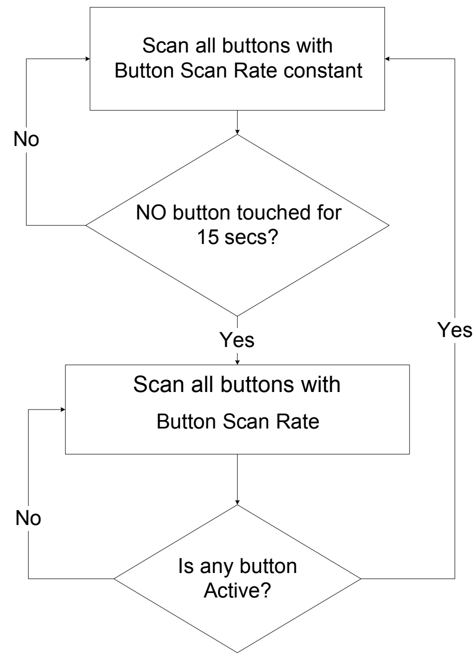
- Ground all unused CapSense inputs
- Minimize Cp using the design guidelines in Getting Started with CapSense, section 3.7.1
- Lower the supply voltage (valid range: 1.71 V to 5.5 V)
- Reduce sensitivity of CS0 button
- Configure design to be power consumption optimized
- Use “High” Noise Immunity level only if required
- Use a higher Button Scan Rate or Deep Sleep operating mode

To know more about the steps to reduce power consumption, refer to the CY8CMBR2010 Design Guide section 5.

Low Power Sleep Mode

The following flow chart describes the low power sleep mode operation.

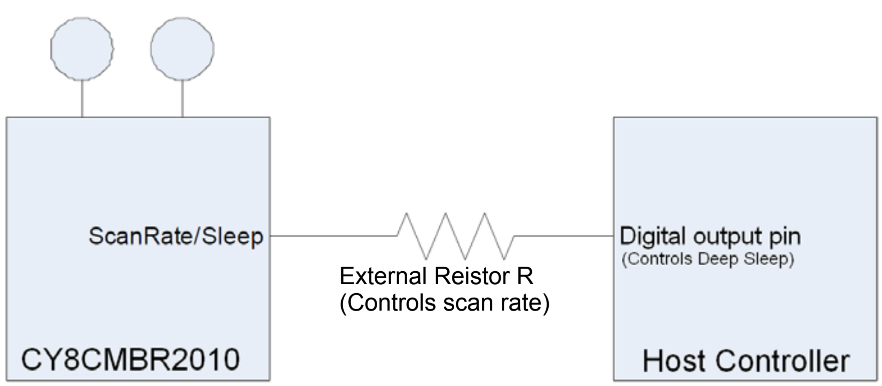
Figure 19. Low Power Sleep Mode Operation



- The Button Scan Rate is equal to the sum of the time the device scans and sleeps.
- An external resistor defines Button Scan Rate offset.
- The offset is added to a constant to get the Button Scan Rate.
- To know about the Button Scan Rate offset and the Button Scan Rate constant, refer to Table 23 on page 29 and Table 24 on page 30 in Appendix.
- The range of scan rate is 25 to 556 ms.

Deep Sleep Mode

Figure 20. ScanRate/Sleep pin Connection to Enable Deep Sleep Mode



- To enable the deep sleep mode, the ScanRate/Sleep pin should be connected to host controller as shown in Figure 20 on page 16.
- Host controller should pull the pin to V_{DD} for the device to go into deep sleep.
- In deep sleep mode, all blocks are turned off and the device power consumption is approximately 0.1 µA.
- There is no CapSense scanning in deep sleep mode.
- ScanRate/Sleep pin should be pulled low for the device to wake up from deep sleep.
- When device comes out of deep sleep mode, the CapSense system is reinitialized. Typical time for reinitialization is 20 ms (if Noise Immunity level is "Normal") or 50 ms (if Noise Immunity level is "High"). Any button touch within this time is not reported.
- At power on, the ScanRate/Sleep pin should be pulled low.
- If the ScanRate/Sleep pin is pulled high at power on, then the device goes to Deep Sleep after the POST and Power-on LED effects are completed.

Response Time

Response time is the minimum amount of time the button should be touched for the device to detect as valid button touch.

It is given by following equation

$$RT_{FBT} = Button\,Scan\,Rate + \left[Button\,Scan\,Rate\,constant \times \left\{Round_{down}\left(\frac{(Debounce - 1)}{3}\right) + 1\right\}\right]$$

$$RT_{CBT} = Button\,Scan\,Rate\,constant + \left[Button\,Scan\,Rate\,constant \times \left\{Round_{down}\left((Debounce - 1)/3\right) + 1\right\}\right]$$

Where

RT_{FBT} is Response time for First button touch

RT_{CBT} is Response time for consecutive button touch after first button touch

Debounce for CS1–CS9 = 3

Debounce for CS0 can be one of 3 / 24 / 48 / 99

$Round_{down}$ is the greatest integer less than or equal to ((Debounce – 1)/3)

For example, consider an eight button design with the Delay pin connected to ground through a 3.2 kΩ resistor. This results in a Response Time optimized design with a User defined Button Scan rate of 556 ms (as per Table 23 on page 29 and Table 24 on page 30).

Assuming that CS0 is not used in the design, the Debounce value for each button (CS1–CS8) is 3. The Button Scan Rate constant for such a design is 50 ms (as per Table 24 on page 30).

The response time for such a design is given as –

$$RT_{FBT} = 556 + \left[50 \times \left\{Round_{down}\left((3-1)/3\right) + 1\right\}\right] = 606\ ms$$

$$RT_{CBT} = 50 + \left[50 \times \left\{Round_{down}\left((3-1)/3\right) + 1\right\}\right] = 100\ ms$$

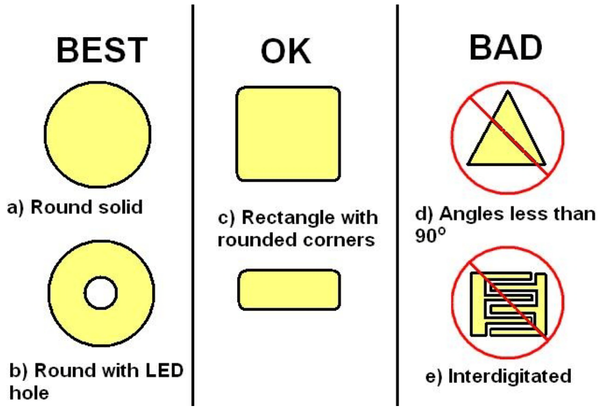
Layout Guidelines and Best Practices

Table 10. Layout Guidelines and Best Practices

Sl. No.	Category	Min	Max	Recommendations/Remarks
1	Button shape	–	–	Solid round pattern, round with LED hole, rectangle with round corners
2	Button size	5 mm	15 mm	Refer Design toolbox.
3	Button-button spacing	Equal to Button Ground Clearance	–	8 mm (Y dimension in Figure 22 on page 19)
4	Button ground clearance	0.5 mm	2 mm	Refer Design toolbox (X dimension in Figure 22 on page 19).
5	Ground flood – top layer	–	–	Hatched ground 7 mil trace and 45 mil grid (15% filling).
6	Ground flood – bottom layer	–	–	Hatched ground 7 mil trace and 70 mil grid (10% filling).
7	Trace length from button pad to CapSense controller pins	–	450 mm	Refer Design toolbox.
8	Trace width	0.17 mm	0.20 mm	0.17 mm (7 mil)
9	Trace routing	–	–	Traces should be routed on the non button side. If any non CapSense trace crosses CapSense trace, ensure that intersection is orthogonal.
10	Via position for the buttons	–	–	Via should be placed near the edge of the button pad to reduce trace length thereby increasing sensitivity.
11	Via hole size for button traces	–	–	10 mil
12	No. of via on button trace	1	2	1
13	Distance of CapSense series resistor from button pin	–	10 mm	Place CapSense series resistors close to the device for noise suppression.CapSense resistors have highest priority; place them first.
14	Distance between any CapSense trace to ground Flood	10 mil	20 mil	20 mil
15	Device placement	–	–	Mount the Device on the layer opposite to button. The CapSense trace length between the Device and buttons should be minimum (see trace length above)
16	Placement of components in two layer PCB	–	–	Top Layer – buttons Bottom layer – device, other components and traces.
17	Placement of components in four layer PCB	–	–	Top Layer – buttons Second Layer – CapSense traces and V_{DD} (avoid V_{DD} traces below the buttons) Third Layer – hatched ground Bottom layer – CapSense controller, other components and non CapSense traces
18	Overlay thickness	0 mm	5 mm	Refer Design toolbox.
19	Overlay material	–	–	Should be non-conductive material. Glass, ABS Plastic, Formica, wood and so on. There should be no air gap between PCB and overlay. Use adhesive to stick the PCB and overlay.
20	Overlay adhesives	–	–	Adhesive should be non conductive and dielectrically homogenous. 467MP and 468MP adhesives made by 3M are recommended.
21	LED back lighting	–	–	Cut a hole in the button pad and use rear mountable LEDs. Refer to the PCB layout below.
22	Board thickness	–	–	Standard board thickness for CapSense FR4 based designs is 1.6 mm.

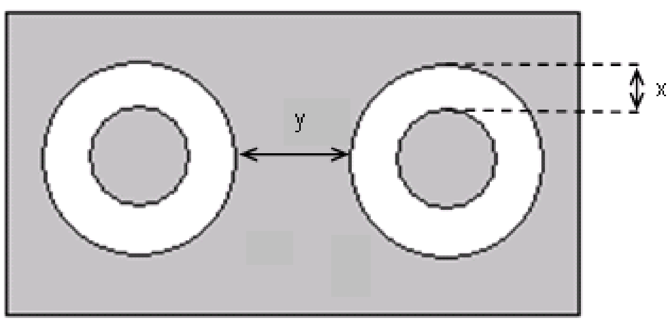
CapSense Button shapes

Figure 21. CapSense button shapes



Button Layout Design

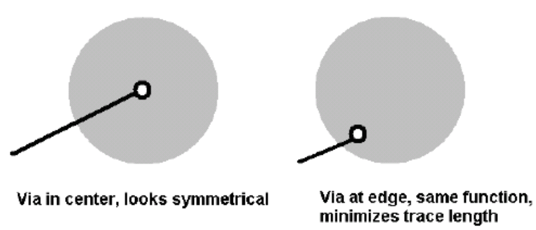
Figure 22. Button Layout Design



x: Button to ground clearance (Refer to Layout Guidelines and Best Practices on page 18).
y: Button to button clearance (Refer to Layout Guidelines and Best Practices on page 18).

Recommended via-hole Placement

Figure 23. Recommended via-hole Placement



Example PCB Layout Design with Ten CapSense Buttons and Ten GPOs

Figure 24. Top Layer

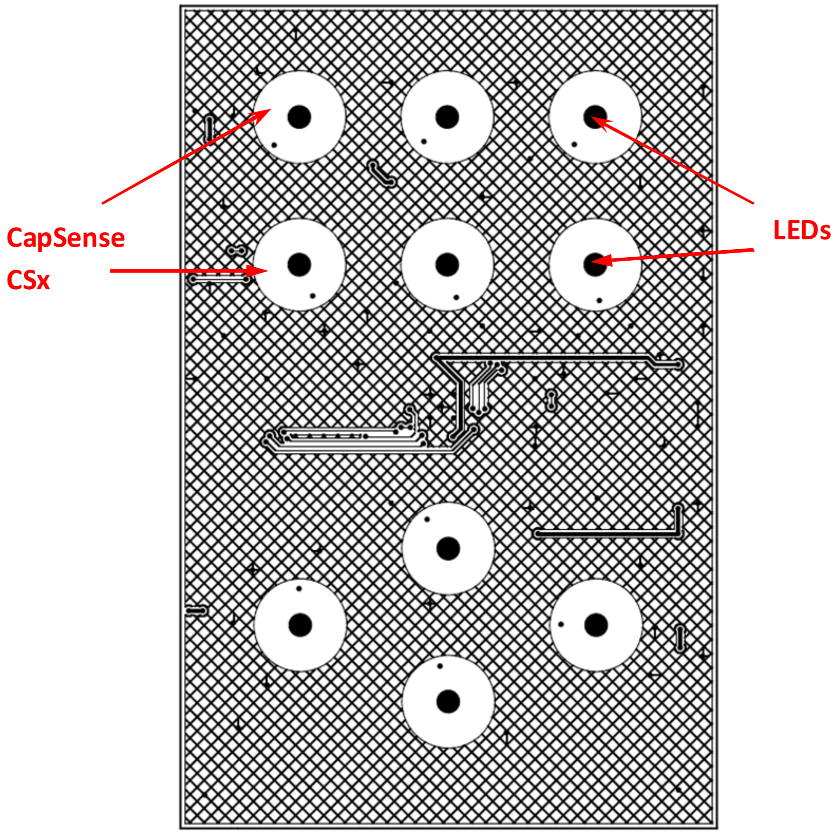
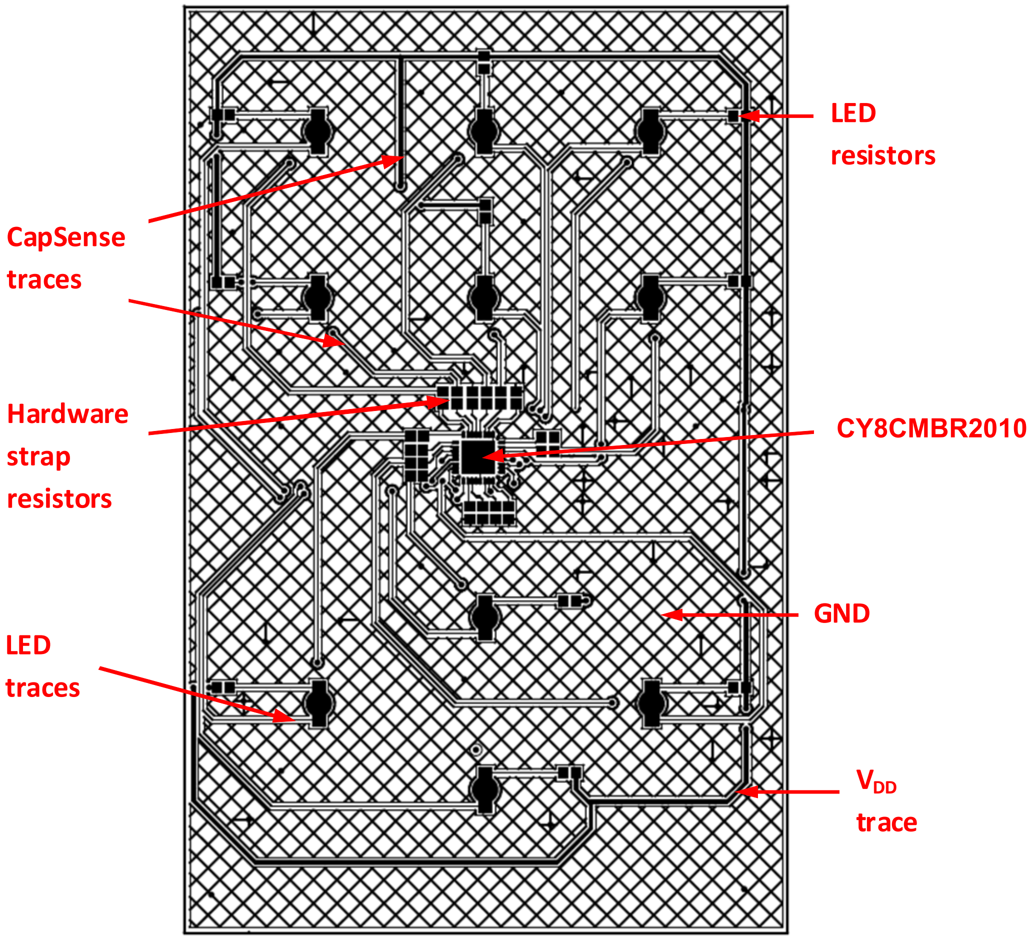


Figure 25. Bottom Layer



Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CMBR2010 device.

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device.

Table 11. Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Unit	Conditions
T_{STG}	Storage temperature	–55	+25	+125	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage at temperatures above 85 °C degrades reliability.
V_{DD}	Supply voltage relative to V_{SS}	–0.5	–	+6.0	V	
V_{IO}	DC voltage on CapSense inputs and digital output pins	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
I_{MIG}	Maximum current into any GPO pin	–25	–	+50	mA	
ESD	Electro static discharge voltage	2000	–	–	V	Human body model ESD
LU	Latch up current	–	–	200	mA	In accordance with JESD78 standard

Operating Temperature

Table 12. Operating Temperature

Parameter	Description	Min	Typ	Max	Unit	Notes
T_A	Ambient temperature	–40	–	+85	°C	
T_C	Commercial temperature	0	–	+70	°C	
T_J	Operational Die Temperature	–40	–	+100	°C	The temperature rise from ambient to junction is package specific. Refer to Table 20 on page 27. The user must limit the power consumption to comply with this requirement.

DC Electrical Characteristics

DC Chip Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 13. DC Chip-Level Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{DD}[4, 5, 6]	Supply voltage	1.71	–	5.5	V	
I_{DD}	Supply current	–	3.4	4.0	mA	V_{DD} = 3.0 V, T_A = 25 °C
I_{DA}	Active current	–	3.4	4.0	mA	V_{DD} = 3.0 V, T_A = 25 °C, continuous button scan
I_{DL}	Low power sleep current	–	1.07	1.50	µA	V_{DD} = 3.0 V, T_A = 25 °C
I_{DS}	Deep sleep current	–	0.1	1.05	µA	V_{DD} = 3.0 V, T_A = 25 °C
I_{AV1}	Average current	–	85.90	–	µA	4-buttons used, 3% touch time, 10 pF < C_P of all buttons < 20 pF, Button Scan Rate = 556 ms, with power consumption optimized, Noise Immunity level “Normal”, CS0 sensitivity “High”
I_{AV2}	Average current	–	131.50	–	µA	8-buttons used, 5% touch time, 10 pF < C_P of all buttons < 20 pF, button scan rate = 556 ms, with response time optimized, Noise Immunity level “Normal”, CS0 sensitivity “High”
I_{AV3}	Average current	–	168.10	–	µA	10-buttons used, 5% touch time, 10 pF < Cp of all buttons < 20 pF, button scan rate = 419 ms, with response time optimized, Noise Immunity level “Normal”, CS0 sensitivity “High”

Notes

4. When V_{DD} remains in the range from 1.75 V to 1.9 V for more than 50 µs, the slew rate when moving from the 1.75 V to 1.9 V range to greater than 2 V must be slower than 1 V/500 µs. This helps to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the SRPOWER_UP parameter.
5. After power-down, ensure that V_{DD} falls below 100 mV before powering back up.
6. For proper CapSense block functionality, if the drop in V_{DD} exceeds 5% of the base V_{DD}, the rate at which V_{DD} drops should not exceed 200 mV/s. Base V_{DD} can be between 1.8 V and 5.5 V.

DC General-Purpose I/O Specifications

These tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and –40 °C ≤ T_A ≤ 85 °C, 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, and 1.71 V to 2.4 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only. .

Table 14. 3.0 V to 5.5 V DC General-Purpose I/O Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{OH1}	High output voltage on GPO0–GPO9 (except GPO5)	V_{DD} – 0.20	–	–	V	I_{OH} ≤ 10 µA, maximum of 10 mA source current in all I/Os
V_{OH2}	High output voltage on GPO0–GPO9 (except GPO5)	V_{DD} – 0.90	–	–	V	I_{OH} = 1 mA, maximum of 20 mA source current in all I/Os
V_{OH3}	High output voltage on GPO5, Backlighting, Delay pins	V_{DD} – 0.20	–	–	V	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os
V_{OH4}	High output voltage on GPO5, Backlighting, Delay pins	V_{DD} – 0.90	–	–	V	I_{OH} = 5 mA, maximum of 20 mA source current in all I/Os
V_{OL}	Low output voltage on all GPOs, Backlighting, Delay pins	–	–	0.75	V	I_{OL} = 25 mA, V_{DD} > 3.3 V, maximum of 60 mA sink current on GPO0, GPO1, GPO2, GPO3, GPO4, Backlighting, Delay pins and 60 mA sink current on GPO5, GPO6, GPO7, GPO8, GPO9 pins.
V_{IL}	Input low voltage	–	–	0.80	V	
V_{IH}	Input high voltage	2.00	–	–	V	

Table 15. 2.4 V to 3.0 V DC General-Purpose I/O Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{OH1}	High output voltage on GPO0–GPO9 (except GPO5)	V_{DD} – 0.20	–	–	V	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os
V_{OH2}	High output voltage on GPO0–GPO9 (except GPO 5)	V_{DD} – 0.40	–	–	V	I_{OH} = 0.2 mA, maximum of 10 mA source current in all I/Os
V_{OH3}	High output voltage on GPO5, Backlighting, Delay pins	V_{DD} – 0.20	–	–	V	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os
V_{OH4}	High output voltage on GPO5, Backlighting, Delay pins	V_{DD} – 0.50	–	–	V	I_{OH} = 2 mA, maximum of 10 mA source current in all I/Os
V_{OL}	Low output voltage on all GPOs, Backlighting, Delay pins	–	–	0.75	–	I_{OL} = 5 mA, maximum of 30 mA sink current on GPO0, GPO1, GPO2, GPO3, GPO4, Backlighting, Delay pins and 30 mA sink current on GPO5, GPO6, GPO7, GPO8, GPO9 pins.
V_{IL}	Input low voltage	–	–	0.72	V	
V_{IH}	Input high voltage	1.40	–	–	V	

Table 16. 1.71 V to 2.4 V DC General-Purpose I/O Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{OH1}	High output voltage on GPO0–GPO9 (except GPO5)	V_{DD} – 0.20	–	–	V	I_{OH} = 10 µA, maximum of 10 mA source current in all I/Os
V_{OH2}	High output voltage on GPO0–GPO9 (except GPO5)	V_{DD} – 0.50	–	–	V	I_{OH} = 0.5 mA, maximum of 10 mA source current in all I/Os

Table 16. 1.71 V to 2.4 V DC General-Purpose I/O Specifications *(continued)*

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{OH3}	High output voltage on GPO5, Backlighting, Delay pins	V_{DD} – 0.20	–	–	V	I_{OH} = 100 µA, maximum of 10 mA source current in all I/Os
V_{OH4}	High output voltage on GPO5, Backlighting, Delay pins	V_{DD} – 0.50	–	–	V	I_{OH} = 2 mA, maximum of 10 mA source current in all I/Os
V_{OL}	Low output voltage on all GPOs, Backlighting, Delay pins	–	–	0.4	–	I_{OL} = 5 mA, maximum of 20 mA sink current on GPO5, GPO6, GPO7, GPO8, GPO9 pins and 30 mA sink current on GPO0, GPO1, GPO2, GPO3, GPO4 , Backlighting, Delay pins.
V_{IL}	Input low voltage	–	–	0.3 × V_{DD}	V	
V_{IH}	Input high voltage	0.65 × V_{DD}	–	–	V	

AC Electrical Specifications

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 17. AC Chip – Level Specifications

Parameter	Description	Min	Max	Unit	Notes
SR_{POWER_UP}	Power supply slew rate	–	250	V/ms	V_{DD} slew rate during power-up.
T_{XRST}	External reset pulse width at power-up	1	–	ms	Applicable after device power supply is active
T_{XRST2}	External reset pulse width after power-up	10	–	µs	Applicable after device V_{DD} has reached max value

AC General-Purpose I/O Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 18. AC General-Purpose I/O Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{Rise1}	Rise time, strong mode on GPO0–GPO9 (except GPO5), C_{load} = 50 pF	15	–	80	ns	V_{DD} = 3.0 to 3.6 V, 10% to 90%
T_{Rise2}	Rise time, strong mode low supply on GPO5, Backlighting, Delay pins, C_{load} = 50 pF	10	–	50	ns	V_{DD} = 3.0 to 3.6 V, 10% to 90%
T_{Rise3}	Rise time on GPO0–GPO9 (except GPO5), C_{load} = 50 pF	15	–	80	ns	V_{DD} = 1.71 to 3.0 V, 10% to 90%
T_{Rise2}	Rise time, strong mode low supply on GPO5, Backlighting, Delay pins, C_{load} = 50 pF	10	–	80	ns	V_{DD} = 1.71 to 3.0 V, 10% to 90%
T_{Fall1}	Fall time, strong mode on all GPOs, Backlighting, Delay pins, C_{load} = 50 pF	10	–	50	ns	V_{DD} = 3.0 to 3.6 V, 90% to 10%
T_{Fall2}	Fall time, strong mode low supply on all GPOs, Backlighting, Delay pins, C_{load} = 50 pF	10	–	70	ns	V_{DD} = 1.71 to 3.0 V, 90% to 10%

CapSense Specifications

Table 19. CapSense Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
C_P	Parasitic capacitance	5	–	$(C_P + C_F) < 40$ [7]	pF	C_p is the total capacitance seen by the pin when no finger is present. C_P is sum of C_{BUTTON}, C_{TRACE}, and Capacitance of the vias and C_{PIN}.
C_F	Finger capacitance	0.25	–	$(C_P + C_F) < 40$ [7]	pF	C_F is the capacitance added by the finger touch.
C_{PIN}	Capacitive load on pins as input	0.5	1.7	7	pF	
C_{MOD}	External modulator capacitor	2	2.2	2.4	nF	Mandatory requirement
R_S	Series resistor between Pin and the button	–	560	616	Ω	Reduces the RF noise.

Ordering Information

Ordering Code	Package Type	Operating Temperature	CapSense Inputs	GPO's	XRESPin
CY8CMBR2010-24LQXI	32-pin (5 × 5 × 0.6 mm) QFN	Industrial	10	10	Yes
CY8CMBR2010-24LQXIT	32-pin (5 × 5 × 0.6 mm) QFN (tape and reel)	Industrial	10	10	Yes

Ordering Code Definitions

CY 8 C MBR 2010 - 24 LQ X I X

- X = blank or T
  blank = Tube; T = Tape and Reel
- Temperature Range: I = Industrial = –40 °C to 85 °C
- Pb-free
- Package Type:
  LQ = 32-pin QFN
- Speed: 24 MHz
- Part Number
- Mechanical Button Replacement
- Technology Code: C = CMOS
- Marketing Code: 8 = PSoC
- Company ID: CY = Cypress

Note

7. The max value of parasitic capacitance is 40 pF when the temperature is above 0 °C, and 38 pF at –45 °C.

Package Information

Thermal Impedance

Table 20. Thermal Impedances per Package

Package	Typical θ_{JA}[8]
32-pin QFN[9]	20 °C/W

Solder Reflow Specifications

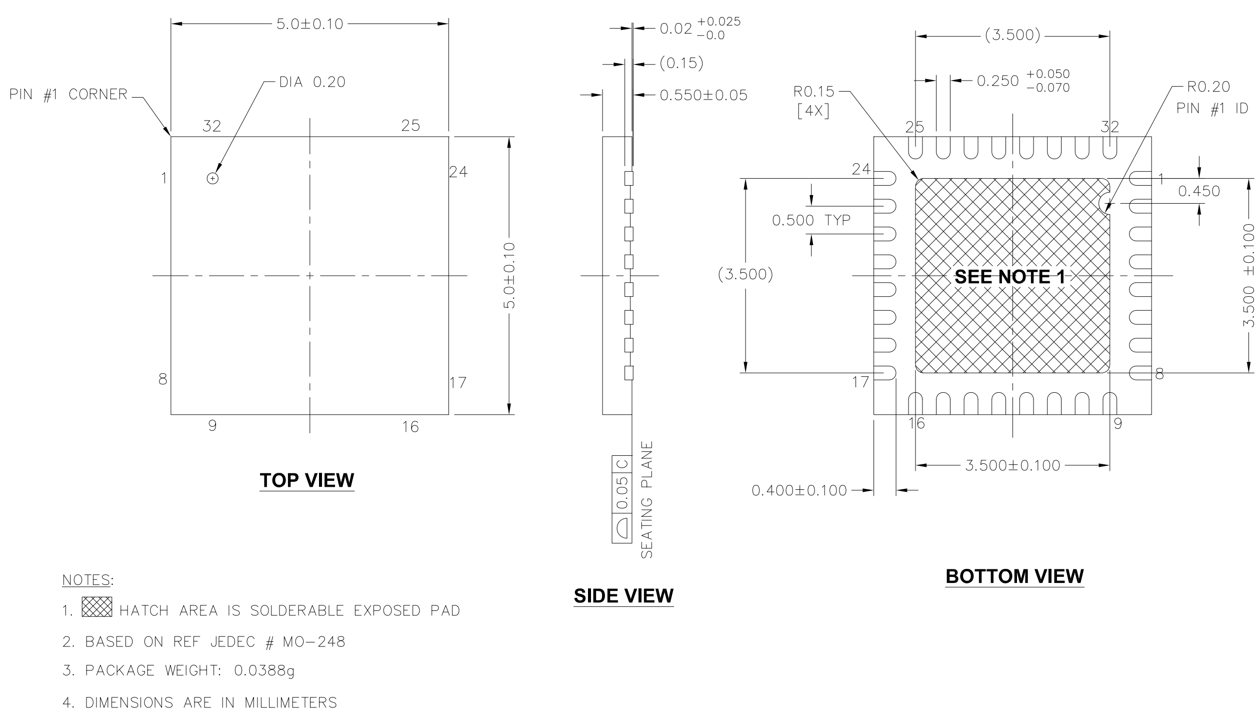
Table 21 shows the solder reflow temperature limits that must not be exceeded.

Table 21. Solder Reflow Specifications

Package	Minimum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
32-pin QFN	260 °C	30 seconds

Package Diagram

Figure 26. 32-pin QFN (5 × 5 × 0.55 mm) LQ32 3.5 × 3.5 E-Pad (Sawn) Package Outline, 001-42168



001-42168 *D

Notes

8. $T_J = T_A + Power \times \theta_{JA}$.
9. To achieve the thermal impedance specified for the QFN package, the center thermal pad must be soldered to the PCB ground plane.

Appendix

Table 22. Device Features vs. Resistor Configuration Matrix

Features	Comments		Pin configuration	Device Pin Name
Toggle ON/OFF / Flanking Sensor Suppression (FSS)	**Toggle ON/OFF**	**Flanking Sensor Suppression (FSS)**		Toggle/FSS
	Disabled	Disabled	Ground / Floating	
	Enabled	Disabled	1.5 kΩ (±5%) to ground	
	Disabled	Enabled	5.1 kΩ (±5%) to ground	
	Enabled	Enabled	V_{DD}	
Noise Immunity / Button Auto Reset	**Noise Immunity**	**Button Auto Reset**		ARST/EMC
	Normal	Disabled	Ground / Floating	
	Normal	Enabled	1.5 kΩ (±5%) to ground	
	High	Disabled	5.1 kΩ (±5%) to ground	
	High	Enabled	V_{DD}	
LED ON Time / Serial Debug Data	**LED ON Time (ms)**	**Serial Debug Data**		Delay
	0	Disabled	Ground / 300 Ω (±1%) to ground	
	20		330 Ω (±1%) to ground	
	40		360 Ω (±1%) to ground	
	…………		…………	
	1980		3270 Ω (±1%) to ground	
	2000		3300 Ω (±1%) to ground	
	0	Enabled	7000 Ω (±1%) to ground	
	20		7030 Ω (±1%) to ground	
	40		7060 Ω (±1%) to ground	
	…………		…………	
	1980		9970 Ω (±1%) to ground	
	2000		10000 Ω (±1%) to ground	
Power-on LED Effects / Analog Voltage support / LED Backlighting	**Power-on LED Effects**	**Analog Voltage Support / LED Backlighting**		LEDFading
	Disabled	Enabled	Ground	
	LED Effect 1	Disabled	1.5 kΩ (±5%) to ground	
	LED Effect 2	Disabled	5.1 kΩ (±5%) to ground	
	LED Effect 3	Disabled	V_{DD}	
	Disabled	Disabled	Floating	
Sensitivity and debounce control for CS0 button	**Sensitivity Control for CS0 Button**	**Debounce Control for CS0 Button**		CS0Sensitivity
	High	3	Ground / Floating	
	High	24	1.5 kΩ (±5%) to ground	
	High	48	5.1 kΩ (±5%) to ground	
	Low	99	V_{DD}	

Table 23. ScanRate/Sleep pin Configuration

ScanRate/Sleep pin Connection		Button Scan Rate offset
Response Time Optimized design	Power Consumption Optimized design	
Ground	6800 Ω (±1%) to ground	0
100 Ω (±1%) to ground	6900 Ω (±1%) to ground	0
200 Ω (±1%) to ground	7000 Ω (±1%) to ground	6
300 Ω (±1%) to ground	7100 Ω (±1%) to ground	12
400 Ω (±1%) to ground	7200 Ω (±1%) to ground	20
500 Ω (±1%) to ground	7300 Ω (±1%) to ground	29
600 Ω (±1%) to ground	7400 Ω (±1%) to ground	39
700 Ω (±1%) to ground	7500 Ω (±1%) to ground	49
800 Ω (±1%) to ground	7600 Ω (±1%) to ground	61
900 Ω (±1%) to ground	7700 Ω (±1%) to ground	73
1000 Ω (±1%) to ground	7800 Ω (±1%) to ground	86
1100 Ω (±1%) to ground	7900 Ω (±1%) to ground	99
1200 Ω (±1%) to ground	8000 Ω (±1%) to ground	114
1300 Ω (±1%) to ground	8100 Ω (±1%) to ground	128
1400 Ω (±1%) to ground	8200 Ω (±1%) to ground	144
1500 Ω (±1%) to ground	8300 Ω (±1%) to ground	160
1600 Ω (±1%) to ground	8400 Ω (±1%) to ground	176
1700 Ω (±1%) to ground	8500 Ω (±1%) to ground	194
1800 Ω (±1%) to ground	8600 Ω (±1%) to ground	211
1900 Ω (±1%) to ground	8700 Ω (±1%) to ground	229
2000 Ω (±1%) to ground	8800 Ω (±1%) to ground	248
2100 Ω (±1%) to ground	8900 Ω (±1%) to ground	267
2200 Ω (±1%) to ground	9000 Ω (±1%) to ground	287
2300 Ω (±1%) to ground	9100 Ω (±1%) to ground	307
2400 Ω (±1%) to ground	9200 Ω (±1%) to ground	327
2500 Ω (±1%) to ground	9300 Ω (±1%) to ground	348
2600 Ω (±1%) to ground	9400 Ω (±1%) to ground	369
2700 Ω (±1%) to ground	9500 Ω (±1%) to ground	391
2800 Ω (±1%) to ground	9600 Ω (±1%) to ground	413
2900 Ω (±1%) to ground	9700 Ω (±1%) to ground	436
3000 Ω (±1%) to ground	9800 Ω (±1%) to ground	459
3100 Ω (±1%) to ground	9900 Ω (±1%) to ground	482
3200 Ω (±1%) to ground	10000 Ω (±1%) to ground	506

Table 24 gives the Button Scan Rate constant according to the button count and the device optimization. For more details about this constant, refer Power Consumption and Operating Modes on page 16.

Table 24. Button Scan Rate Constant

Button count	Button Scan Rate Constant	
	Response Time Optimized design	Power Consumption Optimized design
≤ 5	25 ms	50 ms
> 5	50 ms	50 ms

Acronyms

Acronym	Description
AC	alternating current
AI	analog input
AO	analog output
ARST	auto reset
DC	direct current
DI	digital input
DO	digital output
C_F	finger capacitance
C_P	parasitic capacitance
CS	CapSense
FSS	flanking sensor suppression
GPO	general-purpose output
I/O	input/output
LED	light-emitting diode
LSB	least significant bit
MSB	most significant bit
P	power
PCB	printed circuit board
POR	power-on reset
POST	power-on self test
QFN	quad flat no lead
RF	radio frequency
SNR	signal to noise ratio

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kΩ	kilohm
µA	microampere
µs	microsecond
mA	milliampere
mil	one thousandth of an inch (1 mil = 0.0254 mm)
mm	millimeter
ms	millisecond
mV	millivolt
nA	nanoampere
nF	nanofarad
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, 01010100b' or '01000011b'). Numbers not indicated by an 'h', 'b', or 0x are decimal.

Document History Page

Document Title: CY8CMBR2010, CapSense® Express™ 10-Button Controller Document Number: 001-74495				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3561834	UDYG / ZINE	03/30/2012	New data sheet.
*A	3715110	UDYG	08/16/2012	Updated title to read as “CY8CMBR2010, CapSense® Express™ 10-Button Controller”. Updated Features (Updated contents in the section). Updated Overview (Updated contents in the section). Updated Pinout (Updated Table 1). Updated Typical Circuits (Updated Figure 1, Figure 2, updated contents in the section). Updated Device Features (Updated contents in the section, updated Button Auto Reset (Updated Figure 9), updated Analog Voltage Support (Updated Figure 13, Figure 14)) Updated Layout Guidelines and Best Practices (Updated contents in the section, updated Example PCB Layout Design with Ten CapSense Buttons and Ten GPOs (Updated Figure 24, Figure 25)). Minor text edits throughout the document.
*B	3837617	UDYG	12/11/2012	Updated Device Features (Updated System Diagnostics (Updated Button Shorted to Ground (Updated contents in the section and added Table 3))).

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