Vishay Siliconix

N-Channel 40 V (D-S) MOSFET



PRODUCT SUMMARY					
V _{DS} (V)	40				
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10 \text{ V}$	0.009				
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5 \text{ V}$	0.012				
Q _g typ. (nC)	15				
I _D (A)	19 ^d				
Configuration	Single				

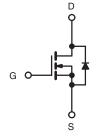
FEATURES

- TrenchFET® power MOSFET
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



APPLICATIONS

- Synchronous rectification
- POL, IBC
 - Secondary side



N-Channel MOSFET

ORDERING INFORMATION				
Package	SO-8			
Lead (Pb)-free	Si4840BDY-T1-E3			
Lead (Pb)-free and halogen-free	Si4840BDY-T1-GE3			

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	40	V
Gate-source voltage		V_{GS}	± 20	
	T _C = 25 °C		19	
Continuous drain surrent (T. 150 °C)	T _C = 70 °C	1 , \square	15	
Continuous drain current (T _J = 150 °C)	T _A = 25 °C	l _D	12.4 ^{a, b}	
	T _A = 70 °C		9.9 ^{a, b}	Α
Pulsed drain current		I _{DM}	50	
Avalanche current		I _{AS}	15	
Avalanche energy	L = 0.1 mH	E _{AS}	11	mJ
Continuous source-drain diode current	$T_C = 25 ^{\circ}C$		5	
	T _A = 25 °C	I _S	2.1 ^{a, b}	A
Maximum power dissipation	T _C = 25 °C		6	
	T _C = 70 °C		3.8	w
	T _A = 25 °C	P _D	2.5 ^{a, b}	
	T _A = 70 °C		1.6 ^{a, b}	
Operating junction and storage temperature	T _{.I} , T _{sto}	-55 to +150	°C	

THERMAL RESISTANCE RATINGS							
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT		
Maximum junction-to-ambient a, c	t ≤ 10 s	R_{thJA}	37	50	°C/W		
Maximum junction-to-foot (drain)	Steady state	R_{thJF}	17	21	C/VV		

Notes

- a. Surface mounted on 1" x 1" FR4 board
- b. t = 10 s
- c. Maximum under steady state conditions is 85 °C/W
- d. Based on $T_C = 25\ ^{\circ}C$

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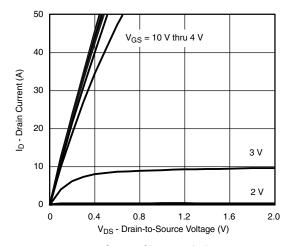
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	40	-	-	V	
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	L 050 A	-	40	-		
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA	-	-6	-	mV/°C	
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_{D} = 250 \mu A$	1	-	3	V	
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA	
Zono del college del conseile		$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	1 5 μΑ	
Zero gate voltage drain current	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V, T _J = 55 °C	-	-	5		
On-state drain current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	50	-	-	Α	
5	_	V _{GS} = 10 V, I _D = 12.4 A	-	0.0074	0.0090	Ω	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 10.8 A	-	0.0095	0.0120		
Forward transconductance a	9 _{fs}	V _{DS} = 15 V, I _D = 12.4 A	-	56	-	S	
Dynamic ^b	•	<u> </u>					
Input capacitance	C _{iss}		-	2000	-	pF	
Output capacitance	C _{oss}	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz	-	260	-		
Reverse transfer capacitance	C _{rss}		-	150	-		
Total gate charge	Q_g	V _{DS} = 20 V, V _{GS} = 10 V, I _D = 12.4 A	-	33	50	nC	
			-	15	23		
Gate-source charge	Q_{gs}	$V_{DS} = 20 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 12.4 \text{ A}$	_	6.7	-		
Gate-drain charge	Q_{gd}		-	5.1	-		
Gate resistance	R_{g}	f = 1 MHz	-	1.4	2.1	Ω	
Turn-on delay time	t _{d(on)}		-	25	40		
Rise time	t _r	$V_{DD} = 20 \text{ V}, R_L = 2 \Omega$	_	12	20		
Turn-off delay time	t _{d(off)}	$I_D \cong 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$	-	25	40		
Fall time	t _f		-	10	15		
Turn-on delay time	t _{d(on)}		-	10	15	ns	
Rise time	t _r	$V_{DD} = 20 \text{ V}, R_{L} = 2 \Omega$	-	15	25		
Turn-off delay time	t _{d(off)}	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	30	45		
Fall time	t _f		-	10	15		
Drain-Source Body Diode Characterist	cs		l				
Continuous source-drain diode current	Is	T _C = 25 °C	-	-	30		
Pulse diode forward current	I _{SM}		-	-	50	Α	
Body diode voltage	V _{SD}	I _S = 10 A, V _{GS} = 0 V	-	0.8	1.2	V	
Body diode reverse recovery time	t _{rr}		-	30	60	ns	
Body diode reverse recovery charge	Q _{rr}	1	-	26	52	nC	
Reverse recovery fall time	t _a	$I_F = 10 \text{ A, di/dt} = 100 \text{ A/}\mu\text{s, T}_J = 25 ^{\circ}\text{C}$	-	17.5	-		
•	t _b	1	-	12.5	1	ns	

Notes

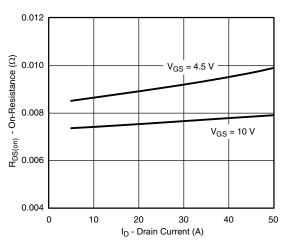
- a. Pulse test: pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

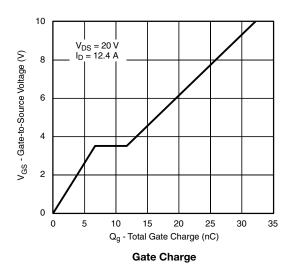


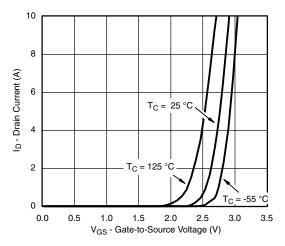


Output Characteristics

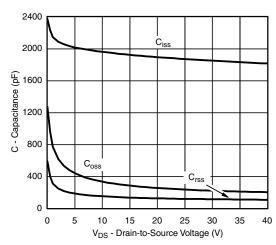


On-Resistance vs. Drain Current and Gate Voltage

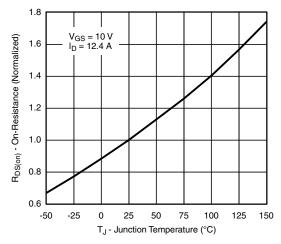




Transfer Characteristics

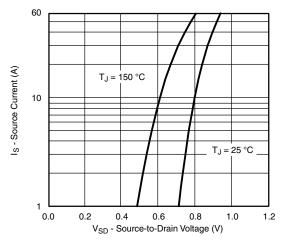


Capacitance

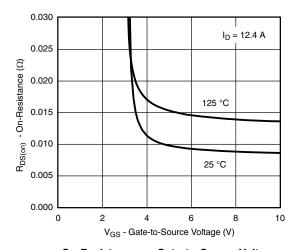


On-Resistance vs. Junction Temperature

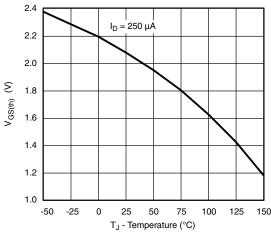




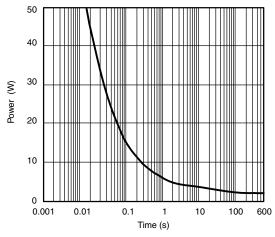
Source-Drain Diode Forward Voltage



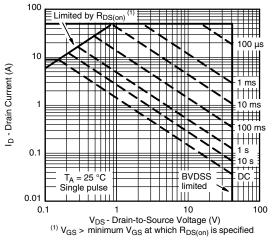
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

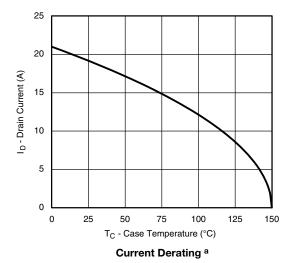


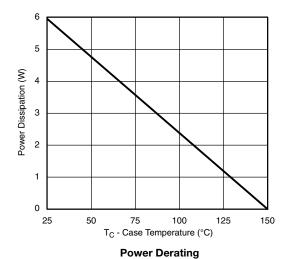
Single Pulse Power (Junction-to-Ambient)



Safe Operating Area, Junction-to-Ambient



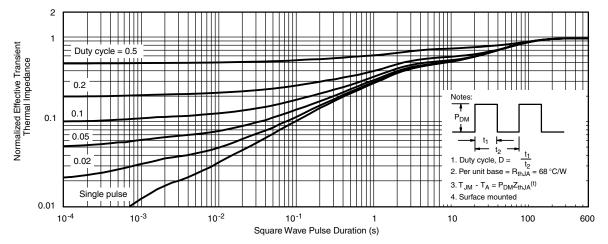




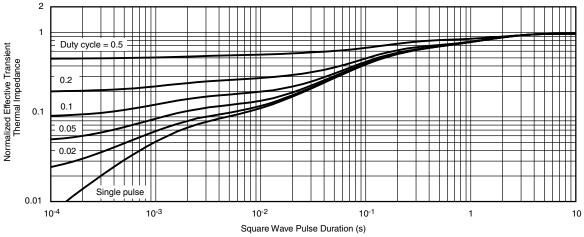
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Ambient

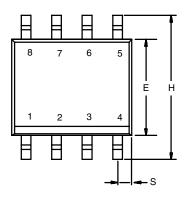


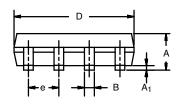
Normalized Thermal Transient Impedance, Junction-to-Foot

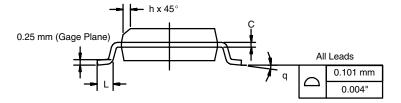
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SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIMETERS		INCHES		
DIM	Min	Max	Min	Max	
Α	1.35	1.75	0.053	0.069	
A ₁	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
Е	3.80	4.00	0.150	0.157	
е	1.27	BSC	0.050 BSC		
Н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
ECN: C-06527-Rev. I. 11-Sep-06					

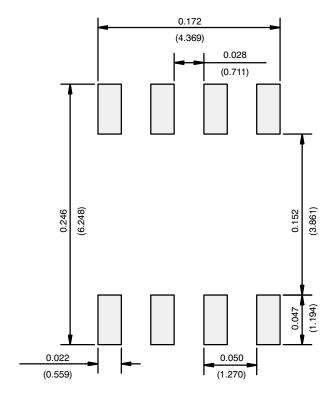
DWG: 5498

Document Number: 71192 www.vishay.com 11-Sep-06

LON NOTE



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)

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