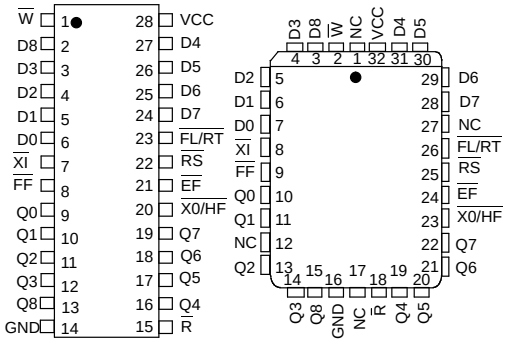
DALLAS SEMICONDUCTOR

DS2009
512 x 9 FIFO Chip

FEATURES

- First-in, first-out memory-based architecture
- Flexible 512 x 9 organization
- Low-power HCMOS technology
- Asynchronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- High performance
- Available in 35 ns, 50 ns, 65 ns, 80 ns, and 120 ns access times
- Optional industrial temperature range -40°C to +85°C available, designated N

PIN ASSIGNMENT



28-Pin DIP(300 and 600 Mil) 32-Pin PLCC

PIN DESCRIPTION

$\overline{W}$	–	WRITE
$\overline{R}$	–	READ
$\overline{RS}$	–	RESET
$\overline{FL/RT}$	–	First Load/Retransmit
D_{0-8}	–	Data In
Q_{0-8}	–	Data Out
$\overline{XI}$	–	Expansion In
$\overline{XO/HF}$	–	Expansion Out/Half Full
$\overline{FF}$	–	Full Flag
$\overline{EF}$	–	Empty Flag
V_{CC}	–	5 Volts
GND	–	Ground
NC	–	No Connect

DESCRIPTION

The DS2009 512 x 9 FIFO Chip implements a first-in, first-out algorithm featuring asynchronous read/write operations, full, empty and half-full flags, and unlimited expansion capability in both word size and depth. The main application of the DS2009 is as a rate buffer, sourcing and absorbing data at different rates (e.g., interfacing fast processors and slow peripherals). The full and empty flags are provided to prevent data overflow and underflow. A half-full flag is available in the single-device and width-expansion configurations. The data is loaded and emptied on a first-in, first-out (FIFO) basis, and the latency for the retrieval of data is approximately one load cycle (write). Since the writes and reads are internally sequential, thereby requiring no address information, the pinout definition will serve this and future higher-density devices. The ninth bit is provided to support control or parity functions.

OPERATION

Unlike conventional shift register-based FIFOs, the DS2009 employs a memory-based architecture wherein a byte written into the device does not ripple through. Instead, a byte written into the DS2009 is stored at a specific location where it remains until over-written. The byte can be read and re-read as often as desired.

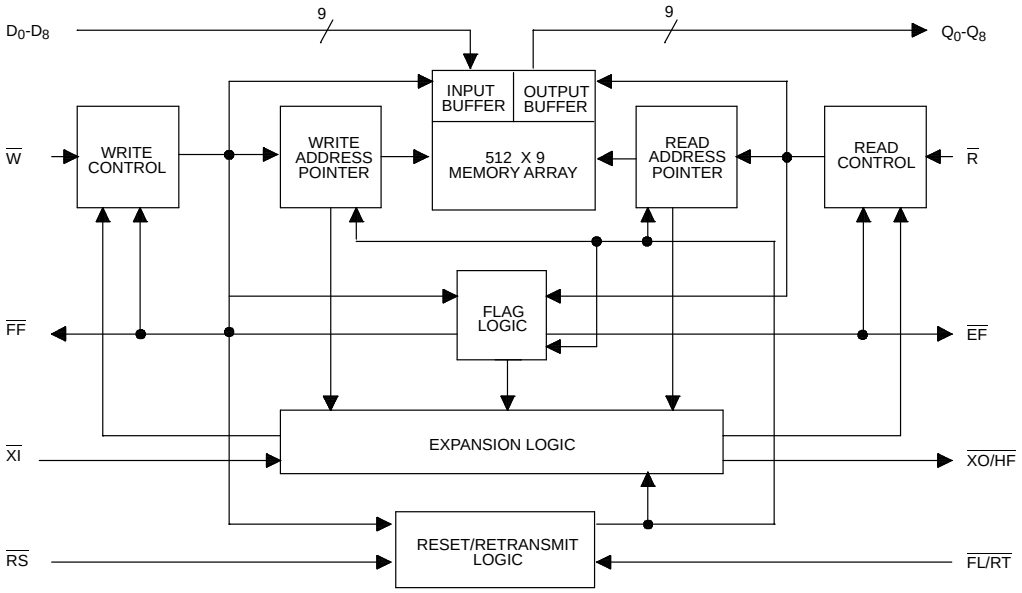
Twin address pointers (ring counters) automatically generate the address required for each write and read operation. The empty/full flag circuit prevents illogical operations, such as reading unwritten bytes (reading while empty) or over-writing unread bytes (writing while full). Once a byte stored at a given address has been read, it can be over-written.

Address pointers automatically loop back to address zero after reaching address 511. The empty/full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location. As long as the pointers do not catch one another, the FIFO can be written and read continuously without ever becoming full or empty.

Resetting the FIFO simply resets the address pointers to address zero. Pulsing retransmit resets the read address pointer without affecting the write address pointer.

With conventional FIFOs, implementation of a larger FIFO is accomplished by cascading the individual FIFOs. The penalty of cascading is often unacceptable ripple-through delays. The DS2009 allows implementation of very large FIFOs with no timing penalties. The memory-based architecture of the DS2009 can connect the read, write, data in, and data out lines of the DS2009 in parallel. The write and read control circuits of the individual FIFOs are then automatically enabled and disabled through the expansion in and expansion out pins as appropriate (see the "Expansion Timing" section for a more complete discussion).

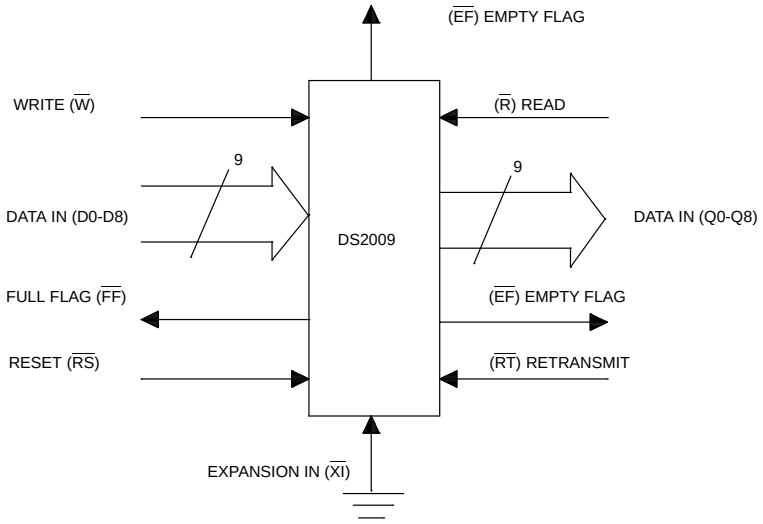
BLOCK DIAGRAM Figure 1



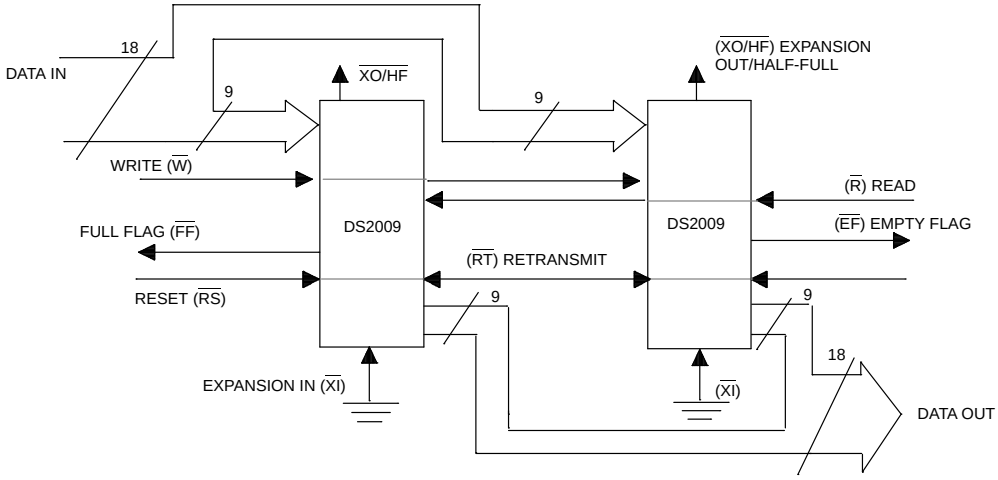
SINGLE DEVICE CONFIGURATION

A single DS2009 can be used when application requirements are for 512 words or less. The DS2009 is placed in single device configuration mode when the chip is reset with the Expansion In pin ($\overline{XI}$) grounded (see Figure 2).

A SINGLE 512 X 9 FIFO CONFIGURATION Figure 2



A 512 X 18 FIFO CONFIGURATION (WIDTH EXPANSION) Figure 3



NOTE:

Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$ and $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect flag output signals together.

DEPTH EXPANSION (DAISY CHAIN)

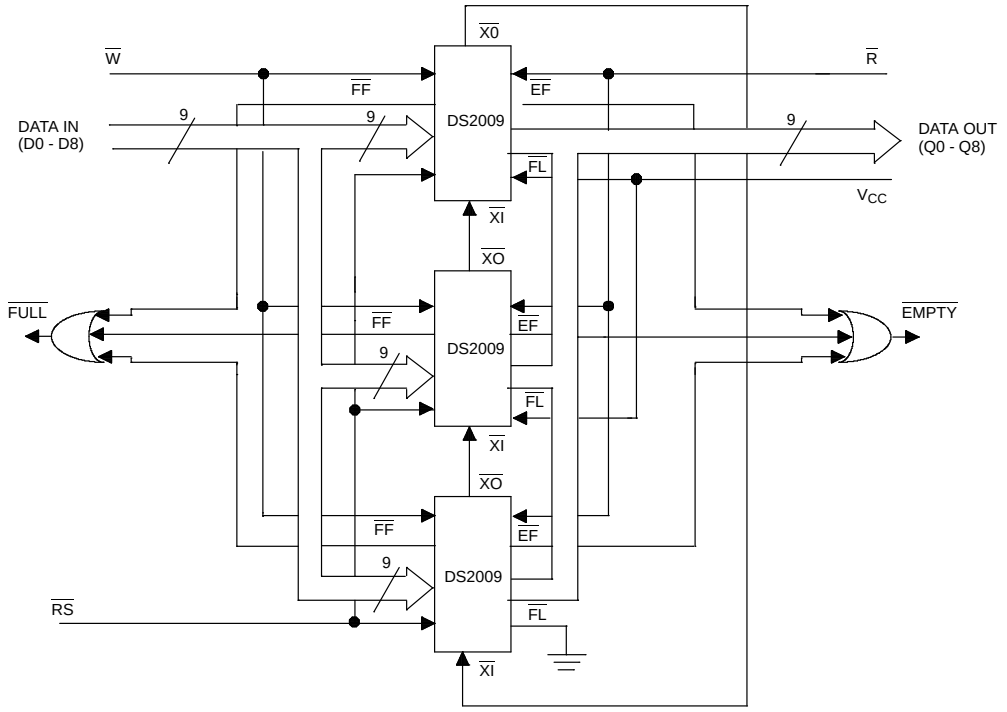
The DS2009 can easily be adapted to applications where more than 512 words are required. Figure 4 demonstrates depth expansion using three DS2009s. Any depth can be attained by adding DS2009s.

External logic is needed to generate a composite full flag and empty flag. This requires the ORing of all $\overline{EF}$s and the ORing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).

The DS2009 operates in the depth expansion configuration after the chip is reset under the following conditions.

1. The first device must be designated by grounding the First Load pin ($\overline{FL}$). The retransmit function is not allowed in the depth expansion mode.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. The half-full capability is not allowed in depth expansion.

A 1536 X 9 FIFO CONFIGURATION (DEPTH EXPANSION) Figure 4



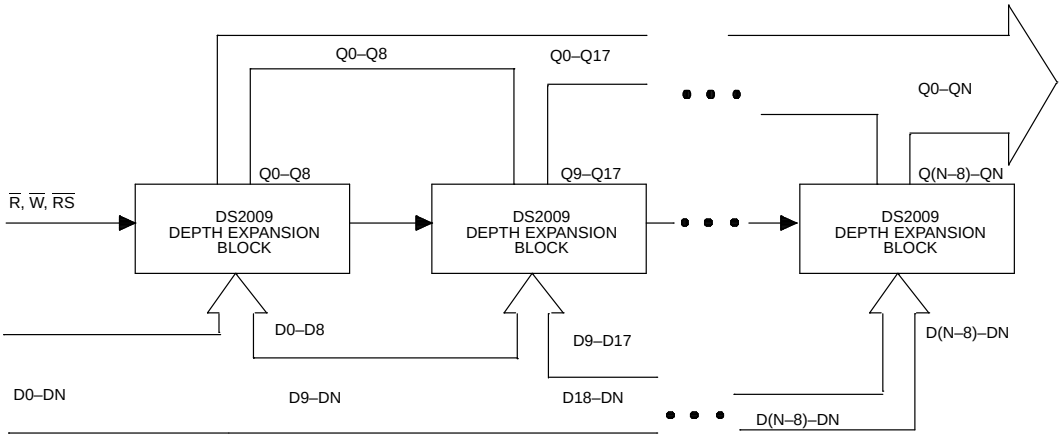
COMPOUND EXPANSION

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 5).

BIDIRECTIONAL APPLICATIONS

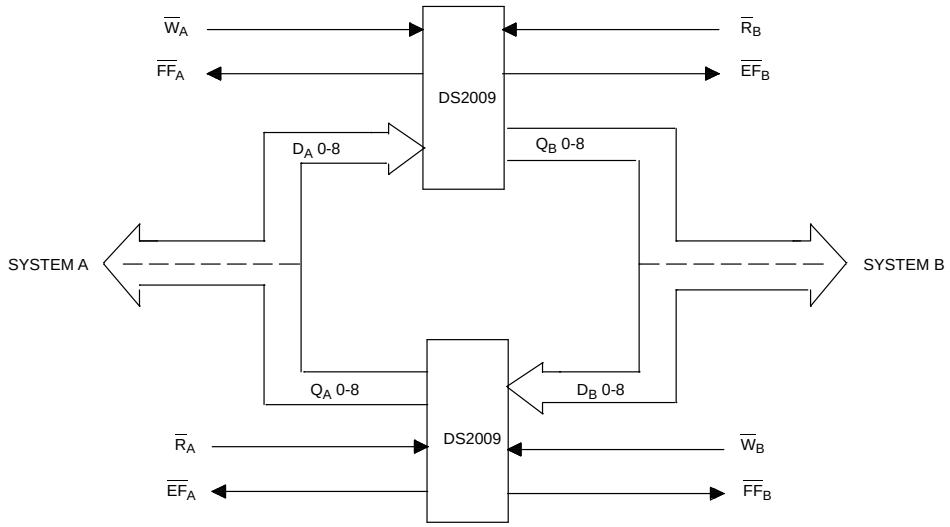
Bidirectional applications that require data buffering between two systems (each system capable of read and write operations) can be achieved by pairing DS2009s as shown in Figure 6. Care must be taken to assure that the appropriate flag is monitored by each system (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both depth expansion and width expansion can be used in this mode.

COMPOUND FIFO EXPANSION Figure 5



NOTES:
1. For depth expansion block diagram see "Depth Expansion" section and Figure 4.
2. For flag operation see "Width Expansion" section and Figure 3.

BIDIRECTIONAL FIFO APPLICATION Figure 6



HALF-FULL CAPABILITY

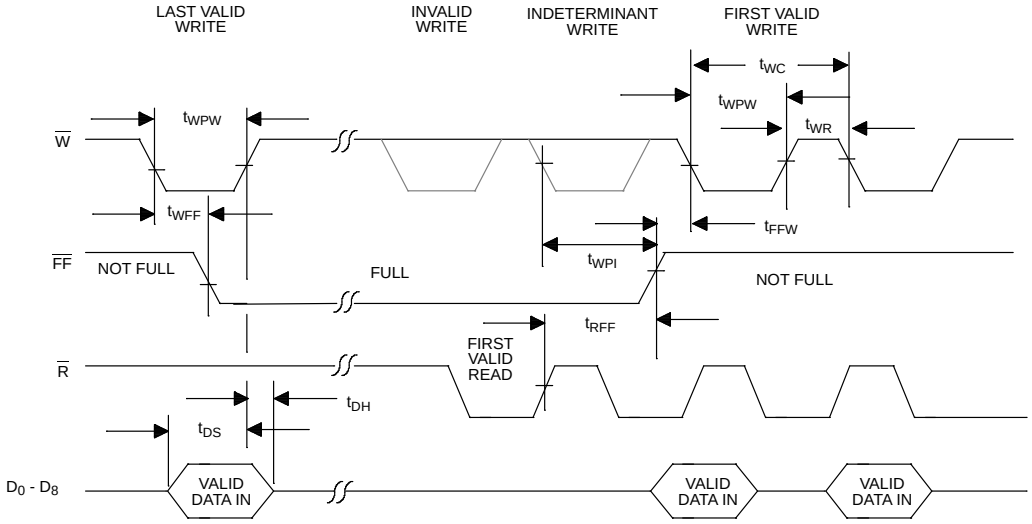
In the single-device and width-expansion modes, the $\overline{XO}/\overline{HF}$ output acts as an indication of a half-full memory. ($\overline{XI}$ must be tied low.) After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain low until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The half-full flag is then reset (forced high) by the rising edge of the read operation.

WRITE MODE

The DS2009 initiates a write cycle (see Figure 7) on the falling edge of the write enable control input ($\overline{W}$), provided that the Full Flag ($\overline{FF}$) is not asserted. Data setup

and hold time requirements must be satisfied with respect to the rising edge of $\overline{W}$. The data is stored sequentially and independent of any ongoing read operations. $\overline{FF}$ is asserted during the last valid write as the DS2009 becomes full. Write operations begun with $\overline{FF}$ low are inhibited. $\overline{FF}$ will go high t_{RFF} after completion of a valid read operation. Writes beginning after $\overline{FF}$ goes low and more than t_{WPI} before $\overline{FF}$ goes high are invalid (ignored). Writes beginning less than t_{WPI} before $\overline{FF}$ goes high and less than t_{FFW} later may or may not occur (be valid), depending on internal flag status.

WRITE AND FULL FLAG TIMING Figure 7



WRITE AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC}=5.0V ± 10%)

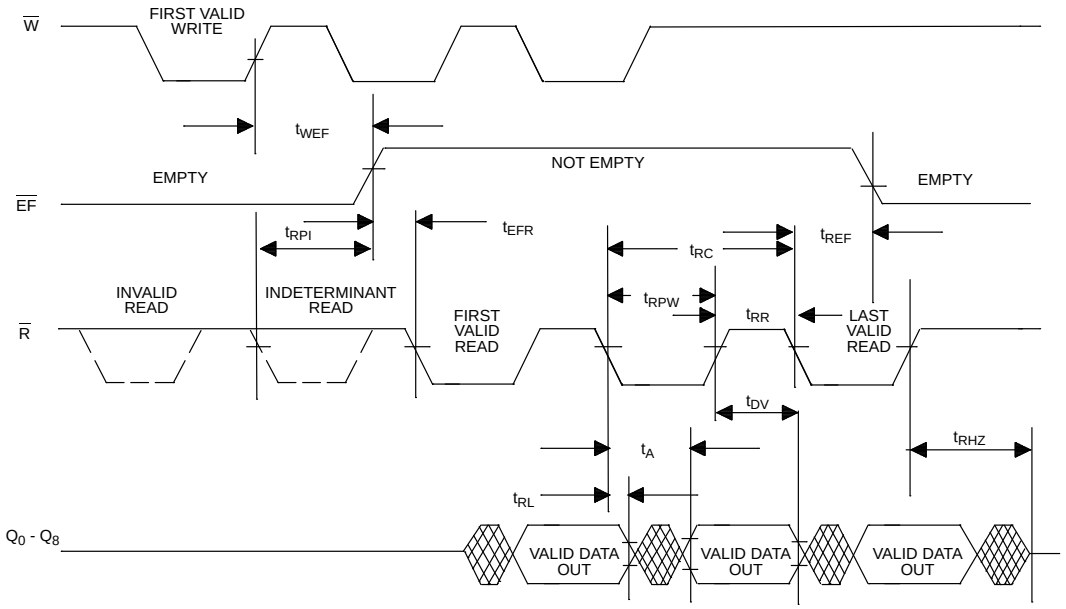
		DS2009-35		DS2009-50		DS2009-65		DS2009-80		DS2009-120			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**U**	**NOTES**
Write Cycle Time	t_{WC}	45		65		80		100		140		ns	
Write Pulse Width	t_{WPW}	35		50		65		80		120		ns	1
Write Recovery Time	t_{WR}	10		15		15		20		20		ns	
Data Setup Time	t_{DS}	15		20		25		30		40		ns	
Data Hold Time	t_{DH}	5		5		10		10		10		ns	
$\overline{W}$ Low to $\overline{FF}$ Low	t_{WFF}		30		45		60		70		110	ns	2
$\overline{FF}$ High to Valid Write	t_{FFW}		5		5		10		10		10	ns	2
$\overline{R}$ High to $\overline{FF}$ High	t_{RFF}		30		45		60		70		110	ns	2
Write Protect Indeterminate	t_{WPI}		15		20		25		25		35	ns	2

READ MODE

The DS2009 initiates a read cycle (see Figure 8) on the falling edge of Read Enable control input ($\overline{R}$), provided that the Empty Flag ($\overline{EF}$) is not asserted. In the read mode of operation, the DS2009 provides fast access to data from 9 of 4608 locations in the static storage array. The data is accessed on a FIFO basis independent of any ongoing write operations. After $\overline{R}$ goes high, data outputs will return to a high impedance condition until the next read operation.

In the event that all data has been read from the FIFO, the $\overline{EF}$ will go low, and further read operations will be inhibited (the data outputs will remain in high impedance). $\overline{EF}$ will go high t_{WEF} after completion of a valid write operation. Reads beginning t_{EFR} after $\overline{EF}$ goes high are valid. Reads begun after $\overline{EF}$ goes low and more than t_{RPI} before $\overline{EF}$ goes high are invalid (ignored). Reads beginning less than t_{RPI} before $\overline{EF}$ goes high and less than t_{EFR} later may or may not occur (be valid) depending on internal flag status.

READ AND EMPTY FLAG TIMING Figure 8



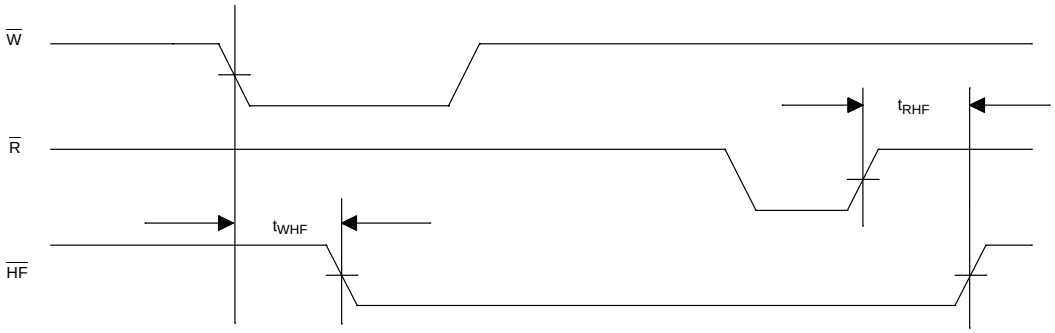
READ AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC}=5.0V ± 10%)

		DS2009-35		DS2009-50		DS2009-65		DS2009-80		DS2009–120			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**U**	**NOTES**
Read Cycle Time	t_{RC}	45		65		80		100		140		ns	
Access Time	t_A		35		50		65		80		120	ns	1
Read Recovery Time	t_{RR}	10		15		15		20		20		ns	
Read Pulse Width	t_{RPW}	35		50		65		80		120		ns	1
$\overline{R}$ Low to Low Z	t_{RL}	5		10		10		10		20		ns	2
Data Valid from $\overline{R}$ High	t_{DV}	5		5		5		5		5		ns	2
$\overline{R}$ High to High Z	t_{RHZ}		20		25		25		25		35	ns	2
$\overline{R}$ Low to $\overline{EF}$ Low	t_{REF}		30		45		60		70		110	ns	2
$\overline{EF}$ High to Valid Read	t_{EFR}		5		5		10		10		10	ns	2
$\overline{W}$ High to $\overline{EF}$ High	t_{WEF}		30		45		60		70		110	ns	2
Read Protect Indeterminate	t_{RPI}		15		20		25		25		35	ns	2

HALF-FULL MODE

Unlike the full and empty flags, the half-full flag does not prevent device reads and writes. This flag is set by the next falling edge of write when the memory is 256 locations full. The flag will remain set until the memory is less than or equal to 256 locations full. The read operation (rising edge), which results in the memory being 256 locations full, removes the flag.

HALF-FULL FLAG TIMING Figure 9



HALF-FULL FLAG AC CHARACTERISTICS (0°C to 70°C; V_{CC}=5.0V ± 10%)

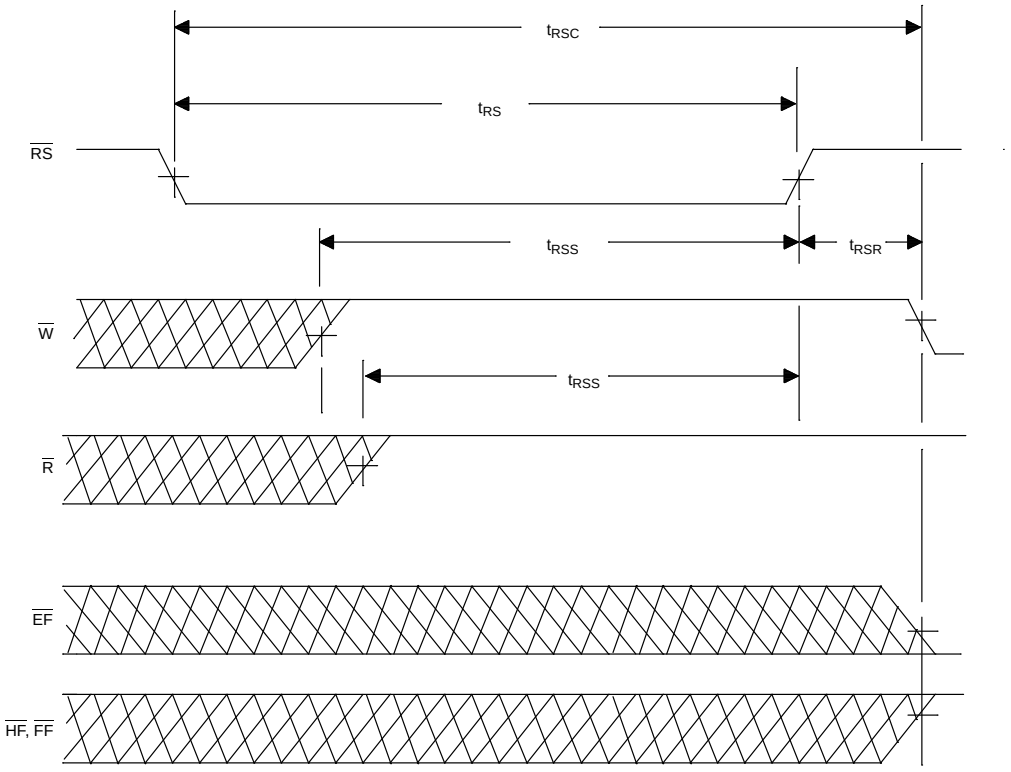
		DS2009-35		DS2009-50		DS2009-65		DS2009-80		DS2009-120		
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
Write Low to Half-Full Flag Low	t_{WHF}		45		65		80		100		140	ns
Read High to Half-Full Flag High	t_{RHF}		45		65		80		100		140	ns

RESET

The DS2009 is reset (see Figure 10) whenever the Reset pin ($\overline{RS}$) is in the low state. During a reset, both the internal read and write pointer are set to the first location. Reset is required after a power-up before a write operation can begin.

Although neither $\overline{W}$ or $\overline{R}$ need be high when $\overline{RS}$ goes low, both $\overline{W}$ are $\overline{R}$ must be high t_{RSS} before $\overline{RS}$ goes high and must remain high t_{RSR} afterwards. Refer to the following discussion for the required state of $\overline{FL}/\overline{RT}$ and $\overline{XI}$ during reset.

RESET Figure 10



NOTES:

$\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during reset, but flags will be valid at t_{RSC}.

RESET AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC}=5.0V ± 10%)

		DS2009-35		DS2009-80		DS2009-65		DS2009-80		DS2009-120			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**U**	**N**
Reset Cycle Time	t_{RSC}	45		65		80		100		140		ns	
Reset Pulse Width	t_{RS}	35		50		65		80		120		ns	1
Reset Recovery Time	t_{RSR}	10		15		15		20		20		ns	
Reset Setup Time	t_{RSS}	30		40		50		60		100		ns	2

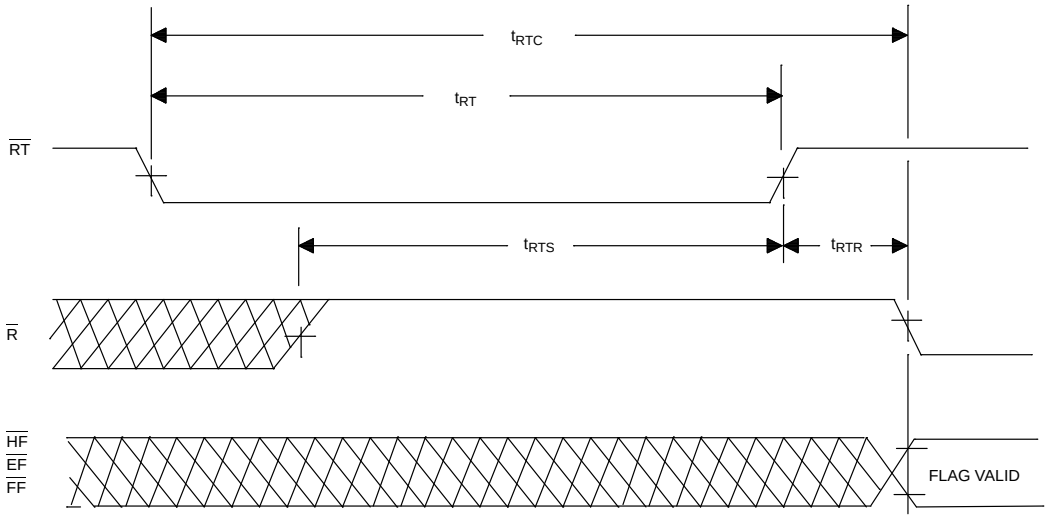
RETRANSMIT

The DS2009 can be made to retransmit (re-read previously read data) after the Retransmit pin ($\overline{RT}$) is pulsed low (see Figure 11).

A retransmit operation sets the internal read pointer to the first physical location in the array but will not affect the position of the write pointer. $\overline{R}$ must be inactive t_{RTS} before $\overline{RT}$ goes high and must remain high for t_{RTR} afterwards.

The retransmit function is particularly useful when blocks of less than 512 writes are performed between resets. The retransmit feature is not compatible with depth expansion.

RETRANSMIT Figure 11



NOTE:
$\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during retransmit, but flags will be valid at t_{RTC}.

RETRANSMIT
AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5.0V ± 10%)

		DS2009-35		DS2009-80		DS2009-65		DS2009-80		DS2009-120			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**U**	**N**
Retransmit Cycle Time	t_{RTC}	45		65		80		100		140		ns	
Retransmit Pulse Width	t_{RT}	35		50		65		80		120		ns	1
Retransmit Recovery Time	t_{RTR}	10		15		15		20		20		ns	
Retransmit Setup Time	t_{RTS}	30		40		50		60		100		ns	

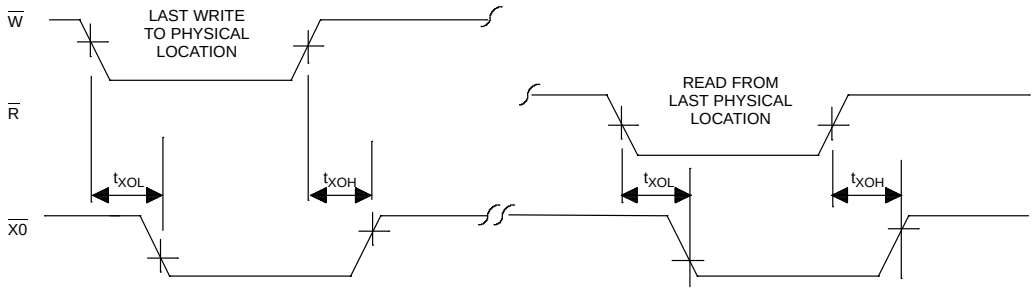
EXPANSION TIMING

Figures 12 and 13 illustrate the timing of the expansion out and expansion in signals. Discussion of expansion out/expansion in timing is provided to clarify how depth expansion works. Inasmuch as expansion out pins are generally connected only to expansion in pins, the user need not be concerned with actual timing in a normal depth expanded application unless extreme propagation delays exist between the $\overline{XO}$ and $\overline{XI}$ pin pairs.

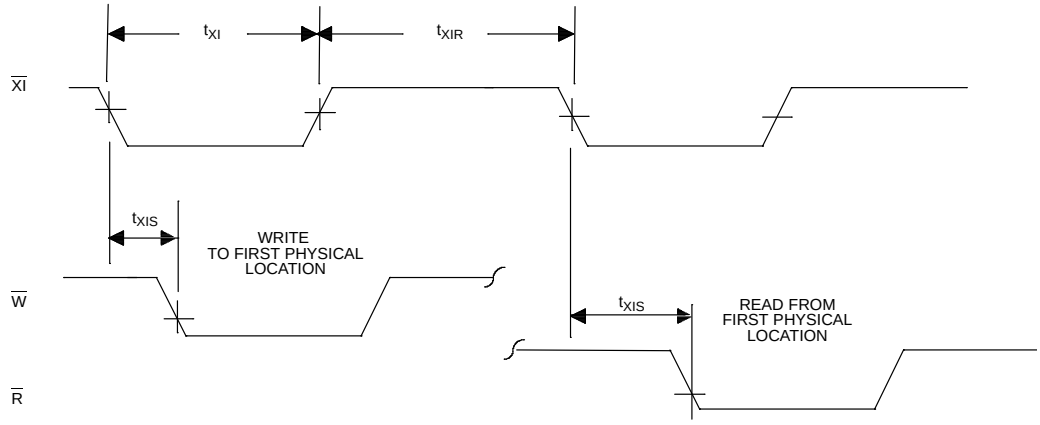
Expansion out pulses are the image of the write and read signals that cause them: delayed in time by t_{XOL} and t_{XOH}. The expansion out signal is propagated when the last physical location in the memory array is written and again when it is read (last read). This is in contrast to when the full and empty flags are activated, which is in response to writing and reading a last available location.

When in depth expansion mode, a given DS2009 will begin writing and reading as soon as valid write and read signals begin, provided $\overline{FL}$ was grounded at reset time. A DS2009 in depth expansion mode with $\overline{FL}$ high at reset will not begin writing until after an expansion in pulse occurs. It will not begin reading until a second expansion in pulse occurs and the empty flag has gone high. Expansion in pulses must occur t_{XIS} before the write and read signals they are intended to enable. Minimum expansion in pulse width, t_{XI}, and recovery time, t_{XIR}, must be observed.

EXPANSION OUT TIMING Figure 12



EXPANSION IN TIMING Figure 13



EXPANSION LOGIC
AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 5.0V ± 10%)

		DS2009-35		DS2009-80		DS2009-65		DS2009-80		DS2009-120			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**U**	**N**
Expansion Out Low	t_{XOL}		30		45		55		70		100	ns	
Expansion Out High	t_{XOH}		30		45		55		70		100	ns	
Expansion in Pulse Width	t_{XI}	35		50		65		80		120		ns	1
Expansion in Recovery Time	t_{XIR}	10		15		15		20		20		ns	
Expansion in Setup Time	t_{XIS}	15		20		25		30		40		ns	

AC TEST CONDITIONS

Input Levels	GND to 3.0V
Transition Times	5ns
Input Signal Timing Reference Level	1.5V
Output Signal Timing Reference Level	0.8V and 2.2V
Ambient Temperature	0°C to +70°C
V_{CC}	5.0V ± 10%

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Total Device Power Dissipation	1 Watt
Output Current per Pin	20 mA

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	3
Ground	GND		0		V	
Logic 1 Voltage All Inputs	V_{IH}	2.0		V_{CC} +0.3	V	3
Logic 0 Inputs	V_{IL}	-0.3		+0.8	V	3, 4

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5.0V $\pm$ 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current (Any Input)	I_{IL}	-1		1	µA	5
Output Leakage Current	I_{OL}	-10		10	µA	6
Output Logic 1 Voltage I_{OUT} = -1mA	V_{OH}	2.4			V	3
Output Logic 0 Voltage I_{OUT} = 4mA	V_{OL}			0.4	V	3
Average V_{CC} Power Supply Current – 35ns, 50ns, 60ns, 80ns, 120ns	I_{CC1}			100	mA	7, 9
Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RST}$ = $\overline{FL/RT}$ = V_{IH})	I_{CC2}			8	mA	7
Power Down Current (All Input = V_{CC} -0.2V)	I_{CC3}			500	µA	7, 10

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance on Input Pins	C_I			7	pF	
Capacitance on Output Pins	C_O			12	pF	8

NOTES:

1. Pulse widths less than minimum values are not allowed.
2. Measured using output load shown in Output Load diagram.
3. All voltages are referenced to ground.
4. -1.5 volt undershoots are allowed for 10ns once per cycle.
5. Measured with $0.4 \leq V_{IN} \leq V_{CC}$.
6. $\overline{R} \geq V_{IH}$, $0.4 \geq V_{OUT} \leq V_{CC}$.
7. I_{CC} measurements are made with outputs open.
8. With output buffer deselected.
9. DS2010, DS2011, DS2012, and DS2013 have I_{CC1}, = 120 mA MAX for 50ns, 65ns, 80ns, and 120ns speed grades.
10. DS2010 has I_{CC3} = 1mA MAX; DS2011, DS2012, DS2013 have I_{CC3} = 2mA MAX.

OUTPUT LOAD Figure 14