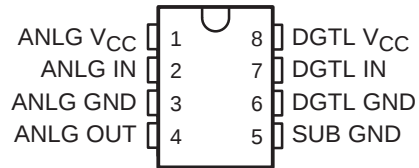


TL1591 SAMPLE-AND-HOLD CIRCUIT FOR CCD IMAGERS

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- 15-MHz Sampling Rate
- 30-ns Acquisition Time
- Diode-Bridge Switch
- 25-MHz Bandwidth
- Low-Voltage Supply

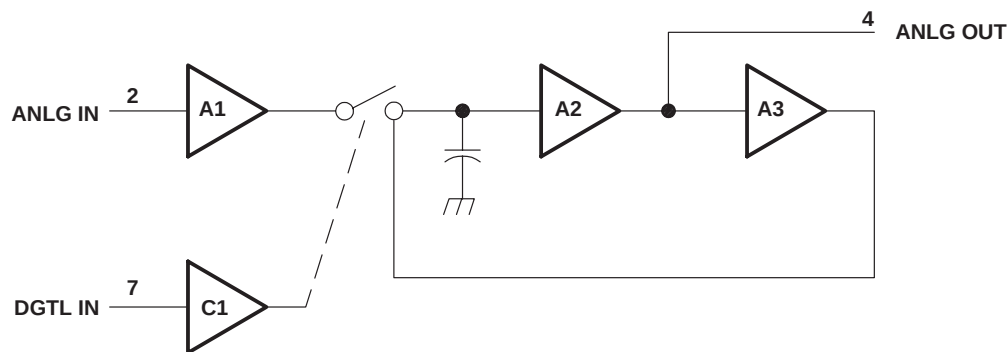
P OR PS PACKAGE
(TOP VIEW)



description

The TL1591 is a monolithic integrated sample-and-hold circuit that uses the BiFET process with Schottky-barrier diodes and is designed for use with CCD area imagers. This device consists of an ultra-fast input-buffer amplifier, a digital-controlled diode-bridge switch, and a high-impedance output buffer amplifier. The electronic switch is controlled by an LS-TTL-compatible logic input.

functional block diagram



This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, precautions should be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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TL1591

SAMPLE-AND-HOLD CIRCUIT FOR CCD IMAGERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage range, V_I	0 to V_{CC}
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	–25°C to 80°C
Storage temperature range, T_{STG}	–55°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 80^\circ\text{C}$
	POWER RATING		POWER RATING
P	1000 mW	8.0 mW/°C	560 mW
PS	725 mW	5.8 mW/°C	406 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.5	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Peak-to-peak input voltage, $V_{I(PP)}$			0.8	V
Operating free-air temperature, T_A	–25		80	°C

electrical characteristics over ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP [‡]	MAX	UNIT
V_{IK}	Input clamp voltage					–1.5	V
$V_{O(PP)}$	Peak-to-peak output voltage				1.1		V
I_{IH}	High-level input current	$V_{CC} = 5.5\text{ V}$, $V_{IH} = 2.7\text{ V}$				20	μA
I_{IL}	Low-level input current	$V_{CC} = 5.5\text{ V}$, $V_{IL} = 0.4\text{ V}$		–0.28		–0.4	mA
I_O	Output current				0.6		mA
I_{CC}	Supply current	$V_{CC} = 5.5\text{ V}$			15	20	mA
r_i	Input resistance				10		kΩ
r_o	Output resistance				50		Ω

operating characteristics

PARAMETER		MIN	TYP [‡]	MAX	UNIT
	Linearity		0.7%	2%	
A_V	Voltage amplification		0.8	0.9	V/V
	Sample-to-hold offset error		15		mV
	Sample-mode offset error	–150	–50	50	mV
	Hold-mode feedthrough			–50	dB
	Hold-mode droop			100	μV/μs

[‡] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.



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dynamic characteristics (see Figure 1)

PARAMETER	MIN	TYP [†]	MAX	UNIT
Acquisition time, 0.6 V to 2%		18		ns
Acquisition time, 0.6 V to 1%		31		ns
Hold-mode settling time		35		ns
Sampling-mode bandwidth		25		MHz
Sampling rate			15	MHz

[†] All typical values are at $V_{CC} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION

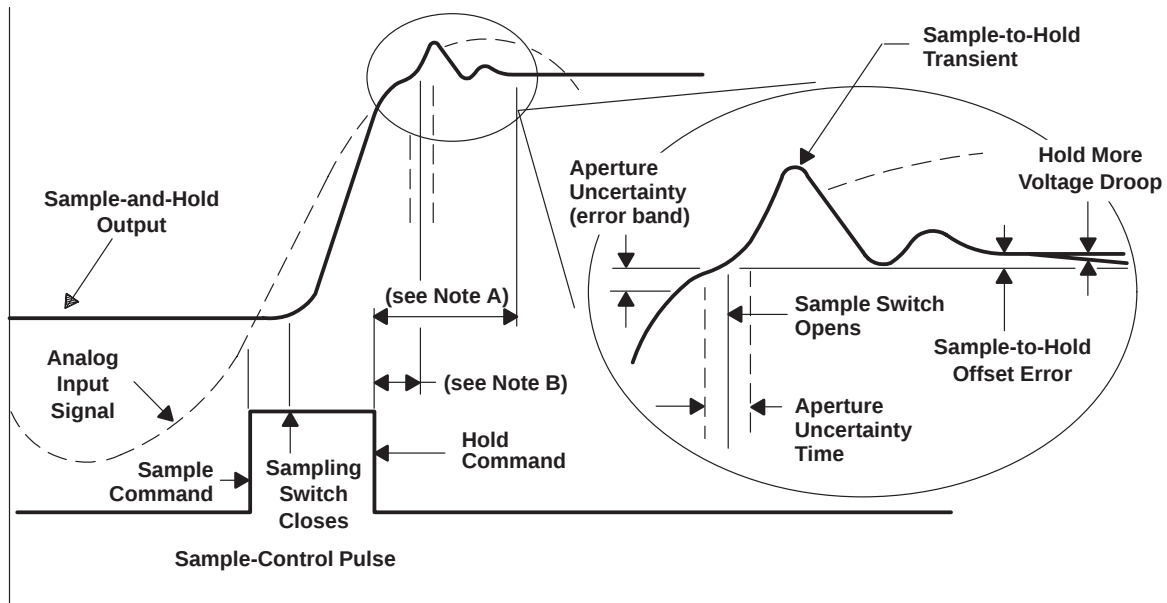


Figure 1. Sample-Hold Definitions

- NOTES: A. Hold-mode settling time is the time from the hold command transition until the output has settled within a specified error band around the final value.
- B. Acquisition time is the time required, after the closing of the sampling switch, for the hold capacitor to charge to a full-scale voltage change and then remain within a specified error band around the final value.

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PARAMETER MEASUREMENT INFORMATION

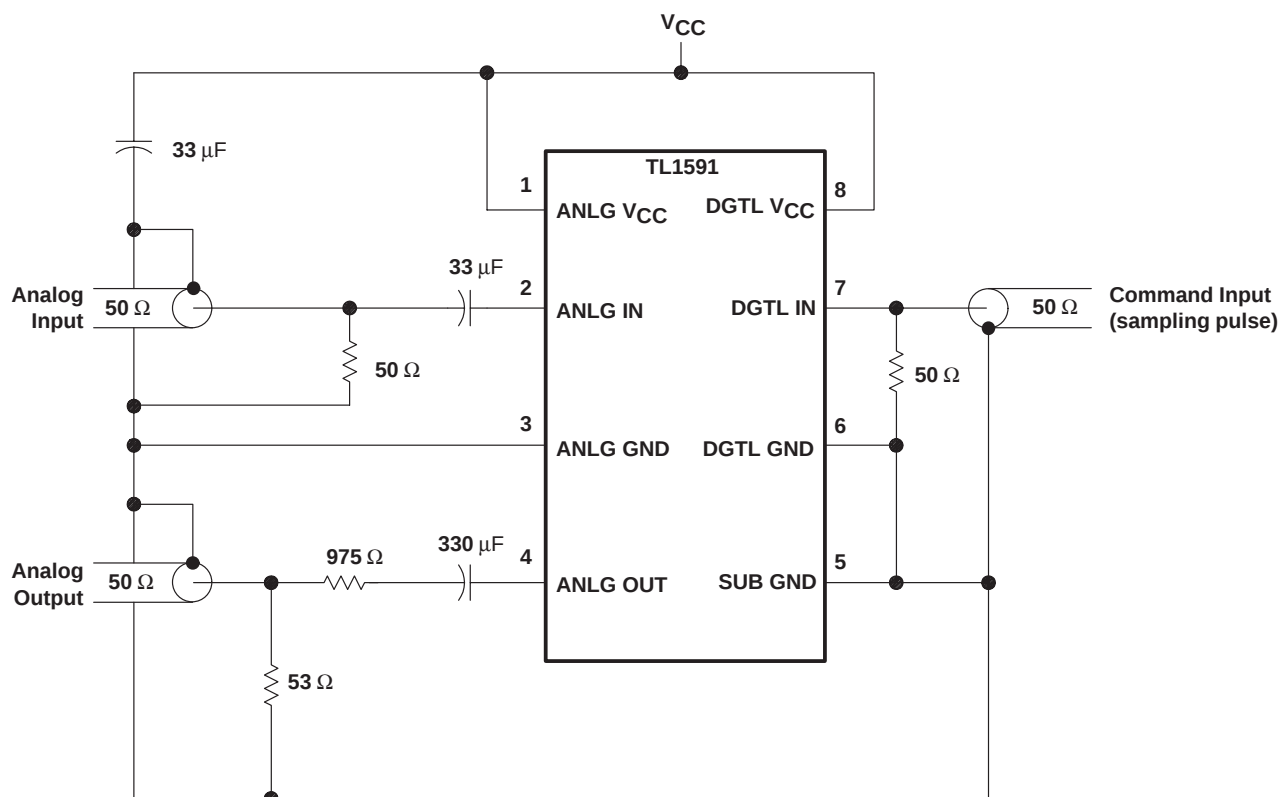


Figure 2. Test Circuit

TYPICAL CHARACTERISTICS

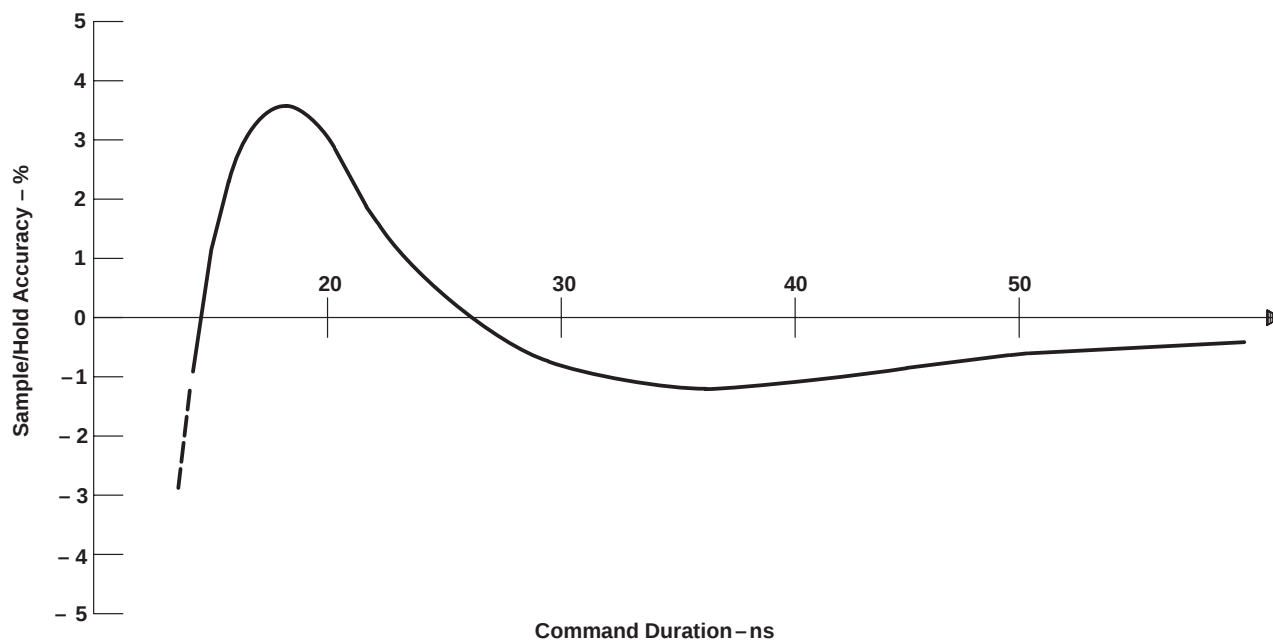


Figure 3. Sample/Hold Accuracy Versus Command Duration

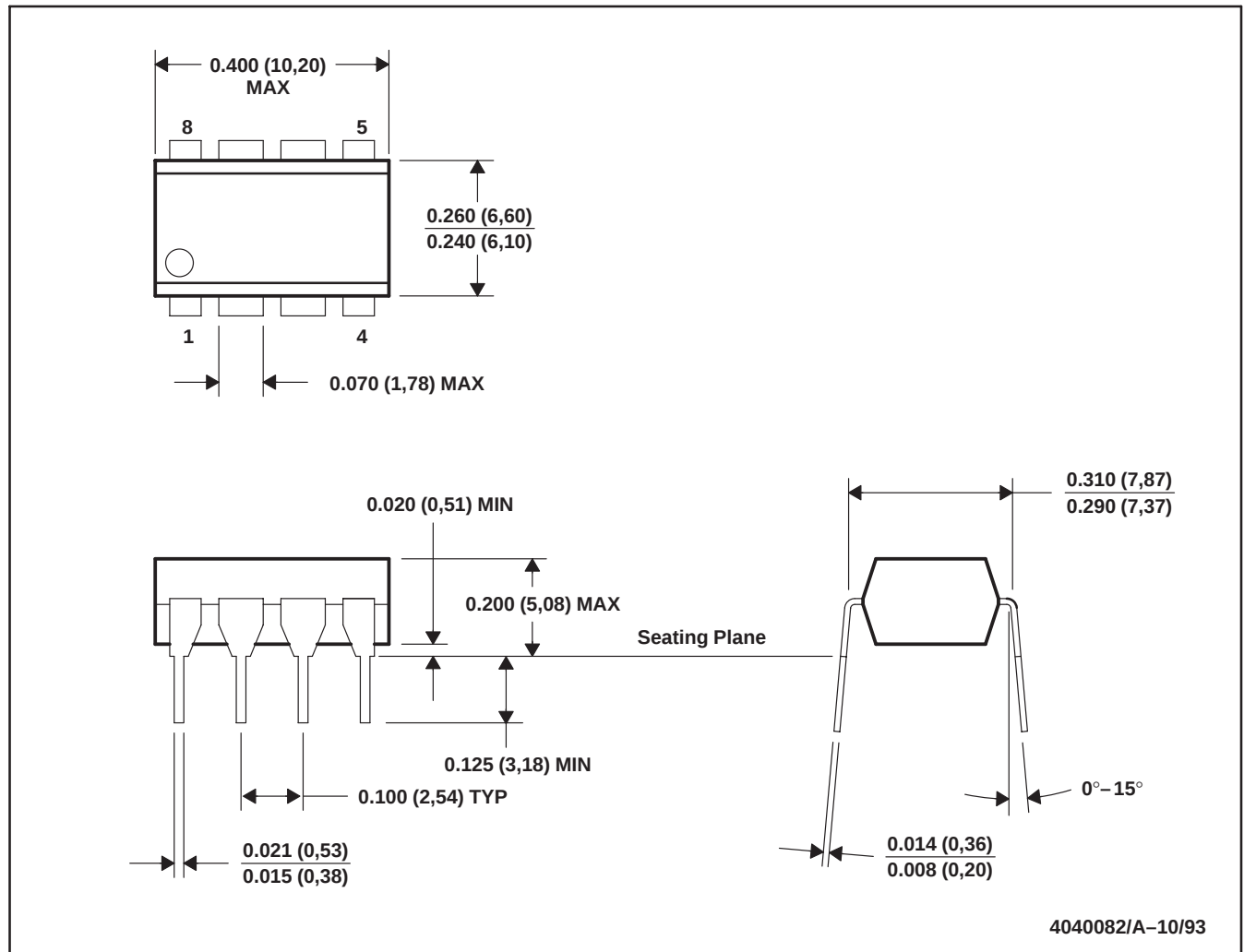
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MECHANICAL DATA

P(R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE

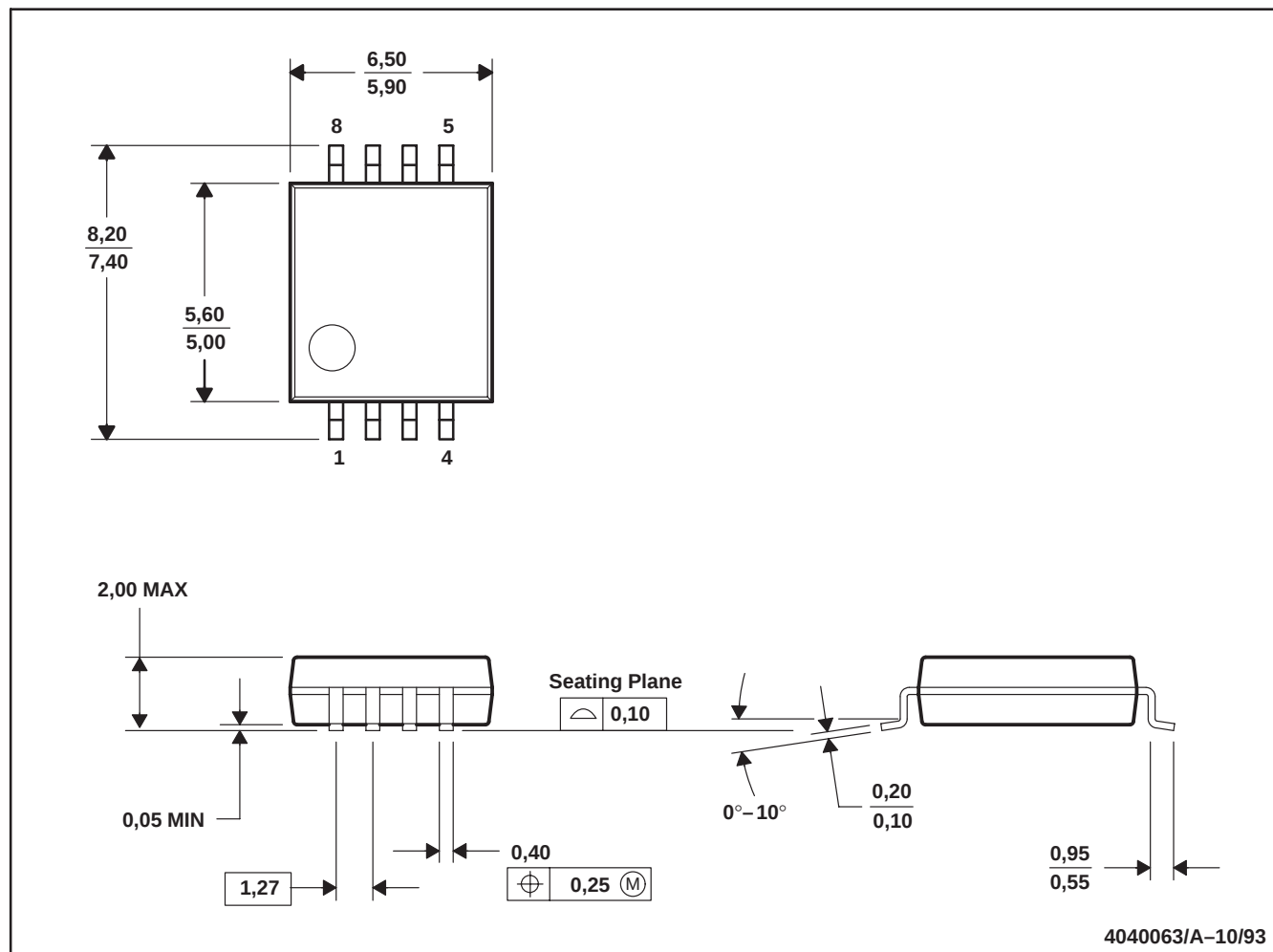


- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

MECHANICAL DATA

PS/R-PDSO-G8

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

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