

FEATURES

- **Low Offset Voltage: 750 μ V Maximum**
- **Low Offset Drift: 5 μ V/ $^{\circ}$ C Maximum**
- **Low Input Bias Current:**
1pA (Typical at 25 $^{\circ}$ C)
40pA ($\leq$ 85 $^{\circ}$ C)
- **Rail-to-Rail Inputs and Outputs**
- **2.5V to 5.5V Operation Voltage**
- **Gain Bandwidth Product: 1.5MHz**
- **CMRR: 70dB Minimum**
- **PSRR: 94dB Minimum**
- **Supply Current: 110 μ A per Amplifier**
- **Shutdown Current: 1.1 μ A per Amplifier**
- **Available in 8-Lead MSOP and 10-Lead DFN Packages (LTC6084) and 16-Lead SSOP and DFN Packages (LTC6085)**

APPLICATIONS

- Portable Test Equipment
- Medical Equipment
- Consumer Electronics
- Data Acquisition

DESCRIPTION

The LTC[®]6084/LTC6085 are dual/quad, low cost, low offset, rail-to-rail input/output, unity-gain stable CMOS operational amplifiers that feature 1pA of input bias current.

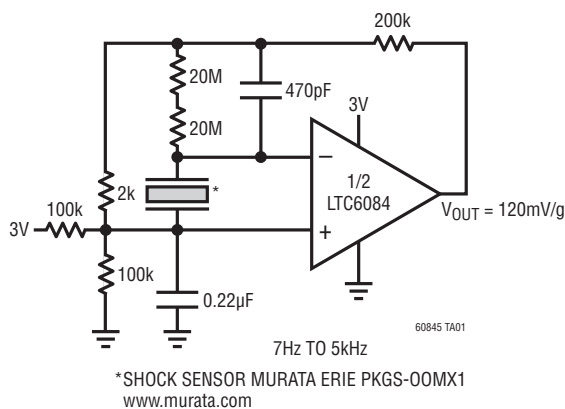
A 1.5MHz gain bandwidth, and 0.5V/ μ s slew rate, along with the wide supply range and a low 0.75mV offset, make the LTC6084/LTC6085 useful in an extensive variety of applications from data acquisition to medical equipment and consumer electronics. The 110 μ A supply current and the shutdown mode are ideal for signal processing applications which demand performance with minimal power.

The LTC6084/LTC6085 have an output stage which swings within 5mV of either supply rail to maximize signal dynamic range in low supply applications. The input common mode range includes the entire supply voltage. These op amps are specified on power supply voltages of 2.5V and 5V from -40 $^{\circ}$ C to 125 $^{\circ}$ C. The dual amplifier LTC6084 is available in 8-lead MSOP and 10-lead DFN packages. The quad amplifier LTC6085 is available in 16-lead SSOP and DFN packages.

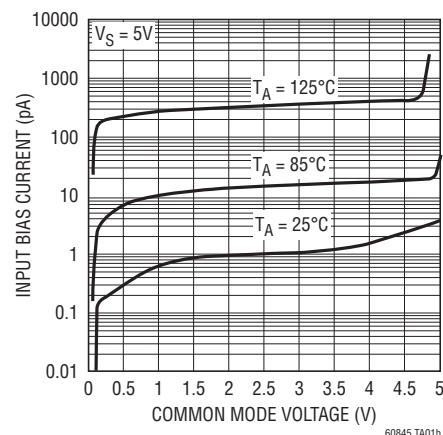
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TYPICAL APPLICATION

Shock Sensor Amplifier



**Input Bias Current
vs Common Mode Voltage**



LTC6084/LTC6085

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-)	6V
Input Voltage	V^- to V^+
Input Current	$\pm 10\text{mA}$
SHDNA/SHDNB Voltage	V^- to V^+
Output Short-Circuit Duration (Note 2)	Indefinite
Operating Temperature Range (Note 3)	
LTC6084C/LTC6085C	-40°C to 85°C
LTC6084H/LTC6085H	-40°C to 125°C

Specified Temperature Range (Note 4)	
LTC6084C/LTC6085C	0°C to 70°C
LTC6084H/LTC6085H	-40°C to 125°C
Junction Temperature	150°C
Storage Temperature Range	-65°C to 125°C
Lead Temperature (Soldering, 10 sec)	
MS8, GN Only	300°C

PIN CONFIGURATION

TOP VIEW MS8 PACKAGE 8-LEAD PLASTIC MSOP $T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 200^\circ\text{C/W}$	TOP VIEW DD PACKAGE 10-LEAD (3mm $\times$ 3mm) PLASTIC DFN $T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 43^\circ\text{C/W}$ EXPOSED PAD (PIN 11) IS V^-, MUST BE SOLDERED TO PCB
TOP VIEW GN PACKAGE 16-LEAD PLASTIC SSOP NARROW $T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 110^\circ\text{C/W}$	TOP VIEW DHC PACKAGE 16-LEAD (5mm $\times$ 3mm) PLASTIC DFN $T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 43^\circ\text{C/W}$ EXPOSED PAD (PIN 17) IS V^-, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6084CMS8#PBF	LTC6084CMS8#TRPBF	LTDNG	8-Lead Plastic MSOP	0°C to 70°C
LTC6084HMS8#PBF	LTC6084HMS8#TRPBF	LTDNG	8-Lead Plastic MSOP	-40°C to 125°C
LTC6084CDD#PBF	LTC6084CDD#TRPBF	LDNH	10-Lead (3mm $\times$ 3mm) Plastic DFN	0°C to 70°C
LTC6084HDD#PBF	LTC6084HDD#TRPBF	LDNH	10-Lead (3mm $\times$ 3mm) Plastic DFN	-40°C to 125°C

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6085CGN#PBF	LTC6085CGN#TRPBF	6085	16-Lead Plastic SSOP	0°C to 70°C
LTC6085HGN#PBF	LTC6085HGN#TRPBF	6085	16-Lead Plastic SSOP	–40°C to 125°C
LTC6085CDHC#PBF	LTC6085CDHC#TRPBF	6085	16-Lead (5mm × 3mm) Plastic DFN	0°C to 70°C
LTC6085HDHC#PBF	LTC6085HDHC#TRPBF	6085	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. Test conditions are $V^+ = 2.5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 0.5\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		C SUFFIX			H SUFFIX			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Offset Voltage (Note 5)	LTC6084MS8, LTC6085GN			300	750		300	750	μV
		LTC6084DD, LTC6085DHC	●		300	1100		300	1100	μV
		LTC6084MS8, LTC6085GN	●			900			1100	μV
		LTC6084DD, LTC6085DHC	●			1350			1600	μV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift (Note 6)		●		2	5		2	5	$\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current (Notes 5, 7)	Guaranteed by 5V Test	●		1	40		1	750	pA
I_{OS}	Input Offset Current (Notes 5, 7)	Guaranteed by 5V Test	●		0.5	30		0.5	150	pA
e_n	Input Noise Voltage Density	$f = 1\text{kHz}$ $f = 10\text{kHz}$			31 27			31 27		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$
	Input Noise Voltage	0.1Hz to 10Hz			3			3		μV_{P-P}
i_n	Input Noise Current Density (Note 8)				0.56			0.56		$\text{fA}/\sqrt{\text{Hz}}$
	Input Common Mode Range		●	V^-		V^+	V^-		V^+	V
C_{IN}	Input Capacitance Differential Mode Common Mode	$f = 100\text{kHz}$			5 9			5 9		pF pF
CMRR	Common Mode Rejection Ratio	$0 \leq V_{CM} \leq 2.5\text{V}$	●	64 63	80		64 61	80		dB dB
PSRR	Power Supply Rejection Ratio	$V_S = 2.5\text{V}$ to 5.5V	●	94 91	115		94 89	115		dB dB
V_{OUT}	Output Voltage, High, (Referred to V^+)	No Load	●		0.5	5		0.5	10	mV
		$I_{SOURCE} = 1\text{mA}$	●		39	85		39	100	mV
		$I_{SOURCE} = 5\text{mA}$	●		220	460		220		mV
	Output Voltage, Low, (Referred to V^-)	No Load	●		0.5	5		0.5	10	mV
		$I_{SINK} = 1\text{mA}$	●		36	85		36	100	mV
		$I_{SINK} = 5\text{mA}$	●		200	460		200		mV
A_{VOL}	Large-Signal Voltage Gain	$R_{LOAD} = 10\text{k}\Omega$, $0.4\text{V} \leq V_{OUT} \leq 2.1\text{V}$	●	400 200	2000		400 150	2000		V/mV V/mV

LTC6084/LTC6085

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. Test conditions are $V^+ = 2.5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = 0.5\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		C SUFFIX			H SUFFIX			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{SC}	Output Short-Circuit Current	Source and Sink	●	7.7 6	12.5		7.7 4.5	12.5		mA mA
SR	Slew Rate	$A_V = 1$			0.5			0.5		V/ μs
GBW	Gain Bandwidth Product ($f_{\text{TEST}} = 10\text{kHz}$)	$R_{\text{LOAD}} = 50\text{k}\Omega$, $V_{\text{CM}} = 1.25\text{V}$	●	0.9 0.7	1.5		0.9 0.6	1.5		MHz
Φ_0	Phase Margin	$R_L = 10\text{k}\Omega$, $C_L = 150\text{pF}$, $A_V = 1$			45			45		Deg
t_S	Settling Time 0.1%	$V_{\text{STEP}} = 1\text{V}$, $A_V = 1$			6			6		μs
I_S	Supply Current (Per Amplifier)	No Load	●		110	130 140		110	130 145	μA μA
	Shutdown Current (Per Amplifier)	Shutdown, $V_{\text{SHDNx}} \leq 0.5\text{V}$	●		0.2	0.3		0.2	0.5	μA
V_S	Supply Voltage Range	Guaranteed by the PSRR Test	●	2.5		5.5	2.5		5.5	V
	Channel Separation	$f_S = 10\text{kHz}$			-120			-120		dB
	Shutdown Logic	SHDNx High SHDNx Low		1.8		0.5	1.8		0.5	V V
t_{ON}	Turn On Time	$V_{\text{SHDNx}} = 0.5\text{V}$ to 1.8V			7			7		μs
t_{OFF}	Turn Off Time	$V_{\text{SHDNx}} = 1.8\text{V}$ to 0.5V			1			1		μs
	Leakage of SHDN Pin	$V_{\text{SHDNx}} = 0\text{V}$	●		0.2	0.3		0.2	0.5	μA

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. Test conditions are $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = 0.5\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		C SUFFIX			H SUFFIX			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Offset Voltage (Note 5)	LTC6084MS8, LTC6085GN LTC6084DD, LTC6085DHC LTC6084MS8, LTC6085GN LTC6084DD, LTC6085DHC	● ●		300 300	750 1100 900 1350		300 300	750 1100 1100 1600	μV μV μV μV
$\Delta V_{\text{OS}}/\Delta T$	Input Offset Voltage Drift (Note 6)		●		2	5		2	5	$\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current (Notes 5, 7)		●		1	40		1	750	pA pA
I_{OS}	Input Offset Current (Notes 5, 7)		●		0.5	30		0.5	150	pA pA
e_n	Input Noise Voltage Density	$f = 1\text{kHz}$ $f = 10\text{kHz}$			31 27			31 27		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$
	Input Noise Voltage	0.1Hz to 10Hz			3			3		$\mu\text{V}_{\text{P-P}}$
i_n	Input Noise Current Density (Note 8)				0.56			0.56		$\text{fA}/\sqrt{\text{Hz}}$
	Input Common Mode Range		●	V^-		V^+	V^-		V^+	V
C_{IN}	Input Capacitance Differential Mode Common Mode	$f = 100\text{kHz}$			5 9			5 9		pF pF

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. Test conditions are $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = 0.5\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		C SUFFIX			H SUFFIX			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
CMRR	Common Mode Rejection Ratio	$0 \leq V_{\text{CM}} \leq 5\text{V}$	●	70 68	84		70 66	84		dB dB
PSRR	Power Supply Rejection Ratio	$V_S = 2.5\text{V}$ to 5.5V	●	94 91	115		94 89	115		dB dB
V_{OUT}	Output Voltage, High, (Referred to V^+)	No Load	●		0.5	5		0.5	10	mV
		$I_{\text{SOURCE}} = 1\text{mA}$	●		39	85		39	100	mV
		$I_{\text{SOURCE}} = 5\text{mA}$	●		220	460		220		mV
	Output Voltage, Low, (Referred to V^-)	No Load	●		0.5	5		0.5	10	mV
		$I_{\text{SINK}} = 1\text{mA}$	●		36	85		36	100	mV
		$I_{\text{SINK}} = 5\text{mA}$	●		200	460		200		mV
A_{VOL}	Large-Signal Voltage Gain	$R_{\text{LOAD}} = 10\text{k}\Omega$, $0.5\text{V} \leq V_{\text{OUT}} \leq 4.5\text{V}$	●	1000 400	5000		1000 300	5000		V/mV V/mV
I_{SC}	Output Short-Circuit Current	Source and Sink	●	7.7 6	12.5		7.7 4.5	12.5		mA mA
SR	Slew Rate	$A_V = 1$			0.5			0.5		V/ μs
GBW	Gain Bandwidth Product ($f_{\text{TEST}} = 10\text{kHz}$)	$R_{\text{LOAD}} = 50\text{k}\Omega$, $V_{\text{CM}} = 2.5\text{V}$	●	0.9 0.7	1.5		0.9 0.6	1.5		MHz
Φ_0	Phase Margin	$R_L = 10\text{k}\Omega$, $C_L = 150\text{pF}$, $A_V = 1$			45			45		Deg
t_S	Settling Time 0.1%	$V_{\text{STEP}} = 1\text{V}$, $A_V = 1$			5			5		μs
I_S	Supply Current (Per Amplifier)	No Load	●		110	130 140		110	130 145	μA μA
	Shutdown Current (Per Amplifier)	Shutdown, $V_{\text{SHDNx}} \leq 1.2\text{V}$	●		1.1	1.8		1.1	2	μA
V_S	Supply Voltage Range	Guaranteed by the PSRR Test	●	2.5		5.5	2.5		5.5	V
	Channel Separation	$f_S = 10\text{kHz}$			-120			-120		dB
	Shutdown Logic	$\overline{\text{SHDNx}}$ High $\overline{\text{SHDNx}}$ Low		3.5		1.2	3.5		1.2	V V
t_{ON}	Turn On Time	$V_{\text{SHDNx}} = 1.2\text{V}$ to 3.5V			7			7		μs
t_{OFF}	Turn Off Time	$V_{\text{SHDNx}} = 3.5\text{V}$ to 1.2V			1			1		μs
	Leakage of $\overline{\text{SHDN}}$ Pin	$V_{\text{SHDNx}} = 0\text{V}$	●		0.5	0.9		0.5	1.2	μA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and the total output current.

Note 3: The LTC6084C/LTC6085C are guaranteed functional over the operating temperature range of -40°C to 85°C . The LTC6084H/LTC6085H are guaranteed functional over the operating temperature range of -40°C to 125°C .

Note 4: The LTC6084C/LTC6085C are guaranteed to meet specified performance from 0°C to 70°C . The LTC6084C/LTC6085C are designed, characterized and expected to meet specified performance from -40°C to 85°C but are not tested or QA sampled at these temperatures. The LTC6084H/LTC6085H are guaranteed to meet specified performance from -40°C to 125°C .

Note 5: ESD (Electrostatic Discharge) sensitive device. ESD protection devices are used extensively internal to the LTC6084/LTC6085; however, high electrostatic discharge can damage or degrade the device. Use proper ESD handling precautions.

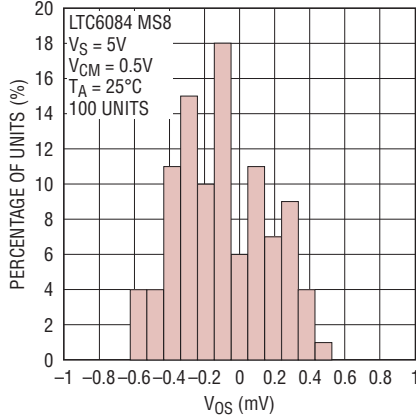
Note 6: This parameter is not 100% tested.

Note 7: This specification is limited by high speed automated test capability. See Typical Performance Characteristic curves for actual performance.

Note 8: Current noise is calculated from $i_n = \sqrt{2qI_B}$, where $q = 1.6 \cdot 10^{-19}$ coulombs.

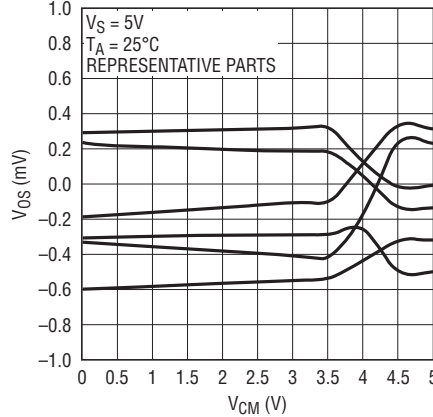
TYPICAL PERFORMANCE CHARACTERISTICS

V_{OS} Distribution



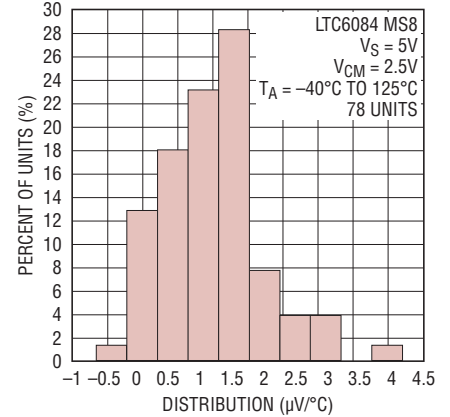
60845 G01

V_{OS} vs V_{CM}



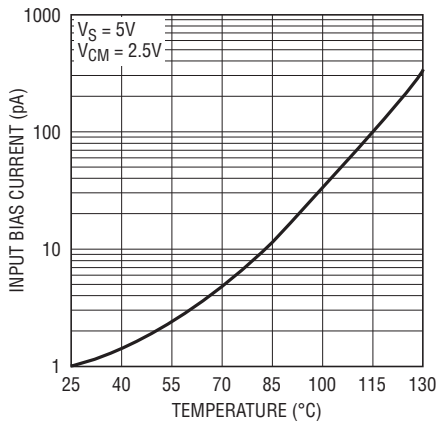
60845 G02

V_{OS} Drift Distribution



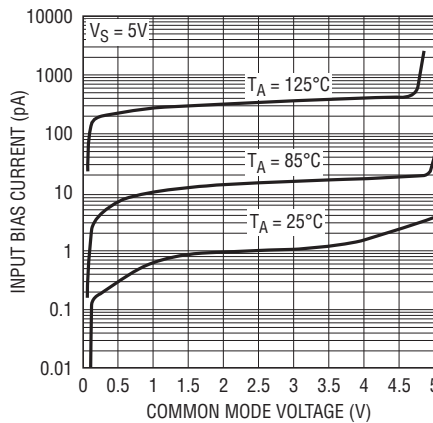
60845 G03

Input Bias vs Temperature



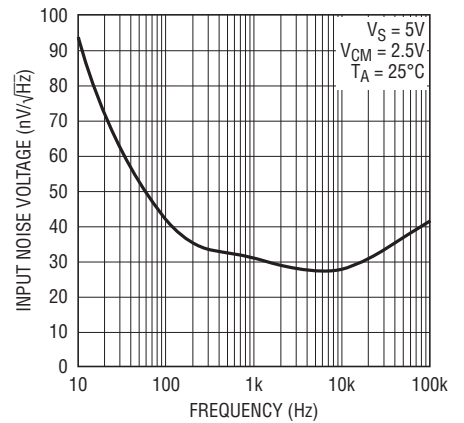
60845 G04

Input Bias Current vs Common Mode Voltage



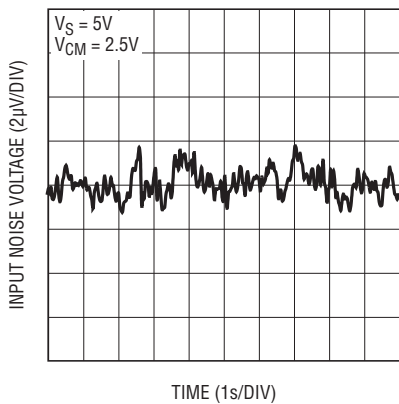
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Input Noise Voltage vs Frequency



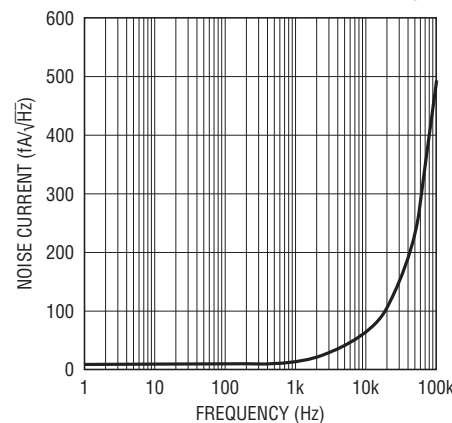
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0.1Hz to 10Hz Output Voltage Noise



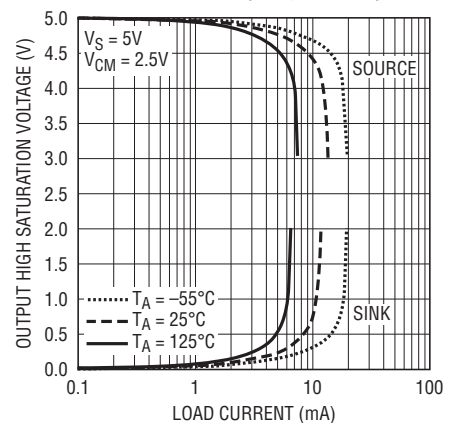
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Input Noise Current vs Frequency



60845 G08

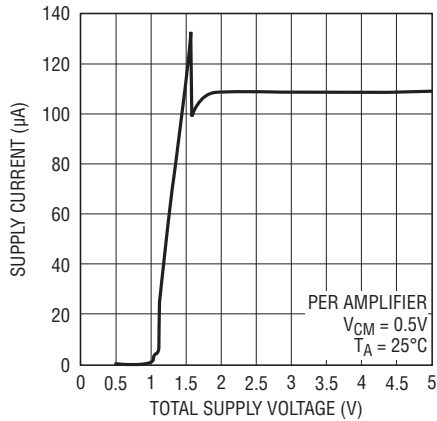
Output Saturation Voltage vs Load Current (Output High)



60845 G09

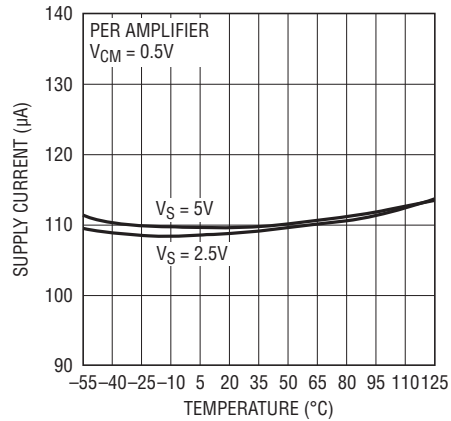
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage



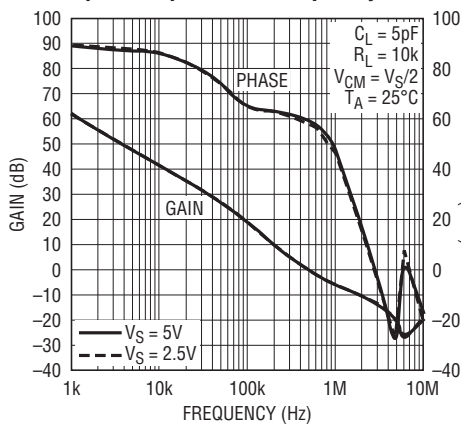
60845 G10

Supply Current vs Temperature



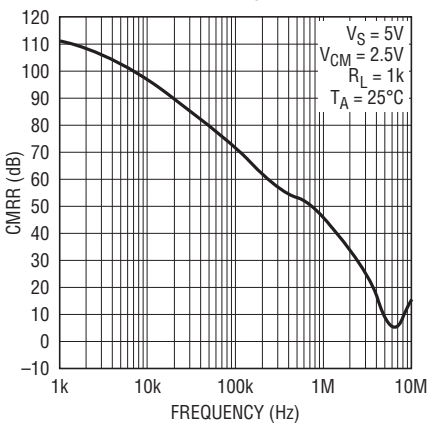
60845 G11

Open-Loop Gain vs Frequency



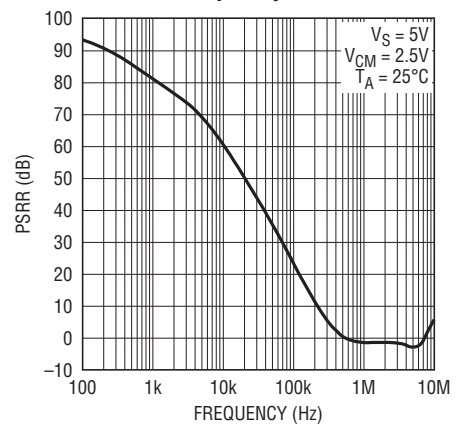
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CMRR vs Frequency



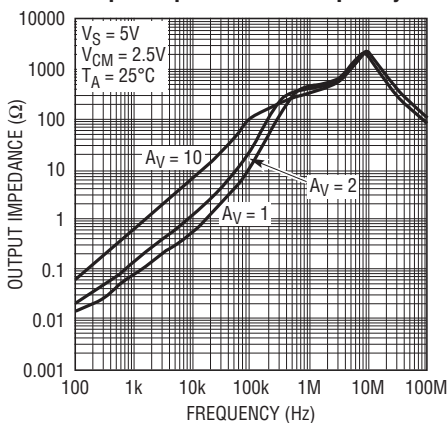
60845 G13

PSRR vs Frequency



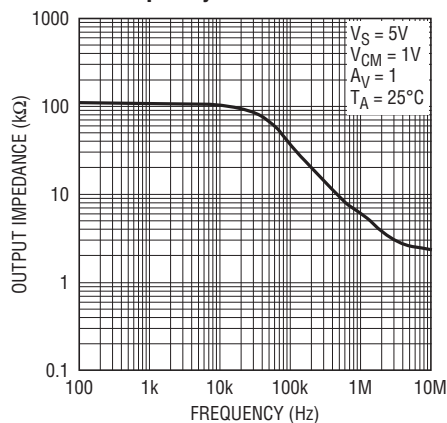
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Output Impedance vs Frequency



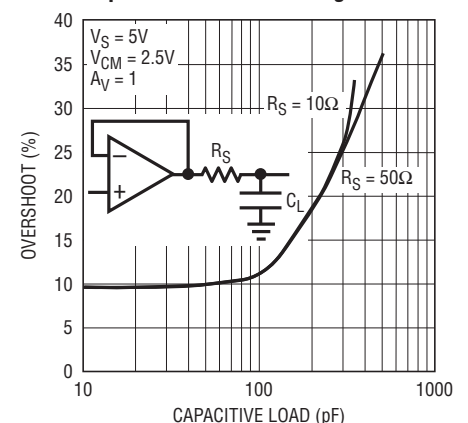
60845 G15

Disabled Output Impedance vs Frequency



60845 G16

Capacitive Load Handling

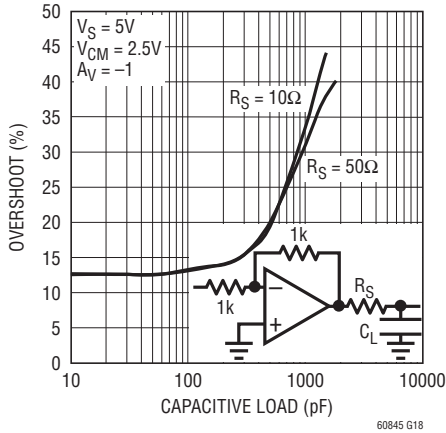


60845 G17

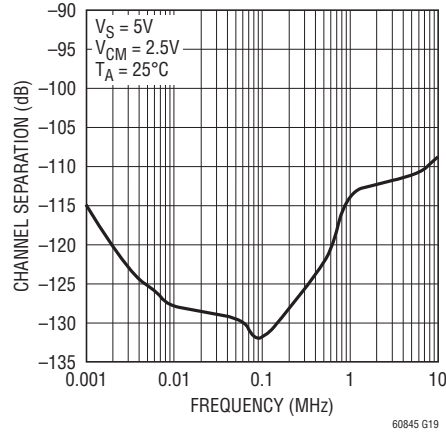
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TYPICAL PERFORMANCE CHARACTERISTICS

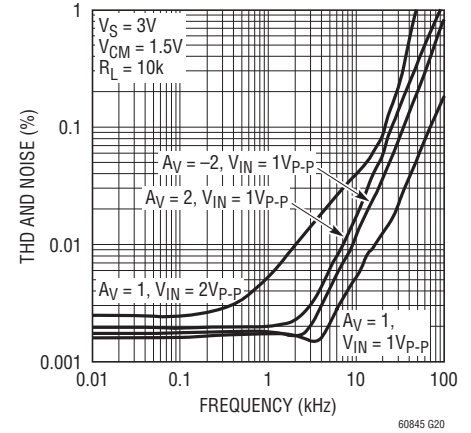
Capacitive Load Handling



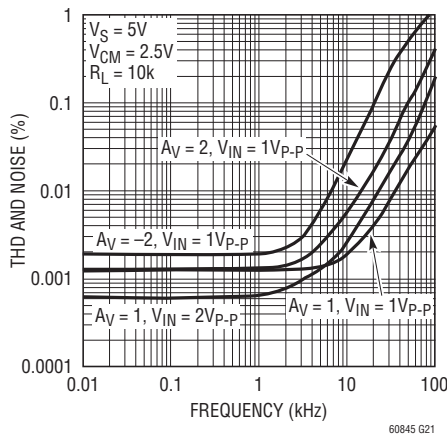
Channel Separation vs Frequency



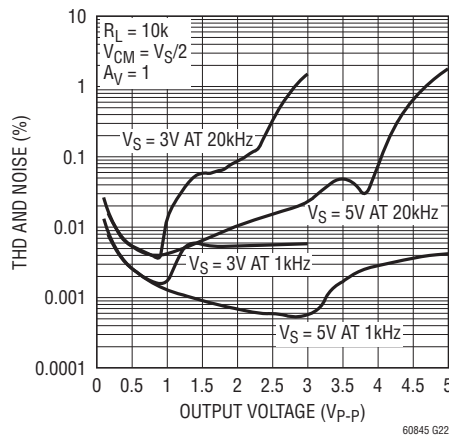
Total Harmonic Distortion and Noise vs Frequency



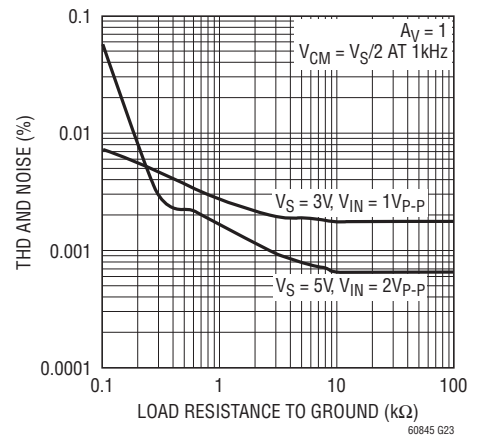
Total Harmonic Distortion and Noise vs Frequency



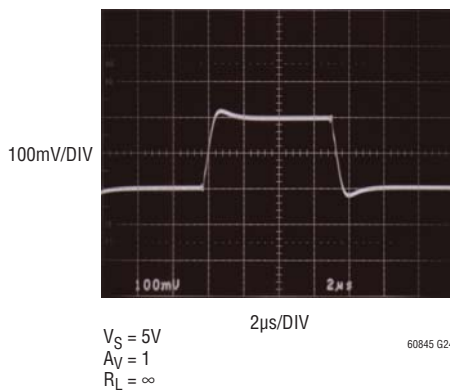
Total Harmonic Distortion and Noise vs Output Voltage



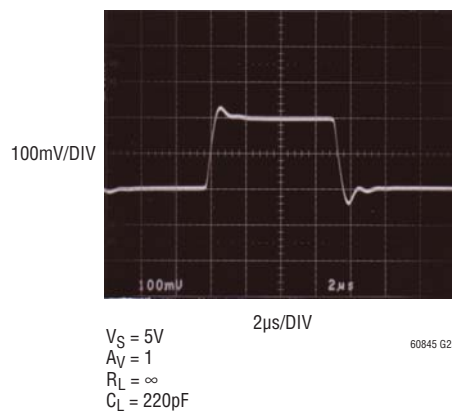
Total Harmonic Distortion and Noise vs Load Resistance



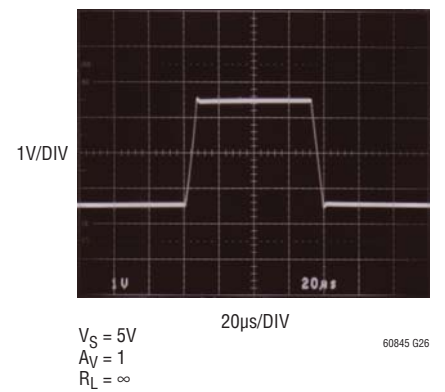
Small Signal Response



Small Signal Response

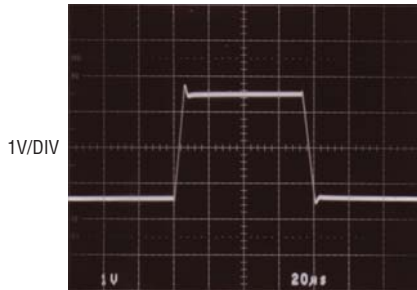


Large Signal Response



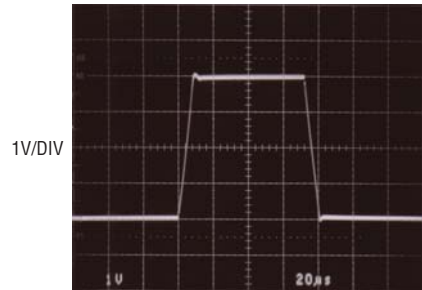
TYPICAL PERFORMANCE CHARACTERISTICS

Large Signal Response



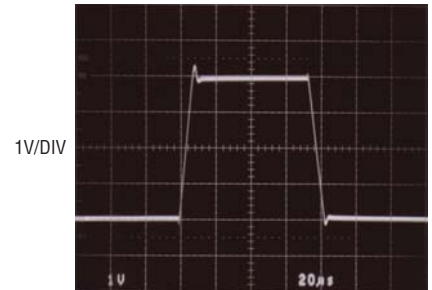
$V_S = 5V$
 $A_V = -1$
 $R_L = 1k$
 60845 G27

Large Signal Response



$V_S = 5V$
 $A_V = 1$
 $R_L = \infty$
 60845 G28

Large Signal Response



$V_S = 5V$
 $A_V = -1$
 $R_L = 1k$
 60845 G29

PIN FUNCTIONS

OUT: Amplifier Output.

-IN: Inverting Input.

+IN: Noninverting Input.

V⁺: Positive Supply.

V⁻: Negative Supply.

SHDNA: Shutdown Pin of Amplifier A, active low and only available with the LTC6084DD. An internal current source pulls the pin to V⁺ when floating.

SHDNB: Shutdown Pin of Amplifier B, active low and only available with the LTC6084DD. An internal current source pulls the pin to V⁺ when floating.

NC: Not Internally Connected.

Exposed Pad: Connected to V⁻.

APPLICATIONS INFORMATION

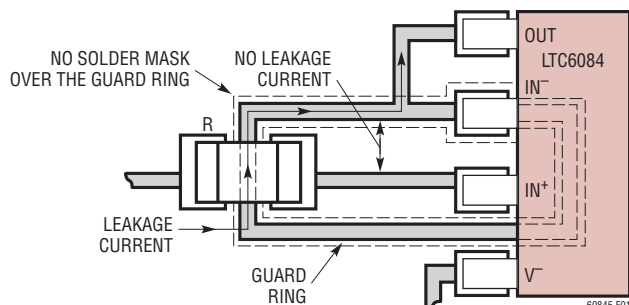


Figure 1. Sample Layout. Unity-Gain Configuration. Using Guard Ring to Shield High Impedance Input from Board Leakage

Rail-to-Rail Input

The input stage of LTC6084/LTC6085 combines both PMOS and NMOS differential pairs, extending its input common mode voltage to both positive and negative supply voltages. At high input common mode range, NMOS pair is on. At low common mode range, the PMOS pair is on. The transition happens when the common voltage is between 1.3 and 0.9V below the positive supply.

Achieving Low Input Bias Current

The DD and DHC packages are leadless and make contact to the PCB beneath the package. Solder flux used during the attachment of the part to the PCB can create leakage current paths and can degrade the input bias current performance of the part. All inputs are susceptible because the backside paddle is connected to V^- internally. As the input voltage or V^- changes, a leakage path can be formed and alter the observed input bias current. For lowest bias current use the LTC6084/LTC6085 in the leaded MSOP/GN package. With fine PCB design rules, you can also provide a guard ring around the inputs.

For example, in high source impedance applications such as pH probes, photo diodes, strain gauges, etc., the low input bias current of these parts requires a clean board layout to minimize additional leakage current into a high impedance signal node. A mere 100G Ω of PC board resistance between a 5V supply trace and input trace near ground potential adds 50pA of leakage current. This leakage is far greater

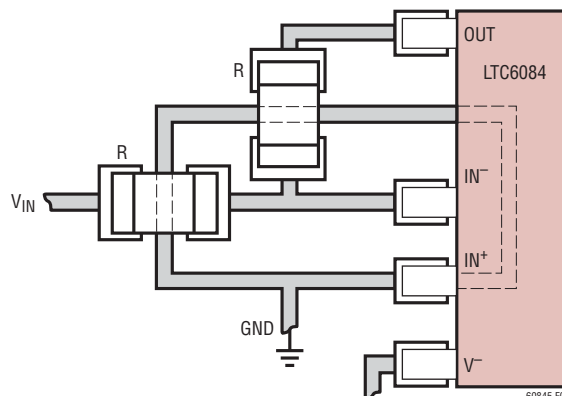


Figure 2. Sample Layout. Inverting Gain Configuration. Using Guard Ring to Shield High Impedance Input from Board Leakage

than the bias current of the operational amplifier. A guard ring around the high impedance input traces driven by a low impedance source equal to the input voltage prevents such leakage problems. The guard ring should extend as far as necessary to shield the high impedance signal from any and all leakage paths. Figure 1 shows the use of a guard ring in a unity-gain configuration. In this case the guard ring is connected to the output and is shielding the high impedance noninverting input from V^- . Figure 2 shows the inverting gain configuration.

Rail-to-Rail Output

The output stage of the LTC6084/LTC6085 swings within 5mV of the supply rails when driving high impedance loads, in other words when no DC load current is present. See the Typical Performance Characteristics for curves of output swing versus load current. The class AB design of the output stage enables the op amp to supply load currents which are much greater than the quiescent supply current. For example, the room temperature short-circuit current is typically 12.5mA.

Capacitive Load

LTC6084/LTC6085 can drive a capacitive load up to 300pF in unity gain. The capacitive load driving capability increases as the amplifier is used in higher gain configurations. A small series resistance between the output and the load further increases the amount of capacitance the amplifier can drive.

APPLICATIONS INFORMATION

SHDN Pins

Pins 5 and 6 are used for power shutdown of the LTC6084 in the DD package. If they are floating, internal current sources pull pins 5 and 6 to V^+ and the amplifiers operate normally. In shutdown the amplifier output is high impedance, and each amplifier draws less than $1\mu\text{A}$ current. This feature allows the part to be used in muxed output applications as shown in Figure 3.

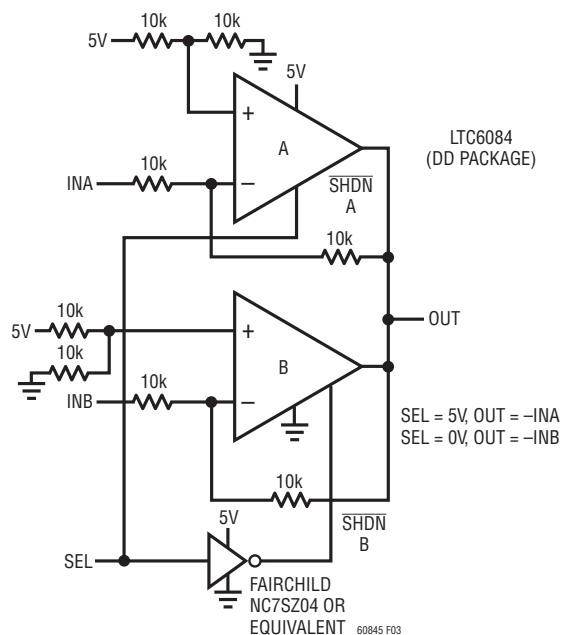


Figure 3. Inverting Amplifier with Muxed Output

ESD

The LTC6084/LTC6085 has reverse-biased ESD protection diodes on all inputs and outputs as shown in the Simplified Schematic. If these pins are forced beyond either supply, unlimited current will flow through these diodes. If the current is transient and limited to 100mA or less, no damage to the device will occur.

The amplifier input bias current is the leakage current of these ESD diodes. This leakage is a function of the temperature and common mode voltage of the amplifier, as shown in the Typical Performance Characteristics.

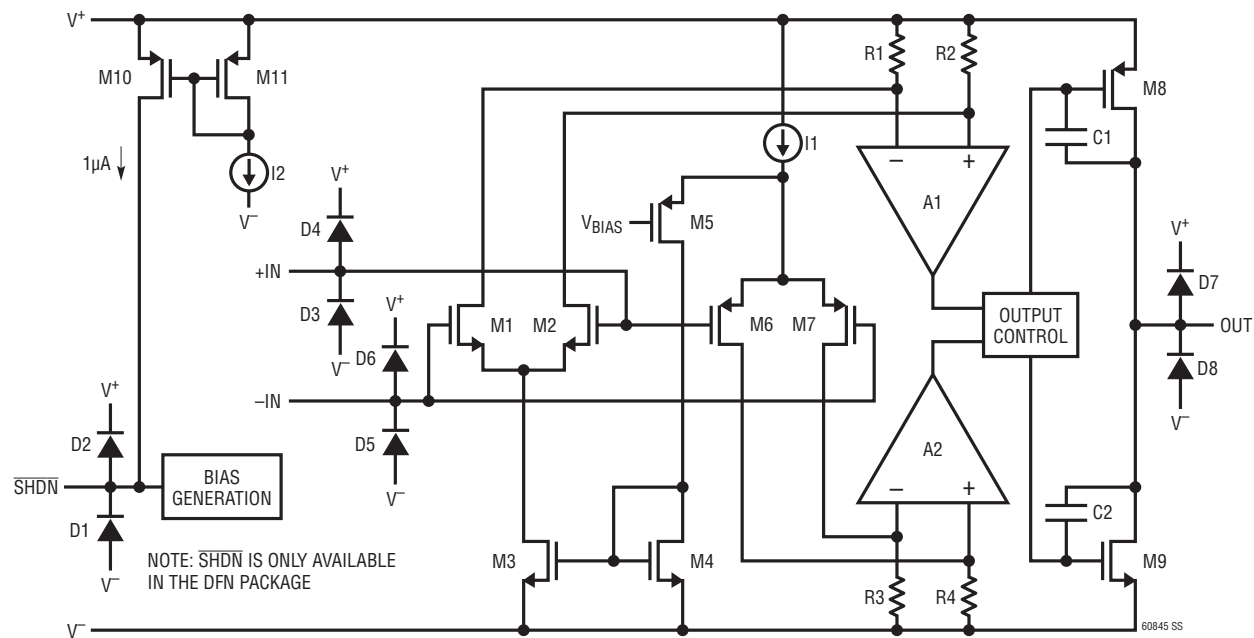
Noise

In the frequency region above 1kHz, the LTC6084/LTC6085 shows good noise voltage performance. In this region, noise can be dominated by the total source resistance of the particular application. Specifically, these amplifiers exhibit the noise of a 58k resistor, meaning it is desirable to keep the source and feedback resistance at or below this value, i.e., $R_S + R_G || R_{FB} \leq 58\text{k}$. Above this total source impedance, the noise voltage is dominated by the resistors.

At low frequency, noise current can be estimated from the expression $i_n = \sqrt{2qI_B}$, where $q = 1.6 \cdot 10^{-19}$ coulombs. Equating $\sqrt{4kTR\Delta f}$ and $R\sqrt{2qI_B\Delta f}$ shows that for a source resistor below $50\text{G}\Omega$ the amplifier noise is dominated by the source resistance. Noise current rises with frequency. See the curve Input Noise Current vs Frequency in the Typical Performance Characteristics section.

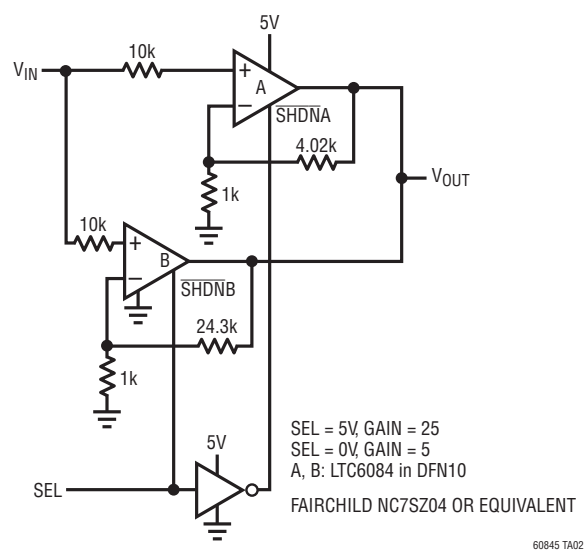
SIMPLIFIED SCHEMATIC

Simplified Schematic of the Amplifier



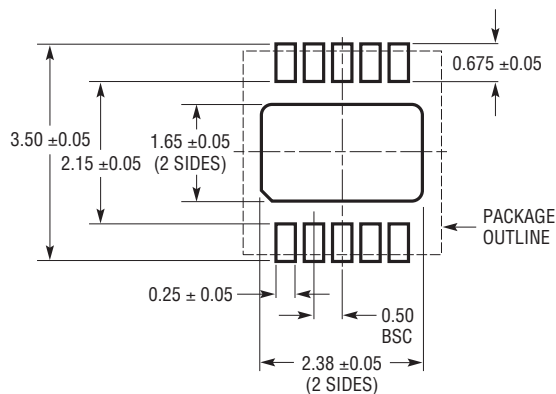
TYPICAL APPLICATIONS

Gain Selectable Amplifier

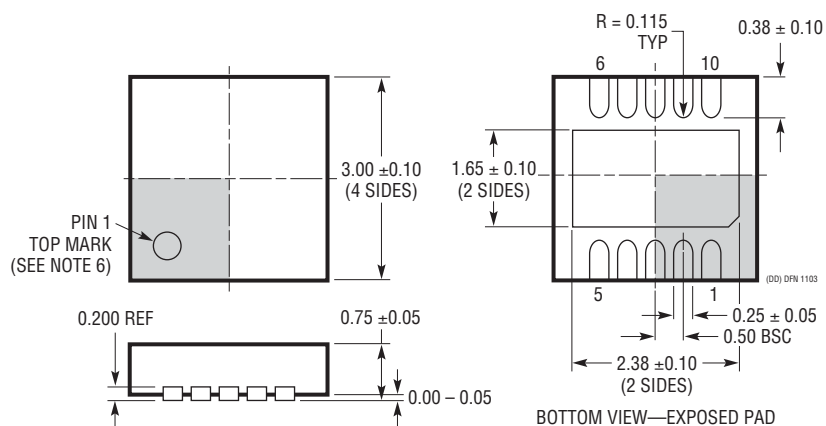


PACKAGE DESCRIPTION

DD Package 10-Lead Plastic DFN (3mm × 3mm) (Reference LTC DWG # 05-08-1699)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

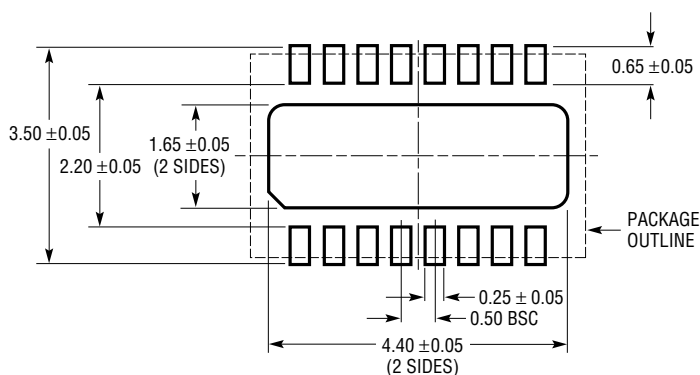


NOTE:

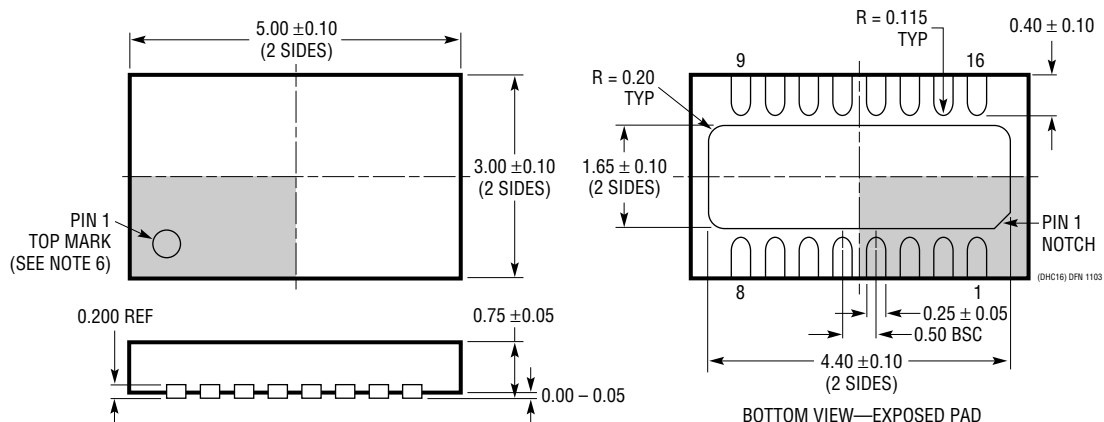
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

DHC Package 16-Lead Plastic DFN (5mm × 3mm) (Reference LTC DWG # 05-08-1706)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

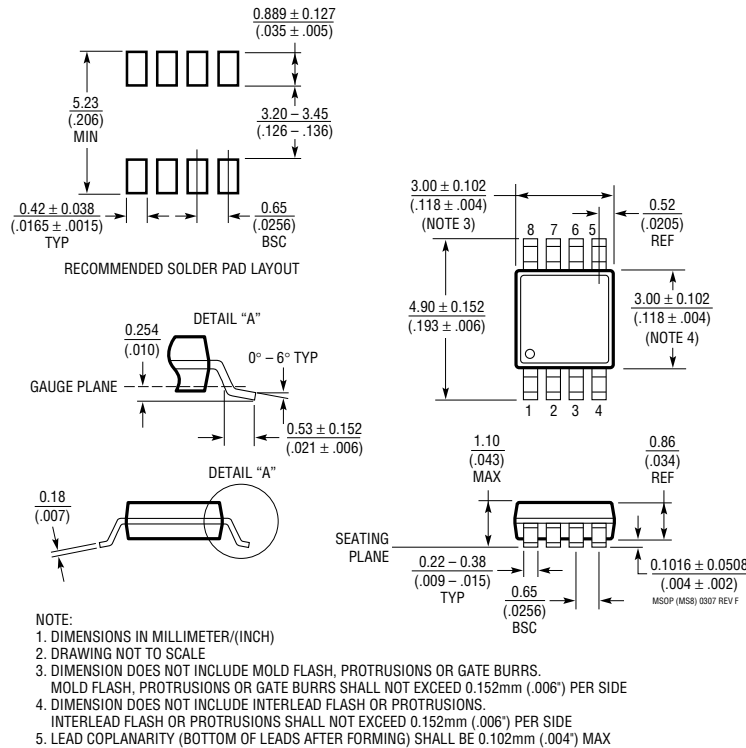


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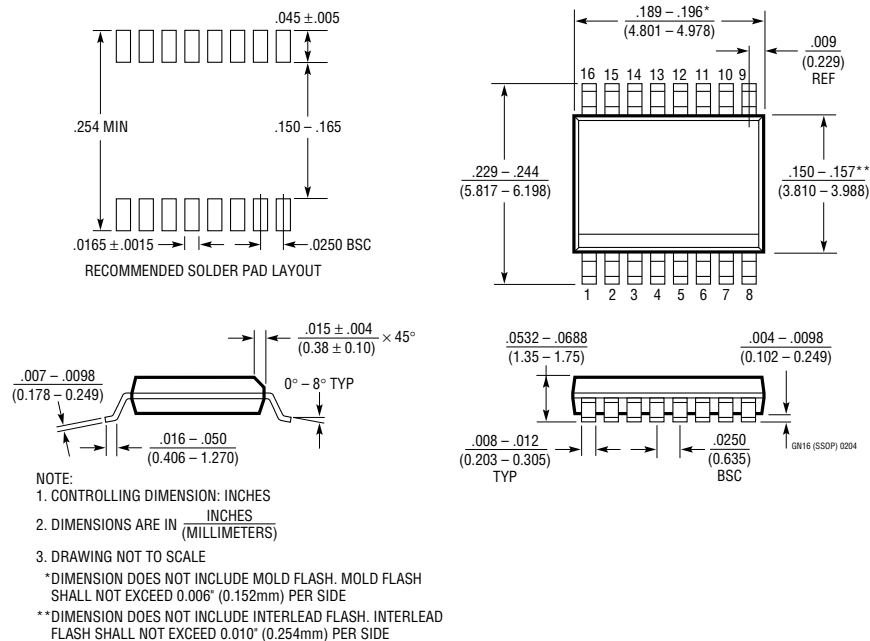
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2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

MS8 Package 8-Lead Plastic MSOP (Reference LTC DWG # 05-08-1660)



GN Package 16-Lead Plastic SSOP (Narrow .150 Inch) (Reference LTC DWG # 05-08-1641)



60845fa

Two circuit diagrams for a 100ns 10V CMOS differential-to-single-ended converter.

Left Diagram (Differential Pair): This circuit uses two LTC6084 op-amp halves. The input V_{IN} is connected to two 1MΩ resistors. The first half has its non-inverting input (+) connected to ground and its inverting input (-) connected to the first 1MΩ resistor. The second half has its inverting input (-) connected to ground and its non-inverting input (+) connected to the second 1MΩ resistor. Both op-amp halves have a feedback capacitor of 10pF and a feedback resistor of 2kΩ. The output of the first half is connected to a diode OC1 (cathode to ground, anode to output), and the output of the second half is connected to a diode OC2 (cathode to ground, anode to output). The outputs are labeled OC1 and OC2.

Right Diagram (Single Op-Amp): This circuit uses a single LTC6240HV op-amp. The input V_{IN} is connected to two 1MΩ resistors. The non-inverting input (+) is connected to the first 1MΩ resistor, and the inverting input (-) is connected to the second 1MΩ resistor. The op-amp is configured with a feedback capacitor of 3pF and a feedback resistor of 2kΩ. The output is connected to a diode OC1 (cathode to ground, anode to output) and a diode OC2 (cathode to output, anode to ground). The output is labeled $V_{OUT} = V_{IN}$.

Specifications:

- Bandwidth: $BW \approx 40\text{kHz}$
- Either polarity
- Large signal transition delay: $\approx 50\mu\text{s}$
- Small signal dead zone: $|V_{IN}| \leq 10\text{mV}$

$V_{OUT} = \pm 5V$,
RELATIVE TO GNDB

60845 TA03

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC6078/LTC6079	Dual/Quad Micropower Precision Rail-to-Rail Op Amps	25μV V _{OS(MAX)} , 0.7μV/°C V _{OS} Drift(MAX), 1pA I _{BIAS(MAX)}
LTC6081/LTC6082	Dual/Quad Precision Rail-to-Rail Input/Output Amps	70μV V _{OS(MAX)} , 0.8μV/°C V _{OS} Drift(MAX), 1pA I _{BIAS(MAX)}
LTC6087/LTC6088	Dual/Quad 14MHz Rail-to-Rail Input/Output Amps	750μV V _{OS(MAX)} , 5μV/°C V _{OS} Drift(MAX), 1pA I _{BIAS}
LTC6240/LTC6241/ LTC6242	Single/Dual/Quad Low Noise Rail-to-Rail Output Op Amps	7nV/√Hz Noise, 0.2pA I _{BIAS} , 18MHz Gain Bandwidth
LTC6244	Dual Low Noise Rail-to-Rail Output Op Amps	8nV/√Hz Noise, 1pA I _{BIAS} , 50MHz Gain Bandwidth