

Octal Line Driver

FEATURES

- Eight Single Ended Line Drivers in One Package
- Meets EIA Standards EIA232E/V.28, EIA423A and CCITT V.10/X.26
- Single External Resistor Controls Slew Rate
- Wide Supply Voltage Range
- Tri-State Outputs
- Output Short-Circuit Protection

DESCRIPTION

The UC5170C is a single-ended octal line driver designed to meet both standard modem control applications (EIA232E/V.28), and long line drive applications (EIA423A/V.10/X.26). The slew rate for all eight drivers is controlled by a single external resistor. The slew rate and output levels in Low Mode are independent of the power variations.

Mode selection is easily accomplished by taking the select pins (Ms+ and Ms-) to ground for low output mode (EIA232E/V.28 and EIA423A/V.10) or to their respective supplies for high mode (EIA232E/V.28). High mode should only be used to drive adapters that take power from the control lines, or applications using high threshold receivers.

ABSOLUTE MAXIMUM RATINGS (Note 1)

V+ (Pin 20)	15V
V- (Pin 11)	-15V
PLCC Power Dissipation, TA = 25°C (Note 2)	1000 mW
DIP Power Dissipation, TA = 25°C (Note 2)	1250 mW
Input Voltage	-1.5 to +7V
Output Voltage	-12V to +12V
Slew Rate Resistor	2k to 10kΩ
Storage Temperature	-65°C to +150°C

Note 1: All voltages are with respect to ground, pin 18.

Note 2: Consult Packaging Section of Databook for thermal limitations and considerations of packages.

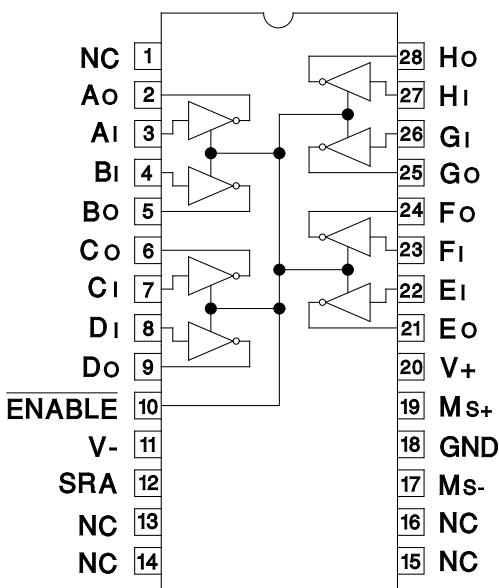
FUNCTIONAL TABLE

INPUTS		OUTPUTS	
EN	DATA	HIGH	LOW
		EIA-232E ⁽²⁾	EIA423A+EIA232E
0	0	(V+)-3V	5V to 6V
0	1	(V-)-3V	-5V to -6V
1	X	High Z	High Z

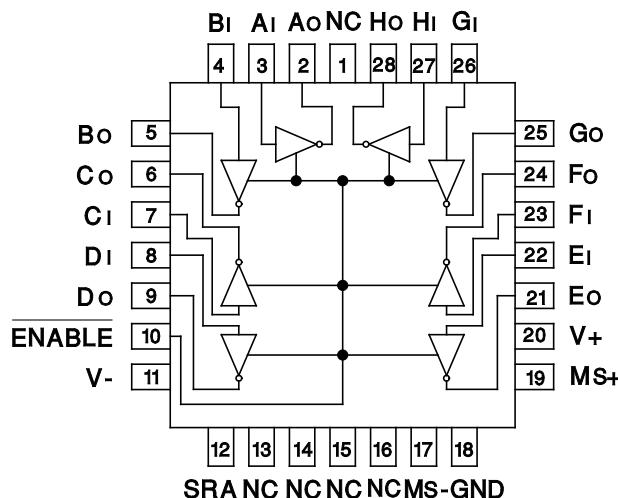
Note 2: Minimum output swings.

CONNECTION DIAGRAMS

N PACKAGE (TOP VIEW)



Q PACKAGE (TOP VIEW)



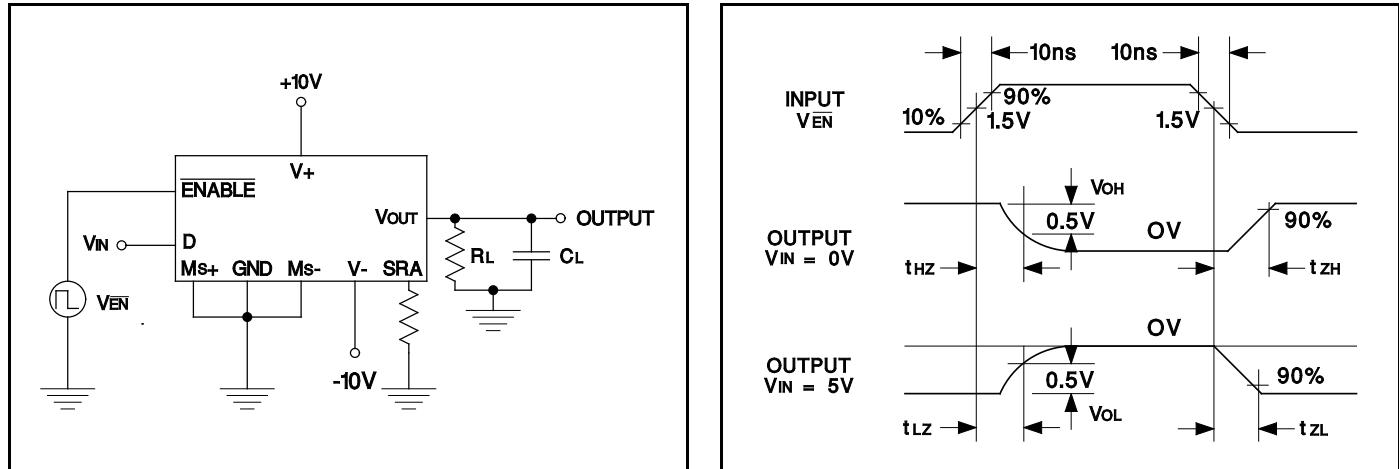
DC ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications hold for $|V_+| = |V_-| = 10V$, $0 < T_A < +70^\circ C$, $Ms+ = Ms- = 0V$, $RSRA = +10k$, $T_A = T_J$.

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS						
V+ Range			9		15	V
V- Range			-9		-15	V
V+ Supply Current	I+	RL = Infinite $\bar{En} = 0V$		25	42	mA
V- Supply Current	I-	RL = Infinite $\bar{En} = 0V$		-23	-42	mA
INPUTS						
High Level Input Voltage	VIH		2.0			V
Low Level Input Voltage	VIL				0.8	V
Input Clamp Voltage	VIK	$I_I = -15 \text{ mA}$		-1.1	-1.8	V
High Level Input Current	IIH	$VIH = 2.4V$		0.25	40	μA
Low Level Input Current	IIL	$VIL = 0.4V$	-200	-8.0		μA
OUTPUTS						
High Level (Low Mode) Output Voltage (EIA423A/V.10, EIA232E/V.28)	VOH	$V_{IN} = 0.8V \quad RL = \text{Inf.}$	5.0	5.3	6.0	V
		$\bar{En} = 0.8V \quad RL = 3k$	5.0	5.3	6.0	V
		$RL = 450$	4.5	5.2	6.0	V
Low Level (Low Mode) Output Voltage (EIA423A/V.10, EIA232E/V.28)	VOL	$V_{IN} = 2.0V \quad RL = \text{Inf.}$	-5.0	-5.3	-6.0	V
		$\bar{En} = 0.8V \quad RL = 3k$	-5.0	-5.3	-6.0	V
		$RL = 450$	-4.5	-5.2	-6.0	V
Output Balance (EIA423A/V.10)	VBAL	$RL = 450 \quad VOH - VOL = V_{BAL}$		0.2	0.4	V
High Level (High Mode) Output Voltage (EIA232E/V.28)	VOH	$V_{IN} = 0.8V \quad RL = \text{Inf.}, Ms+ = V_+, Ms- = V_-$	7.0	7.6	10	V
		$\bar{En} = 0.8V \quad RL = 3k, Ms+ = V_+, Ms- = V_-$	7.0	7.6	10	V
Low Level (High Mode) Output Voltage (EIA232E, V.28)	VOL	$V_{IN} = 2.0V \quad RL = \text{Inf.}, Ms+ = V_+, Ms- = V_-$	-7.0	-7.7	-10	V
		$\bar{En} = 0.8V \quad RL = 3k, Ms+ = V_+, Ms- = V_-$	-7.0	-7.7	-10	V
Off-State Output Current	IOZ	$\bar{En} = 2.0V, VO = \pm 6V, V_+ = 15V, V_- = -15V$	-100		100	μA
Short-Circuit Current	IOS	$V_{IN} = 0V, \bar{En} = 0V$	-25	-50		mA
		$V_{IN} = 5V, \bar{En} = 0V$	25	40		mA

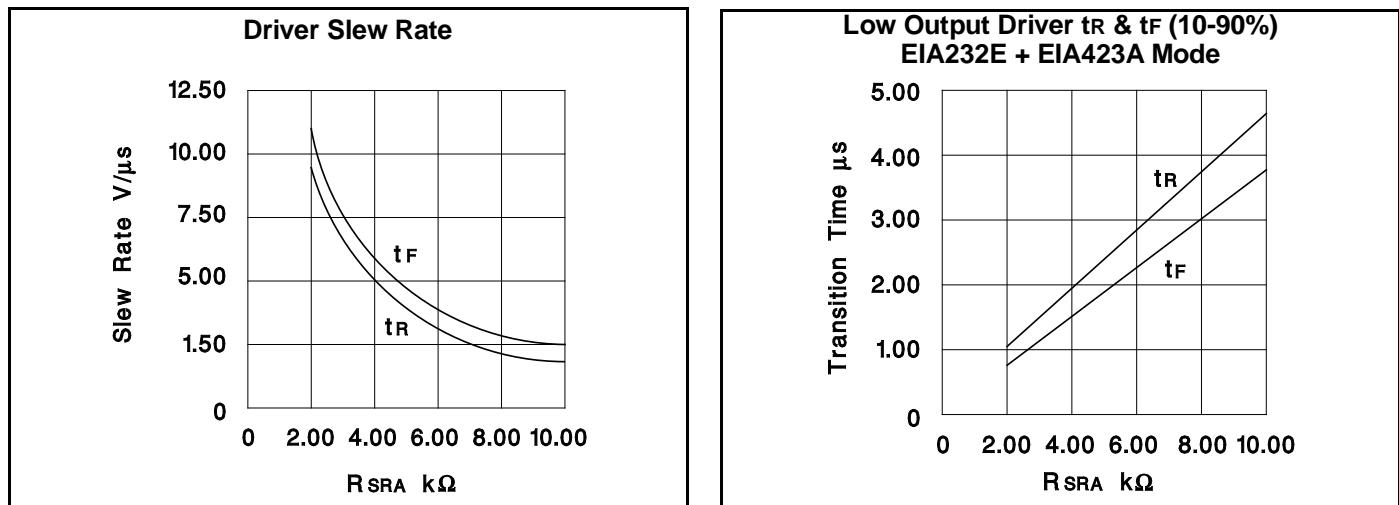
AC ELECTRICAL CHARACTERISTICS: $at |V_+| = |V_-| = 10V, 0 < T_A < +70^\circ C, Ms+ = Ms- = 0V, T_A = T_J$.

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Slew Rate	tR	$RSRA = 2k$	6.65	9.5	12.3	$V/\mu\text{s}$
	tF	$RL = 450, CL = 50\text{pF}$	6.65	10	12.3	$V/\mu\text{s}$
Output Slew Rate	tR	$RSRA = 10k$	1.33	1.9	2.45	$V/\mu\text{s}$
	tF	$RL = 450, CL = 50\text{pF}$	1.33	2.2	2.45	$V/\mu\text{s}$
Propagation Output to High Impedance	tHz	$RSRA = 10k$		0.3	1.0	μs
	tLz	$RL = 450, CL = 50\text{pF}$		0.5	2.0	μs
Propagation High Impedance to Output	tzH	$RSRA = 10k$		6.0	17	μs
	tzL	$RL = 450, CL = 50\text{pF}$		7.0	17	μs

AC PARAMETER TEST CIRCUIT AND WAVEFORMS



AC CHARACTERISTICS



APPLICATION INFORMATION

Slew Rate Programming

Slew rate for the UC5170C is set up by a single external resistor connected between the SRA pin and ground. Slew rate adjustments can be approximated by using the following formula:

$$V/\mu\text{s} = \frac{20}{R_{SRA}} \text{ (} R_{SRA} \text{ in } k\Omega \text{)}$$

The slew rate resistor can vary between 2k and 10k which allows slew rates between 10 to 2.2V/μs, respectively. The relationship between slew rate and RSRA is shown in the typical characteristics.

Waveshaping of the output lets the user control the level of interference (near-end crosstalk) that may be coupled to adjacent circuits in an interconnection. The recommended output characteristics for cable length and data rates can be found in EIA standard EIA423A +V.10. Approximations of these standards are given by the following equations:

Max. Data Rate = $300/t$ (For data rates 1k to 100k bit/s)

Max. Cable Length (feet) = $100 \times t$ (Max. length 4000 feet)

where t is the transition time from 10% to 90% of the output swing in microseconds. For data rates below 1k bit/s t may be up to 300 microseconds.

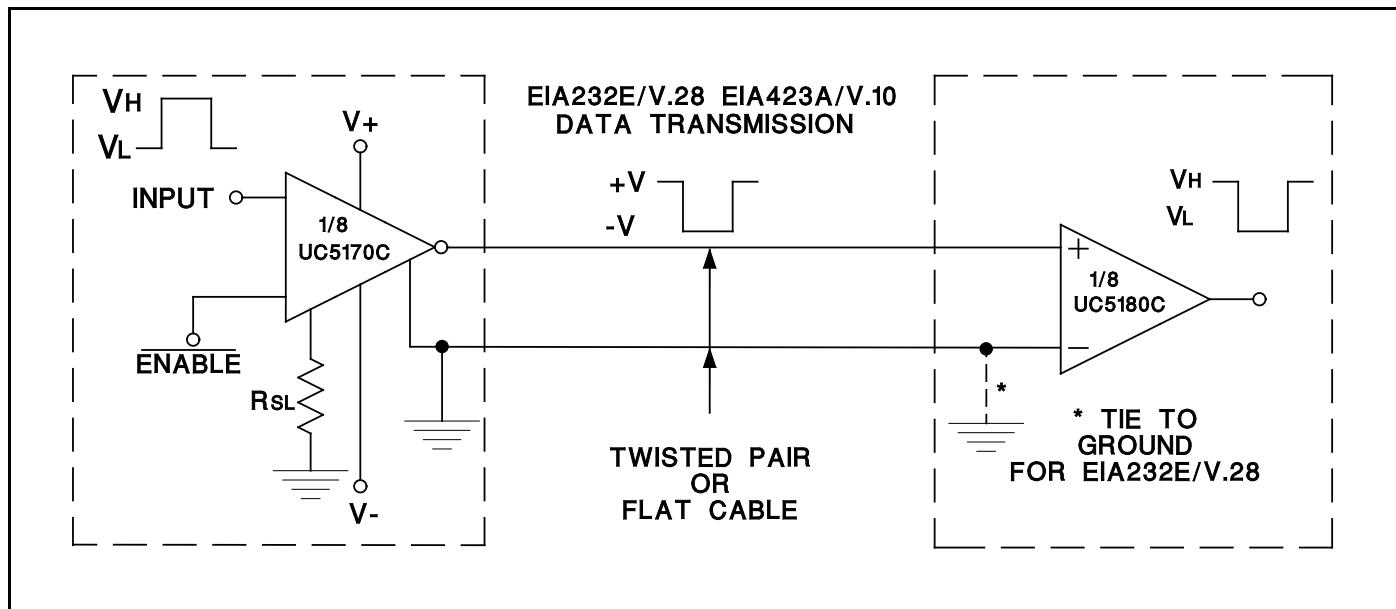
Output Voltage Programming

The UC5170C has two programmable output modes, either a low voltage mode which meets EIA423A, EIA232E/V.28/V.10 specifications, or the high output mode which meets the EIA232E, V.28 specifications.

The high output mode provides greater output swings, minimum of 3V below and supply rails for driving higher, attenuated lines. This mode is selected by connecting the mode select pins to their respected supplies, Ms+ to V+ and Ms- to V-.

The low output mode provides a controlled output swing and is accomplished by connecting both mode select pins to ground.

APPLICATIONS



SPECIFIC LAYOUT NOTES

The UC5170C layout must have bulk bypassing close to the device. Peak slew current is greater than 500mA when all eight drivers slew at once in the same direction. Some applications mount the UC5170C on a bulkhead or isolated plane for RFI/FCC/VDE reasons. If bulk bypassing is not used, the -10V supply may go above -8.5 volts, causing the slew rate control circuit to become unstable.

The UC5170C can have output oscillation at 100kHz if the +10V supply is applied before the -10V supply. This has been a problem in some terminal designs where the +10V was developed from the flyback, which can result in a 500ms difference in the application of the supplies at power up.

GENERAL LAYOUT NOTES

The drivers and receivers should be mounted close to the system common ground point, with the ground reference tied to the common point to reduce RFI/EMI.

Filter connectors or transzorbs should be used to reduce the RFI/EMI, protecting the system from static (ESD), and electrical overstress (EOS). A filter connector or capacitor will reduce the ESD pulse by 90% typically. A cable dragged across a carpet and connected to a system can easily be charged to over 25,000 volts. This is a metal to metal contact when the cable is connected to the system (no resistance), currents exceed 80 amps with less than a nanosecond rise time. A transzorb provides two functions, the device capacitance inherently acts as a filter capacitor, and the device clamps the ESD and EOS pulses which would pass through the capacitor and destroy the devices. The recommended transzorb for the UC5170C is P6KEIOCA.

*Transzorb is a trademark of General Semiconductor Industries.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC5170CJ	OBsolete	CDIP	J	28		TBD	Call TI	Call TI			
UC5170CN	OBsolete		UTR			TBD	Call TI	Call TI			
UC5170CQ	OBsolete	PLCC	FN	28		TBD	Call TI	Call TI		UC5170CQ	
UC5170CQTR	OBsolete	PLCC	FN	28		TBD	Call TI	Call TI		UC5170CQ	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM

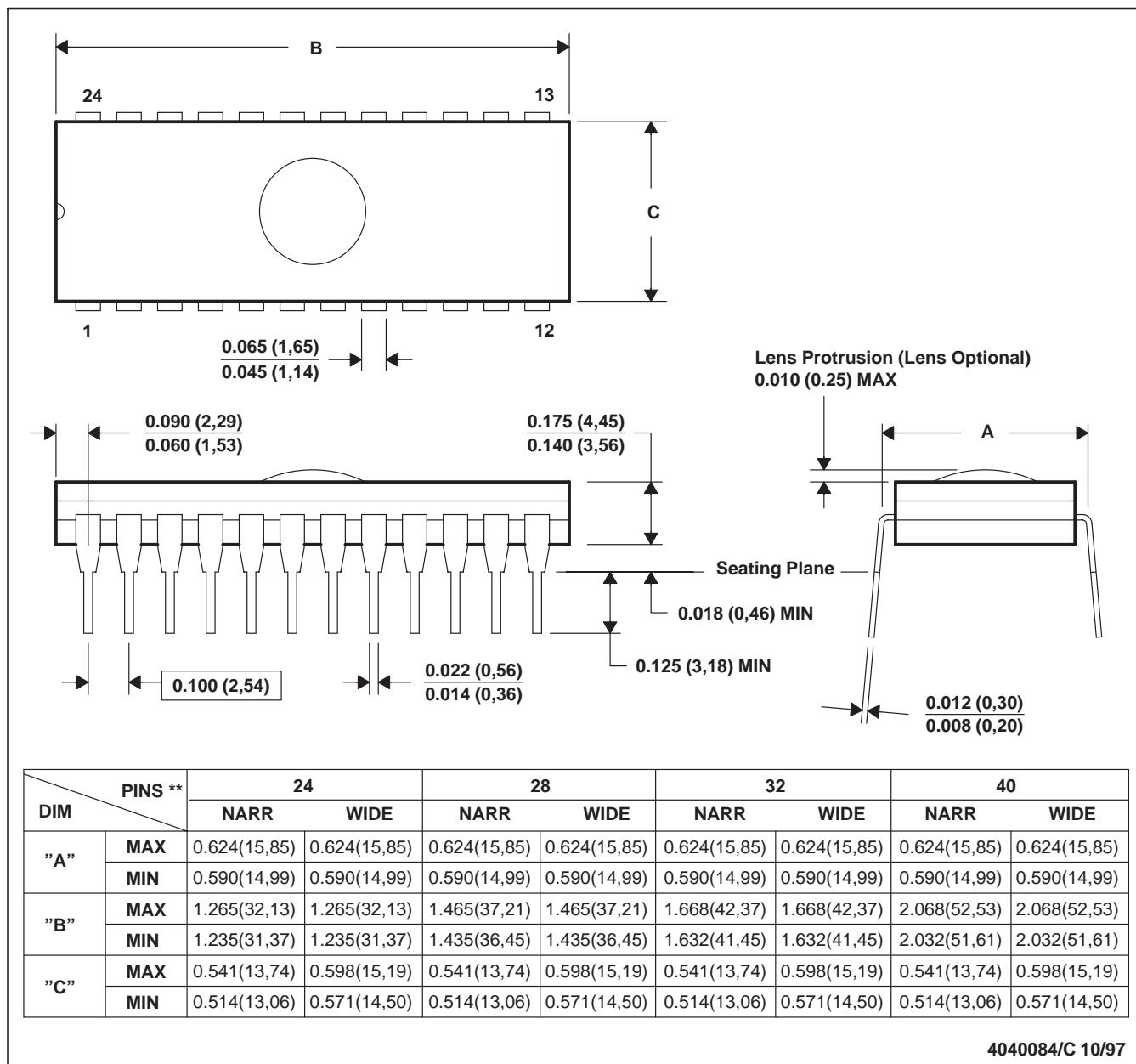
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J (R-GDIP-T**)

CERAMIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN

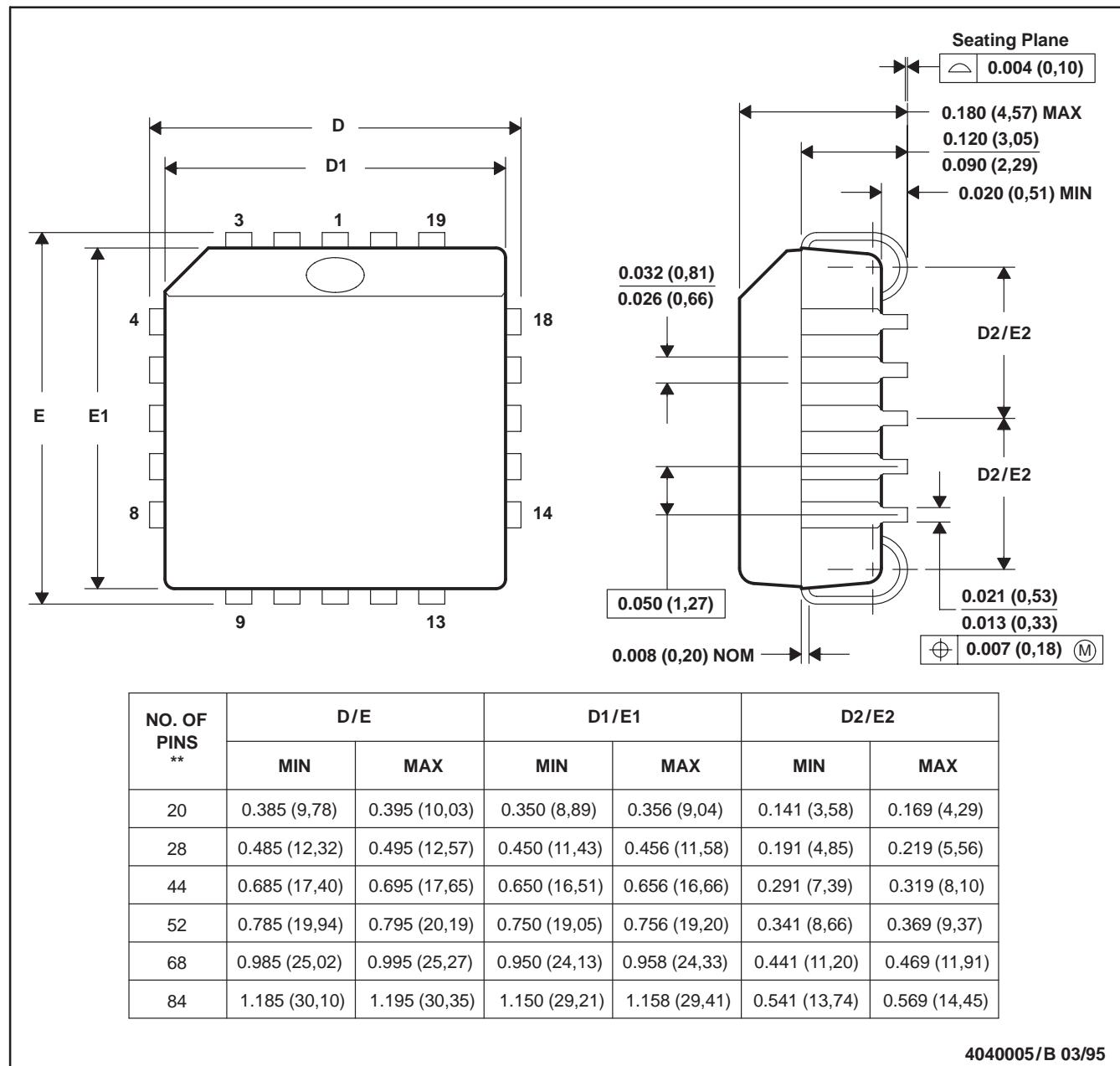


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Window (lens) added to this group of packages (24-, 28-, 32-, 40-pin).
 D. This package can be hermetically sealed with a ceramic lid using glass frit.
 E. Index point is provided on cap for terminal identification.

FN (S-PQCC-J**)

20 PIN SHOWN

PLASTIC J-LEADED CHIP CARRIER



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-018

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