

## E Series Power MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V) at $T_J$ max.	700
$R_{DS(on)}$ max. at 25 °C ( $\Omega$ )	$V_{GS} = 10$ V   0.9
$Q_g$ max. (nC)	34
$Q_{gs}$ (nC)	4
$Q_{gd}$ (nC)	8
Configuration	Single

### FEATURES

- Low Figure-of-Merit (FOM)  $R_{on} \times Q_g$
- Low Input Capacitance ( $C_{iss}$ )
- Reduced Switching and Conduction Losses
- Ultra Low Gate Charge ( $Q_g$ )
- Avalanche Energy Rated (UIS)
- Material categorization: For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

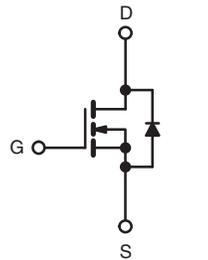
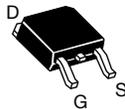


**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Server and Telecom Power Supplies
- Switch Mode Power Supplies (SMPS)
- Power Factor Correction Power Supplies (PFC)
- Lighting
  - High-Intensity Discharge (HID)
  - Fluorescent Ballast Lighting
- Industrial
  - Welding
  - Induction Heating
  - Motor Drives
  - Battery Chargers
  - Renewable Energy
  - Solar (PV Inverters)

**DPAK  
(TO-252)**



N-Channel MOSFET

### ORDERING INFORMATION

Package	DPAK (TO-252)
Lead (Pb)-free and Halogen-free	SiHD6N62E-GE3

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	620	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Gate-Source Voltage AC ( $f > 1$ Hz)		30	
Continuous Drain Current ( $T_J = 150$ °C)	$V_{GS}$ at 10 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	12	
Linear Derating Factor		0.63	W/°C
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	88	mJ
Maximum Power Dissipation	$P_D$	78	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	°C
Drain-Source Voltage Slope	$dV/dt$	$T_J = 125$ °C	V/ns
Reverse Diode $dV/dt$ <sup>d</sup>		12	
Soldering Recommendations (Peak Temperature) <sup>c</sup>	for 10 s	300	°C

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 2.5$  A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$ ,  $dI/dt = 100$  A/ $\mu$ s, starting  $T_J = 25$  °C.

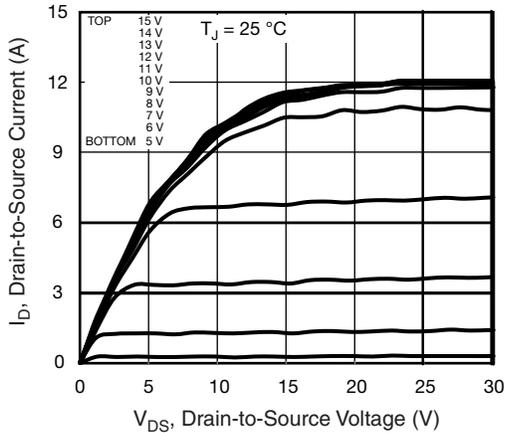
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.6	

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		620	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$		-	0.76	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2	-	4	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 620\text{ V}, V_{GS} = 0\text{ V}$		-	-	1	$\mu\text{A}$
		$V_{DS} = 496\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	10	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 3\text{ A}$	-	0.78	0.90	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 30\text{ V}, I_D = 3\text{ A}$		-	1.8	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V},$ $V_{DS} = 100\text{ V},$ $f = 1\text{ MHz}$		-	578	-	pF
Output Capacitance	$C_{oss}$			-	36	-	
Reverse Transfer Capacitance	$C_{rss}$			-	4	-	
Effective Output Capacitance, Energy Related <sup>a</sup>	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 496\text{ V}, V_{GS} = 0\text{ V}$		-	31	-	
Effective Output Capacitance, Time Related <sup>b</sup>	$C_{o(tr)}$			-	87	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 3\text{ A}, V_{DS} = 496\text{ V}$	-	17	34	nC
Gate-Source Charge	$Q_{gs}$			-	4	-	
Gate-Drain Charge	$Q_{gd}$			-	8	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 496\text{ V}, I_D = 3\text{ A},$ $V_{GS} = 10\text{ V}, R_g = 9.1\text{ }\Omega$		-	12	24	ns
Rise Time	$t_r$			-	10	20	
Turn-Off Delay Time	$t_{d(off)}$			-	22	44	
Fall Time	$t_f$			-	16	32	
Gate Input Resistance	$R_g$	$f = 1\text{ MHz}, \text{ open drain}$		-	1.3	-	$\Omega$
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	7	A
Pulsed Diode Forward Current	$I_{SM}$			-	-	12	
Diode Forward Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 3\text{ A}, V_{GS} = 0\text{ V}$		-	0.9	1.2	V
Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = I_S = 3\text{ A},$ $dI/dt = 100\text{ A}/\mu\text{s}, V_R = 400\text{ V}$		-	190	-	ns
Reverse Recovery Charge	$Q_{rr}$			-	1.3	-	$\mu\text{C}$
Reverse Recovery Current	$I_{RRM}$			-	11	-	A

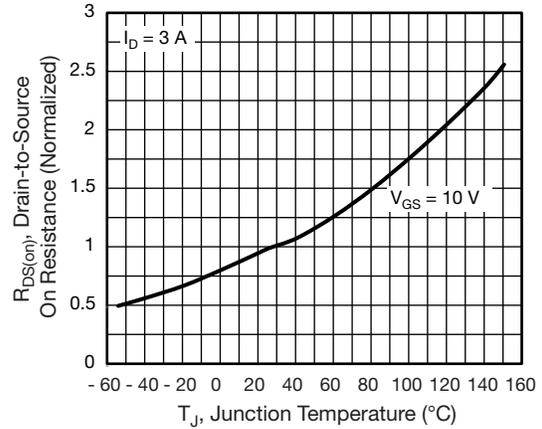
**Notes**

- a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .  
 b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .

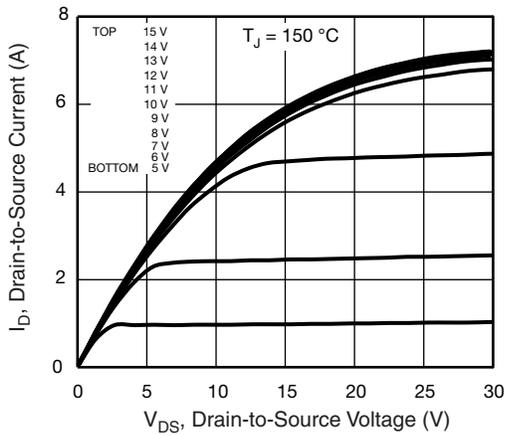
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



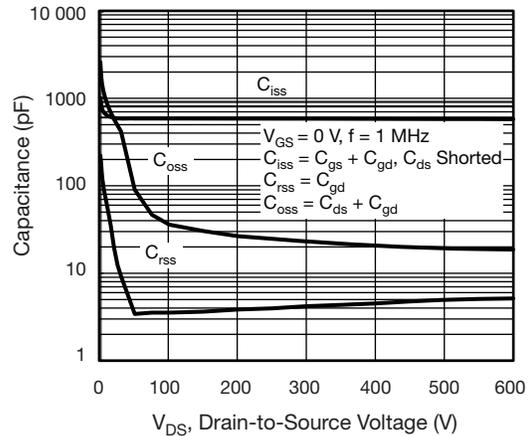
**Fig. 1 - Typical Output Characteristics**



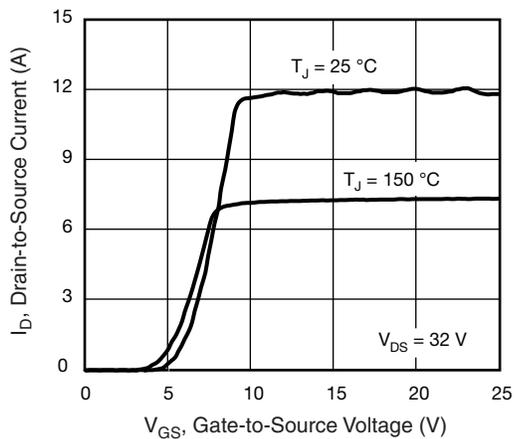
**Fig. 4 - Normalized On-Resistance vs. Temperature**



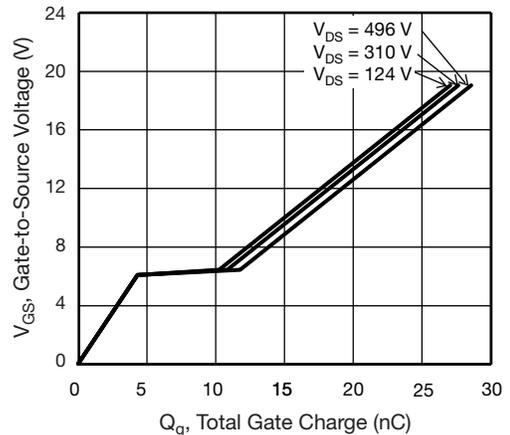
**Fig. 2 - Typical Output Characteristics**



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**

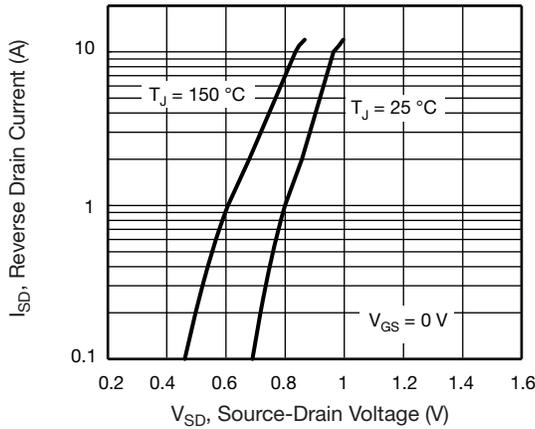


Fig. 7 - Typical Source-Drain Diode Forward Voltage

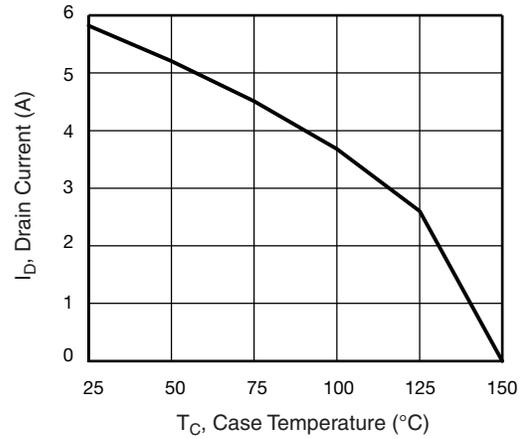


Fig. 9 - Maximum Drain Current vs. Case Temperature

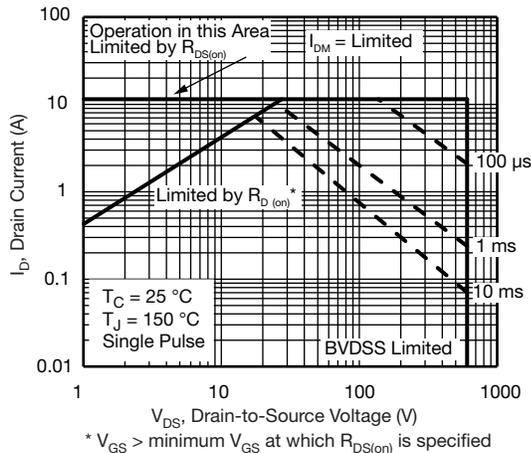


Fig. 8 - Maximum Safe Operating Area

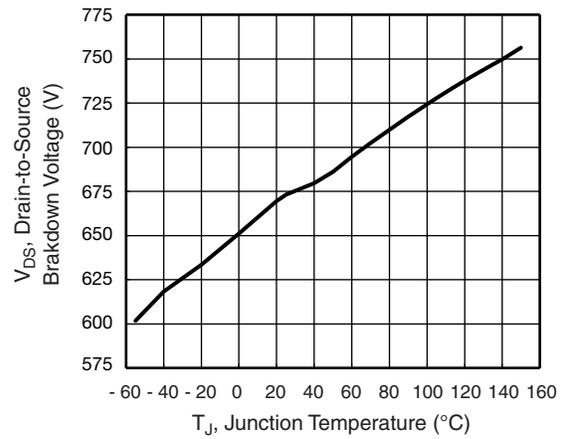


Fig. 10 - Temperature vs. Drain-to-Source Voltage

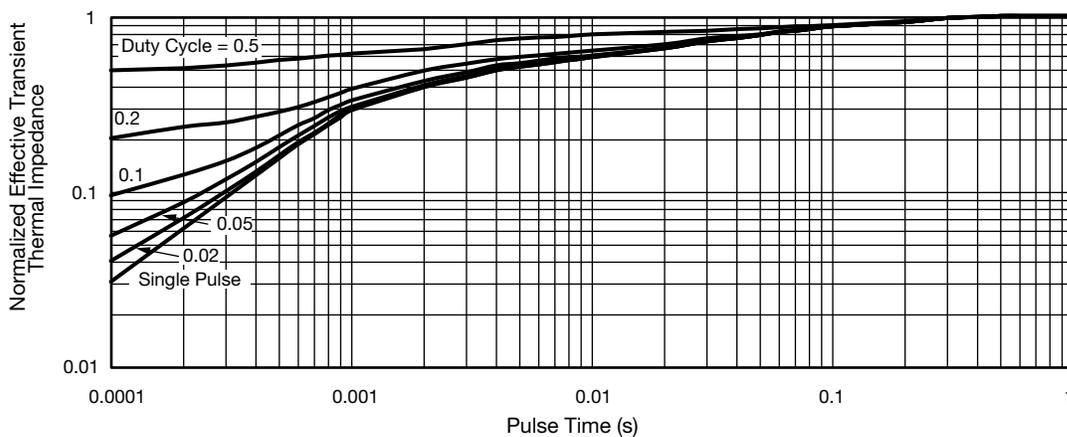


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

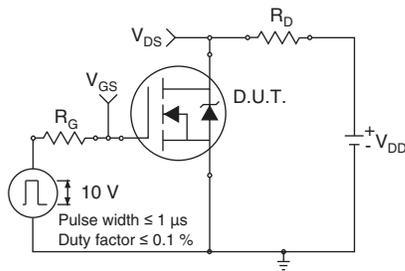


Fig. 12 - Switching Time Test Circuit

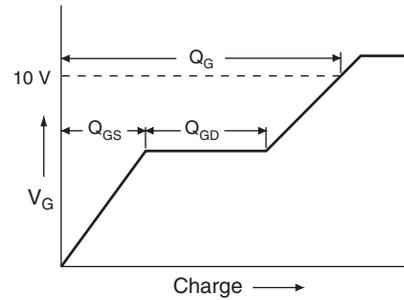


Fig. 16 - Basic Gate Charge Waveform

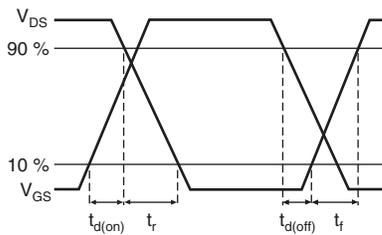


Fig. 13 - Switching Time Waveforms

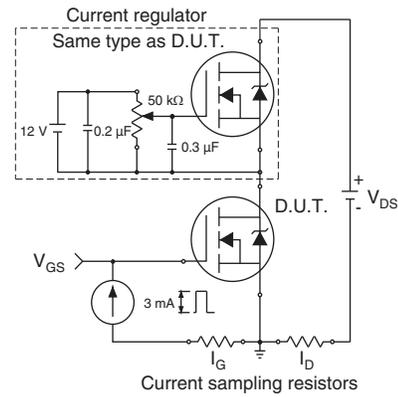


Fig. 17 - Gate Charge Test Circuit

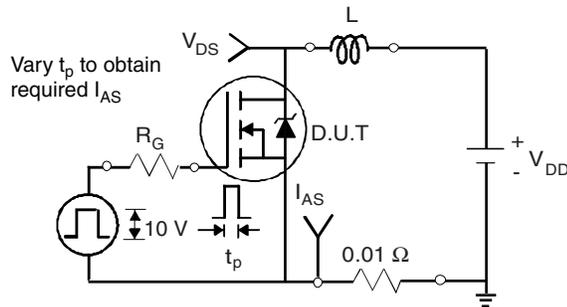


Fig. 14 - Unclamped Inductive Test Circuit

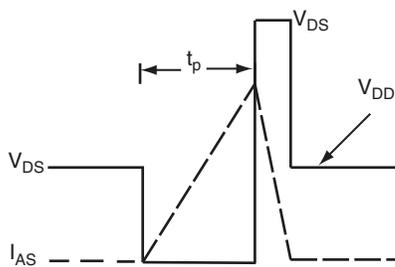
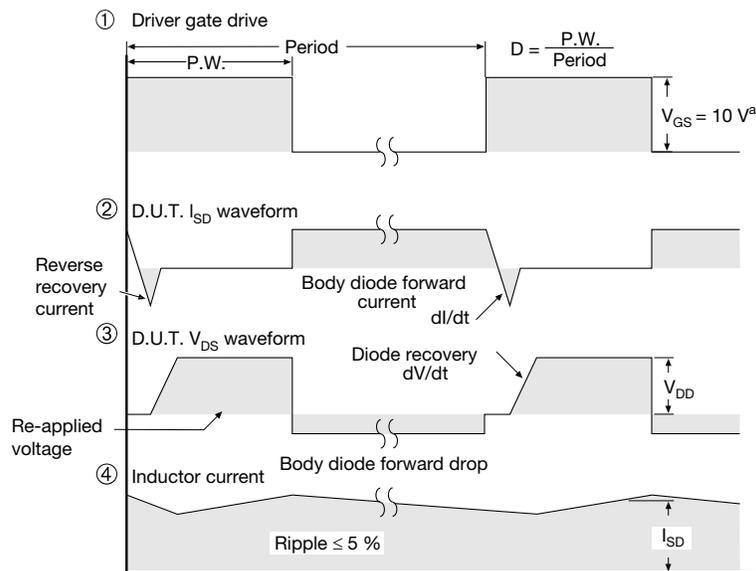
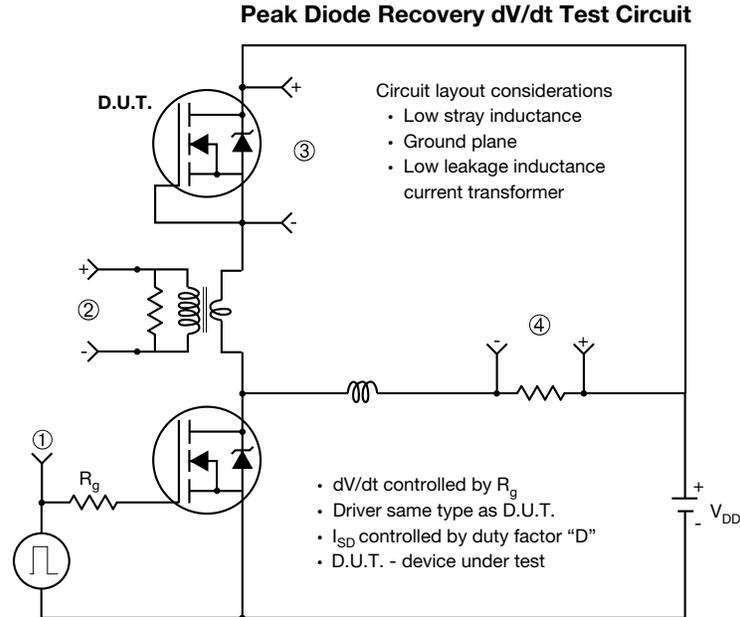


Fig. 15 - Unclamped Inductive Waveforms



**Note**

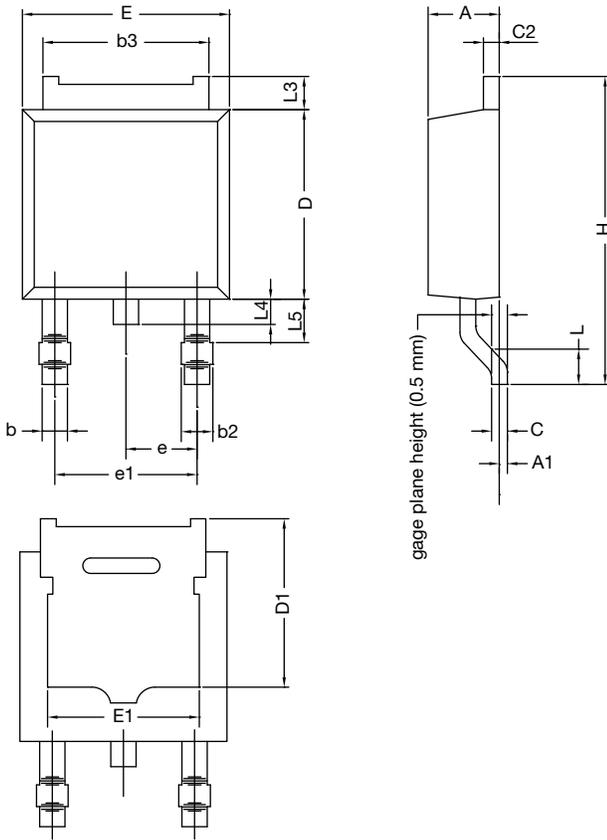
a.  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 18 - For N-Channel**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?91558](http://www.vishay.com/ppg?91558).



## TO-252AA Case Outline

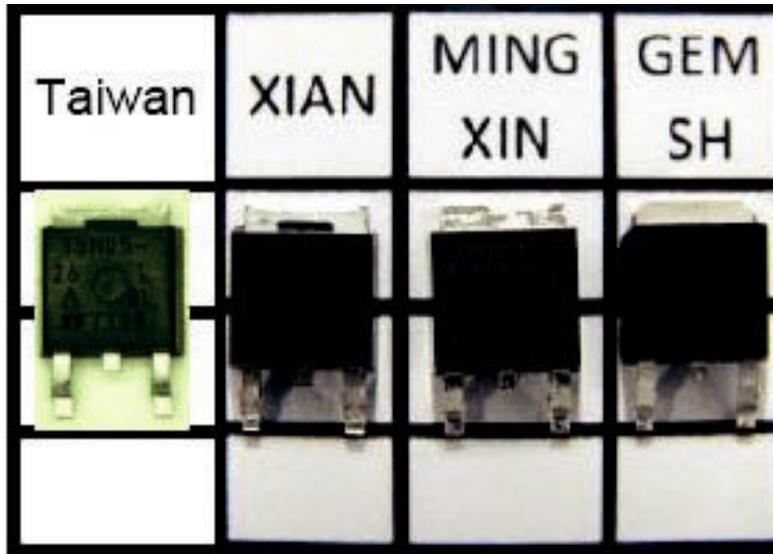


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060

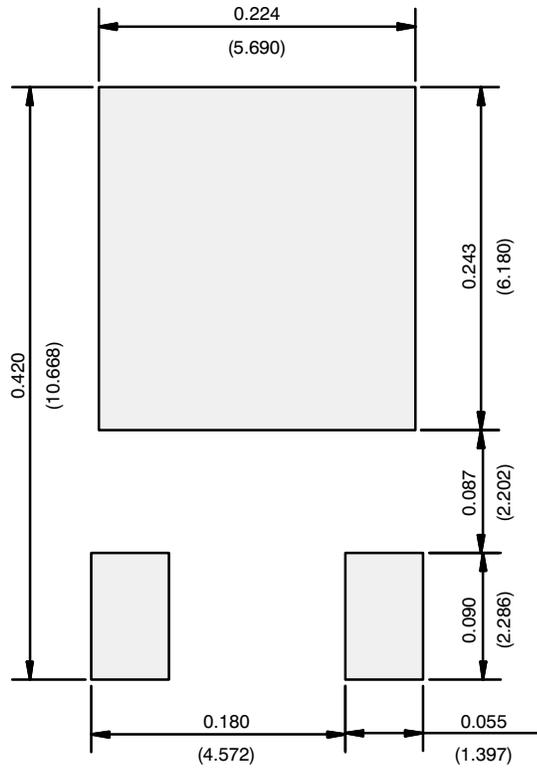
ECN: T13-0359-Rev. O, 03-Jun-13  
DWG: 5347

### Notes

- Dimension L3 is for reference only.
- Xi'an, Mingxin, and GEM SH actual photo.



## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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## Material Category Policy

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