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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION⁽¹⁾

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	SPECIFIED TEMPERATURE RANGE	PACKAGE- LEAD	PACKAGE DESIGNATOR	ORDERING NUMBER	TRANSPORT MEDIA QUANTITY
DAC8803	±1	±1	-40°C to +85°C	SSOP-28	DB	DAC8803IDBT	Tape and Reel, 250
						DAC8803IDBR	Tape and Reel, 2500

- (1) For the most current specifications and package information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

	DAC8803	UNIT
V_{DD} to GND	-0.3 to +8	V
V_{REF} to GND	-18 to +18	V
Logic inputs and output to GND	-0.3 to +8	V
$V(I_{OUT})$ to GND	-0.3 to $V_{DD} + 0.3$	V
A_{GNDX} to DGND	-0.3 to +0.3	V
Input current to any pin except supplies	±50	mA
Package power dissipation	$(T_{Jmax} - T_A)/\theta_{JA}$	W
Thermal resistance, θ_{JA}	28-Lead shrink surface-mount (RS-28)	100
		°C/W
Maximum junction temperature (T_{Jmax})	150	°C
Operating temperature range, Model A	-40 to +85	°C
Storage temperature range	-65 to +150	°C

- (1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

$V_{DD} = +2.7\text{ V}$ to $+5.5\text{ V}$; $I_{OUTX} = \text{Virtual GND}$, $A_{GNDX} = 0\text{ V}$, $V_{REFA, B, C, D} = 10\text{ V}$, $T_A = \text{full operating temperature range}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC8803			UNIT	
			MIN	TYP	MAX		
STATIC PERFORMANCE ⁽¹⁾							
Resolution			14			Bits	
Relative accuracy			±1			LSB	
Differential nonlinearity	DNL		±1			LSB	
Output leakage current	I _{OUTX}	Data = 0000h, T _A = 25°C	10			nA	
	I _{OUTX}	Data = 0000h, T _A = T _A max	20			nA	
Full-scale gain error	G _{FSE}	Data = 3FFFh	±0.75	±3		mV	
Full-scale tempco ⁽²⁾	TCV _{FS}		1			ppm/°C	
Feedback resistor	R _{FB} X	V _{DD} = 5 V				kΩ	
REFERENCE INPUT							
V _{REF} X Range	V _{REF} X		-15	15		V	
Input resistance	R _{REF} X		4	5	6	kΩ	
Input resistance match	R _{REF} X	Channel-to-channel	1			%	
Input capacitance ⁽²⁾	C _{REF} X		5			pF	
ANALOG OUTPUT							
Output current	I _{OUTX}	Data = 3FFFh	1.6	2.5		mA	
Output capacitance ⁽²⁾	C _{OUT} X	Code-dependent	50			pF	
LOGIC INPUTS AND OUTPUT							
Input low voltage	V _{IL}	V _{DD} = +2.7 V	0.6			V	
	V _{IL}	V _{DD} = +5 V	0.8			V	
Input high voltage	V _{IH}	V _{DD} = +2.7 V	2.1			V	
	V _{IH}	V _{DD} = +5 V	2.4			V	
Input leakage current	I _{IL}		1			μA	
Input capacitance ⁽²⁾	C _{IL}		10			pF	
Logic output low voltage	V _{OL}	I _{OL} = 1.6 mA	0.4			V	
Logic output high voltage	V _{OH}	I _{OH} = 100 μA	4			V	
INTERFACE TIMING ^{(2), (3)}							
Clock width high	t _{CH}		25			ns	
Clock width low	t _{CL}		25			ns	
$\overline{\text{CS}}$ to Clock setup	t _{CSS}		0			ns	
Clock to $\overline{\text{CS}}$ hold	t _{CSH}		25			ns	
Clock to SDO prop delay	t _{PD}		2			20	ns
Load DAC pulsewidth	t _{LDAC}		25			ns	
Data setup	t _{DS}		20			ns	
Data hold	t _{DH}		20			ns	
Load setup	t _{LDS}		5			ns	
Load hold	t _{LDH}		25			ns	

(1) All static performance tests (except I_{OUT}) are performed in a closed-loop system using an external precision OPA277 I-to-V converter amplifier. The DAC8803 R_{FB} terminal is tied to the amplifier output. Typical values represent average readings measured at 25°C .

(2) These parameters are specified by design and not subject to production testing.

(3) All input control signals are specified with $t_R = t_F = 2.5\text{ ns}$ (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.

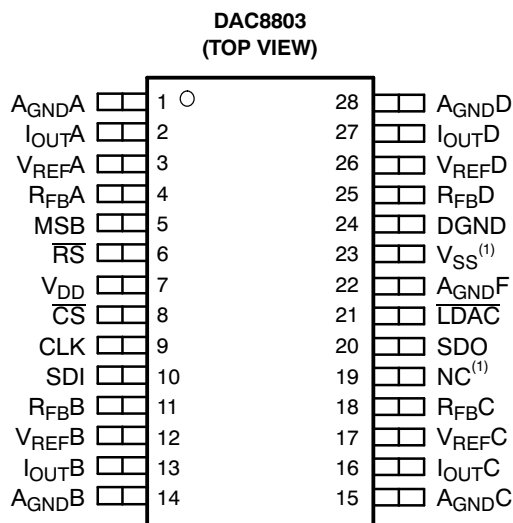
ELECTRICAL CHARACTERISTICS (continued)

$V_{DD} = +2.7\text{ V to }+5.5\text{ V}$; $I_{OUTX} = \text{Virtual GND}$, $A_{GNDX} = 0\text{ V}$, $V_{REFA, B, C, D} = 10\text{ V}$, $T_A = \text{full operating temperature range}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC8803			UNIT
			MIN	TYP	MAX	
SUPPLY CHARACTERISTICS						
Power supply range	V _{DD RANGE}		2.7		5.5	V
Positive supply current	I _{DD}	Logic inputs = 0 V, V _{DD} = +4.5 V to +5.5 V		2	5	μA
	I _{DD}	Logic inputs = 0 V, V _{DD} = +2.7 V to +3.6 V		1	2.5	μA
Power dissipation	P _{DISS}	Logic inputs = 0 V			0.025	mW
Power supply sensitivity	P _{SS}	ΔV _{DD} = ±5%			0.006	%
AC CHARACTERISTICS ⁽⁴⁾						
Output voltage settling time	t _s	To ±0.1% of full-scale, Data = 0000h to 3FFFh to 0000h		0.3		μs
	t _s	To ±0.006% of full-scale, Data = 0000h to 3FFFh to 0000h		0.5		μs
Reference multiplying BW	BW -3 dB	V _{REFX} = 100 mV _{RMS} , Data = 3FFFh, C _{FB} = 3 pF		10		MHz
DAC glitch impulse	Q	V _{REFX} = 10 V, Data = 1FFFh to 2000h to 1FFFh		1		nV/s
Feedthrough error	V _{OUTX} /V _{REFX}	Data = 0000h, V _{REFX} = 100 mV _{RMS} , f = 100 kHz		-70		dB
Crosstalk error	V _{OUTA} /V _{REFB}	Data = 0000h, V _{REFB} = 100 mV _{RMS} , Adjacent channel, f = 100 kHz		-100		dB
Digital feedthrough	Q	$\overline{CS} = 1$ and f _{CLK} = 1 MHz		1		nV/s
Total harmonic distortion	THD	V _{REF} = 5 V _{PP} , Data = 3FFFh, f = 1 kHz		-105		dB
Output spot noise voltage	e _n	f = 1 kHz, BW = 1 Hz		12		nV/√Hz

(4) All ac characteristic tests are performed in a closed-loop system using a THS4011 I-to-V converter amplifier.

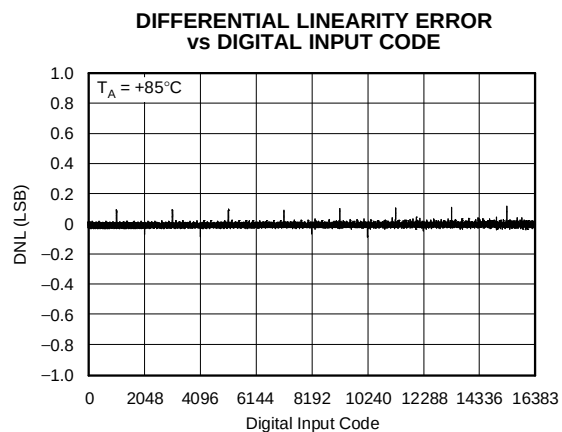
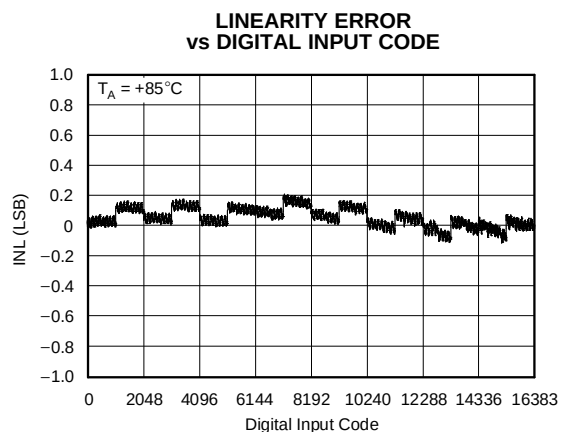
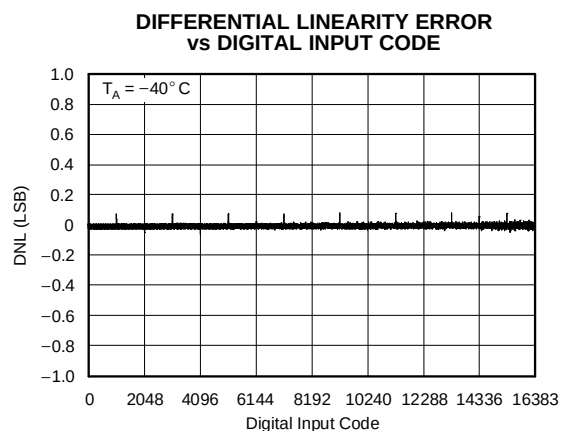
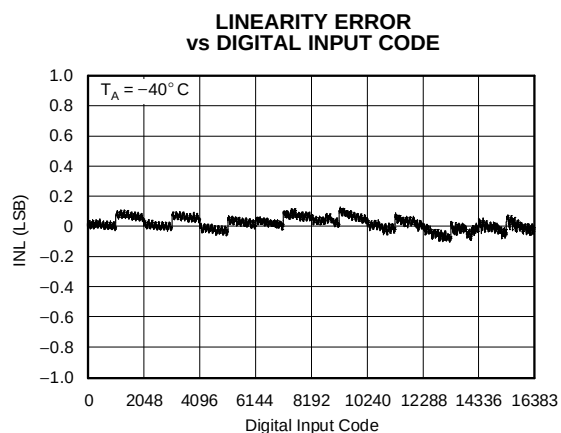
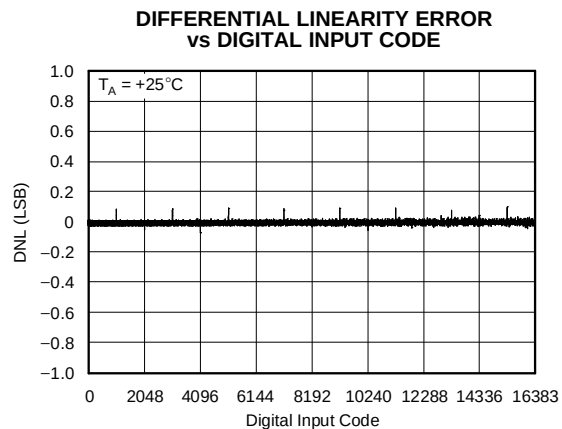
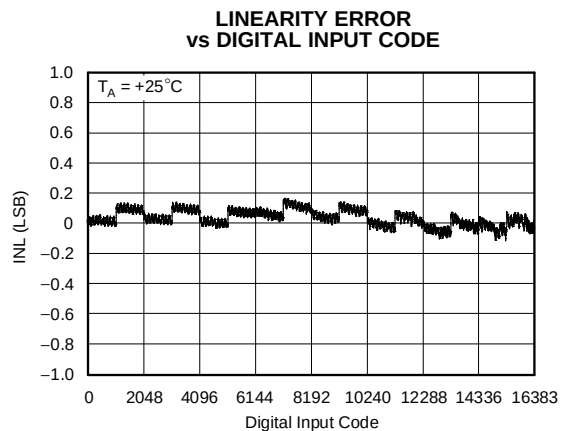
PIN CONFIGURATIONS



Note (1): No internal connection

PIN DESCRIPTION

PIN	NAME	DESCRIPTION
1, 14, 15, 28	AGNDA, AGNDB, AGNDC, AGNDD	DAC A, B, C, D Analog ground
2, 13, 16, 27	IOUTA, IOUTB, IOUTC, IOUTD	DAC A, B, C, D Current output
3, 12, 17, 26	VREFA, VREFB, VREFC, VREFD	DAC A, B, C, D Reference voltage input terminal. Establishes DAC A, B, C, D full-scale output voltage. Can be tied to VDD.
4, 11, 18, 25	RFB A, RFB B, RFB C, RFB D,	Establish voltage output for DAC A, B, C, D by connecting to external amplifier output.
5	MSB	MSB Bit set during a reset pulse (RS) or at system power-on if tied to ground or VDD.
6	RS	Reset pin, active low. Input register and DAC registers are set to all zeros or half-scale code (2000h) determined by the voltage on the MSB pin. Register data = 2000h when MSB = 1.
7	VDD	Positive power-supply input. Specified range of operation +2.7 V to +5.5 V.
8	CS	Chip select; active low input. Disables shift register loading when high. Transfers shift register data to input register when CS/LDAC goes high. Does not affect LDAC operation.
9	CLK	Clock input; positive edge triggered clocks data into shift register
10	SDI	Serial data input; data loads directly into the shift register.
19	NC	Not connected; leave floating
20	SDO	Serial data output; input data load directly into shift register. Data appears at SDO, 17 clock pulses after input at the SDI pin.
21	LDAC	Load DAC register strobe; level sensitive active low. Transfers all input register data to the DAC registers. Asynchronous active low input. See Table 1 for operation.
22	AGNDF	High current analog force ground.
23	VSS	No internal connection.
24	DGND	Digital ground.

TYPICAL CHARACTERISTICS: $V_{DD} = +5\text{ V}$ At $T_A = +25^\circ\text{C}$, $+V_{DD} = +5\text{ V}$, unless otherwise noted.**Channel A**

TYPICAL CHARACTERISTICS: $V_{DD} = +5\text{ V}$ (continued)

At $T_A = +25^\circ\text{C}$, $+V_{DD} = +5\text{ V}$, unless otherwise noted.

Channel B

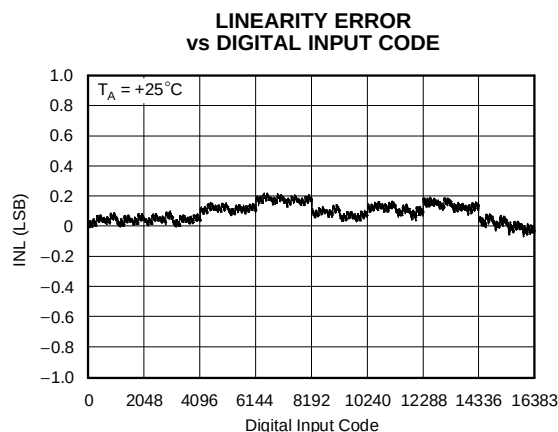


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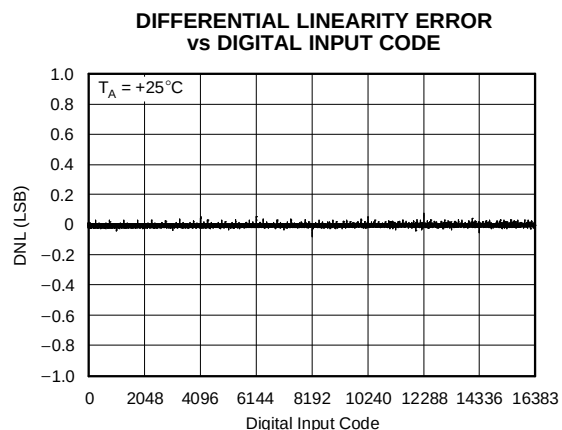


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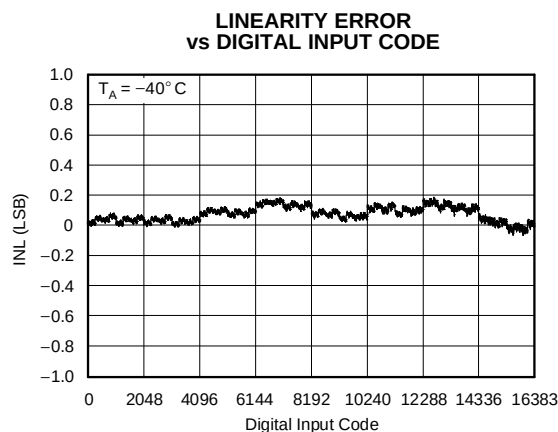


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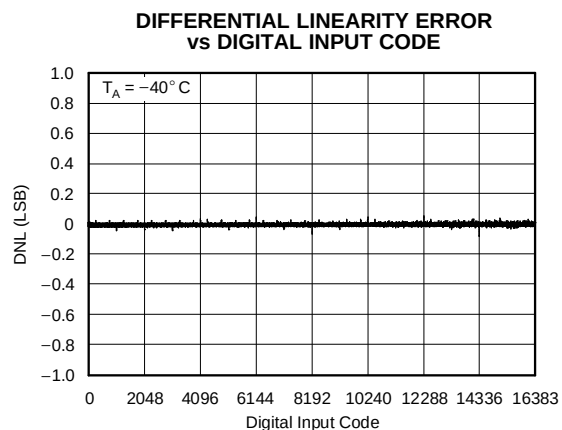


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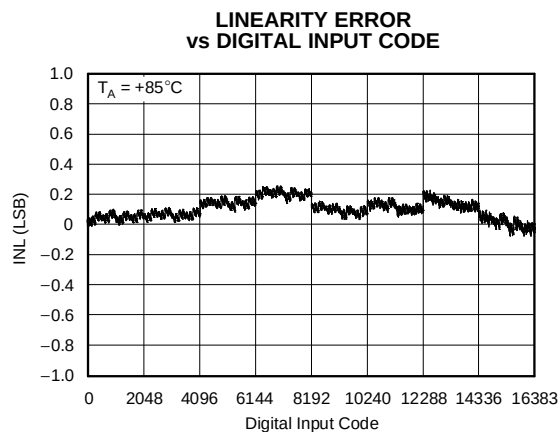


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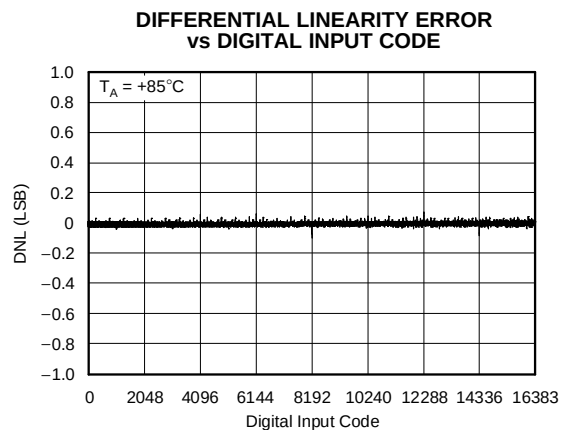
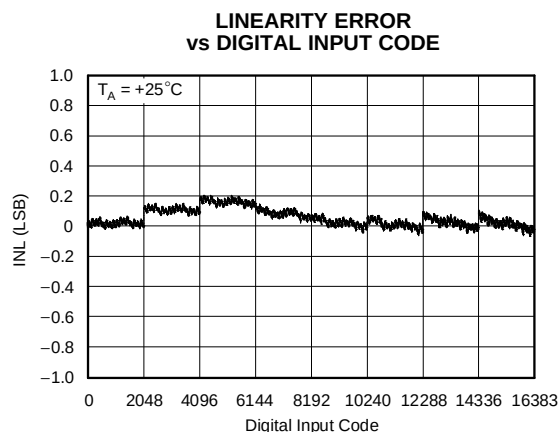
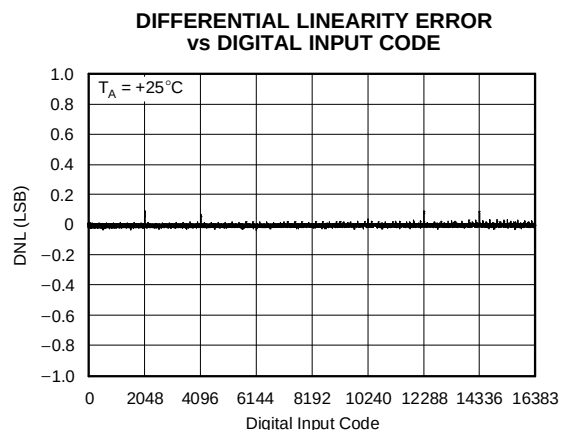
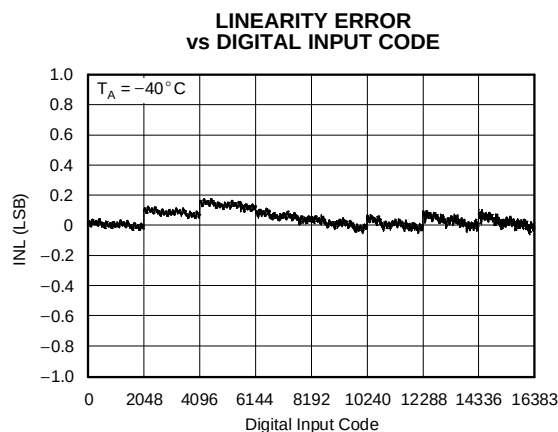
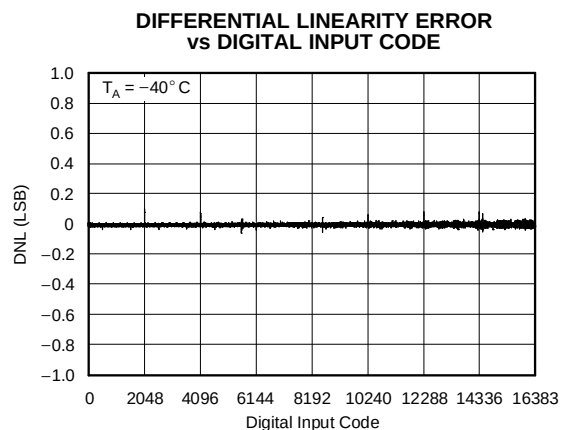
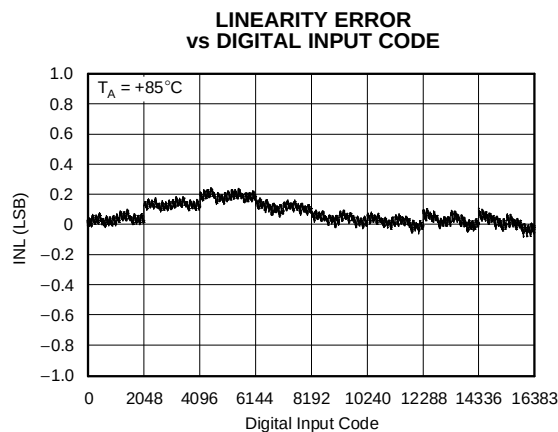
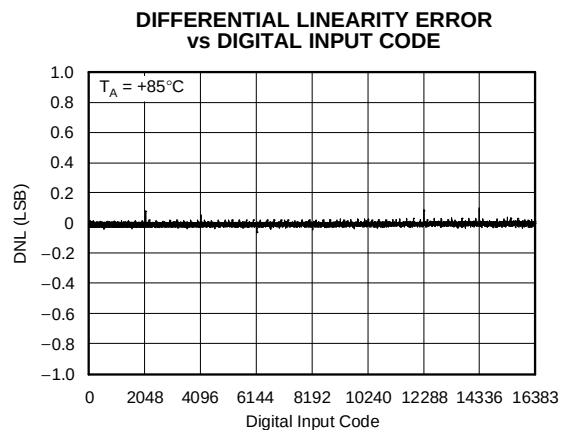


Figure 12.

TYPICAL CHARACTERISTICS: $V_{DD} = +5\text{ V}$ (continued)

At $T_A = +25^\circ\text{C}$, $+V_{DD} = +5\text{ V}$, unless otherwise noted.

Channel C**Figure 13.****Figure 14.****Figure 15.****Figure 16.****Figure 17.****Figure 18.**

TYPICAL CHARACTERISTICS: $V_{DD} = +5\text{ V}$ (continued)

At $T_A = +25^\circ\text{C}$, $+V_{DD} = +5\text{ V}$, unless otherwise noted.

Channel D

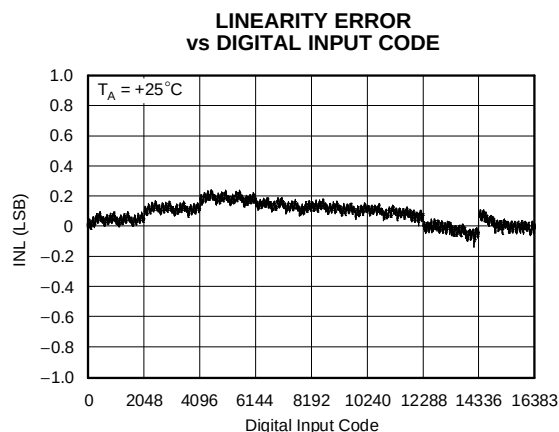


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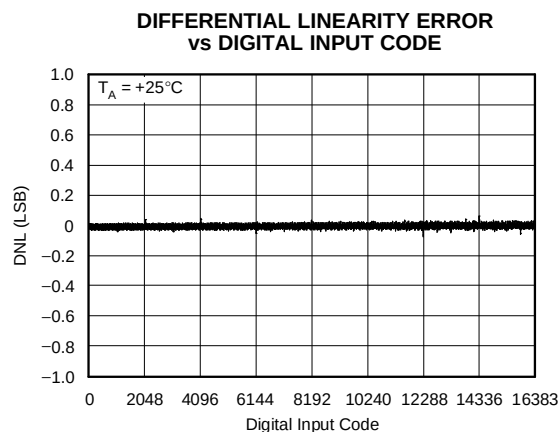


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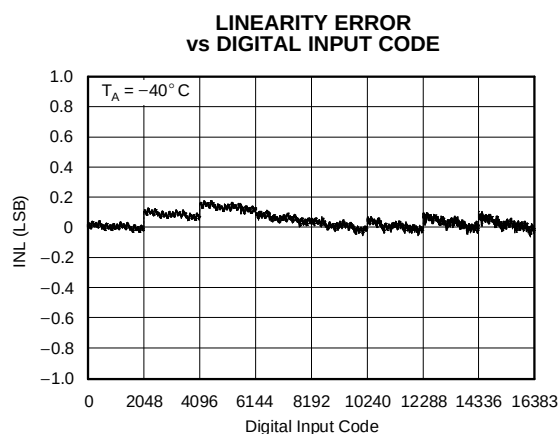


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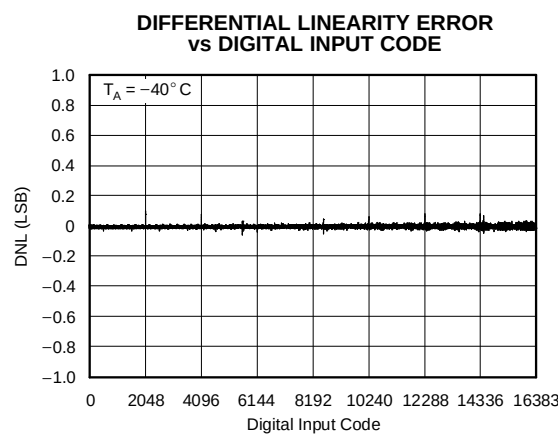


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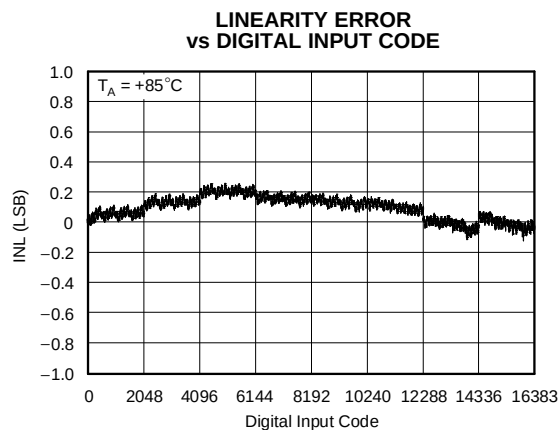


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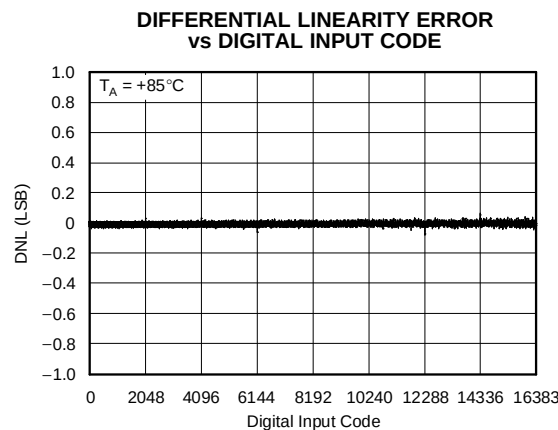


Figure 24.

TYPICAL CHARACTERISTICS: $V_{DD} = +5\text{ V}$ (continued)

At $T_A = +25^\circ\text{C}$, $+V_{DD} = +5\text{ V}$, unless otherwise noted.

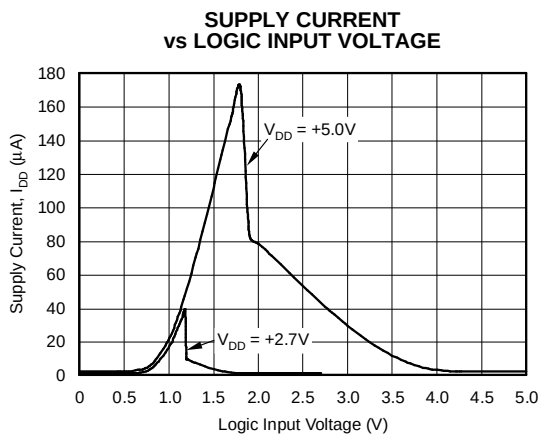


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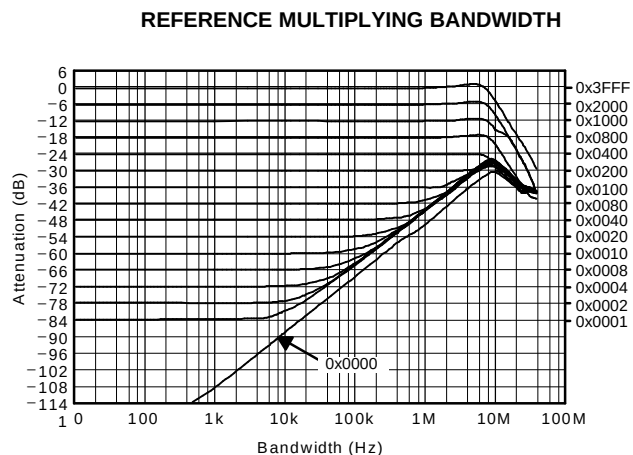


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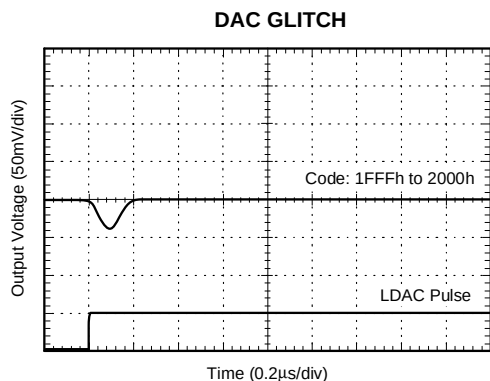


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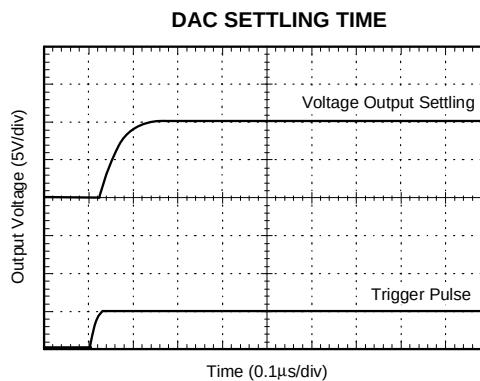


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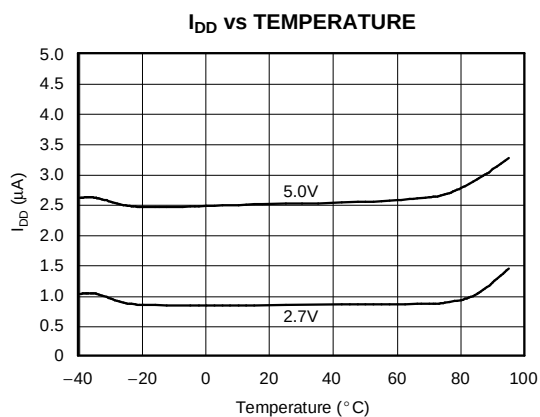


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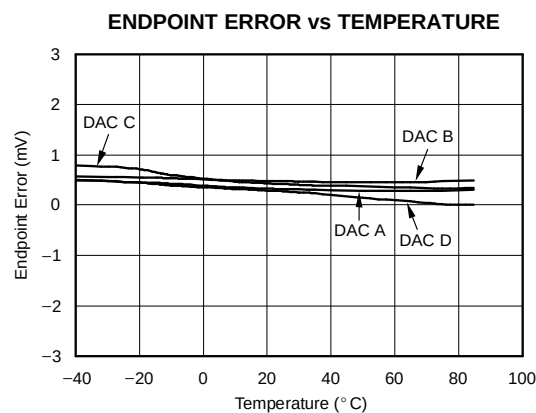


Figure 30.

TYPICAL CHARACTERISTICS: $V_{DD} = +2.7\text{ V}$

At $T_A = +25^\circ\text{C}$, $+V_{DD} = +2.7\text{ V}$, unless otherwise noted.

Channel A

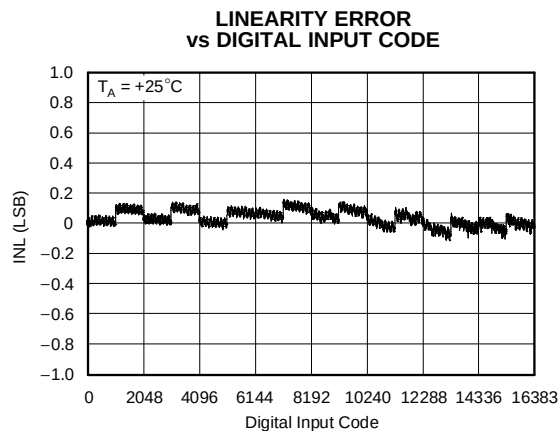


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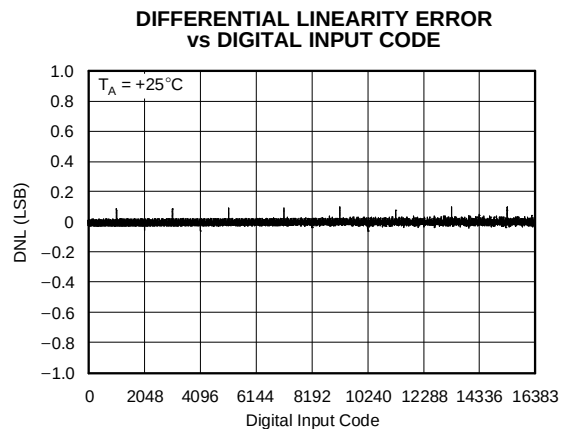


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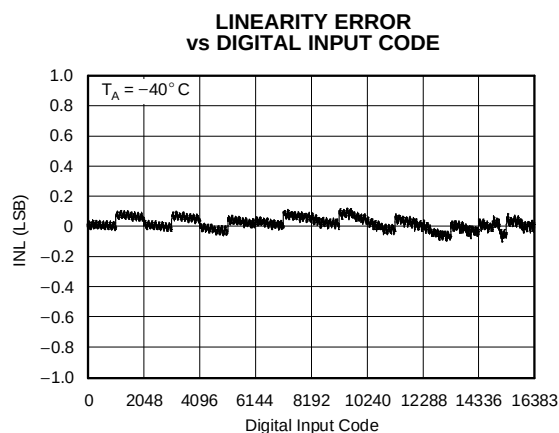


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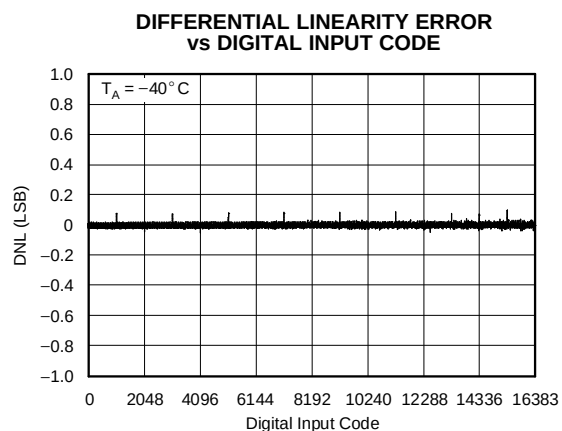


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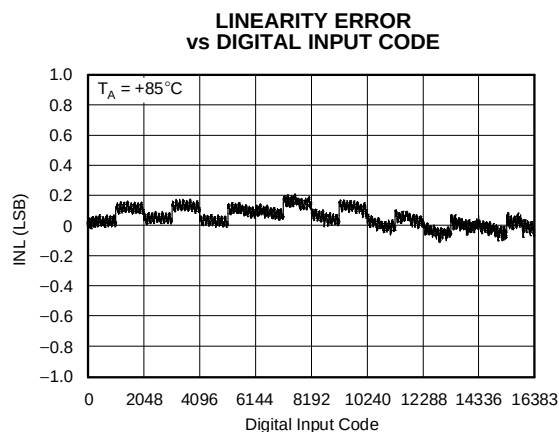


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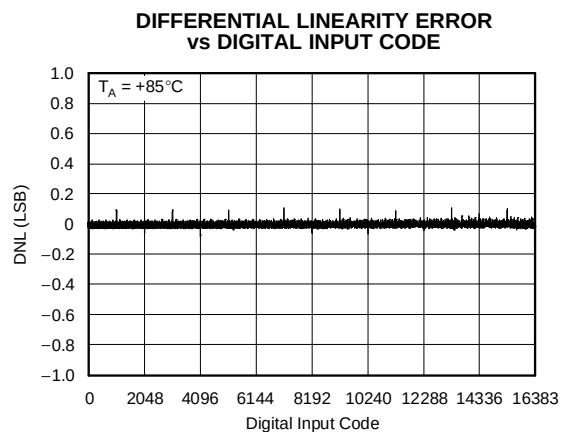
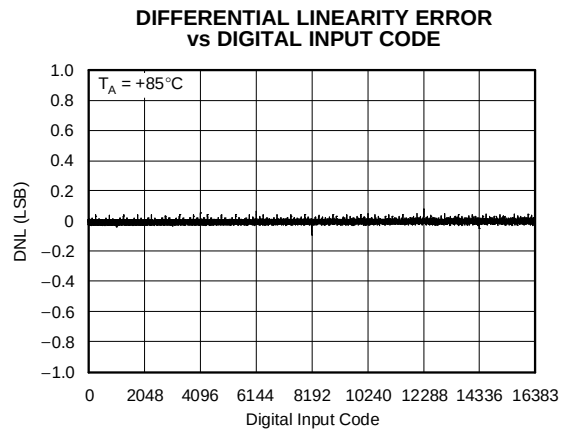
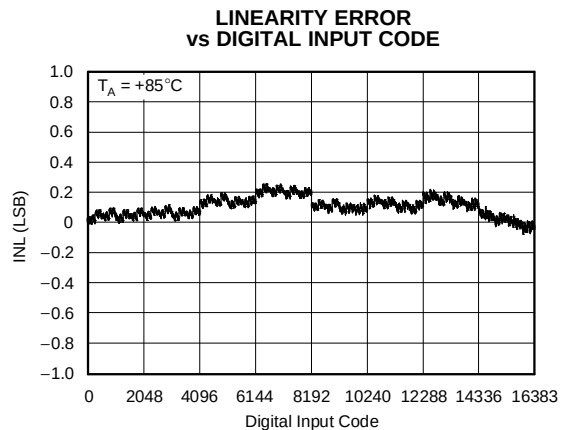
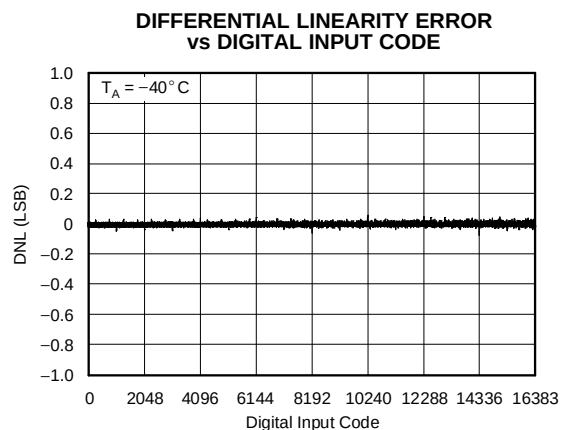
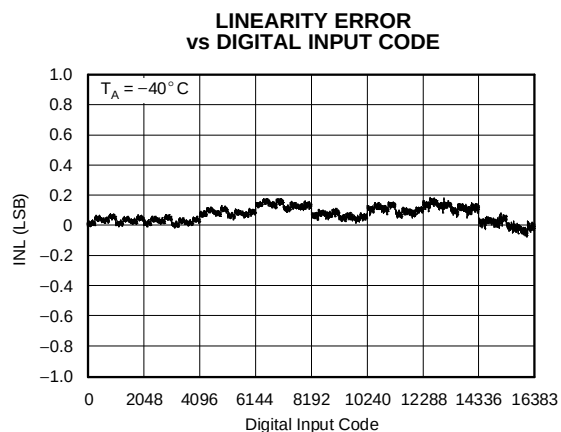
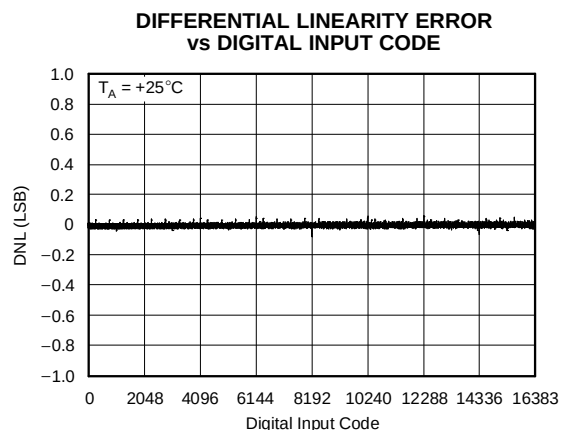
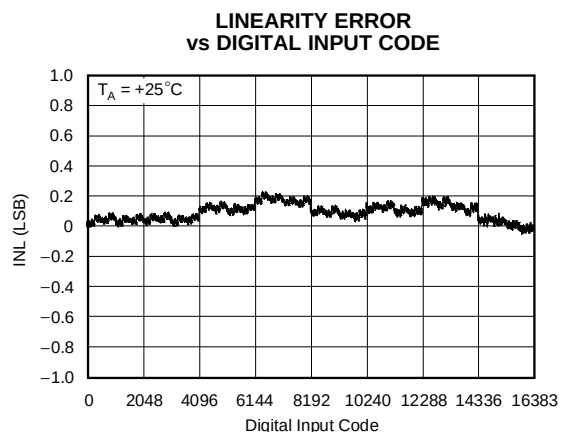


Figure 36.

TYPICAL CHARACTERISTICS: $V_{DD} = +2.7$ V (continued)

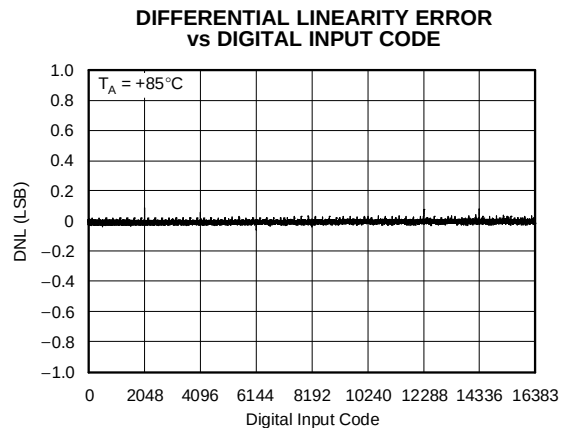
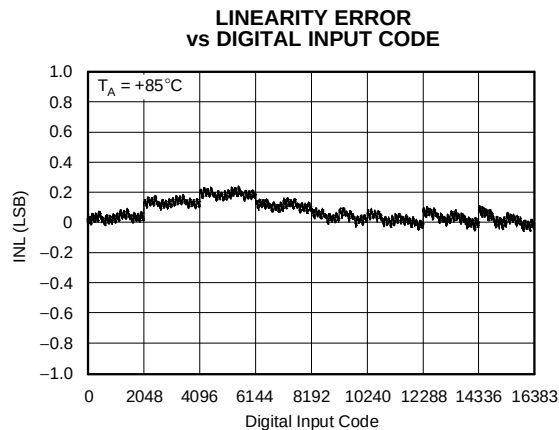
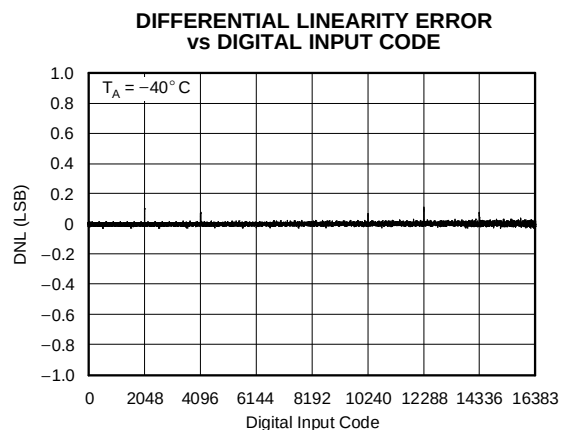
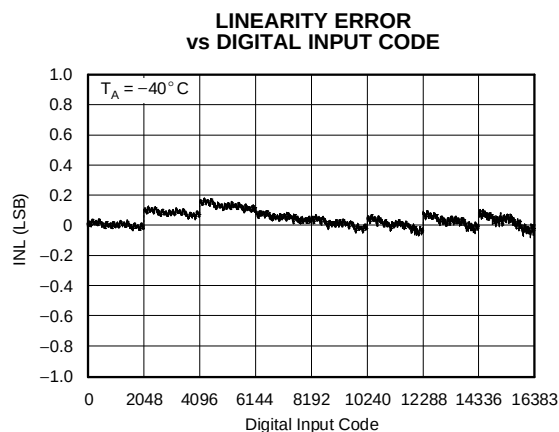
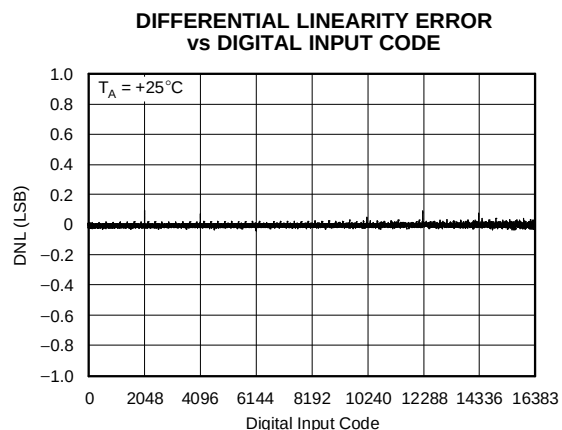
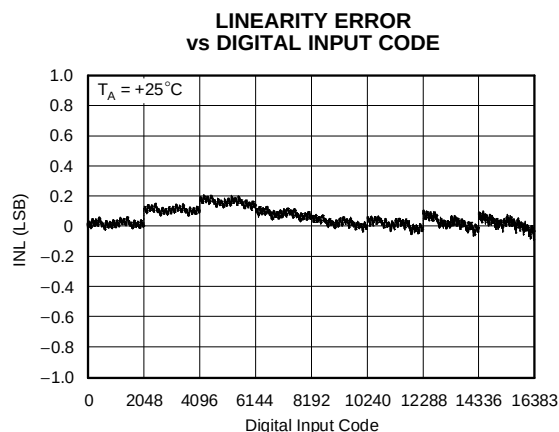
At $T_A = +25^\circ\text{C}$, $+V_{DD} = +2.7$ V, unless otherwise noted.

Channel B

TYPICAL CHARACTERISTICS: $V_{DD} = +2.7$ V (continued)

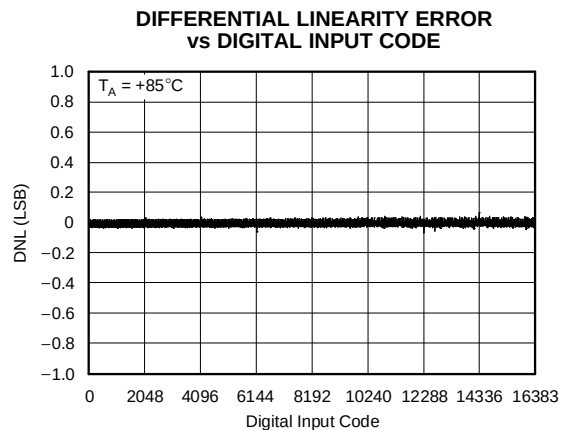
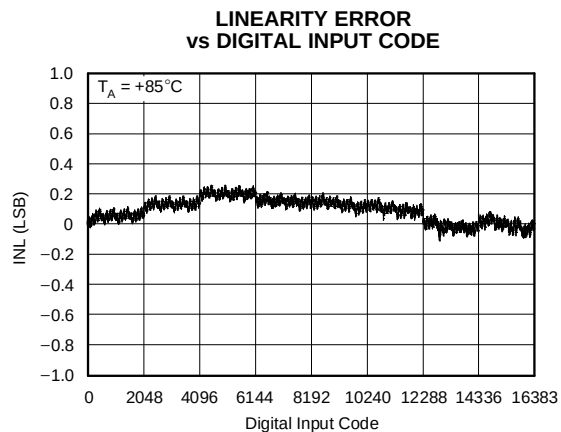
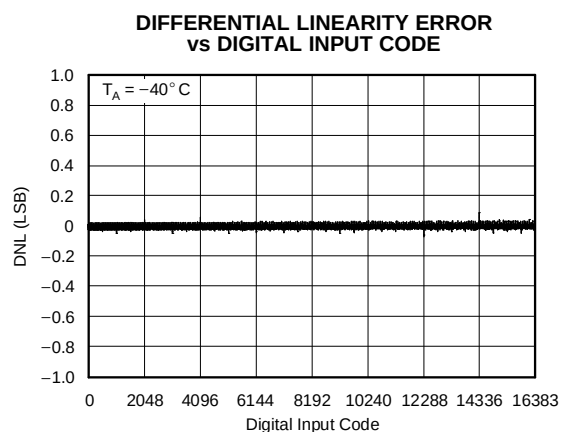
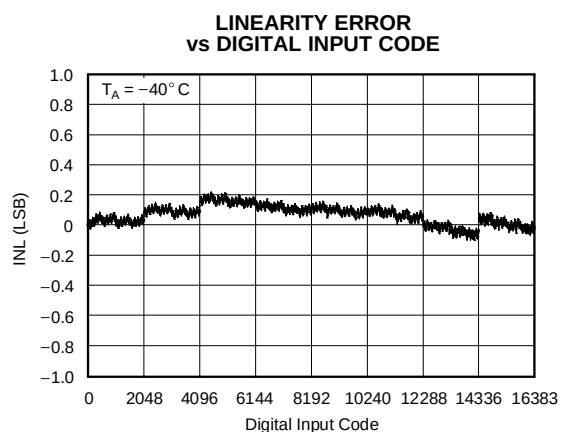
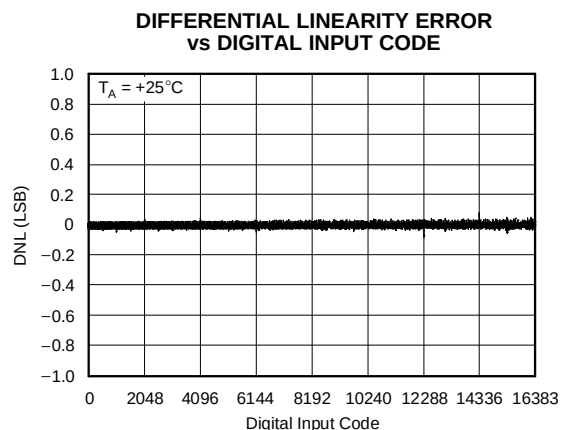
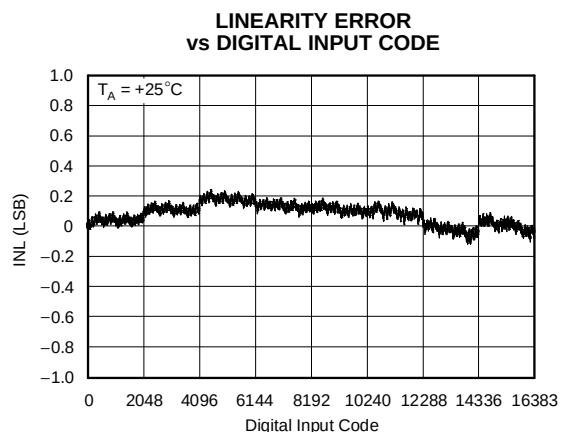
At $T_A = +25^\circ\text{C}$, $+V_{DD} = +2.7$ V, unless otherwise noted.

Channel C



TYPICAL CHARACTERISTICS: $V_{DD} = +2.7$ V (continued)

At $T_A = +25^\circ\text{C}$, $+V_{DD} = +2.7$ V, unless otherwise noted.

Channel D

TYPICAL CHARACTERISTICS: $V_{DD} = +2.7\text{ V}$ (continued)

At $T_A = +25^\circ\text{C}$, $+V_{DD} = +2.7\text{ V}$, unless otherwise noted.

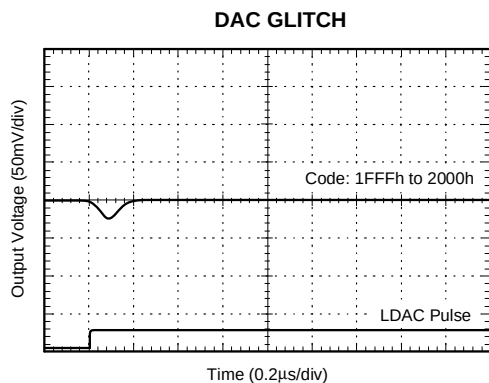


Figure 55.

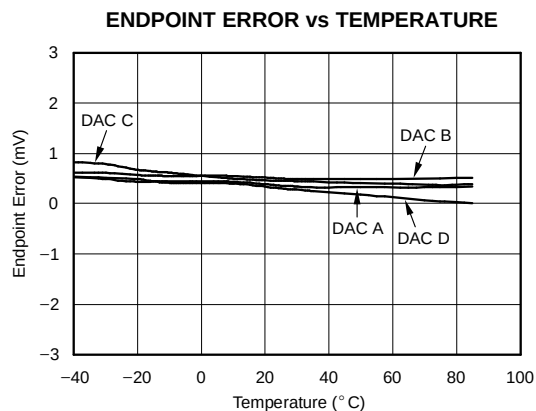


Figure 56.

TIMING INFORMATION

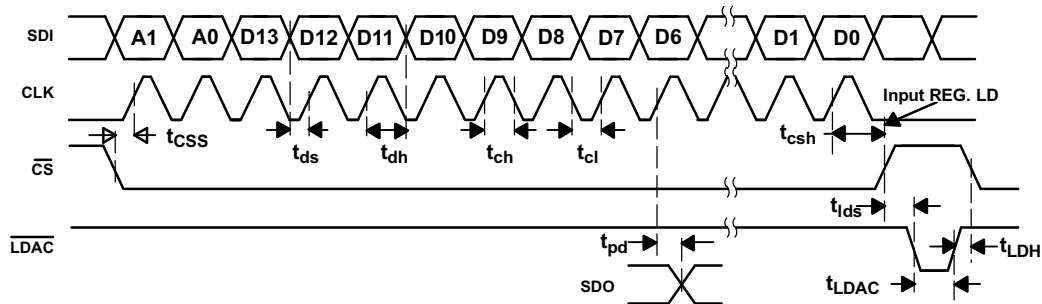


Figure 57. DAC8803 Timing Diagram

THEORY OF OPERATION

CIRCUIT OPERATION

The DAC8803 contains four, 14-bit, current-output, digital-to-analog converters (DACs) respectively. Each DAC has its own independent multiplying reference input. The DAC8803 uses a 3-wire SPI-compatible serial data interface, with a configurable asynchronous $\overline{RS}$ pin for half-scale (MSB = 1) or zero-scale (MSB = 0) preset. In addition, an $\overline{LDAC}$ strobe enables four channel simultaneous updates for hardware synchronized output voltage changes.

D/A Converter

The DAC8803 contains four current-steering R-2R ladder DACs. Figure 58 shows a typical equivalent DAC. Each DAC contains a matching feedback resistor for use with an external I-to-V converter amplifier. The R_{FBX} pin is connected to the output of the external amplifier. The I_{OUTX} terminal is connected to the inverting input of the external amplifier. The A_{GNDX} pin should be Kelvin-connected to the load point in the circuit requiring the full 14-bit accuracy.

The DAC is designed to operate with both negative or positive reference voltages. The V_{DD} power pin is only used by the logic to drive the DAC switches on and off. Note that a matching switch is used in series with the internal 5 k Ω feedback resistor. If users are attempting to measure the value of R_{FB} , power must be applied to V_{DD} in order to achieve continuity. The DAC output voltage is determined by V_{REF} and the digital data (D) according to Equation 1:

$$V_{OUT} = -V_{REF} \times \frac{D}{16384} \quad (1)$$

Note that the output polarity is opposite to the V_{REF} polarity for dc reference voltages.

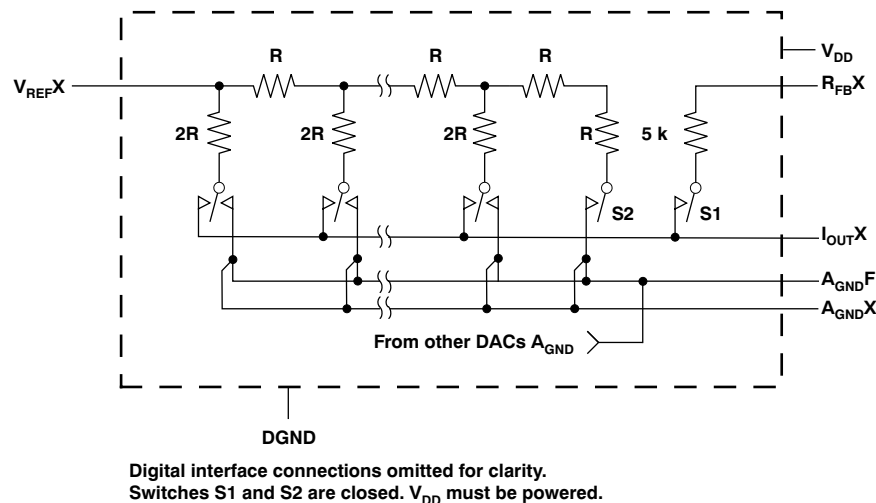


Figure 58. Typical Equivalent DAC Channel

The DAC is also designed to accommodate ac reference input signals. The DAC8803 accommodates input reference voltages in the range of -15 V to +15 V. The reference voltage inputs exhibit a constant nominal input resistance of 5 k Ω , $\pm 20\%$. On the other hand, the DAC outputs I_{OUTA} , B, C, D are code-dependent and produce various output resistances and capacitances.

The choice of external amplifier should take into account the variation in impedance generated by the DAC8803 on the amplifiers' inverting input node. The feedback resistance, in parallel with the DAC ladder resistance, dominates output voltage noise. For multiplying mode applications, an external feedback compensation capacitor (C_{FB}) may be needed to provide a critically damped output response for step changes in reference input voltages.

Figure 26 shows the gain versus frequency performance at various attenuation settings using a 3 pF external feedback capacitor connected across the I_{OUTX} and R_{FBX} terminals. In order to maintain good analog performance, power supply bypassing of 0.01 μF, in parallel with 1 μF, is recommended. Under these conditions, clean power supply with low ripple voltage capability should be used. Switching power supplies are usually not suitable for this application because of the higher ripple voltage and P_{SS} frequency-dependent characteristics. It is best to derive the DAC8803 5-V supply from the system analog supply voltages. (Do not use the digital 5-V supply.) See Figure 59.

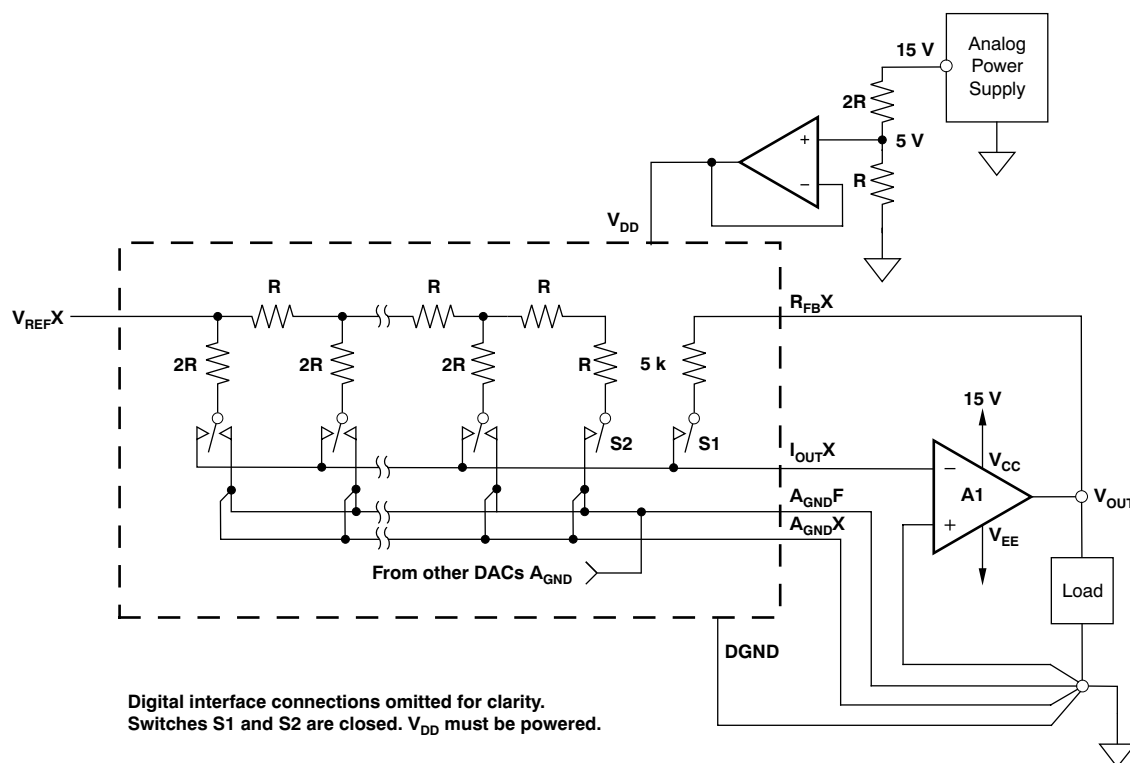


Figure 59. Recommended Kelvin-Sensed Hookup

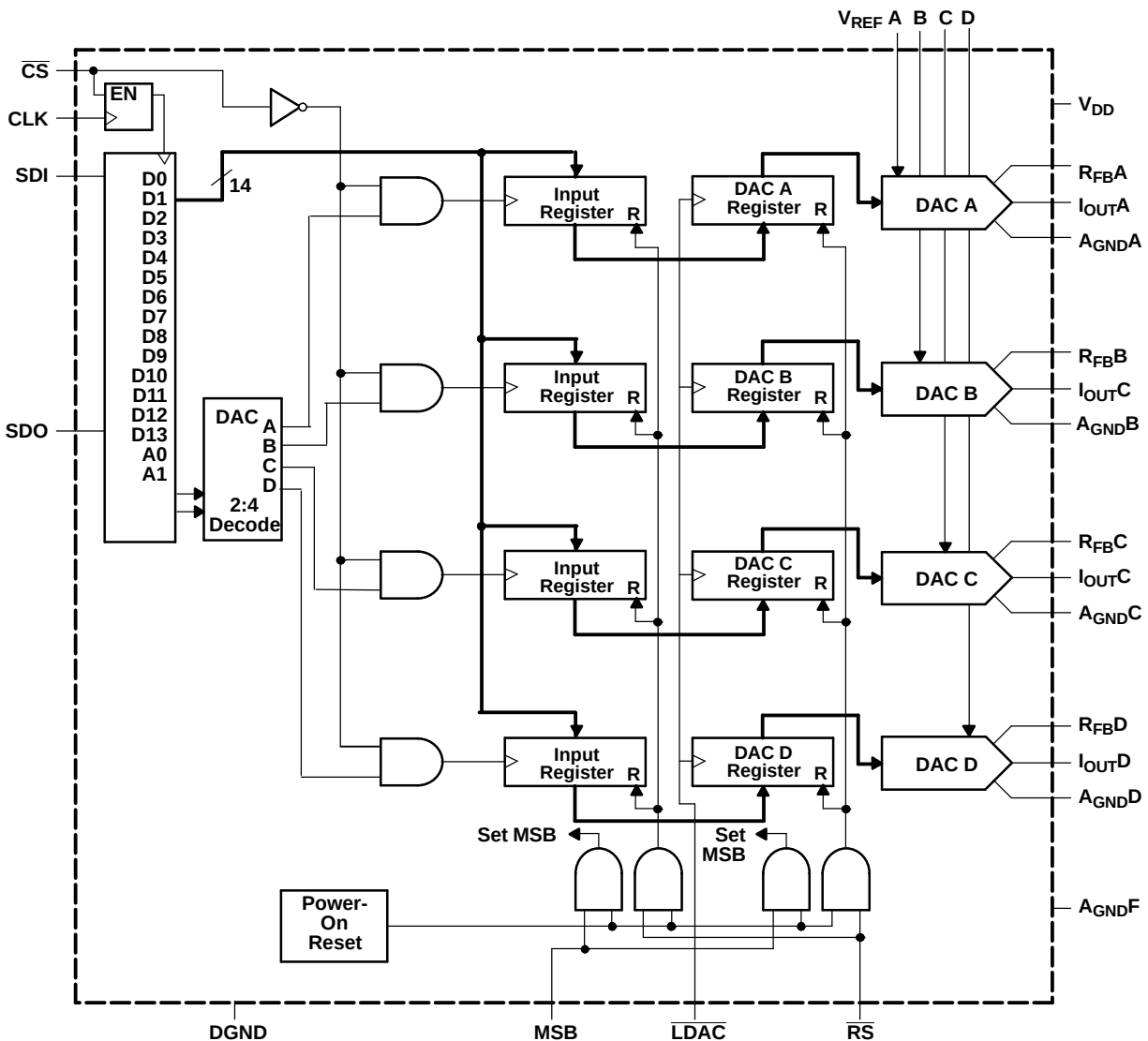


Figure 60. System Level Digital Interfacing

SERIAL DATA INTERFACE

The DAC8803 uses a 3-wire ($\overline{CS}$, SDI, CLK) SPI-compatible serial data interface. Serial data of the DAC8803 is clocked into the serial input register in a 16-bit data-word format. MSB bits are loaded first. [Table 2](#) defines the 16 data-word bits for the DAC8803.

Data is placed on the SDI pin, and clocked into the register on the positive clock edge of CLK subject to the data setup and data hold time requirements specified in the Interface Timing Specifications. Data can only be clocked in while the $\overline{CS}$ chip select pin is active low. For the DAC8803, only the last 16 bits clocked into the serial register are interrogated when the $\overline{CS}$ pin returns to the logic high state.

Since most microcontrollers output serial data in 8-bit bytes, two right-justified data bytes can be written to the DAC8803. Keeping the $\overline{CS}$ line low between the first and second byte transfers results in a successful serial register update.

Once the data is properly aligned in the shift register, the positive edge of the $\overline{CS}$ initiates the transfer of new data to the target DAC register, determined by the decoding of address bits A1 and A0. For the DAC8803, Table 2 and Table 3 define the characteristics of the software serial interface. Figure 61 shows the equivalent logic interface for the key digital control pins for the DAC8803.

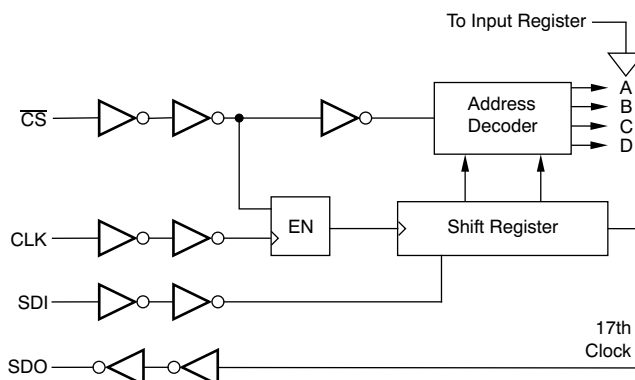


Figure 61. DAC8803 Equivalent Logic Interface

Two additional pins $\overline{RS}$ and MSB provide hardware control over the preset function and DAC register loading. If these functions are not needed, the $\overline{RS}$ pin can be tied to logic high. The asynchronous input $\overline{RS}$ pin forces all input and DAC registers to either the zero-code state (MSB = 0), or the half-scale state (MSB = 1).

POWER ON RESET

When the V_{DD} power supply is turned on, an internal reset strobe forces all the Input and DAC registers to the zero-code state or half-scale, depending on the MSB pin voltage. The V_{DD} power supply should have a smooth positive ramp without drooping in order to have consistent results, especially in the region of $V_{DD} = 1.5$ V to 2.3 V. The DAC register data stays at zero or half-scale setting until a valid serial register data load takes place.

ESD Protection Circuits

All logic-input pins contain back-biased ESD protection zener diodes connected to ground (DGND) and V_{DD} as shown in Figure 62.

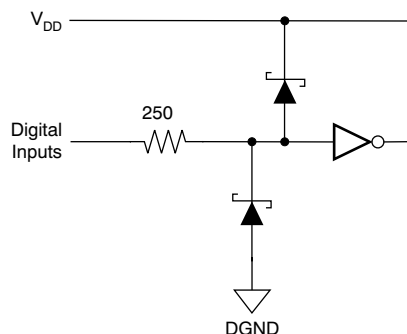


Figure 62. Equivalent ESD Protection Circuits

PCB LAYOUT

The DAC8803 is a high-accuracy DAC that can have its performance compromised by grounding and printed circuit board (PCB) lead trace resistance. The 14-bit DAC8803 with a 10-V full-scale range has an LSB value of 610 μ V. The ladder and associated reference and analog ground currents for a given channel can be as high as 2 mA. With this 2 mA current level, a series wiring and connector resistance of only 305 m Ω will cause 1 LSB of voltage drop. The preferred PCB layout for the DAC8803 is to have all A_{GND}X pins connected directly to an analog ground plane at the unit. The non-inverting input of each channel I/V converter should also either connect directly to the analog ground plane or have an individual sense trace back to the A_{GND}X pin connection. The feedback resistor trace to the I/V converter should also be kept short and low resistance to prevent IR drops from contributing to gain error. This attention to wiring ensures the optimal performance of the DAC8803.

Table 1. Control Logic Truth Table⁽¹⁾

$\overline{CS}$	CLK	$\overline{LDAC}$	$\overline{RS}$	MSB	SERIAL SHIFT REGISTER	INPUT REGISTER	DAC REGISTER
H	X	H	H	X	No effect	Latched	Latched
L	L	H	H	X	No effect	Latched	Latched
L	$\uparrow+$	H	H	X	Shift register data advanced one bit	Latched	Latched
L	H	H	H	X	No effect	Latched	Latched
$\uparrow+$	L	H	H	X	No effect	Selected DAC updated with current SR contents	Latched
H	X	L	H	X	No effect	Latched	Transparent
H	X	H	H	X	No effect	Latched	Latched
H	X	$\uparrow+$	H	X	No effect	Latched	Latched
H	X	H	L	0	No effect	Latched data = 0000h	Latched data = 0000h
H	X	H	L	H	No effect	Latched data = 2000h	Latched data = 2000h

(1) $\uparrow+$ Positive logic transition; X = Do not care

Table 2. Serial Input Register Data Format, Data Loaded MSB First⁽¹⁾

Bit	B15 (MSB)	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
Data	A1	A0	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

(1) Only the last 16 bits of data clocked into the serial register (address + data) are inspected when the $\overline{CS}$ line positive edge returns to logic high. At this point an internally generated load strobe transfers the serial register data contents (bits D13-D0) to the decoded DAC-input-register address determined by bits A1 and A0. Any extra bits clocked into the DAC8803 shift register are ignored; only the last 16 bits clocked in are used. If double-buffered data is not needed, the $\overline{LDAC}$ pin can be tied logic low to disable the DAC registers.

Table 3. Address Decode

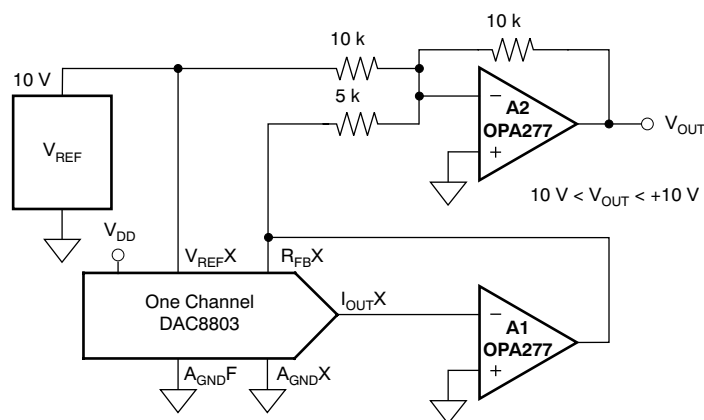
A1	A0	DAC DECODE
0	0	DAC A
0	1	DAC B
1	0	DAC C
1	1	DAC D

APPLICATION INFORMATION

The DAC8803, a 2-quadrant multiplying DAC, can be used to generate a unipolar output. The polarity of the full-scale output I_{OUT} is the inverse of the input reference voltage at V_{REF} .

Some applications require full 4-quadrant multiplying capabilities or bipolar output swing, as shown in Figure 63. An additional external op amp A2 is added as a summing amp. In this circuit the first and second amps (A1 and A2) provide a gain of 2X that widens the output span to 20 V. A 4-quadrant multiplying circuit is implemented by using a 10-V offset of the reference voltage to bias A2. According to the following circuit transfer equation (Equation 2), input data (D) from code 0 to full scale produces output voltages of $V_{OUT} = -10\text{ V}$ to $V_{OUT} = 10\text{ V}$.

$$V_{OUT} = \left(\frac{D}{8192} - 1 \right) \times V_{REF} \quad (2)$$



Digital interface connections omitted for clarity.

Figure 63. Four-Quadrant Multiplying Application Circuit

Cross-Reference

The DAC8803 has an industry-standard pinout. Table 4 provides the cross-reference information.

Table 4. Cross-Reference

PRODUCT	INL (LSB)	DNL (LSB)	SPECIFIED TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKAGE OPTION	CROSS-REFERENCE PART
DAC8803IDB	±1	±1	-40°C to +85°C	28-Lead MicroSOIC	SSOP-28	AD5554BRS

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC8803IDBR	Active	Production	SSOP (DB) 28	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8803
DAC8803IDBR.A	Active	Production	SSOP (DB) 28	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8803
DAC8803IDBRG4	Active	Production	SSOP (DB) 28	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8803
DAC8803IDBT	Active	Production	SSOP (DB) 28	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8803
DAC8803IDBT.A	Active	Production	SSOP (DB) 28	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8803
DAC8803IDBTG4	Active	Production	SSOP (DB) 28	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8803
DAC8803IDBTG4.A	Active	Production	SSOP (DB) 28	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8803

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

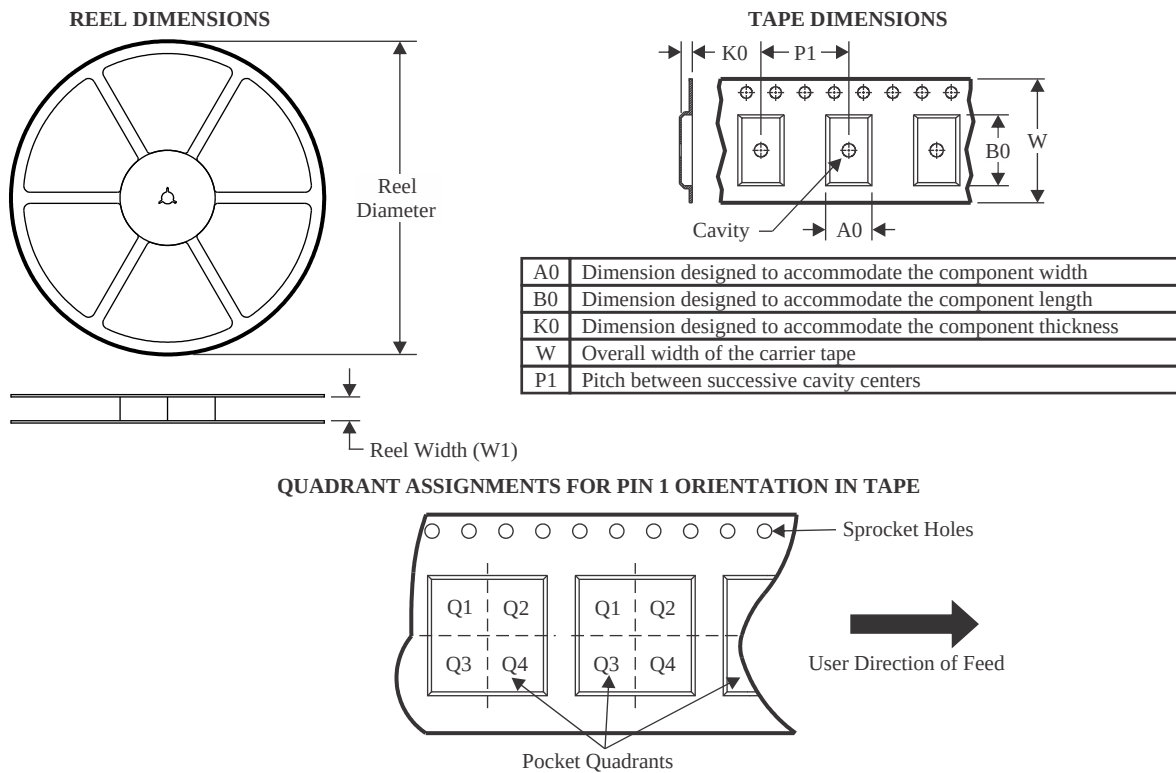
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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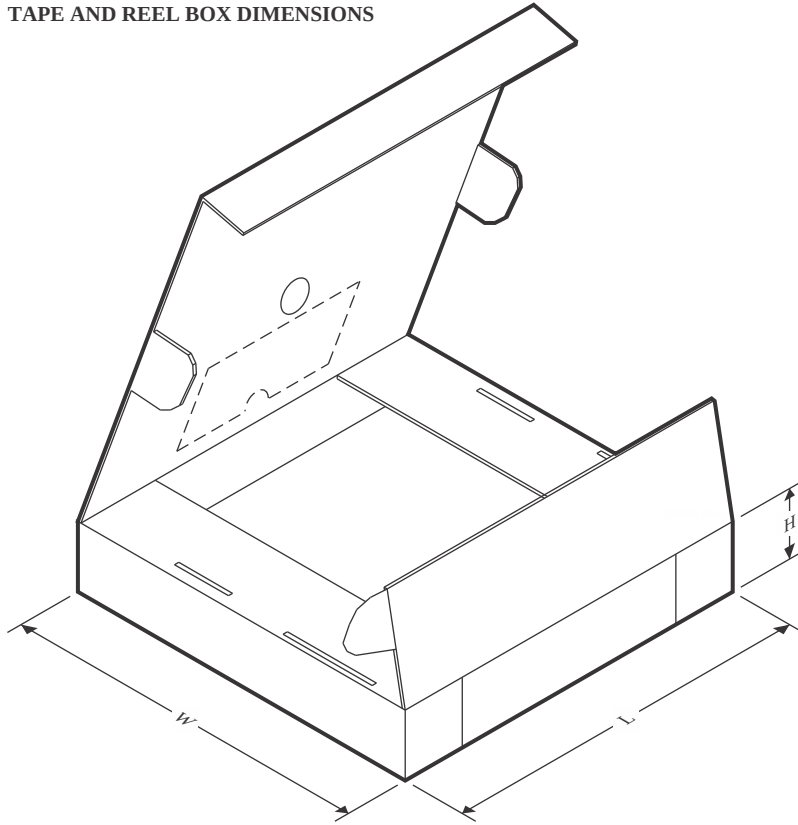
TAPE AND REEL INFORMATION



*All dimensions are nominal

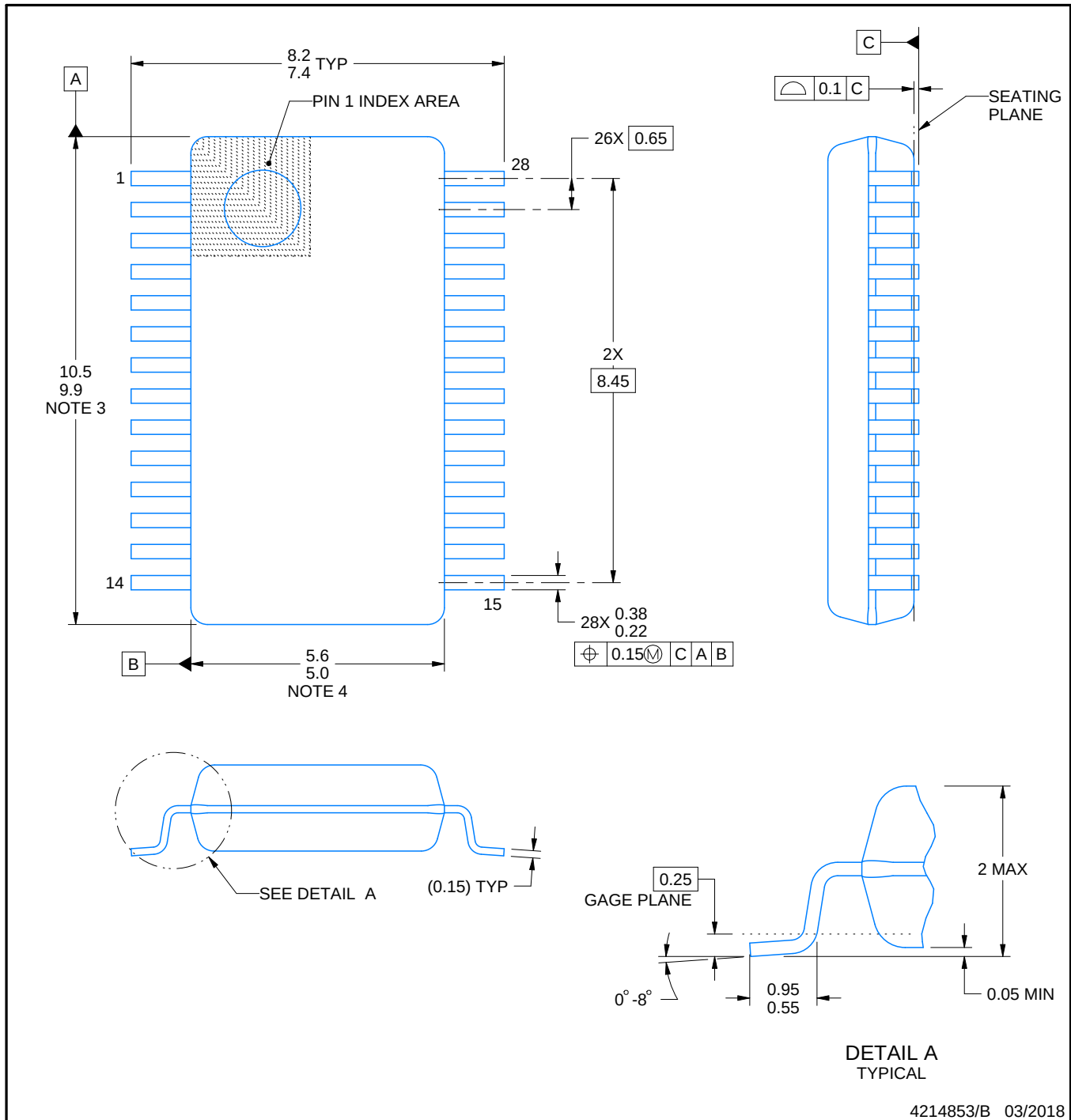
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8803IDBR	SSOP	DB	28	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8803IDBR	SSOP	DB	28	2000	350.0	350.0	43.0



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NOTES:

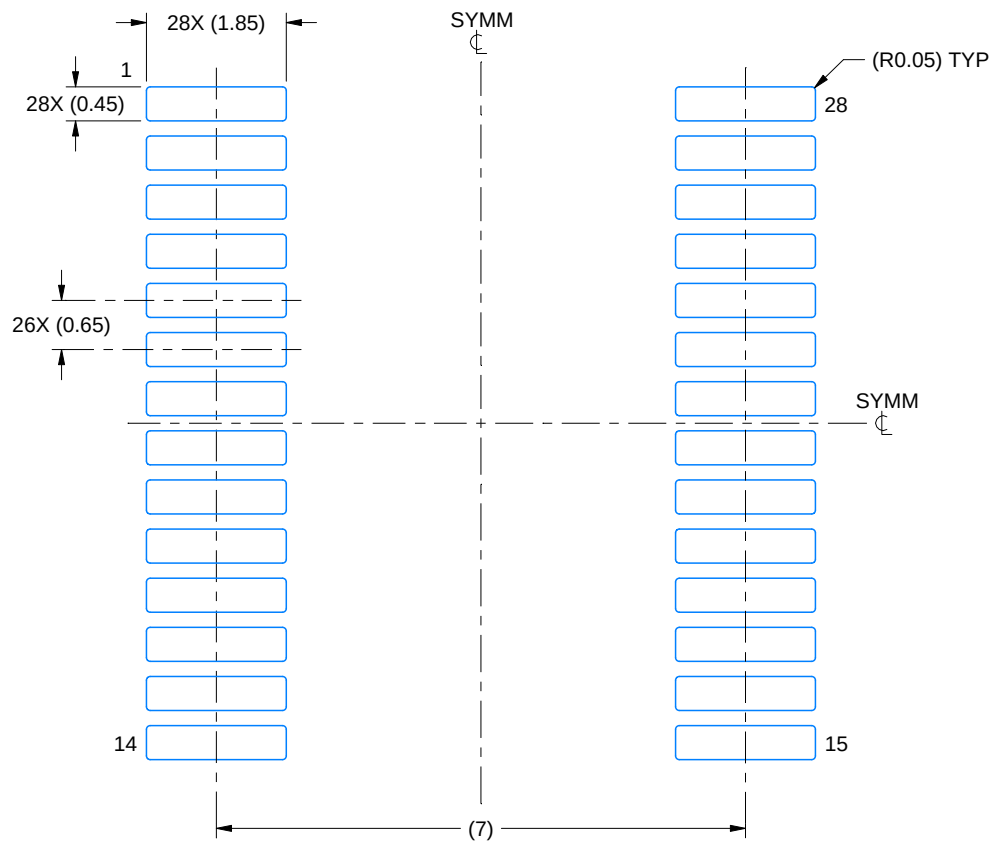
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

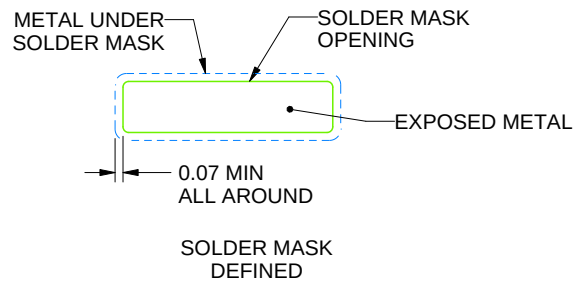
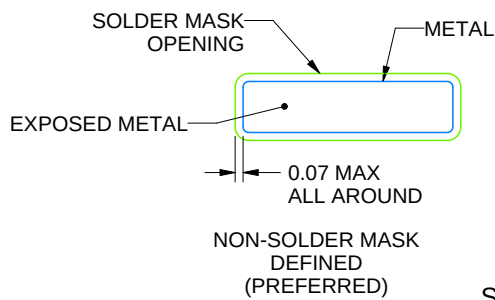
DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

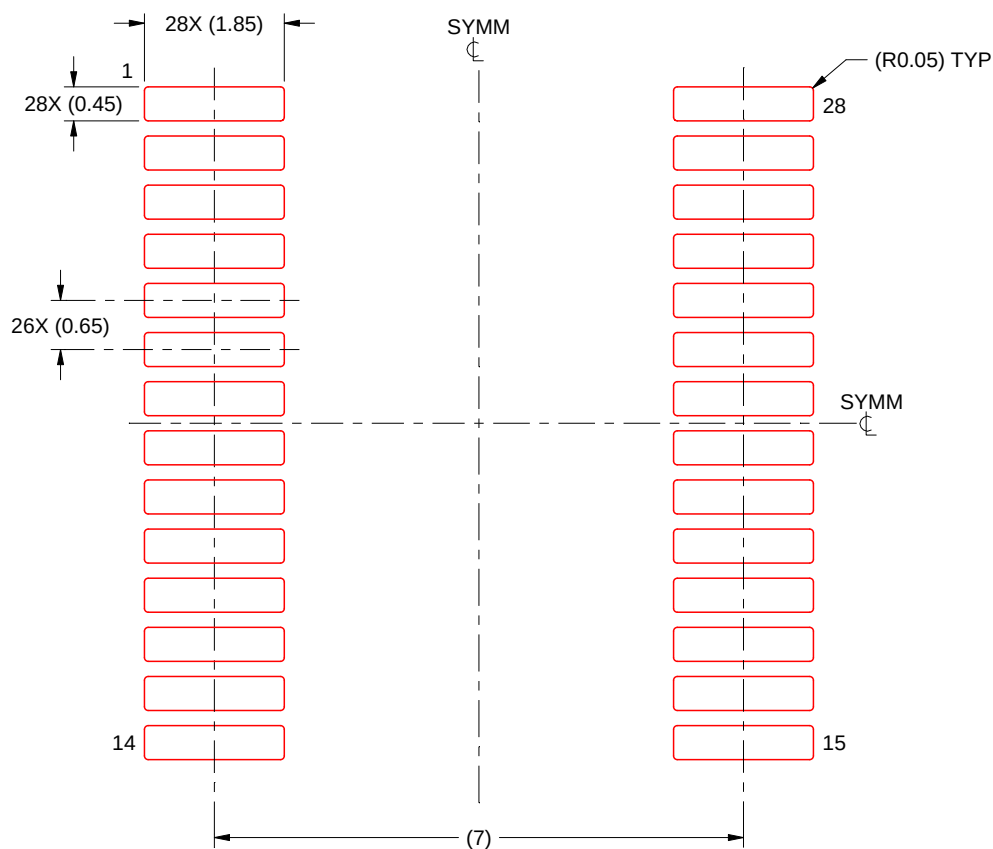
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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