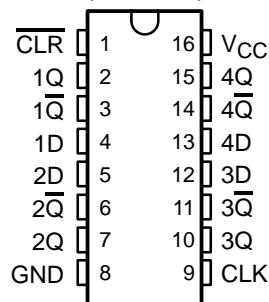


- Contains Four Flip-Flops With Double-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators

### description

This positive-edge-triggered flip-flop utilizes TTL circuitry to implement D-type flip-flop logic with a direct clear (CLR) input. Information at the data (D) inputs meeting setup-time requirements is transferred to outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

D, N, OR NS PACKAGE  
(TOP VIEW)



### ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74F175N	SN74F175N
	SOIC – D	Tube	SN74F175D	F175
		Tape and reel	SN74F175DR	
	SOP – NS	Tape and reel	SN74F175NSR	74F175

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

### FUNCTION TABLE

INPUTS			OUTPUTS	
CLR	CLK	D	Q	$\bar{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	$Q_0$	$\bar{Q}_0$



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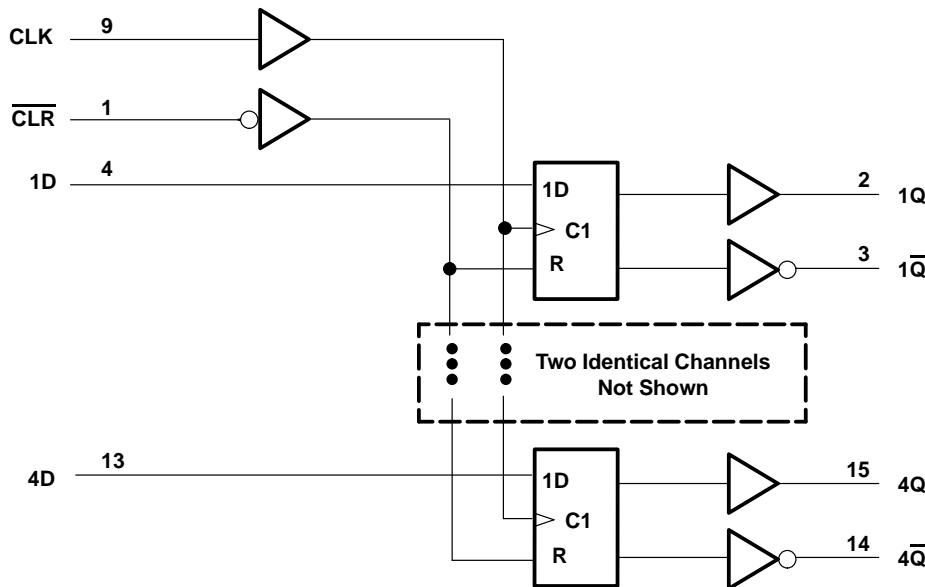
# **SN74F175**

## **QUADRUPLE D-TYPE FLIP-FLOP**

### **WITH CLEAR**

SDFS058B - D293, MARCH 1987 - REVISED MAY 2002

## logic diagram (positive logic)



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input voltage ratings may be exceeded if the input current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JEDEC 51-7.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>IK</sub>	Input clamp current			-18	mA
I <sub>OH</sub>	High-level output current			-1	mA
I <sub>OL</sub>	Low-level output current			20	mA
T <sub>A</sub>	Operating free-air temperature	0		70	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74F175  
QUADRUPLE D-TYPE FLIP-FLOP  
WITH CLEAR

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{IK}$	$V_{CC} = 4.5 \text{ V}$ , $I_I = -18 \text{ mA}$			-1.2	V
$V_{OH}$	$V_{CC} = 4.5 \text{ V}$ , $I_{OH} = -1 \text{ mA}$	2.5	3.4		V
	$V_{CC} = 4.75 \text{ V}$ , $I_{OH} = -1 \text{ mA}$	2.7			
$V_{OL}$	$V_{CC} = 4.5 \text{ V}$ , $I_{OL} = 20 \text{ mA}$	0.3	0.5		V
$I_I$	$V_{CC} = 5.5 \text{ V}$ , $V_I = 7 \text{ V}$			0.1	mA
$I_{IH}$	$V_{CC} = 5.5 \text{ V}$ , $V_I = 2.7 \text{ V}$			20	$\mu\text{A}$
$I_{IL}$	$V_{CC} = 5.5 \text{ V}$ , $V_I = 0.5 \text{ V}$			-0.6	mA
$I_{OS}^{\ddagger}$	$V_{CC} = 5.5 \text{ V}$ , $V_O = 0$	-60		-150	mA
$I_{CC}$	$V_{CC} = 5.5 \text{ V}$ , See Note 4	22.5	34		mA

† All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 4:  $I_{CC}$  is measured with outputs open, with 4.5 V applied to all data inputs after a momentary ground, followed by 4.5 V applied to CLK.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

		$V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$	MIN	MAX	UNIT
		MIN	MAX		
$f_{clock}$	Clock frequency	100	100		MHz
$t_w$	Pulse duration	CLK high	4	4	ns
		CLK low	5	5	
		CLR low	5	5	
$t_{su}$	Setup time, data before CLK↑	High or low	3	3	ns
	Setup time, inactive state, data before CLK↑\$	CLR high	5	5	
$t_h$	Hold time, data after CLK↑	High or low	1	1	ns

\$ Inactive-state setup time also is referred to as recovery time.

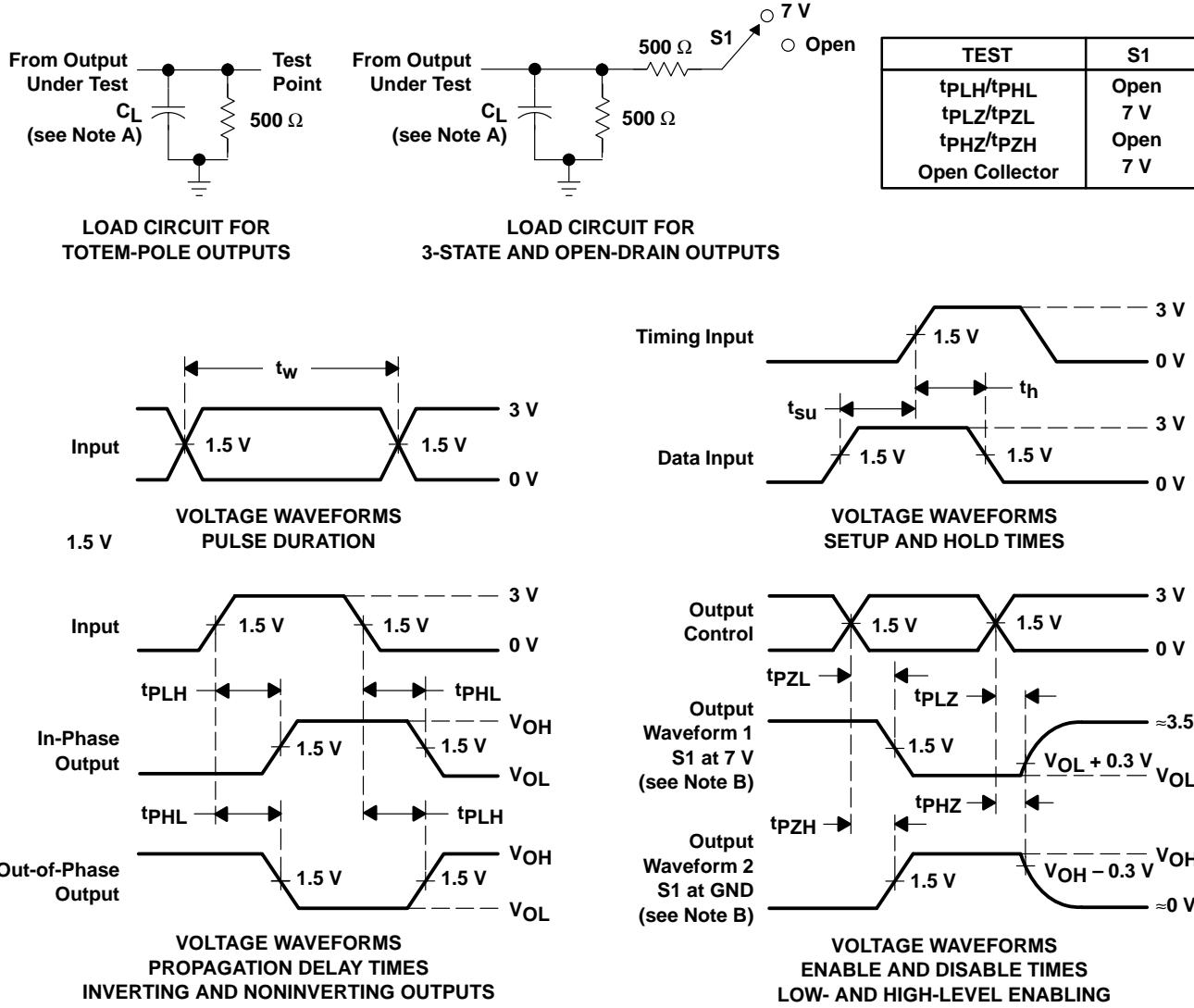
**switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$			UNIT	
			MIN	TYP	MAX		
$f_{max}$			100	140		100	MHz
$t_{PLH}$	CLK	Q or $\bar{Q}$	3.2	4.6	6.5	3.2	ns
			3.2	6.1	8.5	3.2	
$t_{PHL}$	CLR	$\bar{Q}$	3.2	6.1	8.5	3.2	ns
		Q	3.7	8.6	11.5	3.7	

**SN74F175**  
**QUADRUPLE D-TYPE FLIP-FLOP**  
**WITH CLEAR**

SDF5058B – D293, MARCH 1987 – REVISED MAY 2002

**PARAMETER MEASUREMENT INFORMATION**



NOTES:

- C<sub>L</sub> includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>r</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns, duty cycle = 50%.
- The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74F175D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F175DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F175DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F175DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F175DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F175DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F175N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74F175N3	OBsolete	PDIP	N	16		TBD	Call TI	Call TI
SN74F175NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74F175NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F175NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F175NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

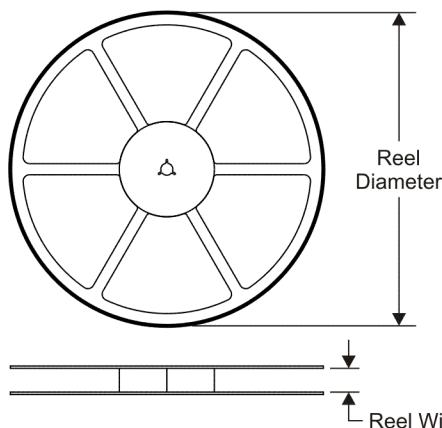
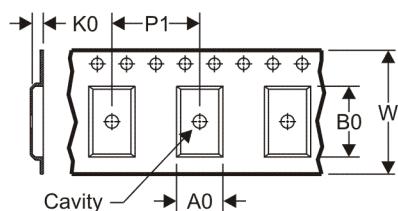
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

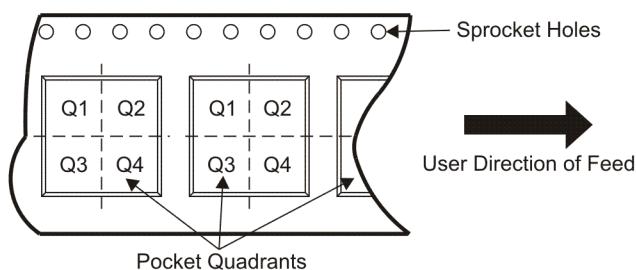
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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


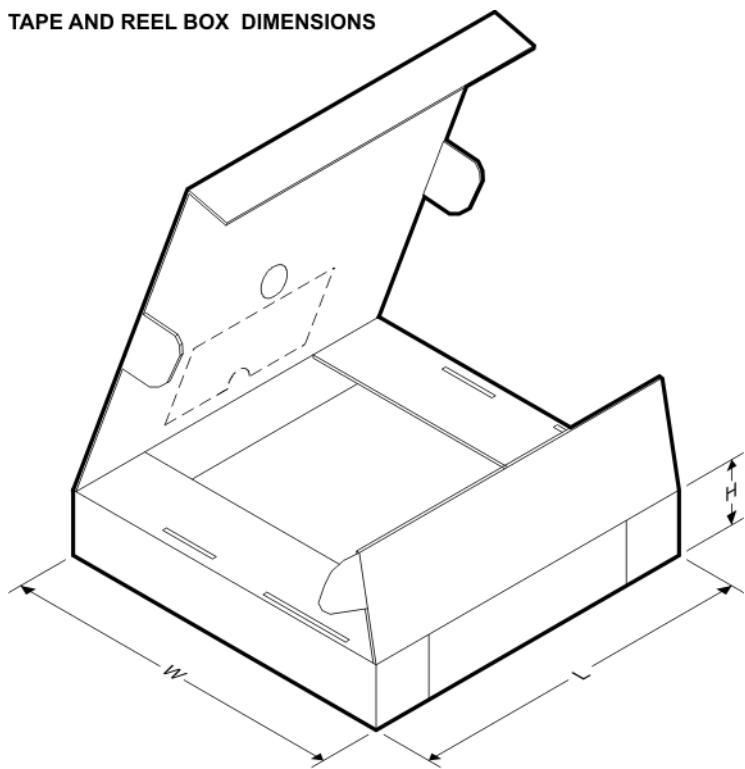
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F175DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74F175NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

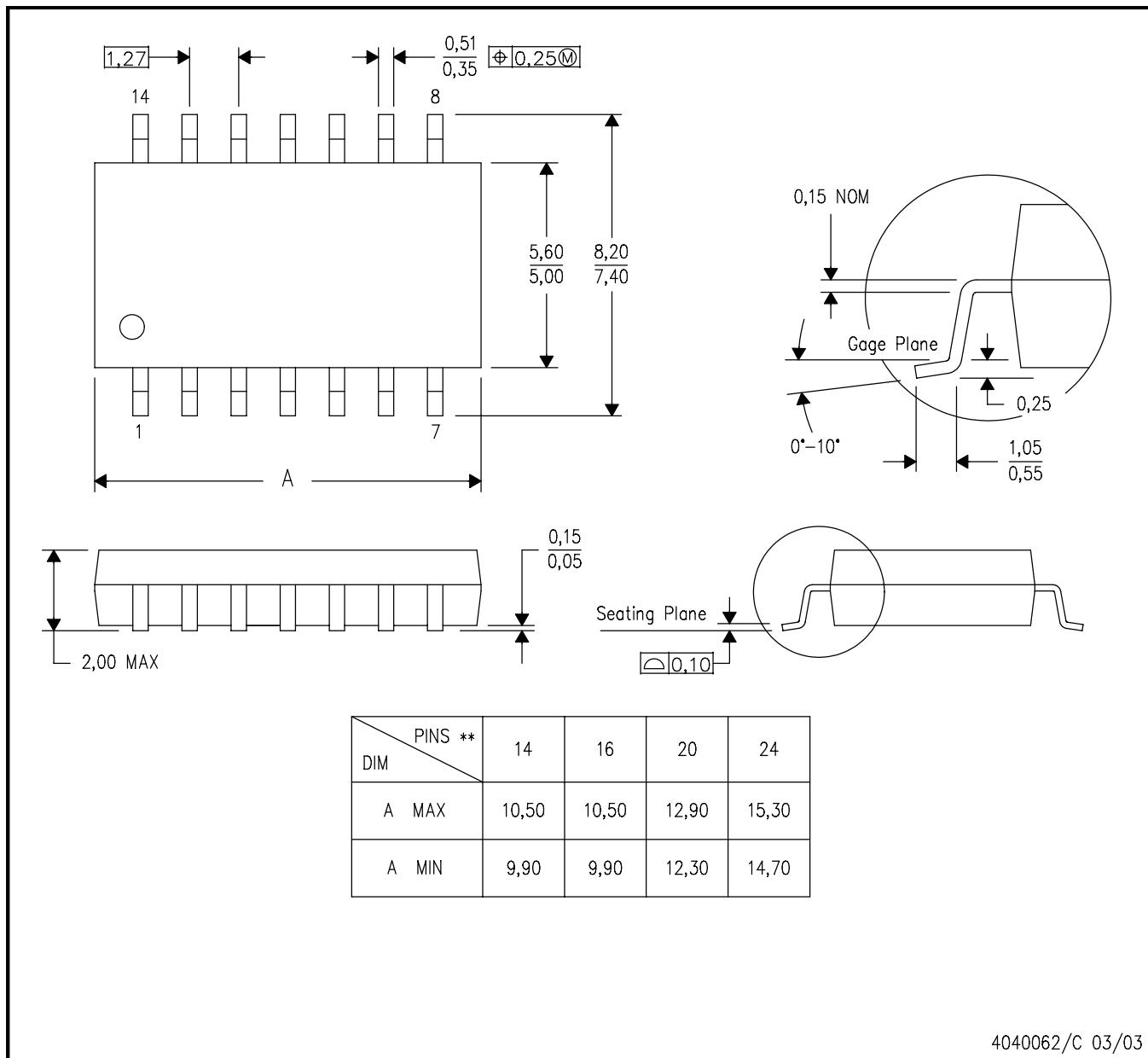
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F175DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74F175NSR	SO	NS	16	2000	346.0	346.0	33.0

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

## PLASTIC SMALL-OUTLINE PACKAGE

**14-PINS SHOWN**

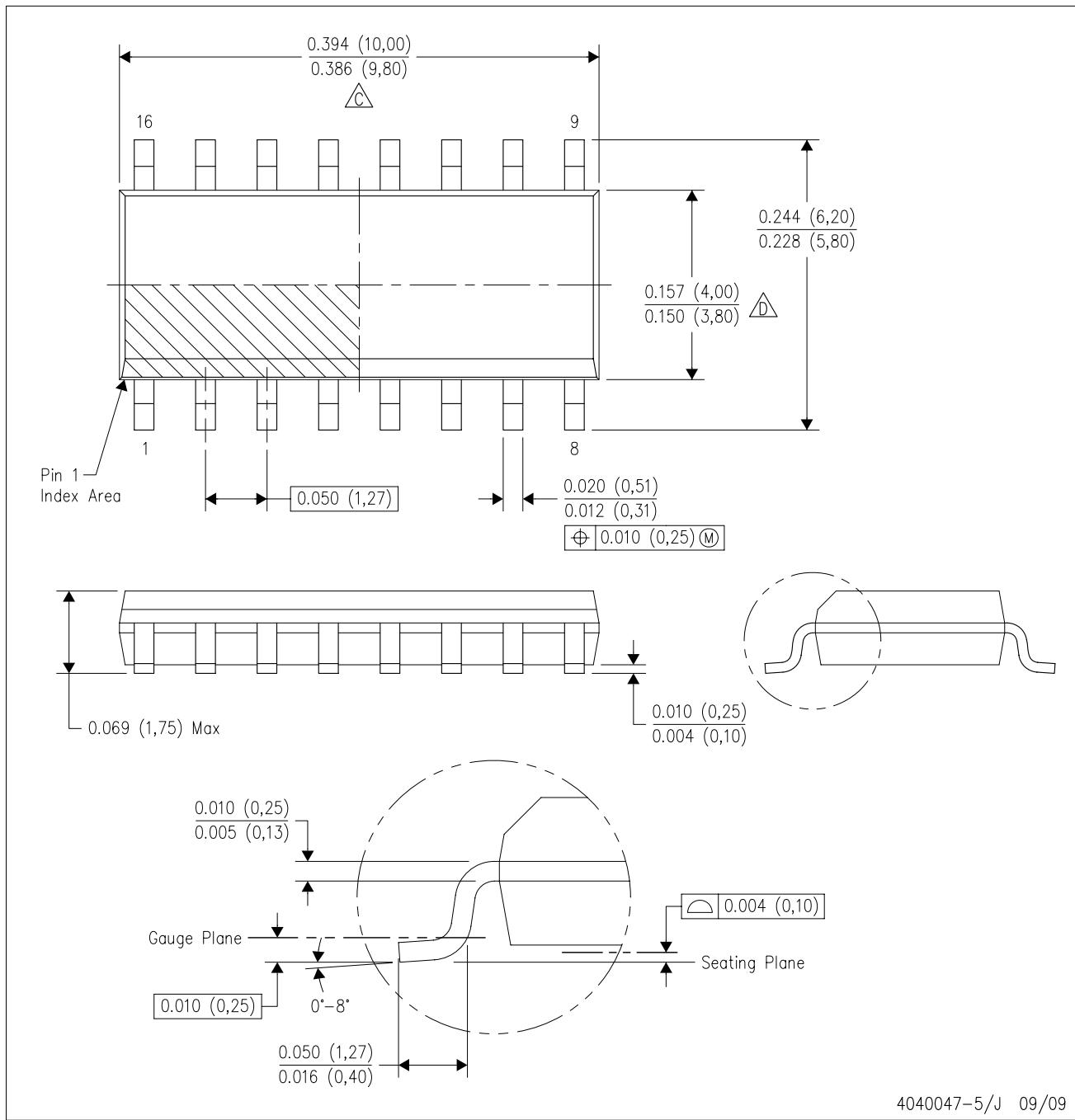


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.

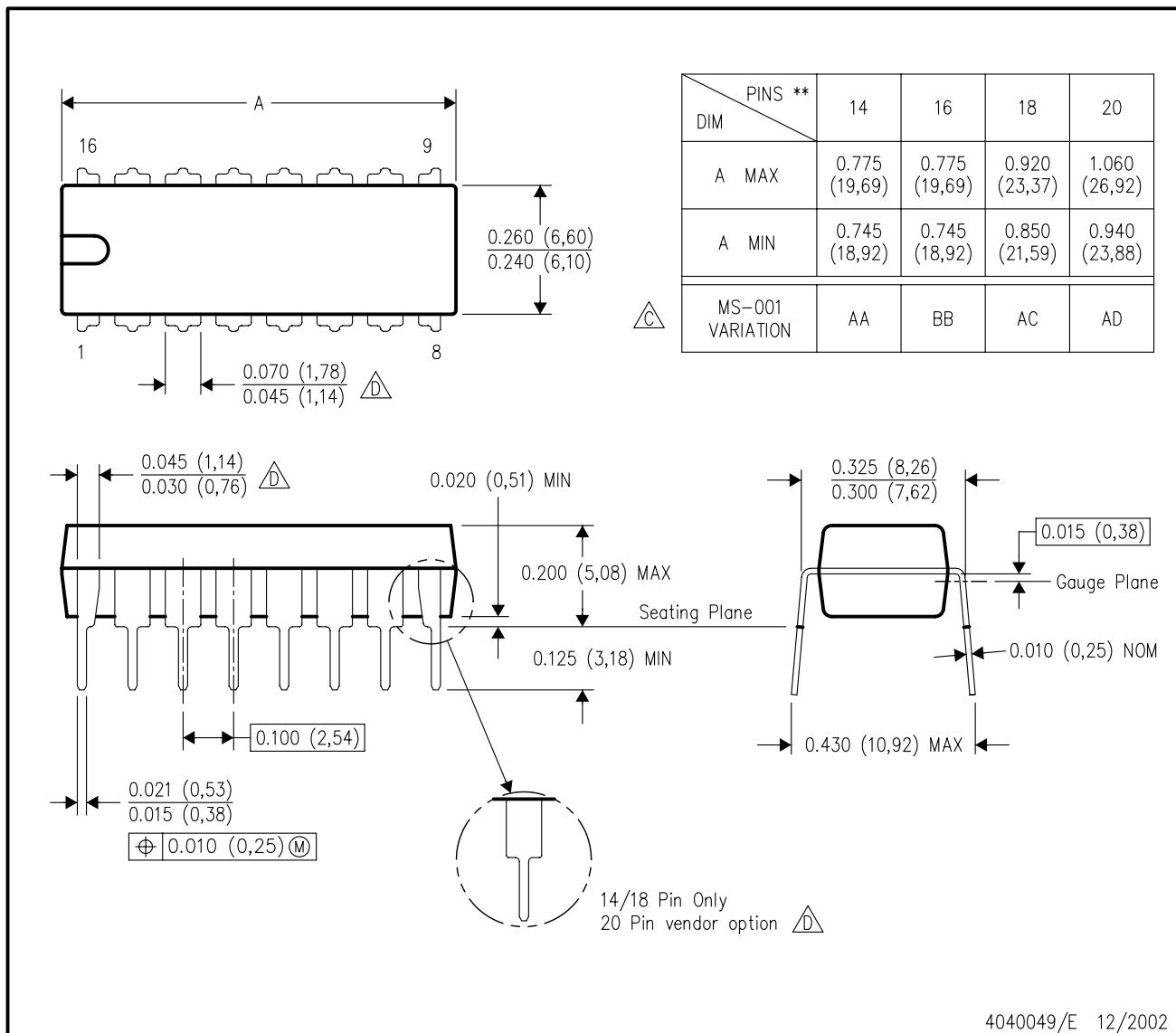
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.

E. Reference JEDEC MS-012 variation AC.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



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