



BUK98150-55

N-channel TrenchMOS logic level FET

19 March 2014

Product data sheet

1. General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

2. Features and benefits

- AEC Q101 compliant
- Electrostatically robust due to integrated protection diodes
- Low conduction losses due to low on-state resistance

3. Applications

- Automotive and general purpose power switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25 \text{ }^\circ\text{C}; T_j \leq 150 \text{ }^\circ\text{C}$		-	-	55	V
I_D	drain current	$T_{sp} = 25 \text{ }^\circ\text{C}$		-	-	5.5	A
P_{tot}	total power dissipation	$T_{sp} = 25 \text{ }^\circ\text{C}; \text{Fig. 4}$		-	-	8.3	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$		-	120	150	$\text{m}\Omega$
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 1.9 \text{ A}; V_{sup} \leq 25 \text{ V}; R_{GS} = 50 \Omega; V_{GS} = 5 \text{ V}; T_{j(init)} = 25 \text{ }^\circ\text{C}; \text{unclamped}$		-	-	15	mJ

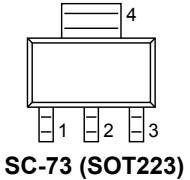
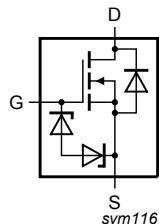


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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 SC-73 (SOT223)	 sym116
2	D	drain		
3	S	source		
4	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK98150-55	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223
BUK98150-55/CU	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK98150-55	
BUK98150-55/CU	915055

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25^\circ\text{C}$; $T_j \leq 150^\circ\text{C}$	-	55	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	55	V
V_{GS}	gate-source voltage		-10	10	V
P_{tot}	total power dissipation	$T_{sp} = 25^\circ\text{C}$; Fig. 4	-	8.3	W
I_D	drain current		-	5.5	A
	$T_{sp} = 100^\circ\text{C}$	-	3.5	A	

Symbol	Parameter	Conditions		Min	Max	Unit
I_{DM}	peak drain current	$T_{sp} = 25^\circ\text{C}$; pulsed		-	30	A
T_{stg}	storage temperature			-55	150	°C
T_j	junction temperature			-55	150	°C
Source-drain diode						
I_S	source current	$T_{sp} = 25^\circ\text{C}$		-	5.5	A
I_{SM}	peak source current	pulsed; $T_{sp} = 25^\circ\text{C}$		-	30	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 1.9 \text{ A}$; $V_{sup} \leq 25 \text{ V}$; $R_{GS} = 50 \Omega$; $V_{GS} = 5 \text{ V}$; $T_{j(init)} = 25^\circ\text{C}$; unclamped		-	15	mJ
Electrostatic discharge						
V_{esd}	electrostatic discharge voltage	HBM; $C = 100 \text{ pF}$; $R = 1.5 \text{ k}\Omega$		-	2	kV

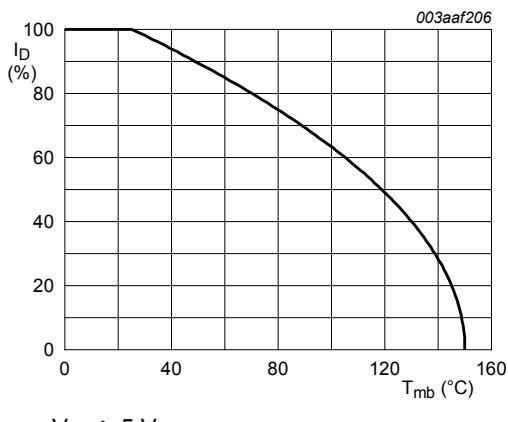


Fig. 1. Normalized continuous drain current as a function of mounting base temperature

$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100 \%$$

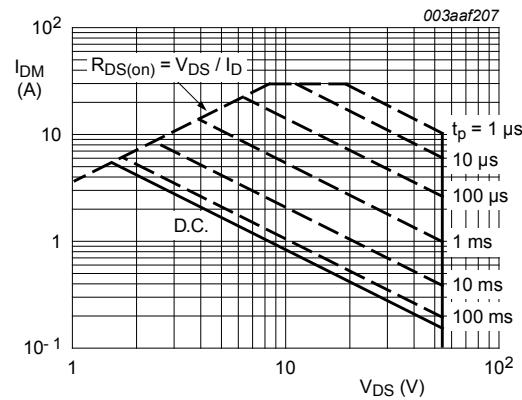


Fig. 2. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

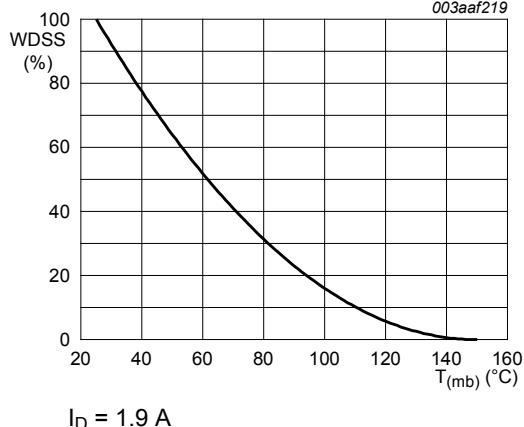


Fig. 3. Normalised drain-source non-repetitive avalanche energy rating; avalanche energy as a function of mounting base temperature

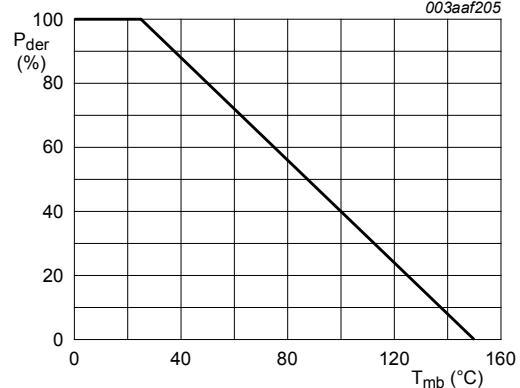


Fig. 4. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot}(25^\circ\text{C})} \times 100 \%$$

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	mounted on any printed-circuit board	-	12	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board	-	120	-	K/W

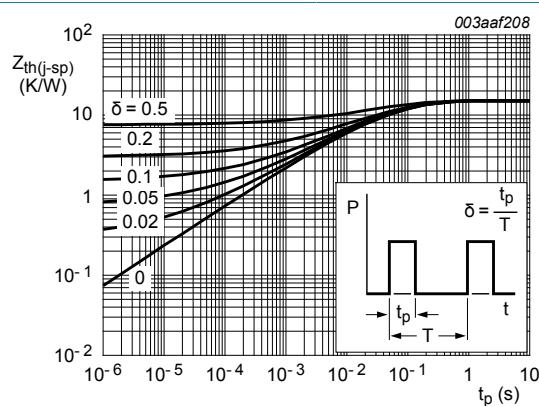


Fig. 5. Transient thermal impedance from junction to solder point as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$		55	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$		50	-	-	V
$V_{GS(\text{th})}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$		1	1.5	2	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C}$		-	-	2.3	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C}$		0.6	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$		-	0.05	10	μA
		$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$		-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$		-	0.02	1	μA
		$V_{GS} = -5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$		-	0.02	1	μA
		$V_{GS} = 5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$		-	-	5	μA
		$V_{GS} = -5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$		-	-	5	μA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 150 \text{ }^\circ\text{C}$		-	-	277	$\text{m}\Omega$
		$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$		-	120	150	$\text{m}\Omega$
$V_{(BR)GSS}$	gate-source breakdown voltage	$V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}; I_G = 1 \text{ mA}$		10	-	-	V
		$V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}; I_G = -1 \text{ mA}$		10	-	-	V
Dynamic characteristics							
C_{iss}	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}$		-	250	330	pF
C_{oss}	output capacitance			-	65	80	pF
C_{rss}	reverse transfer capacitance			-	35	50	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 6 \Omega; V_{GS} = 5 \text{ V}; R_{G(\text{ext})} = 10 \Omega; T_j = 25 \text{ }^\circ\text{C}; I_D = 5 \text{ A}$		-	11	17	ns
t_r	rise time			-	38	60	ns
$t_{d(off)}$	turn-off delay time			-	25	38	ns
t_f	fall time			-	20	38	ns
g_{fs}	transfer conductance	$V_{DS} = 25 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$		3	5	-	s
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 2 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$		-	0.85	1.1	V
t_{rr}	reverse recovery time	$I_S = 2 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = -10 \text{ V}; V_{DS} = 30 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$		-	43	-	ns
Q_r	recovered charge			-	0.16	-	μC

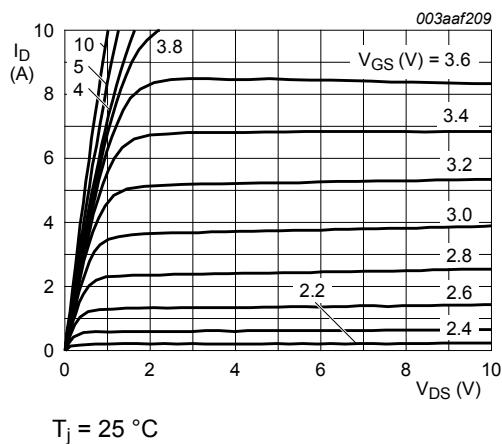


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

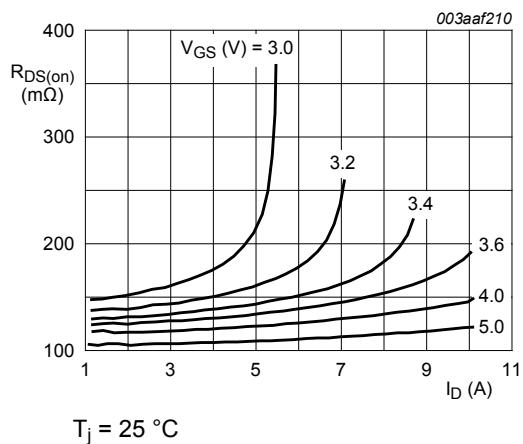


Fig. 7. Drain-source on-state resistance as a function of drain current; typical values

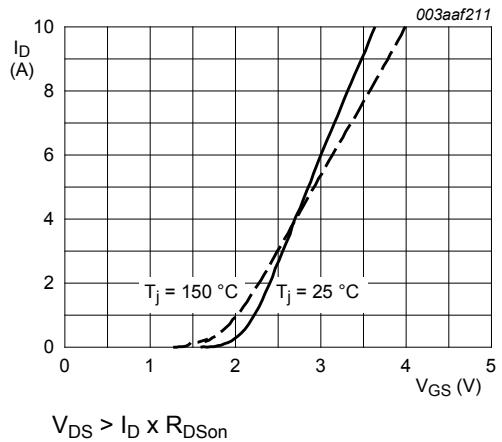


Fig. 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values

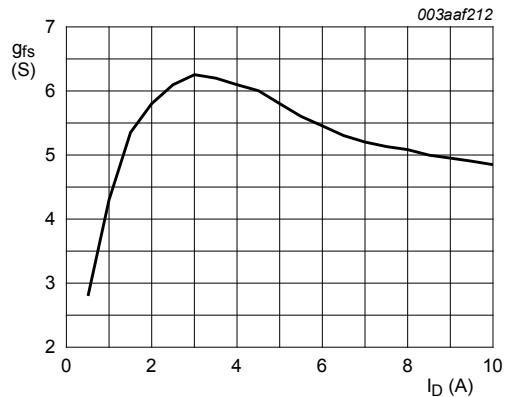


Fig. 9. Forward transconductance as a function of drain current; typical values

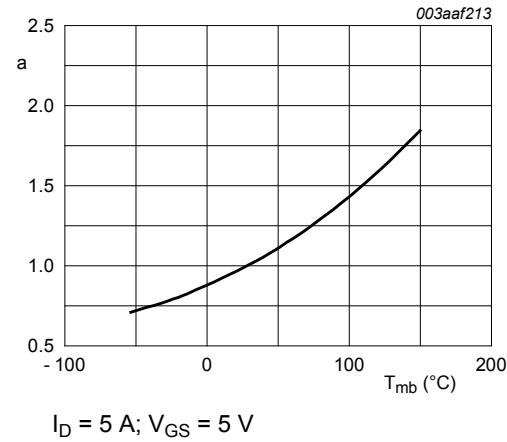


Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)25°C}}$$

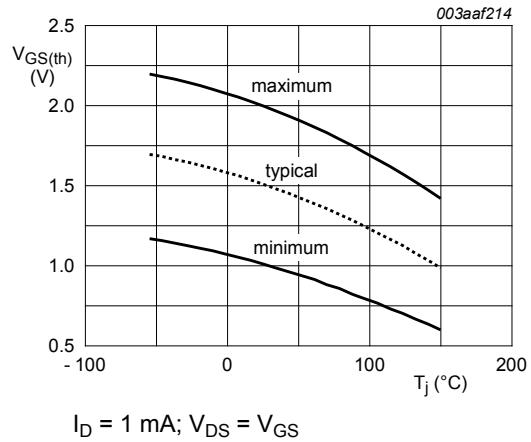


Fig. 11. Gate-source threshold voltage as a function of junction temperature

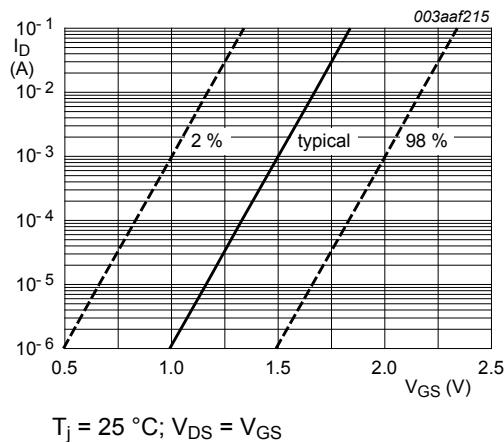


Fig. 12. Sub-threshold drain current as a function of gate-source voltage

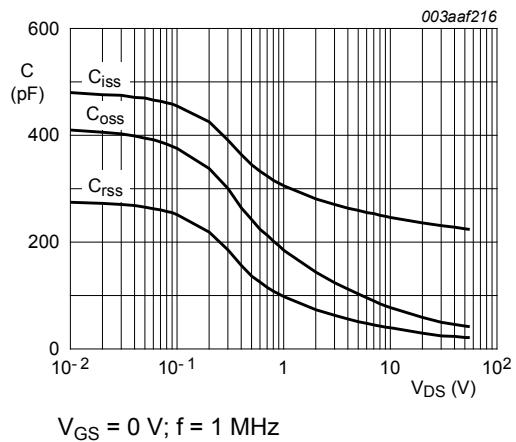


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

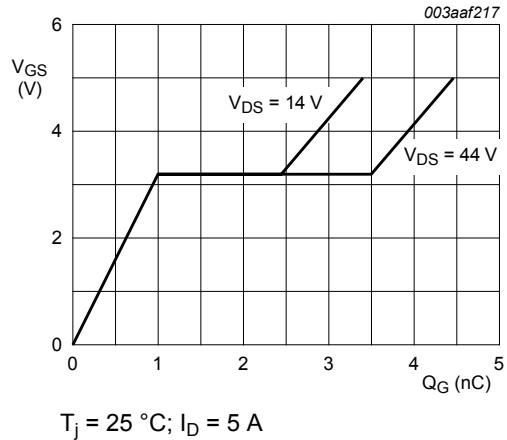


Fig. 14. Gate-source voltage as a function of gate charge; typical values

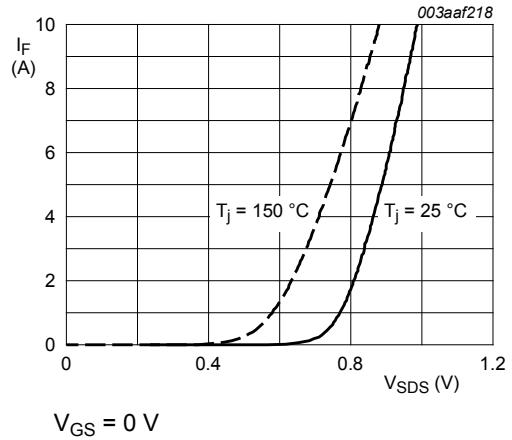
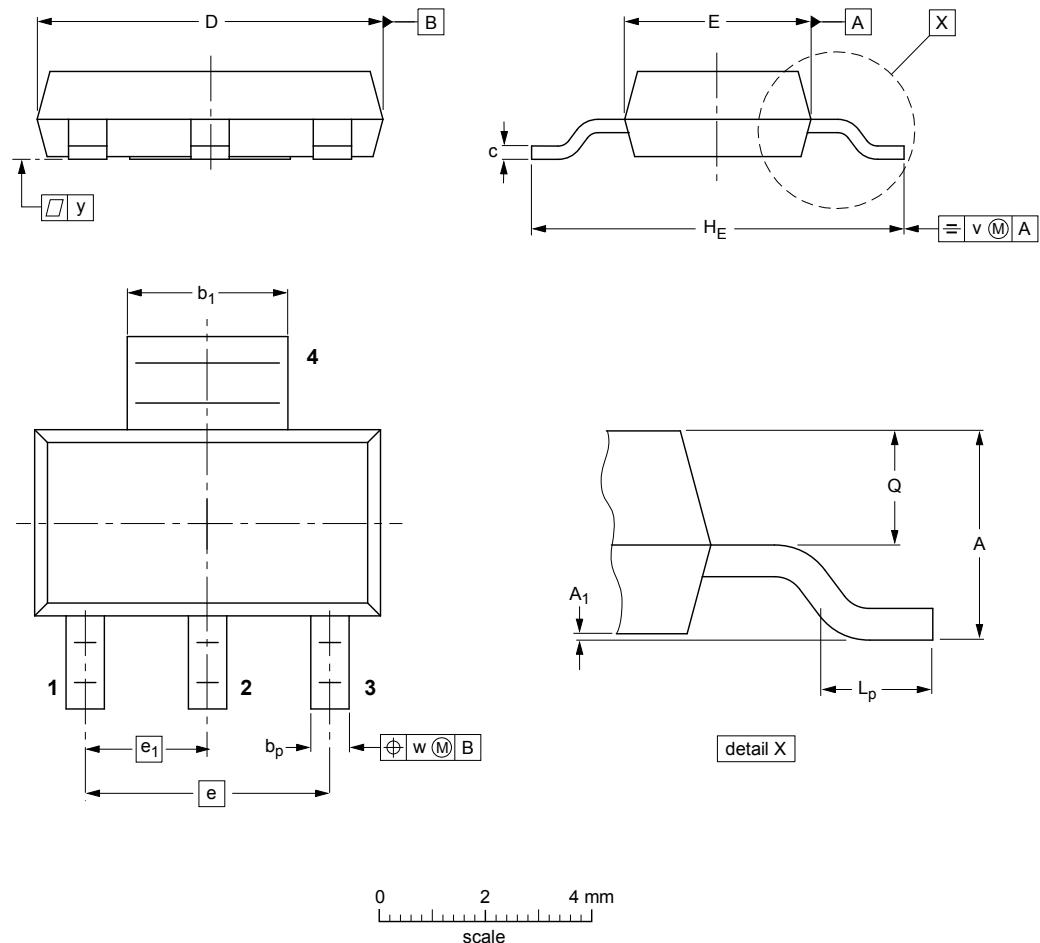


Fig. 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

11. Package outline

Plastic surface-mounted package with increased heatsink; 4 leads

SOT223



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.8	0.10	0.80	3.1	0.32	6.7	3.7	4.6	2.3	7.3	1.1	0.95	0.2	0.1	0.1
	1.5	0.01	0.60	2.9	0.22	6.3	3.3	4.6	2.3	6.7	0.7	0.85			

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA	SC-73		
SOT223						04-11-10 06-03-16

Fig. 16. Package outline SC-73 (SOT223)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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