

BUK98150-55

N-channel TrenchMOS logic level FET

19 March 2014

Product data sheet

1. General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

2. Features and benefits

- AEC Q101 compliant
- Electrostatically robust due to integrated protection diodes
- Low conduction losses due to low on-state resistance

3. Applications

- Automotive and general purpose power switching

4. Quick reference data

Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|--|---|-----|-----|-----|------------|
| V_{DS} | drain-source voltage | $T_j \geq 25\text{ }^{\circ}\text{C}$; $T_j \leq 150\text{ }^{\circ}\text{C}$ | - | - | 55 | V |
| I_D | drain current | $T_{sp} = 25\text{ }^{\circ}\text{C}$ | - | - | 5.5 | A |
| P_{tot} | total power dissipation | $T_{sp} = 25\text{ }^{\circ}\text{C}$; Fig. 4 | - | - | 8.3 | W |
| Static characteristics | | | | | | |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 5\text{ V}$; $I_D = 5\text{ A}$; $T_j = 25\text{ }^{\circ}\text{C}$ | - | 120 | 150 | m Ω |
| Avalanche ruggedness | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D = 1.9\text{ A}$; $V_{sup} \leq 25\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 5\text{ V}$; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$; unclamped | - | - | 15 | mJ |

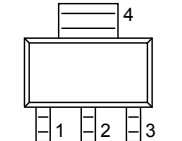
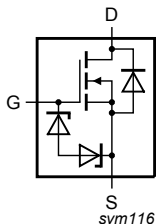


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5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-------------|---|---|
| 1 | G | gate |  SC-73 (SOT223) |  sym116 |
| 2 | D | drain | | |
| 3 | S | source | | |
| 4 | D | drain | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|----------------|---------|--|---------|
| | Name | Description | Version |
| BUK98150-55 | SC-73 | plastic surface-mounted package with increased heatsink; 4 leads | SOT223 |
| BUK98150-55/CU | SC-73 | plastic surface-mounted package with increased heatsink; 4 leads | SOT223 |

7. Marking

Table 4. Marking codes

| Type number | Marking code |
|----------------|--------------|
| BUK98150-55 | |
| BUK98150-55/CU | 915055 |

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|--|-----|-----|------|
| V_{DS} | drain-source voltage | $T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$ | - | 55 | V |
| V_{DGR} | drain-gate voltage | $R_{GS} = 20\text{ k}\Omega$ | - | 55 | V |
| V_{GS} | gate-source voltage | | -10 | 10 | V |
| P_{tot} | total power dissipation | $T_{sp} = 25\text{ °C}$; Fig. 4 | - | 8.3 | W |
| I_D | drain current | $T_{sp} = 25\text{ °C}$ | - | 5.5 | A |
| | | $T_{sp} = 100\text{ °C}$ | - | 3.5 | A |

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|-------------------------|--|---|--|-----|-----|--------------------|
| I_{DM} | peak drain current | $T_{sp} = 25\text{ }^{\circ}\text{C}$; pulsed | | - | 30 | A |
| T_{stg} | storage temperature | | | -55 | 150 | $^{\circ}\text{C}$ |
| T_j | junction temperature | | | -55 | 150 | $^{\circ}\text{C}$ |
| Source-drain diode | | | | | | |
| I_S | source current | $T_{sp} = 25\text{ }^{\circ}\text{C}$ | | - | 5.5 | A |
| I_{SM} | peak source current | pulsed; $T_{sp} = 25\text{ }^{\circ}\text{C}$ | | - | 30 | A |
| Avalanche ruggedness | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D = 1.9\text{ A}$; $V_{sup} \leq 25\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 5\text{ V}$; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; unclamped | | - | 15 | mJ |
| Electrostatic discharge | | | | | | |
| V_{esd} | electrostatic discharge voltage | HBM; $C = 100\text{ pF}$; $R = 1.5\text{ k}\Omega$ | | - | 2 | kV |

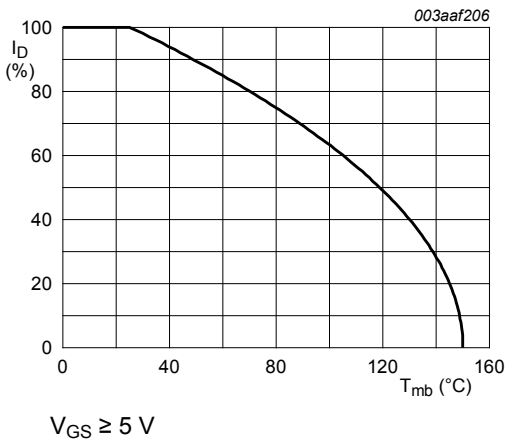


Fig. 1. Normalized continuous drain current as a function of mounting base temperature

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100\%$$

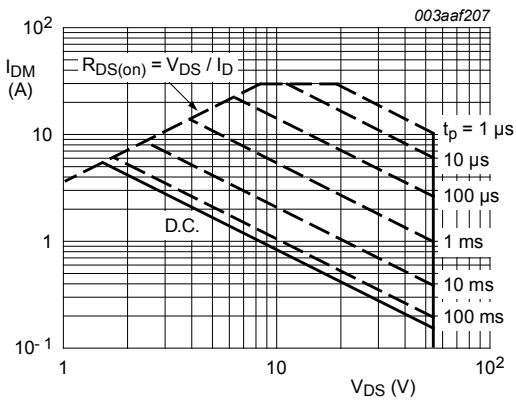
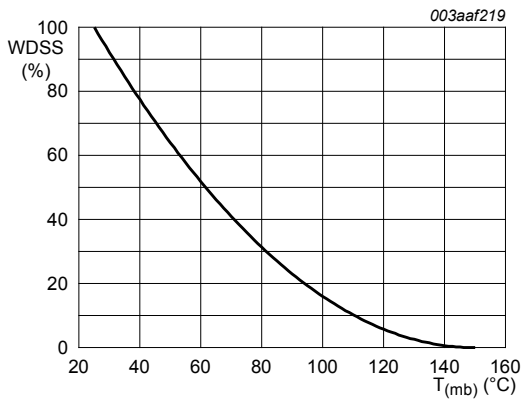


Fig. 2. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



$I_D = 1.9\text{ A}$

Fig. 3. Normalised drain-source non-repetitive avalanche energy rating; avalanche energy as a function of mounting base temperature

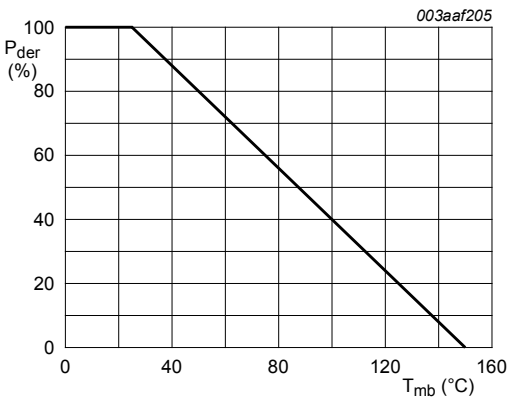


Fig. 4. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|--|--------------------------------------|-----|-----|-----|------|
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | mounted on any printed-circuit board | - | 12 | 15 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | mounted on a printed-circuit board | - | 120 | - | K/W |

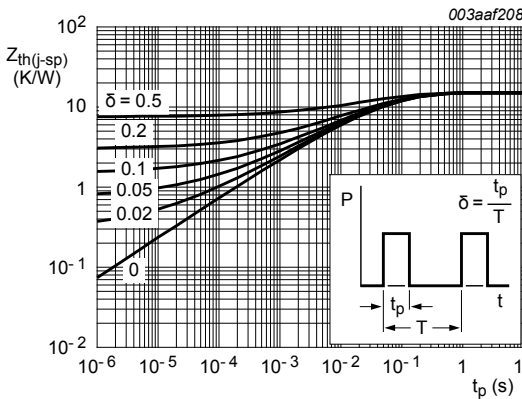


Fig. 5. Transient thermal impedance from junction to solder point as a function of pulse duration

10. Characteristics

Table 7. Characteristics

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|-------------------------|----------------------------------|---|--|-----|------|-----|------|
| Static characteristics | | | | | | | |
| V _{(BR)DSS} | drain-source breakdown voltage | I _D = 0.25 mA; V _{GS} = 0 V; T _j = 25 °C | | 55 | - | - | V |
| | | I _D = 0.25 mA; V _{GS} = 0 V; T _j = -55 °C | | 50 | - | - | V |
| V _{GS(th)} | gate-source threshold voltage | I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C | | 1 | 1.5 | 2 | V |
| | | I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C | | - | - | 2.3 | V |
| | | I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 150 °C | | 0.6 | - | - | V |
| I _{DSS} | drain leakage current | V _{DS} = 55 V; V _{GS} = 0 V; T _j = 25 °C | | - | 0.05 | 10 | μA |
| | | V _{DS} = 55 V; V _{GS} = 0 V; T _j = 150 °C | | - | - | 100 | μA |
| I _{GSS} | gate leakage current | V _{GS} = 5 V; V _{DS} = 0 V; T _j = 25 °C | | - | 0.02 | 1 | μA |
| | | V _{GS} = -5 V; V _{DS} = 0 V; T _j = 25 °C | | - | 0.02 | 1 | μA |
| | | V _{GS} = 5 V; V _{DS} = 0 V; T _j = 150 °C | | - | - | 5 | μA |
| | | V _{GS} = -5 V; V _{DS} = 0 V; T _j = 150 °C | | - | - | 5 | μA |
| R _{DSon} | drain-source on-state resistance | V _{GS} = 5 V; I _D = 5 A; T _j = 150 °C | | - | - | 277 | mΩ |
| | | V _{GS} = 5 V; I _D = 5 A; T _j = 25 °C | | - | 120 | 150 | mΩ |
| V _{(BR)GSS} | gate-source breakdown voltage | V _{DS} = 0 V; T _j = 25 °C; I _G = 1 mA | | 10 | - | - | V |
| | | V _{DS} = 0 V; T _j = 25 °C; I _G = -1 mA | | 10 | - | - | V |
| Dynamic characteristics | | | | | | | |
| C _{iss} | input capacitance | V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; T _j = 25 °C | | - | 250 | 330 | pF |
| C _{oss} | output capacitance | | | - | 65 | 80 | pF |
| C _{rss} | reverse transfer capacitance | | | - | 35 | 50 | pF |
| t _{d(on)} | turn-on delay time | V _{DS} = 30 V; R _L = 6 Ω; V _{GS} = 5 V; R _{G(ext)} = 10 Ω; T _j = 25 °C; I _D = 5 A | | - | 11 | 17 | ns |
| t _r | rise time | | | - | 38 | 60 | ns |
| t _{d(off)} | turn-off delay time | | | - | 25 | 38 | ns |
| t _f | fall time | | | - | 20 | 38 | ns |
| g _{fs} | transfer conductance | V _{DS} = 25 V; I _D = 5 A; T _j = 25 °C | | 3 | 5 | - | S |
| Source-drain diode | | | | | | | |
| V _{SD} | source-drain voltage | I _S = 2 A; V _{GS} = 0 V; T _j = 25 °C | | - | 0.85 | 1.1 | V |
| t _{rr} | reverse recovery time | I _S = 2 A; dI _S /dt = -100 A/μs; V _{GS} = -10 V; V _{DS} = 30 V; T _j = 25 °C | | - | 43 | - | ns |
| Q _r | recovered charge | | | - | 0.16 | - | μC |

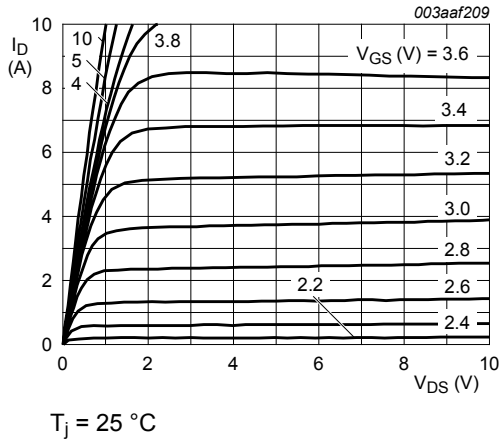


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

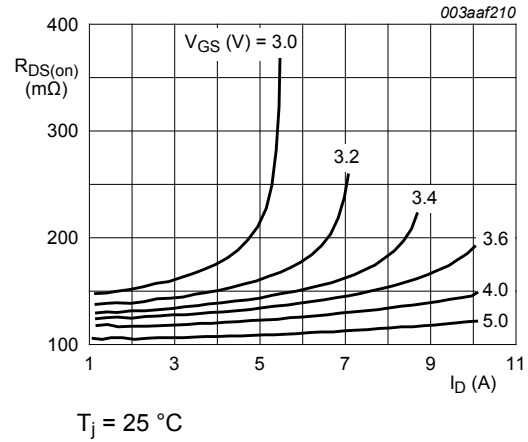


Fig. 7. Drain-source on-state resistance as a function of drain current; typical values

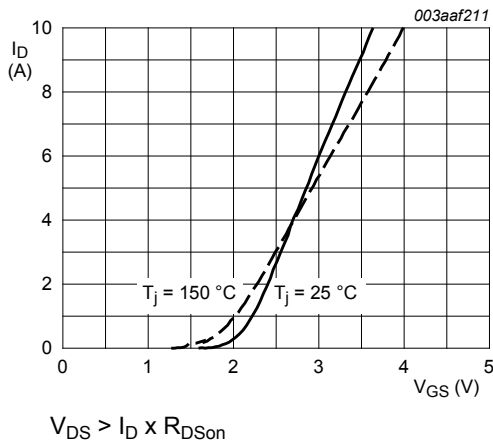


Fig. 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values

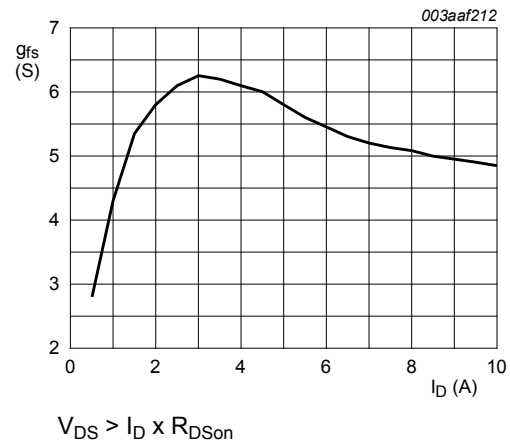


Fig. 9. Forward transconductance as a function of drain current; typical values

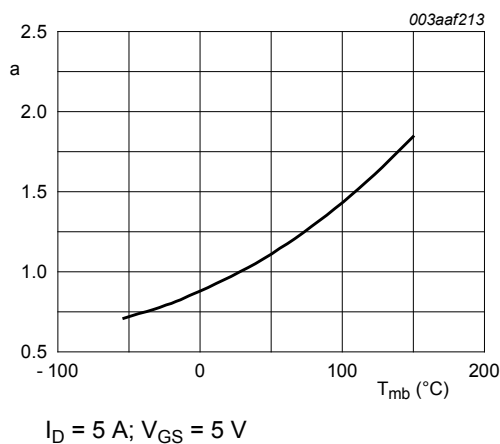


Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)25^{\circ}\text{C}}}$$

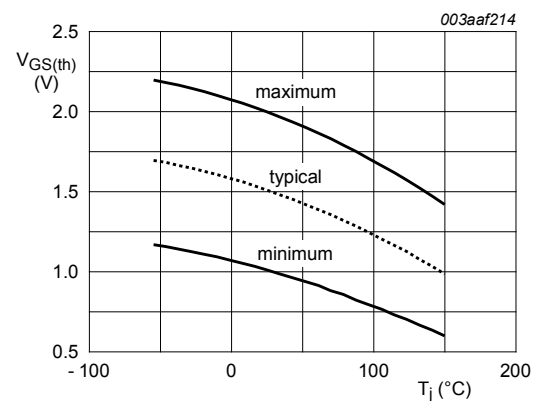


Fig. 11. Gate-source threshold voltage as a function of junction temperature

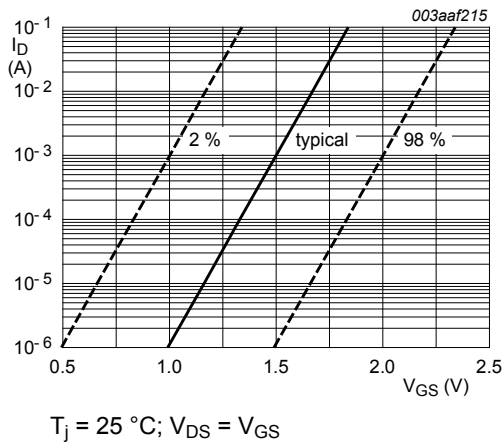


Fig. 12. Sub-threshold drain current as a function of gate-source voltage

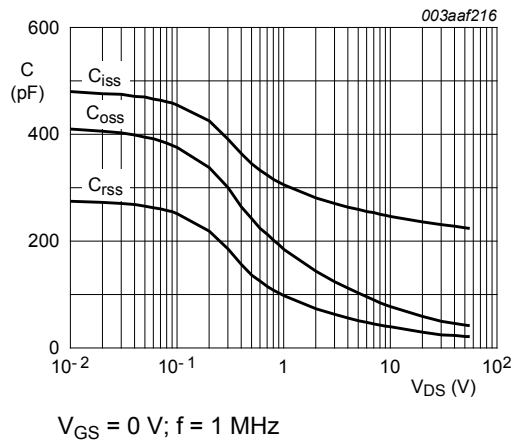


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

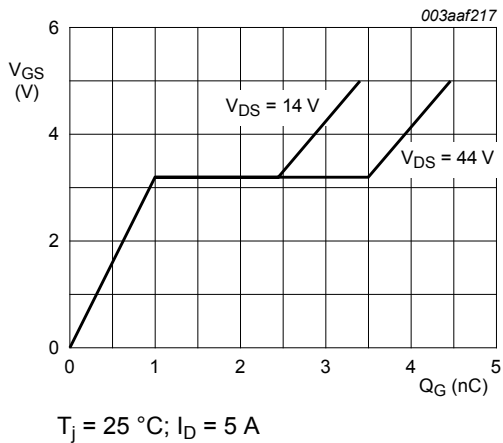


Fig. 14. Gate-source voltage as a function of gate charge; typical values

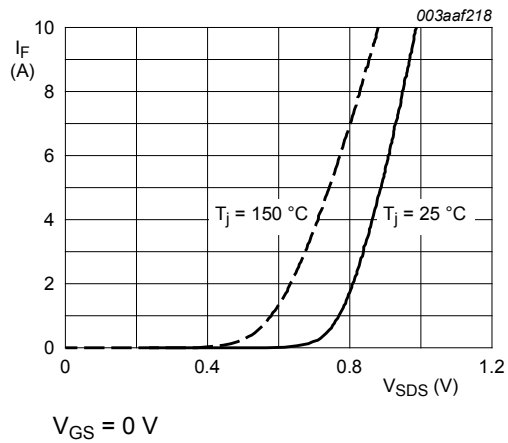


Fig. 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

11. Package outline

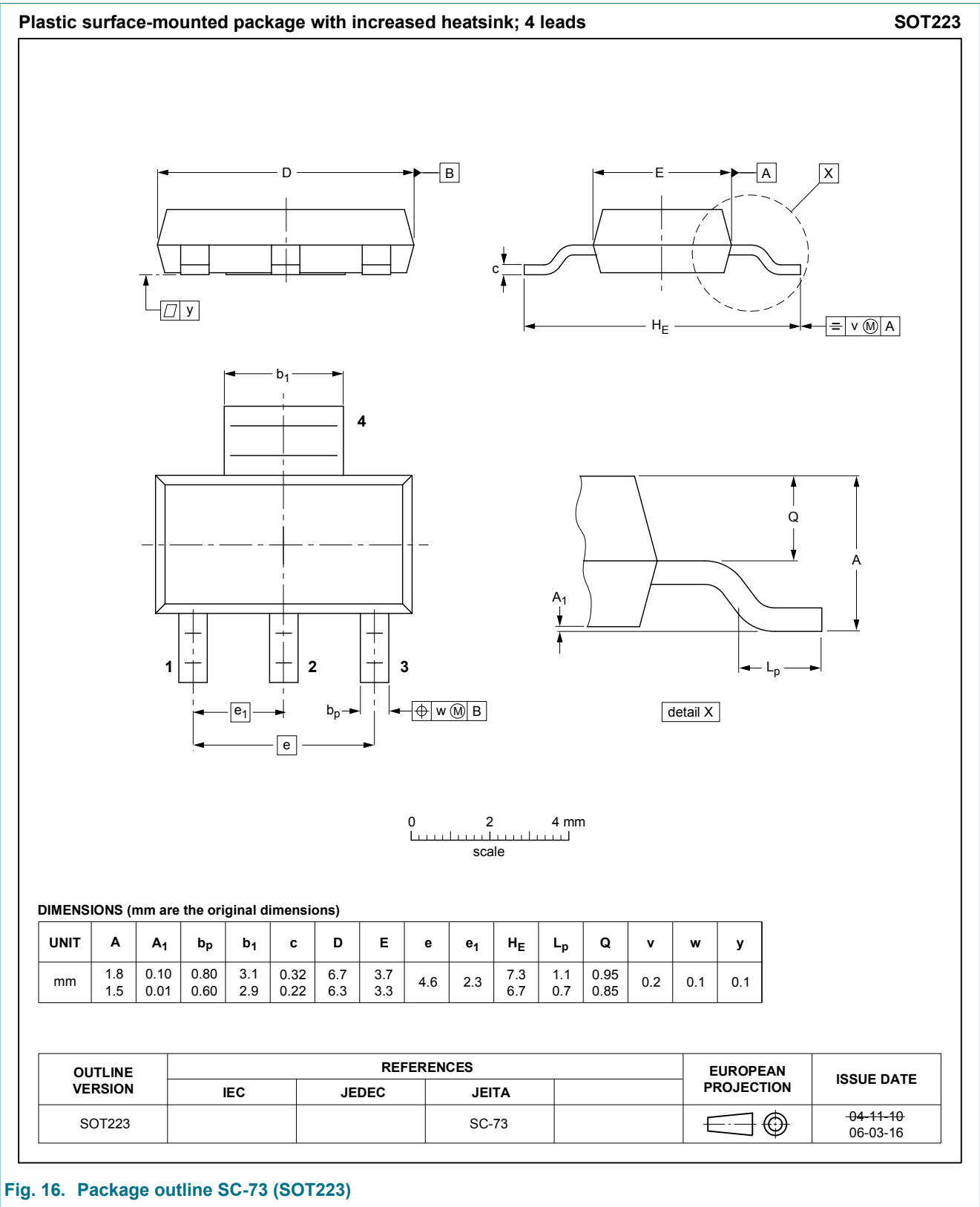


Fig. 16. Package outline SC-73 (SOT223)

12. Legal information

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|--------------------------------|--------------------|---|
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