DS33Z44
Quad Ethernet Mapper

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GENERAL DESCRIPTION

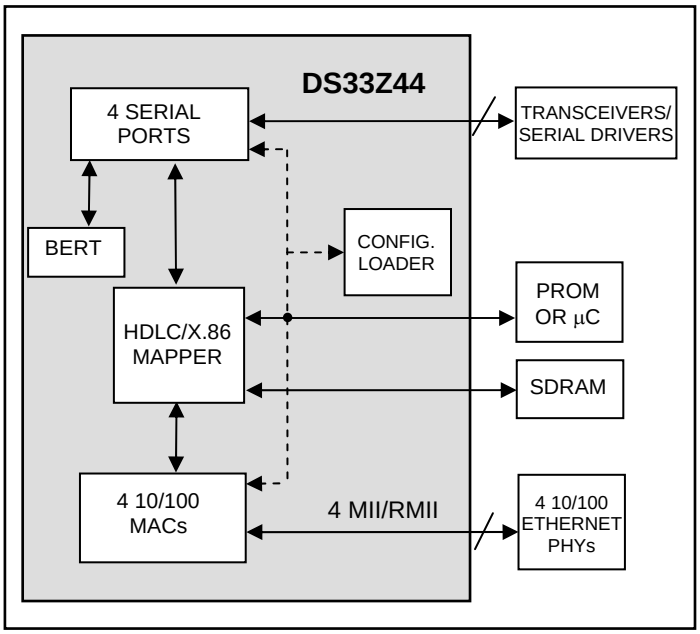
The DS33Z44 extends four 10/100 Ethernet LAN segments by encapsulating MAC frames in HDLC or X.86 (LAPS) for transmission over four PDH/TDM data streams. The serial links support bidirectional synchronous interconnect up to 52Mbps over xDSL, T1/E1/J1, T3/E3, V.35/Optical, OC-1/EC-1, or SONET/SDH Tributary.

The device performs store-and-forward of packets with full wire-speed transport capability. The built-in Committed Information Rate (CIR) controllers provide fractional bandwidth allocation up to the line rate in increments of 512kbps. The DS33Z44 can operate with an inexpensive external processor, EEPROM or in a stand-alone hardware mode.

APPLICATIONS

Transparent LAN Service
LAN Extension
Ethernet Delivery Over T1/E1/J1, T3/E3, OC-1/EC-1, G.SHDSL, or HDSL2/4

FUNCTIONAL DIAGRAM



FEATURES

- Four 10/100 IEEE 802.3 Ethernet MACs (MII and RMII) Half/Full-Duplex with Automatic Flow Control
- Four 52Mbps Synchronous TDM Serial Ports with Independent Transmit and Receive Timing
- HDLC/LAPS Encapsulation with Programmable FCS and Interframe Fill
- Committed Information Rate Controllers Provide Fractional Allocations in 512kbps Increments
- Programmable BERT for Serial (TDM) Interfaces
- External 16MB, 100MHz SDRAM Buffering
- Parallel Microprocessor Interface
- SPI Interface and Hardware Mode for Operation Without a Host Processor
- 1.8V Operation with 3.3V Tolerant I/O
- IEEE 1149.1 JTAG Support

Features Continued on Page 9.

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS33Z44	-40°C to +85°C	256 CSBGA

Go to www.maxim-ic.com/telecom for a complete list of Telecommunications data sheets, evaluation kits, application notes, and software downloads.

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: **www.maxim-ic.com/errata**.*

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1 DESCRIPTION

The DS33Z44 provides interconnection and mapping functionality between Ethernet Packet Systems and WAN Time-Division Multiplexed (TDM) systems such as T1/E1/J1, HDSL, and T3/E3. The device is composed of four 10/100 Ethernet MACs, a packet arbiter, four committed information rate controllers (CIRs), HDLC/X.86 (LAPS) mappers, an SDRAM interface, control ports, and a bit error-rate tester (BERT). The packet interface consists of four Ethernet interfaces using several physical layer protocols. The Ethernet interfaces can be configured for 10Mbps or 100Mbps service. The DS33Z44 encapsulates Ethernet traffic with HDLC or X.86 (LAPS) to be transmitted over the WAN interface. The WAN interfaces also receive encapsulated Ethernet packets and transmit the extracted packets over the Ethernet ports. The WAN physical interfaces support serial data streams up to 52Mbps. The WAN interfaces can be connected to the Dallas Semiconductor/Maxim T1/E1/J1 framers, line interface units (LIUs), and single-chip transceivers (SCTs). The WAN interfaces can also be connected to the Dallas Semiconductor/Maxim T3/E3/STS-1 framers, LIUs, and SCTs to provide T3, E3, and STS1 connectivity. Refer to *Application Note 3411: DS33Z11—Ethernet LAN to Unframed T1/E1 WAN Bridge* for an example of a complete LAN-to-WAN solution.

The DS33Z44 is controlled through an 8-bit microcontroller port. A serial EEPROM (SPI) interface and hardware mode are also included for applications without a host processor. The DS33Z44 has a 100MHz SDRAM controller and interfaces to a 32-bit wide 128Mb SDRAM. The SDRAM is used to buffer the data from the Ethernet and WAN ports for transport. The external SDRAM can accommodate up to 8192 frames with a maximum frame size of 2016 bytes.

Operation without an external host simplifies and reduces the cost of typical applications such as connectivity to T1/T3 and E1/E3 front ends. The DS33Z44 operates with a 1.8V core supply and 3.3V I/O supply.

2 FEATURE HIGHLIGHTS

2.1 General

- 256-pin CSBGA package
- 1.8V supply with 3.3V tolerant inputs and outputs
- IEEE 1149.1 JTAG boundary scan
- Software access to device ID and silicon revision
- Development support includes evaluation kit, driver source code, and reference designs

2.2 Serial Interfaces

- Support line speeds up to 52Mbps
- Support data enable and gapped clocking
- Support byte synchronization input and output for X.86 applications

2.3 HDLC

- Four HDLC controller engines
- Compatible with polled or interrupt driven environments
- Programmable FCS insertion and extraction
- Programmable FCS type
- Supports FCS error insertion
- Programmable packet size limits (minimum 64 bytes and maximum 2016 bytes)
- Supports bit stuffing/destuffing
- Selectable packet scrambling/descrambling ($X^{43}+1$)
- Separate FCS errored packet and aborted packet counts
- Programmable interframe fill for transmit HDLC

2.4 Committed Information Rate (CIR) Controllers

- Four CIR controllers limit transmission of data from the Ethernet Interfaces to the Serial Interfaces
- CIR granularity at 512kbps
- CIR Averaging for smoothing traffic peaks

2.5 X.86 Support

- Programmable X.86 address/control fields for transmit and receive
- Programmable 2-byte protocol (SAPI) field for transmit and receive
- 32 bit FCS
- Transmit Transparency processing–7E is replaced by 7D, 5E
- Transmit Transparency processing–7D replaced by 7D, 5D
- Receive rate adaptation (7D, DD) is deleted.
- Receive Transparency processing–7D, 5E is replaced by 7D
- Receive Transparency processing–7D, 5D is replaced by 7D
- Receive Abort Sequence the LAPS packet is dropped if 7D7E is detect
- Self-synchronizing $X^{43}+1$ payload scrambling.
- Frame indication due to bad address/control/SAPI, FCS error, abort sequence or frame size longer than preset max

2.6 SDRAM Interface

- Interface for 128-Mb, 32-bit-wide SDRAM
- SDRAM Interface speed up to 100MHz
- Auto refresh timing
- Automatic precharge
- Master clock provided to the SDRAM
- No external components required for SDRAM connectivity

2.7 MAC Interfaces

- Four MAC ports with standard MII (less TX_ER) or RMII
- 10Mbps and 100 Mbps data rates
- Configurable DTE or DCE modes
- Facilitates auto-negotiation by host microprocessor
- Programmable half and full-duplex modes
- Flow control for both half-duplex (back-pressure) and full-duplex (PAUSE) modes
- Programmable maximum MAC frame size up to 2016 bytes
- Minimum MAC frame size: 64 bytes
- Discards frames greater than programmed maximum MAC frame size and runt, non-octet bounded, or bad-FCS frames upon reception
- Configurable for promiscuous broadcast-discard mode.
- Programmable threshold for SDRAM queues to initiate flow control and status indication
- MAC loopback support for transmit data looped to receive data at the MII/RMII interface

2.8 Microprocessor Interface

- 8-bit data bus
- Non-multiplexed Intel and Motorola Timing Modes
- Internal software reset and External Hardware reset input pin
- Global interrupt output pin

2.9 Serial SPI Interface—Master Mode Only

- Provides chip select and clock for external EEPROM
- Operation up to 8.33MHz
- 4-signal interface

2.10 Default Configurations

- Three default hardware configurations for operation without an external microprocessor
- Hardware modes set for easy connection to T1/E1 and T3/E3 WAN Systems
- Hardware pins provide some flexibility for configuration

2.11 Test and Diagnostics

- IEEE 1149.1 support
- Programmable on-chip BERT
- Patterns include pseudorandom QRSS, Daly, and user-defined repetitive patterns
- Loopbacks (remote, local, analog, and per-channel loopback)

2.12 Specifications Compliance

The DS33Z44 meets relevant telecommunications specifications. The following table provides the specifications and relevant sections that are applicable to the DS33Z44.

Table 2-1. T1-Related Telecommunications Specifications

IEEE 802.3-2002—*CSMA/CD access method and physical layer specifications*
RFC1662—*PPP in HDLC-like Framing*
RFC2615—*PPP over SONET/SDH*
X.86—*Ethernet over LAPS*
RMII—*Industry Implementation Agreement for "Reduced MII Interface"* (Sept. 1997)

3 APPLICATIONS

- Transparent LAN Service
- LAN Extension
- Ethernet Delivery over T1/E1/J1, T3/E3, OC-1/EC-1, G.SHDSL, or HDSL2/4

Also refer to *Application Note 3411: DS33Z11—Ethernet LAN to Unframed T1/E1 WAN Bridge* for an example of a complete LAN-to-WAN design.

Figure 3-1. Ethernet-to-WAN Extension (No Framing)

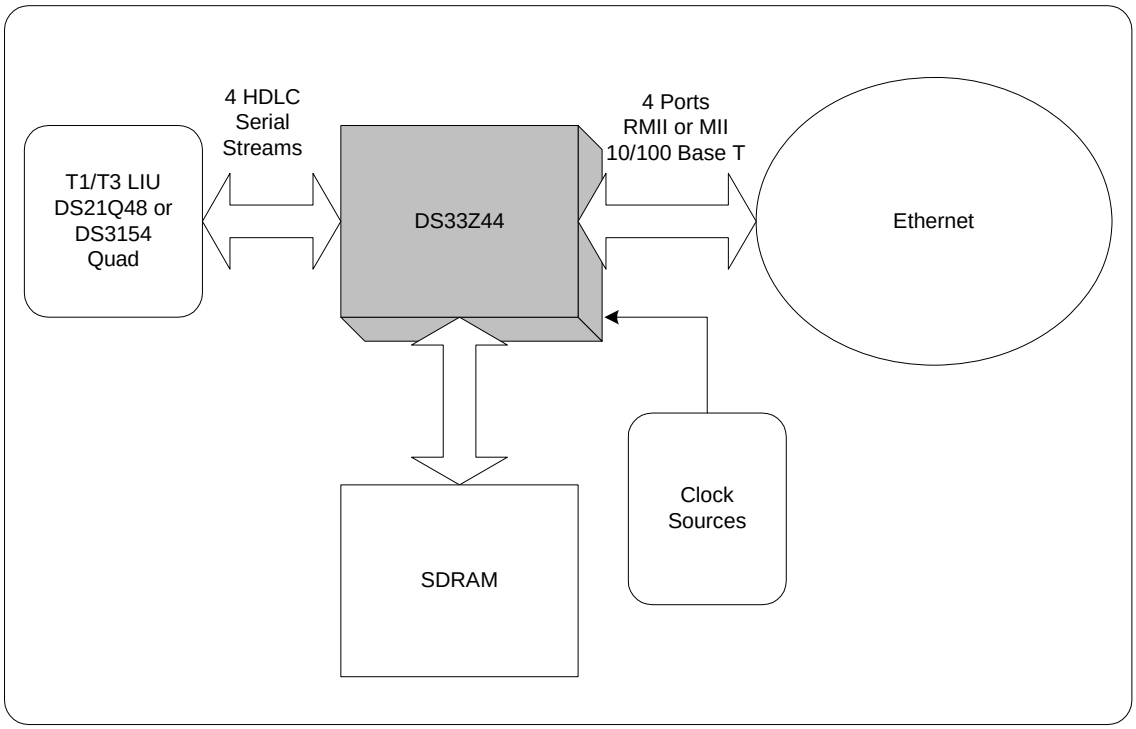


Figure 3-2. Ethernet-to-WAN Extension (T1/E1 Framing and LIU)

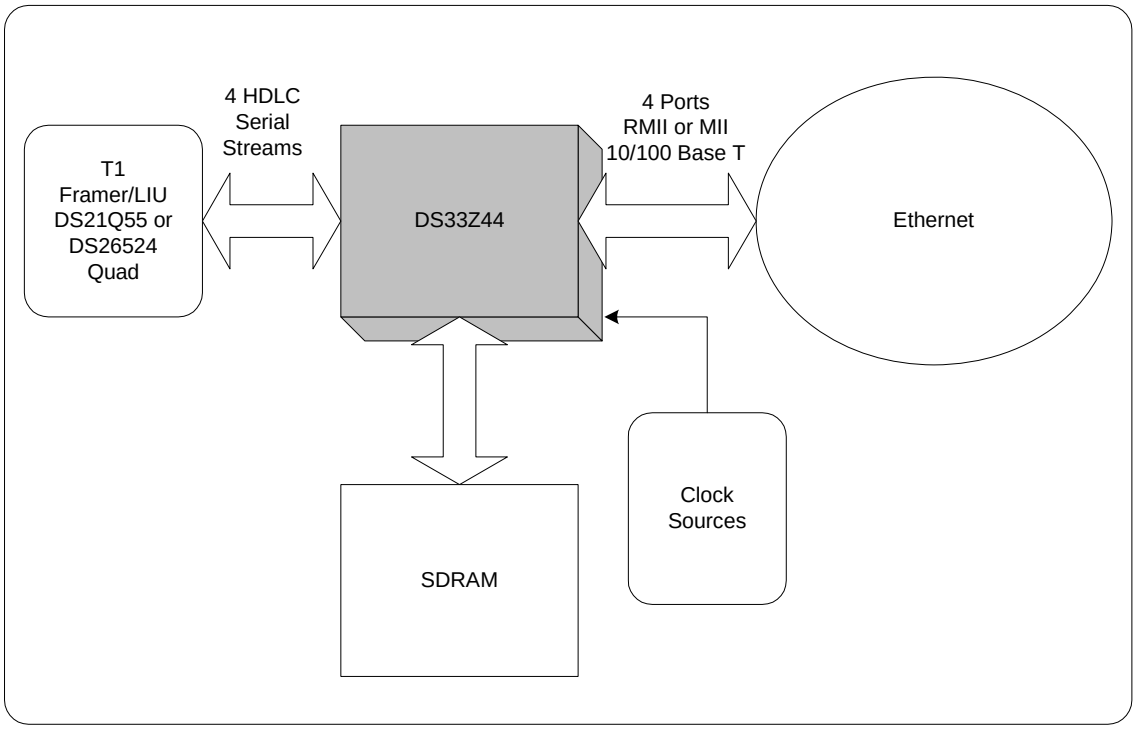


Figure 3-3. Ethernet-to-WAN Extension with T3/E3 Framing

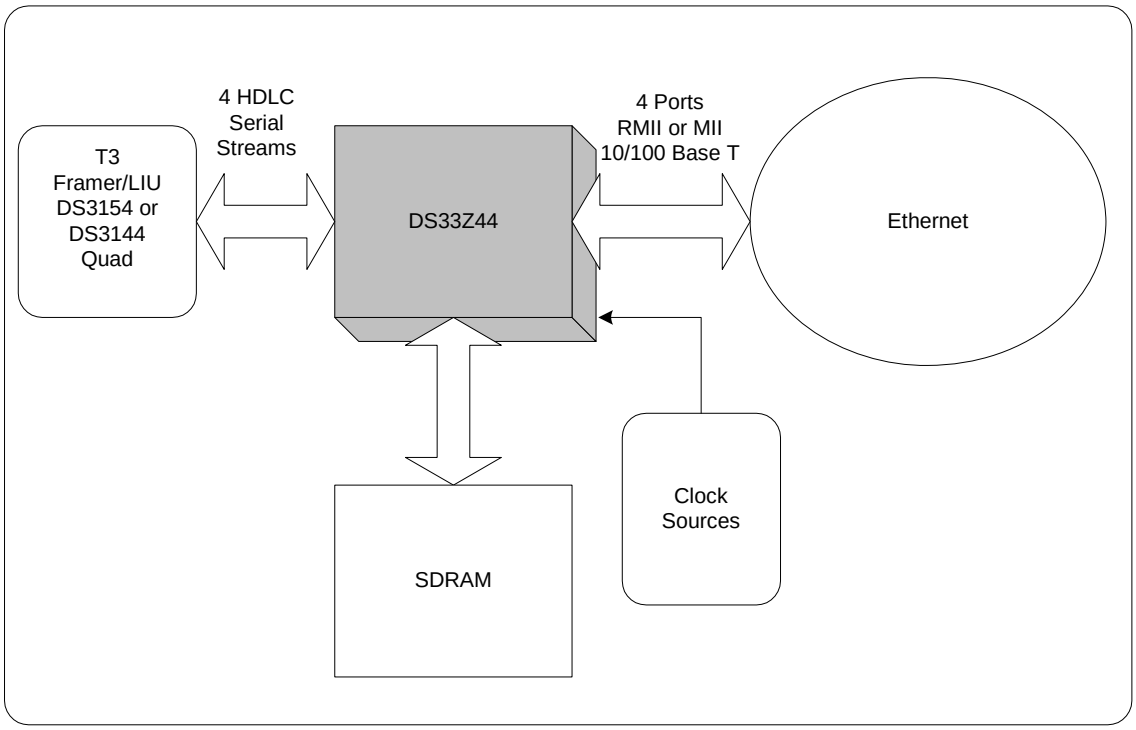


Figure 3-4. Ethernet Over DSL

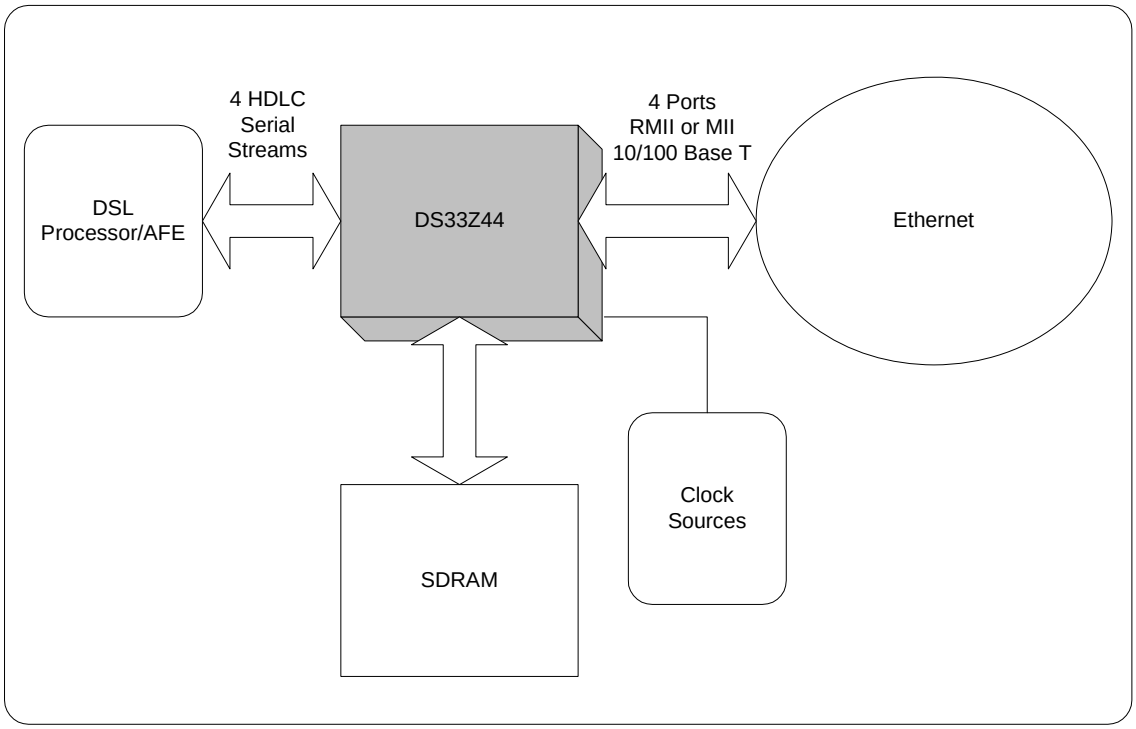
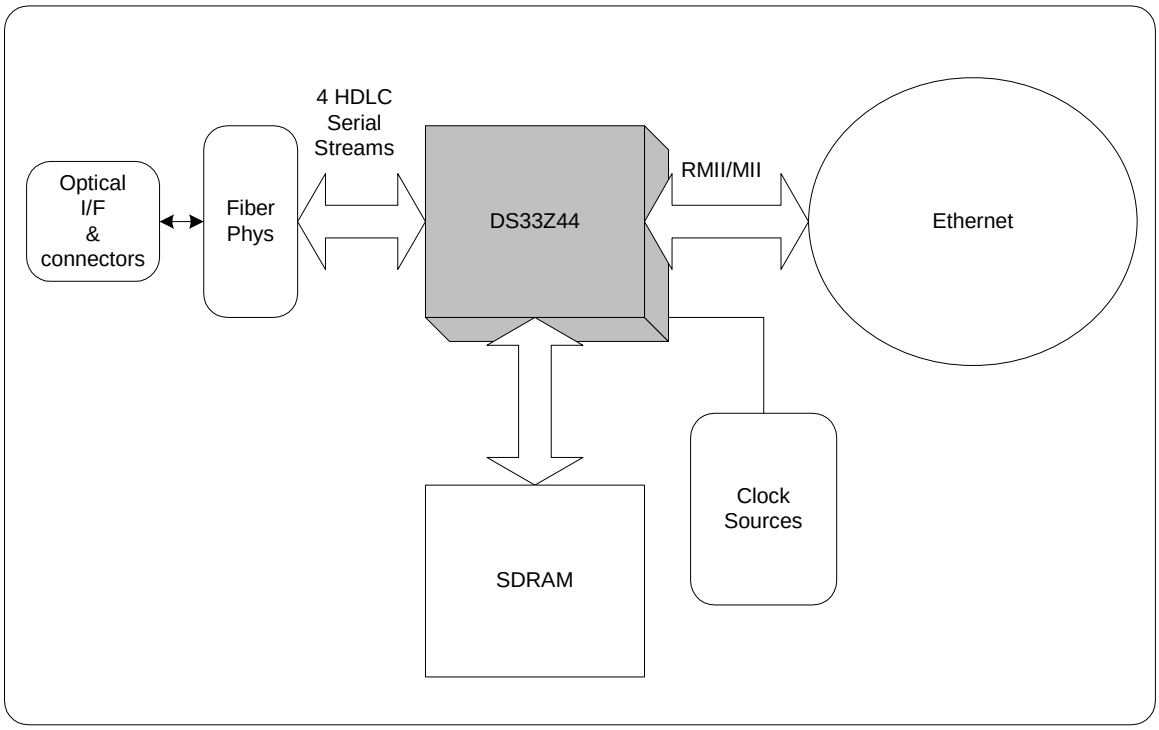


Figure 3-5. Copper-to-Fiber Connection



4 ACRONYMS AND GLOSSARY

- BERT: Bit Error-Rate Tester
- DCE: Data Communication Interface
- DTE: Data Terminating Interface
- FCS: Frame Check Sequence
- HDLC: High-Level Data Link Control
- MAC: Media Access Control
- MII: Media Independent Interface
- RMII: Reduced Media Independent Interface
- WAN: Wide Area Network

Note 1: Previous versions of this document used the term “Subscriber” to refer to the Ethernet Interface function. The register names have been allowed to remain with an “SU.” prefix to avoid register renaming.

Note 2: Previous versions of this document used the term “Line” to refer to the Serial Interface. The register names have been allowed to remain with an “LI.” prefix to avoid register renaming.

Note 3: The terms “Transmit Queue” and “Receive Queue” are with respect to the Ethernet Interface. The Receive Queue is the queue for the data that arrives on the MII/RMII interface, is processed by the MAC and stored in the SDRAM. Transmit queue is for data that arrives from the Serial port, is processed by the HDLC and stored in the SDRAM to be sent to the MAC transmitter.

5 MAJOR OPERATING MODES

The DS33Z44 has three major modes of operation: microprocessor controlled, EEPROM initialized, and Hardware mode.

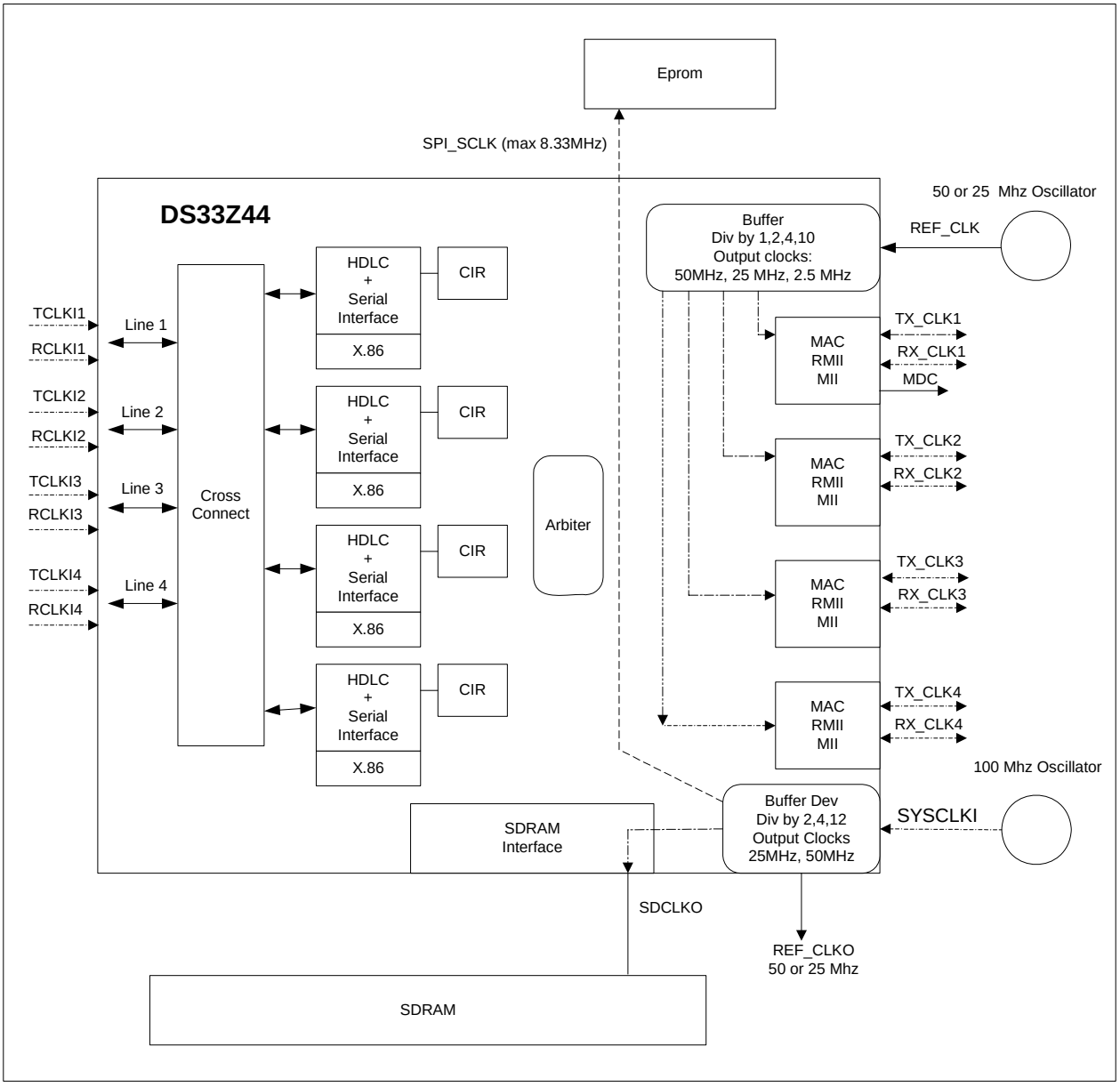
Microprocessor control is possible through the 8-bit parallel control port. More information on microprocessor control is available in Section 8.1.

EEPROM initialization is enabled by the built-in SPI Master that reads a serial EEPROM connected to the SPI port after device reset and initializes the device. More information on EEPROM operation is available in Section 8.2.

Hardware mode allows configuration of the device without a host microprocessor or EEPROM. More information on Hardware mode is available in Section 8.21.

6 BLOCK DIAGRAMS

Figure 6-1. Detailed Block Diagram



7 PIN DESCRIPTIONS

7.1 Pin Functional Description

Note that all digital pins are input/output pins in JTAG mode. This feature increases the effectiveness of board-level ATPG patterns.
I = input; O = output; Ipu = input, with pullup; Oz = output, with tri-state; IO = bidirectional pin; IOz = bidirectional pin, with tri-state

Table 7-1. Detailed Pin Descriptions

NAME	PIN	TYPE	FUNCTION
SERIAL INTERFACE IO PINS			
TCLKI1	F1	I	**Serial Interface Transmit Clock Port n Input.** The clock reference for TSER1–TSER4, which is output on the rising edge of the clock. TCLKIn supports gapped clocking, up to a maximum frequency of 52MHz.
TCLKI2	J1		
TCLKI3	M1		
TCLKI4	R1		
TSER1	F2	O	**Transmit Serial Data Port n Output.** Output on the rising edge of TCLKIn. Selective clock periods can be skipped for output of TSERn dependent on the TDENn settings or gapped clock input (TCLKIn). The maximum data rate is 52Mbps.
TSER2	J2		
TSER3	M2		
TSER4	R2		
TDEN1/TBSYNC1	F5	IO	**Transmit Data Enable Port n (Input).** The transmit data enable is programmable to selectively block/enable the transmit data. The TDENn signal must occur one clock edge prior to the affected data bit. The active polarity of TDENn is programmable in register LI.TSLCR. It is recommended for both T1/E1 and T3/E3 applications that use gapped clocks. The TDENn signal is provided for interfacing to framers that do not have a gapped clock facility. **Transmit Byte Sync Port n (Output).** This output can be used by an external Serial to Parallel to convert TSERn stream to byte wide data. This output indicates the last bit of the byte data sent serially on TSERn. This signal is only active in the X.86 Mode. Note that in Hardware mode and non-X.86 operation this pin must be tied high.
TDEN2/TBSYNC2	K2		
TDEN3/TBSYNC3	P3		
TDEN4/TBSYNC4	R3		
RCLKI1	G2	I	**Serial Interface Receive Clock Input for Port n.** Reference clock for receive serial data on RSERn. Gapped clocking is supported, up to the maximum RCLKIn frequency of 52MHz.
RCLKI2	L2		
RCLKI3	N2		
RCLKI4	T3		
RSER1	H1	I	**Receive Serial Data Input for Port n.** Receive Serial data arrives on the rising edge of the clock.
RSER2	K1		
RSER3	P1		
RSER4	T2		

NAME	PIN	TYPE	FUNCTION
RDEN1/RBSYNC 1	H2	I	**Receive Data Enable Port n.** The receive data enable is programmable to block the receive data. The RDENn must be coincident with the RSERn data bit to be blocked or enabled. The active polarity of RDENn is programmable in register **LI.RSLCR**. It is recommended for both T1/E1 and T3/E3 applications that use gapped clocks. The RDENn signal is provided for interfacing to framers that do not have a gapped clock facility. **Receive Byte Synchronization Input Port n.** Provides byte synchronization input to X.86 decoder. This signal will go high at the last bit of the byte as it arrives. This signal can occur at maximum rate every 8 bits. Note that a long as the DS33Z44 receives one RBSYNCn indicator, the X.86 receiver will determine the byte boundary. Hence the DS33Z44 does not require a continuous 8-bit sync indicator. A new sync pulse is required if the byte boundary changes. Note that in Hardware mode and non-X.86 operation of operation this pin must be tied high.
RDEN2/RBSYNC 2	L1		
RDEN3/RBSYNC 3	N1		
RDEN4/RBSYNC 4	T1		
MII/RMII PORT			
REF_CLK	C15	I	**Reference Clock (RMII and MII):** When in RMII mode, all signals from the PHY are synchronous to this clock input for both transmit and receive. This required clock can be up to 50MHz and should have ±100ppm accuracy. When in MII mode in DCE operation, the DS33Z41 uses this input to generate the RX_CLK and TX_CLK outputs as required for the Ethernet PHY interface. When the MII interface is used with DTE operation, this clock is not required and should be tied low. In DCE and RMII modes, this input must have a stable clock input before setting the $\overline{RST}$ pin high for normal operation.
REF_CLKO	B15	O	**Reference Clock Output (RMII and MII).** A derived clock output up to 50MHz, generated by internal division of the SYSCLKI signal. Frequency accuracy of the REF_CLKO signal will be proportional to the accuracy of the user-supplied SYSCLKI signal. See Section 8.3.2 for more information.
TX_CLK1	A9	IO	**Transmit Clock Port n (MII).** Timing reference for TX_ENn and TXDn[3:0]. The TX_CLKn frequency is 25MHz for 100Mbps operation and 2.5MHz for 10Mbps operation. In DTE mode, this is a clock input provided by the PHY. In DCE mode, this is an output derived from REF_CLK providing 2.5MHz (10Mbps operation) or 25MHz (100Mbps operation).
TX_CLK2	M16		
TX_CLK3	G16		
TX_CLK4	A16		
TX_EN1	E10	O	**Transmit Enable Port n (MII).** This pin is asserted high when data TXDn[3:0] is being provided by the DS33Z44. The signal is deasserted prior to the first nibble of the next frame. This signal is synchronous with the rising edge TX_CLKn. It is asserted with the first bit of the preamble.
TX_EN2	L14		
TX_EN3	E15		

NAME	PIN	TYPE	FUNCTION
TX_EN4	G13		**Transmit Enable Port n (RMII).** When this signal is asserted, the data on TXDn[1:0] is valid. This signal is synchronous to the REF_CLK.
TXD1[0]	B9	O	**Transmit Data Port n 0 through 3(MII).** TXDn[3:0] is presented synchronously with the rising edge of TX_CLKn. TXDn[0] is the least significant bit of the data. When TX_ENn is low the data on TXDn[3:0] should be ignored. **Transmit Data Port n 0 through 1(RMII).** Two bits of data TXDn[1:0] presented synchronously with the rising edge of REF_CLK.
TXD1[1]	C9		
TXD1[2]	D9		
TXD1[3]	E9		
TXD2[0]	R15		
TXD2[1]	R16		
TXD2[2]	L15		
TXD2[3]	N14		
TXD3[0]	F15		
TXD3[1]	G14		
TXD3[2]	H13		
TXD3[3]	H14		
TXD4[0]	B16		
TXD4[1]	C16		
TXD4[2]	D16		
TXD4[3]	E16		
RX_CLK1	A11	IO	**Receive Clock n (MII).** Timing reference for RX_DVn, RX_ERRn and RXDn[3:0], which are clocked on the rising edge. RX_CLKn frequency is 25MHz for 100Mbps operation and 2.5MHz for 10Mbps operation. In DTE mode, this is a clock input provided by the PHY. In DCE mode, this is an output derived from REF_CLK providing 2.5MHz (10Mbps operation) or 25MHz (100Mbps operation).
RX_CLK2	L16		
RX_CLK3	H16		
RX_CLK4	A13		
RXD1[0]	B11	I	**Receive Data Port n 0 through 3(MII).** Four bits of received data, sampled synchronously with the rising edge of RX_CLKn. For every clock cycle, the PHY transfers 4 bits to the DS33Z44. RXDn[0] is the least significant bit of the data. Data is not considered valid when RX_DVn is low. **Receive Data Port n 0 through 1(RMII).** Two bits of received data, sampled synchronously with REF_CLK with 100Mbps Mode. Accepted when CRS_DVn is asserted. When configured for 10Mbps Mode, the data is sampled once every 10 clock periods.
RXD1[1]	C11		
RXD1[2]	D11		
RXD1[3]	E11		
RXD2[0]	K13		
RXD2[1]	K14		
RXD2[2]	H15		
RXD2[3]	K16		
RXD3[0]	G15		
RXD3[1]	J14		
RXD3[2]	J13		
RXD3[3]	J12		
RXD4[0]	B13		
RXD4[1]	C13		
RXD4[2]	B14		
RXD4[3]	C14		

NAME	PIN	TYPE	FUNCTION
RX_DV1	D10	I	**Receive Data Valid Port n (MII).** This active-high signal indicates valid data from the PHY. The data RXDn[3:0] is ignored if RX_DVn is not asserted high.
RX_DV2	K15		
RX_DV3	K11		
RX_DV4	D15		
RX_CRS1/ CRS_DV1	D12	I	**Receive Carrier Sense Port n (MII).** Should be asserted (high) when data from the PHY (RXDn[3:0] is valid. For each clock pulse 4 bits arrive from the PHY. Bit 0 is the least significant bit. In DCE mode, connect to V_{DD}. **Carrier Sense/Receive Data Valid Port n (RMII).** This signal is asserted (high) when data is valid from the PHY. For each clock pulse 2 bits arrive from the PHY. In DCE mode, this signal must be grounded.
RX_CRS2/ CRS_DV2	N16		
RX_CRS3/ CRS_DV3	M15		
RX_CRS4/ CRS_DV4	F14		
RX_ERR1	E12	I	**Receive Error Port n (MII).** Asserted by the MAC PHY for one or more RX_CLKn periods indicating that an error has occurred. Active High indicates Receive code group is invalid. If CRS_DVn is low, RX_ERRn has no effect. This is synchronous with RX_CLKn. In DCE mode, this signal must be grounded. **Receive Error Port n (RMII).** Signal is synchronous to REF_CLK.
RX_ERR2	T16		
RX_ERR3	G11		
RX_ERR4	D14		
COLDET1	D13	I	**Collision Detect Port n (MII).** Asserted by the MAC PHY to indicate that a collision is occurring. In DCE Mode this signal should be connected to ground. This signal is only valid in half-duplex mode, and is ignored in full-duplex mode.
COLDET2	P16		
COLDET3	H11		
COLDET4	F16		
MDC	F11	O	**Management Data Clock (MII).** Clocks management data between the PHY and DS33Z44. The clock is derived from SYSCLKI, with a maximum frequency is 1.67MHz. The user must leave this pin unconnected in the DCE Mode.
MDIO	F10	IO	**MII Management Data IO (MII).** Data path for control information between the PHY and DS33Z44. When not used, pull to logic high externally through a 10kΩ resistor. The MDC and MDIO pins are used to write or read up to 32 Control and Status Registers in 32 PHY Controllers. This port can also be used to initiate Auto-Negotiation for the PHY. The user must leave this pin unconnected in the DCE Mode.

NAME	PIN	TYPE	FUNCTION
MICRO PORT/SPI			
A0/BREO	A1	I	**Address Bit 0.** Address bit 0 of the microprocessor interface. Least Significant Bit **BREO (Hardware Mode).** Used in Hardware Mode to reverse the ordering of HDLC transmit and receive functions. Active high input. When 0, the first bit received is the MSB. When 1, bit the first bit received is the LSB. The software registers used for control of this function are LI.RPPCL and LI.TPPCL.
A1/SCD	B1		**Address Bit 1.** Address bit 1 of the microprocessor interface. **SCD (Hardware Mode).** Used in Hardware Mode to disable $X^{43}+1$ bit scrambling for both the transmit and receive paths. Applies to HDLC and X.86 transport. When 1, $X^{43}+1$ scrambling is disabled. When 0, $X^{43}+1$ scrambling is enabled. The software registers used for control of this function are LI.RPPCL and LI.TPPCL.
A2/X86ED	A2		**Address Bit 2.** Address bit 2 of the microprocessor interface. **X86ED (Hardware Mode).** When in Hardware Mode, setting this pin high enables X.86 encapsulation for both the transmit and receive data. When 0, HDLC encapsulation is used. The register used to control this function in Software Mode is LI.TX86EDE.
A3	B2		**Address Bit 3.** Address bit 3 of the microprocessor interface.
A4	C2		**Address Bit 4.** Address bit 4 of the microprocessor interface.
A5	A3		**Address Bit 5.** Address bit 5 of the microprocessor interface.
A6	B3		**Address Bit 6.** Address bit 6 of the microprocessor interface.
A7	C3		**Address Bit 7.** Address bit 7 of the microprocessor interface.
A8	A4		**Address Bit 8.** Address bit 8 of the microprocessor interface.
A9	B4		**Address Bit 9.** Address bit 9 of the microprocessor interface. Most Significant Bit.
D0/MOSI	A5	IOZ	**Data Bit 0.** Bidirectional data bit 0 of the microprocessor interface. Least Significant Bit. Not driven when $\overline{CS}$ = 1 or $\overline{RST}$ = 0. **Master Out/Slave In (SPI Mode).** Data stream that provides the instruction and address information to the external EEPROM when in SPI Master Mode. MOSI is updated on the rising edge when CKPHA is set high, and on the falling edge when set low.
D1/MISO	A6	IOZ	**Data Bit 1.** Bidirectional data bit 1 of the microprocessor interface. Not driven when $\overline{CS}$ = 1 or $\overline{RST}$ = 0. **Master In/Slave Out (SPI Mode)/** Data path from the SPI EEPROM to the DS33Z44. Must be synchronous with SPICK. The Serial EEPROM SPI Interface will provide data to the DS33Z44, MSB first. MISO is sampled on the falling edge when CKPHA is set high, and on the rising edge when set low.

NAME	PIN	TYPE	FUNCTION
D2/SPICK	A7	IOZ	**Data Bit 2.** Bidirectional data bit 2 of the microprocessor interface. Not driven when $\overline{CS}$ = 1 or $\overline{RST}$ = 0. **SPICK.** Provides clocking for SPI transactions.
D3	B5	IOZ	**Data Bit 3.** Bidirectional data bit 3 of the microprocessor interface. Not driven when $\overline{CS}$ = 1 or $\overline{RST}$ = 0.
D4	B6	IOZ	**Data Bit 4.** Bidirectional data bit 4 of the microprocessor interface. Not driven when $\overline{CS}$ = 1 or $\overline{RST}$ = 0.
D5	B7	IOZ	**Data Bit 5.** Bidirectional data bit 5 of the microprocessor interface. Not driven when $\overline{CS}$ = 1 or $\overline{RST}$ = 0.
D6	C5	IOZ	**Data Bit 6.** Bidirectional data bit 6 of the microprocessor interface. Not driven when $\overline{CS}$ = 1 or $\overline{RST}$ = 0.
D7	C6	IOZ	**Data Bit 7.** Bidirectional data bit 7 of the microprocessor interface. Most Significant Bit. Not driven when $\overline{CS}$ = 1 or $\overline{RST}$ = 0.
$\overline{SPI\_CS}$	E13	O	**Active-Low SPI Chip Select.** This pin provides the chip select to the external EEPROM, when the SPI port is in master mode.
CKPHA	F6	I	**SPI Clock Phase.** MISO is sampled on the falling edge when CKPHA is set high, and on the rising edge when set low. MOSI is updated on the rising edge when CKPHA is set high, and on the falling edge when set low.
$\overline{CS}$	D1	I	**Active-Low Chip Select.** This pin must be taken low for read/write operations. When $\overline{CS}$ is high, the $\overline{RD}$/$\overline{DS}$ and $\overline{WR}$ signals are ignored.
$\overline{RD}$/$\overline{DS}$	E1	I	**Active-Low Read Data Strobe (Intel Mode).** The DS33Z44 drives the data bus (D0–D7) with the contents of the addressed register while $\overline{RD}$ and $\overline{CS}$ are both low. **Active-Low Data Strobe (Motorola Mode).** Used to latch data through the microprocessor interface. $\overline{DS}$ must be low during read and write operations.
$\overline{WR}$/R$\overline{W}$	E2	I	**Active-Low Write (Intel Mode).** The DS33Z44 captures the contents of the data bus (D0–D7) on the rising edge of $\overline{WR}$ and writes them to the addressed register location. $\overline{CS}$ must be held low during write operations. **Active-Low Read Write (Motorola Mode).** Used to indicate read or write operation. R$\overline{W}$ must be set high for a register read cycle and low for a register write cycle.
$\overline{INT}$	D3	OZ	**Active-Low Interrupt Output.** Outputs a logic zero when an unmasked interrupt event is detected. $\overline{INT}$ is deasserted when all interrupts have been acknowledged and serviced. Active low. Inactive state is programmable in register GL.CR1.

NAME	PIN	TYPE	FUNCTION
$\overline{RST}$	D8	I	**Active-Low Reset.** An active-low signal on this pin resets the internal registers and logic. This pin should remain low until power, SYSCLKI, RX_CLK, and TX_CLK are stable, then set high for normal operation. In DCE and RMII modes, the REF_CLK input must also have a stable clock input before setting $\overline{RST}$ high for normal operation. This input requires a clean edge with a rise time of 25ns or less to properly reset the device.
HWMODE	D5	I	**Hardware Mode.** Connect to V_{DD} to place the device in Hardware Mode. MODEC[1:0] determines the default hardware setting to be used. This pin must be held low for control by a microprocessor or an external EEPROM.
MODEC[0], MODEC[1]	D6, D7	I	**Mode Control** Software Mode Options (HWMODE = 0) 00 = Read/Write Strobe Used (Intel Mode) 01 = Data Strobe Used (Motorola Mode) 10 = SPI Master Mode (External EEPROM) 11 = Reserved. Do not use. Hardware Mode Options (HWMODE = 1) 00 = Default Hardware Mode. See Table 8-10. 01 = Reserved. Do not use. 10 = Reserved. Do not use. 11 = Reserved. Do not use.
DCEDTES	A15	I	**DCE or DTE Selection.** The user must set this pin high for DCE Mode selection or low for DTE Mode. This input affects operation in both software and hardware mode. In DCE Mode, the DS33Z44 MAC port can be directly connected to another MAC. In DCE Mode, the Transmit clock (TX_CLKn) and Receive clock (RX_CLKn) are output by the DS33Z44. Note that there is no software bit selection of DCEDTES. Note that DCE Mode is only relevant when the MAC interface is in MII mode.
RMIIMIIS	C4	I	**RMII or MII Selection.** Set high to configure the MAC for RMII interfacing. Set low for MII interfacing. Applies to all four ports.
FULLDS1	A10	I	**Full-Duplex Selection Port n (Hardware Mode).** When in Hardware Mode, this pin selects full-duplex MAC operation when set high. If low, the MAC will operate in half-duplex mode. In software mode, this pin has no effect and duplex selection is controlled in the SU.GCR register.
FULLDS2	J15		
FULLDS3	H12		
FULLDS4	A12		
H10S1	B10	I	**100Mb/10Mb Port n (Hardware Mode).** When in Hardware Mode, this pin selects the packet PHY data rate. Set high for 100Mbps. Set low for the MII/RMII interface to run at 10Mbps. In the software mode this pin has no effect and the rate selection is controlled in the SU.GCR register.
H10S2	L11		
H10S3	F12		
H10S4	B12		
AFCS1	C10	I	**Automatic Flow Control (Hardware Mode).** When in Hardware Mode, set high to enable automatic flow control pause and backpressure application. In the software mode this pin has no effect and the rate selection is controlled by the SU.GCR register.
AFCS2	J16		
AFCS3	J11		
AFCS4	C12		

NAME	PIN	TYPE	FUNCTION
SDRAM CONTROLLER			
SDATA[0]	R4	IOZ	**SDRAM Data Bus, Bits 0 to 31.** The 32 pins of the SDRAM data bus are inputs for read operations and outputs for write operations. At all other times, these pins are high impedance. **Note:** All SDRAM operations are controlled entirely by the DS33Z44. No user programming for SDRAM buffering is required.
SDATA[1]	P5		
SDATA[2]	T4		
SDATA[3]	R5		
SDATA[4]	T5		
SDATA[5]	T6		
SDATA[6]	R6		
SDATA[7]	P7		
SDATA[8]	N6		
SDATA[9]	P6		
SDATA[10]	M6		
SDATA[11]	M3		
SDATA[12]	M5		
SDATA[13]	N4		
SDATA[14]	N5		
SDATA[15]	P4		
SDATA[16]	R12		
SDATA[17]	N12		
SDATA[18]	P12		
SDATA[19]	T13		
SDATA[20]	T12		
SDATA[21]	T14		
SDATA[22]	R13		
SDATA[23]	R14		
SDATA[24]	P14		
SDATA[25]	P13		
SDATA[26]	N15		
SDATA[27]	N13		
SDATA[28]	M13		
SDATA[29]	L12		
SDATA[30]	M12		
SDATA[31]	M11		
SDA[0]	R10	O	**SDRAM Address Bus 0 to 11.** The 12 pins of the SDRAM address bus output the row address first, followed by the column address. The row address is determined by SDA0 to SDA11 at the rising edge of clock. Column address is determined by SDA0-SDA9 and SDA11 at the rising edge of the clock. SDA10 is used as an auto-precharge signal. **Note:** All SDRAM operations are controlled entirely by the DS33Z44. No user programming for SDRAM buffering is required.
SDA[1]	T10		
SDA[2]	R11		
SDA[3]	P11		
SDA[4]	M9		
SDA[5]	N9		
SDA[6]	N10		
SDA[7]	M8		
SDA[8]	N8		
SDA[9]	P9		
SDA[10]	P10		
SDA[11]	T9		

NAME	PIN	TYPE	FUNCTION
SBA[0]	R8	I	**SDRAM Bank Select.** These two bits select 1 of 4 banks for the read/write/precharge operations. **Note:** All SDRAM operations are controlled entirely by the DS33Z44. No user programming for SDRAM buffering is required.
SBA[1]	R9		
$\overline{\text{SRAS}}$	P15	O	**Active-Low SDRAM Row Address Strobe.** This output is used to latch the row address on rising edge of SDCLKO. It is used with commands for Bank Activate, Precharge, and Mode Register Write.
$\overline{\text{SCAS}}$	N7	O	**Active-Low SDRAM Column Address Strobe.** This output is used to latch the column address on the rising edge of SDCLKO. It is used with commands for Bank Activate, Precharge, and Mode Register Write.
$\overline{\text{SWE}}$	R7	O	**Active-Low SDRAM Write Enable.** This output enables write operation and auto precharge.
SDMASK[0]	T8	O	**SDRAM Mask 0 to 3.** When high, a write is done for that byte. The least significant byte is SDATA7 to SDATA0. The most significant byte is SDATA31 to SDATA24.
SDMASK[1]	M7		
SDMASK[2]	T11		
SDMASK[3]	N11		
SDCLKO	T7	O (4mA)	**SDRAM CLK Out.** System clock output to the SDRAM. This clock is a buffered version of SYSCLKI.
SYSCLKI	T15	I	**System Clock In.** 100MHz System Clock input to the DS33Z44, used for internal operation. This clock is buffered and provided at SDCLKO for the SDRAM interface. The DS33Z44 also provides a divided version output at the REF_CLKO pin. A clock supply with ±100ppm frequency accuracy is suggested.
$\overline{\text{SDCS}}$	P8	O	**Active-Low SDRAM Chip Select.** This output enables SDRAM access.
QUEUE STATUS			
QOVF1	C7	O	**Queue Overflow Port n.** This pin goes high when the transmit or receive queue has overflowed. This pin will go low when the high watermark is reached again. This pin functions in both software and hardware mode.
QOVF2	C8		
QOVF3	B8		
QOVF4	A8		
JTAG INTERFACE			
$\overline{\text{JTRST}}$	E6	Ipu	**Active-Low JTAG Reset**
JTCLK	D4	Ipu	**JTAG Clock**
JTDO	E5	Oz	**JTAG Data In**
JTDI	E4	Ipu	**JTAG Data Out**
JTMS	F7	Ipu	**JTAG Mode Select**

NAME	PIN	TYPE	FUNCTION
POWER SUPPLIES			
$V_{DD3.3}$	G3–G10, H3–H10	I	**Connect to 3.3V Power Supply**
$V_{DD1.8}$	C1, D2, E3, E14, F4, F13, G12, K12, L13, M4, M14, N3, P2	I	**Connect to 1.8V Power Supply**
V_{SS}	E7, E8, J3–J10, K3–K10, L3–L10, M10	I	**Connect to Common Supply Ground**
N.C.	F3, F8, F9, G1	—	**No Connection**

Figure 7-1. 256-Ball CSBGA Pinout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	A[0]	A[2]	A[5]	A[8]	D[0]	D[1]	D[2]	QOVF4	TX_CLK1	FULLDS1	RX_CLK1	FULLDS4	RX_CLK4	VDD1.8	DCEDTES	TX_CLK4
B	A[1]	A[3]	A[6]	A[9]	D[3]	D[4]	D[5]	QOVF3	TXD1[0]	H10S1	RXD1[0]	H10S4	RXD4[0]	RXD4[2]	RFCLKO	TXD4[0]
C	$V_{DD1.8}$	A[4]	A[7]	RMIIMIIS	D[6]	D[7]	QOVF1	QOVF2	TXD1[1]	AFCS1	RXD1[1]	AFCS4	RXD4[1]	RXD4[3]	REF_CLK	TXD4[1]
D	$\overline{CS}$	$V_{DD1.8}$	$\overline{INT}$	JTCLK	HWMODE	MODEC0	MODEC1	$\overline{RST}$	TXD1[2]	RX_DV1	RXD1[2]	RX_CRS1	COLDET1	RX_ERR4	RX_DV4	TXD4[2]
E	$\overline{RD}$	$\overline{WR}$	$V_{DD1.8}$	JTDI	JTDO	$\overline{JTRST}$	V_{SS}	V_{SS}	TXD1[3]	TX_EN1	RXD1[3]	RX_ERR1	$\overline{SPI\_CS}$	$V_{DD1.8}$	TX_EN3	TXD4[3]
F	TCLKI1	TSER1	N.C.	$V_{DD1.8}$	TDEN1	CKPHA	JTMS	N.C.	N.C.	MDIO	MDC	H10S3	$V_{DD1.8}$	RX_CRS4	TXD3[0]	COLDET4
G	N.C.	RCLKI1	$V_{DD3.3}$	$V_{DD3.3}$	$V_{DD3.3}$	$V_{DD3.3}$	$V_{DD3.3}$	$V_{DD3.3}$	$V_{DD3.3}$	$V_{DD3.3}$	RX_ERR3	$V_{DD1.8}$	TX_EN4	TXD3[1]	RXD3[0]	TX_CLK3
H	RSER1	RDEN1	$V_{DD3.3}$	$V_{DD3.3}$	$V_{DD3.3}$	$V_{DD3.3}$	$V_{DD3.3}$	$V_{DD3.3}$	$V_{DD3.3}$	$V_{DD3.3}$	COLDET3	FULLDS3	TXD3[2]	TXD3[3]	RXD2[2]	RX_CLK3
J	TCLKI2	TSER2	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	AFCS3	RXD3[3]	RXD3[2]	RXD3[1]	FULLDS2	AFCS2
K	RSER2	TDEN2	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	RX_DV3	$V_{DD1.8}$	RXD2[0]	RXD2[1]	RX_DV2	RXD2[3]
L	RDEN2	RCLKI2	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	H10S2	SDATA[29]	$V_{DD1.8}$	TX_EN2	TXD2[2]	RX_CLK2
M	TCLKI3	TSER3	SDATA[11]	$V_{DD1.8}$	SDATA[12]	SDATA[10]	SDMASK[1]	SDA[7]	SDA[4]	V_{SS}	SDATA[31]	SDATA[30]	SDATA[28]	$V_{DD1.8}$	RX_CRS3	TX_CLK2
N	RDEN3	RCLKI3	$V_{DD1.8}$	SDATA[13]	SDATA[14]	SDATA[8]	$\overline{SCAS}$	SDA[8]	SDA[5]	SDA[6]	SDMASK[3]	SDATA[17]	SDATA[27]	TXD2[3]	SDATA[26]	RX_CRS2
P	RSER3	$V_{DD1.8}$	TDEN3	SDATA[15]	SDATA[1]	SDATA[9]	SDATA[7]	$\overline{SDCS}$	SDA[9]	SDA[10]	SDA[3]	SDATA[18]	SDATA[25]	SDATA[24]	$\overline{SRAS}$	COLDET2
R	TCLKI4	TSER4	TDEN4	SDATA[0]	SDATA[3]	SDATA[6]	$\overline{SWE}$	SBA[0]	SBA[1]	SDA[0]	SDA[2]	SDATA[16]	SDATA[22]	SDATA[23]	TXD2[0]	TXD2[1]
T	RDEN4	RSER4	RCLKI4	SDATA[2]	SDATA[4]	SDATA[5]	SDCLKO	SDMASK[0]	SDA[11]	SDA[1]	SDMASK[2]	SDATA[20]	SDATA[19]	SDATA[21]	SYSCLKI	RX_ERR2

8 FUNCTIONAL DESCRIPTION

The DS33Z44 provides interconnection and mapping functionality between Ethernet Packet Systems and WAN Time-Division Multiplexed (TDM) systems such as T1/E1/J1, HDSL, and T3/E3. The device is composed of four 10/100 Ethernet MACs, Packet Arbiter, four Committed Information Rate controllers (CIR), four HDLC/X.86(LAPS) Mappers, SDRAM interface, control ports, and Bit Error Rate Tester (BERT).

The Ethernet Packet interfaces support MII and RMII interfaces allowing DSZ33Z44 to connect to commercially available Ethernet PHY and MAC devices. The Ethernet interfaces can be individually configured for 10Mbps or 100Mbps service, in DTE and DCE configurations. The DS33Z44 MAC interface can be configured to reject frames with bad FCS and short frames (less than 64 bytes).

Ethernet frames are queued and stored in external 32-bit SDRAM. The DS33Z44 SDRAM controller enables connection to a 128Mb SDRAM without external glue logic, at clock frequencies up to 100MHz. The SDRAM is used for both the Transmit and Receive Data Queues. The Receive Queue stores data to be sent from the Packet interface to the WAN interface. The Transmit Queue stores data to be sent from the WAN interface to the Packet interface. The external SDRAM can accommodate up to 8192 frames with a maximum frame size of 2016 bytes. The sizing of the queues can be adjusted by software. The user can also program high and low watermarks for each queue that can be used for automatic or manual flow control. The packet data stored in the SDRAM is encapsulated in HDLC or X.86 (LAPS) to be transmitted over the WAN interfaces. The device also provides the capability for bit and packet scrambling.

The WAN interfaces also receive encapsulated Ethernet packets and transmit the extracted packets over the Ethernet ports. The WAN physical interface supports serial data streams up to 52Mbps. The WAN serial ports can operate with a gapped clock, and can be connected to a framer, electrical LIU, optical transceiver, or T/E-Carrier transceiver for transmission to the WAN. The WAN interfaces can be connected to the Dallas Semiconductor/Maxim T1/E1/J1 Framers, Line Interface Units (LIUs), and Single-Chip Transceivers (SCTs). The WAN interfaces can also be connected to the Dallas Semiconductor/Maxim T3/E3/STS-1 framers, LIUs, and SCTs to provide T3, E3, and STS1 connectivity.

The DS33Z44 can be configured through an 8-bit microprocessor interface port. A serial EEPROM (SPI) interface and hardware mode are also included for applications without a host microprocessor. Operation without an external host simplifies and reduces the cost of typical applications such as connectivity to T1/T3 and E1/E3 front ends. The DS33Z44 also provides 2 on-board clock dividers for the System Clock input and Reference Clock Input for the 802.3 interfaces, further reducing the need for ancillary devices.

8.1 Processor Interface

Microprocessor control of the DS33Z44 is accomplished through the 20 interface pins of the microprocessor port. The 8-bit parallel data bus can be configured for Intel or Motorola modes of operation with the two MODEC[1:0] pins. When MODEC[1:0] = 00 and HWMODE = 0, bus timing is in Intel mode, as shown in Figure 11-9 and Figure 11-10. When MODEC[1:0] = 01 and HWMODE = 0, bus timing is in Motorola mode, as shown in Figure 11-11 and Figure 11-12. The address space is mapped through the use of eight address lines, A0-A7. Multiplexed Mode is not supported on the processor interface.

The Chip Select ($\overline{CS}$) pin must be brought to a logic low level to gain read and write access to the microprocessor port. With Intel timing selected, the Read ($\overline{RD}$) and Write ($\overline{WR}$) pins are used to indicate read and write operations and latch data through the interface. With Motorola timing selected, the Read-Write ($R\overline{W}$) pin is used to indicate read and write operations while the Data Strobe ($\overline{DS}$) pin is used to latch data through the interface.

The interrupt output pin ($\overline{INT}$) is an open-drain output that will assert a logic-low level upon a number of software maskable interrupt conditions. This pin is normally connected to the microprocessor interrupt input. The register map is shown in Table 9-1.

8.1.1 Read-Write/Data Strobe Modes

The processor interface can operate in either read-write strobe mode or data strobe mode. When MODEC[1:0] = 00 and HWMODE pin = 0 the read-write strobe mode is enabled and a negative pulse on $\overline{RD}$ performs a read cycle, and a negative pulse on $\overline{WR}$ performs a write cycle. When MODEC[1:0] pins = 01 and HWMODE pin = 0 the data strobe mode is enabled and a negative pulse on $\overline{DS}$ when R$\overline{W}$ is high performs a read cycle, and a negative pulse on $\overline{DS}$ when R$\overline{W}$ is low performs a write cycle. The read-write strobe mode is commonly called the “Intel” mode, and the data strobe mode is commonly called the “Motorola” mode.

8.1.2 Clear On Read

The latched status registers will clear on a read access. It is important to note that in a multi-task software environment, the user should handle all status conditions of each register at the same time to avoid inadvertently clearing status conditions. The latched status register bits are carefully designed so that an event occurrence cannot collide with a user read access.

8.1.3 Interrupt and Pin Modes

The interrupt ($\overline{INT}$) pin is configurable to drive high or float when not active. The INTM bit controls the pin configuration, when it is set the $\overline{INT}$ pin will drive high when not active. After reset, the $\overline{INT}$ pin is in high-impedance mode until an interrupt source is active and enabled to drive the interrupt pin.

8.2 SPI Serial EEPROM Interface

The SPI interface is a 4-signal serial interface that allows connection to a serial EEPROM for initialization information. The DS33Z44 will act as an SPI Master when configured with MODEC[1:0] to read from an external Serial EEPROM. The reading sequence is commenced upon initial reset or rising edge of the $\overline{RST}$ input pin. The CKPHA pin controls the sampling and update edges of the MISO and MOSI signals. The MISO data can be sampled on rising or falling edge of SPICK. The MOSI (Master Out Slave In) can be selectively output on the rising or falling edge of SPICK. The SPICK is generated by the DS33Z44 at a frequency of 8.33MHz. This frequency is derived from an external SYSCLKI (100MHz). The instruction to initiate a read is 0000x011; this is followed by the address location 0. The $\overline{SPI\_CS}$ is low till the data addressed (Table 10-1) is read and latched. The DS33Z44 will provide the starting address (0000000) and the data is sequentially latched till the last data is read and latched. The MAC-specific registers that are addressed indirectly are written at the end of the normal control registers. More details of the programming sequence an functional timing information can be found in Section 10.3. The indirect registers related to the MAC are programmed using a special command format as shown in Table 10-2.

8.3 Clock Structure

The DS33Z44 clocks sources and functions are as follows:

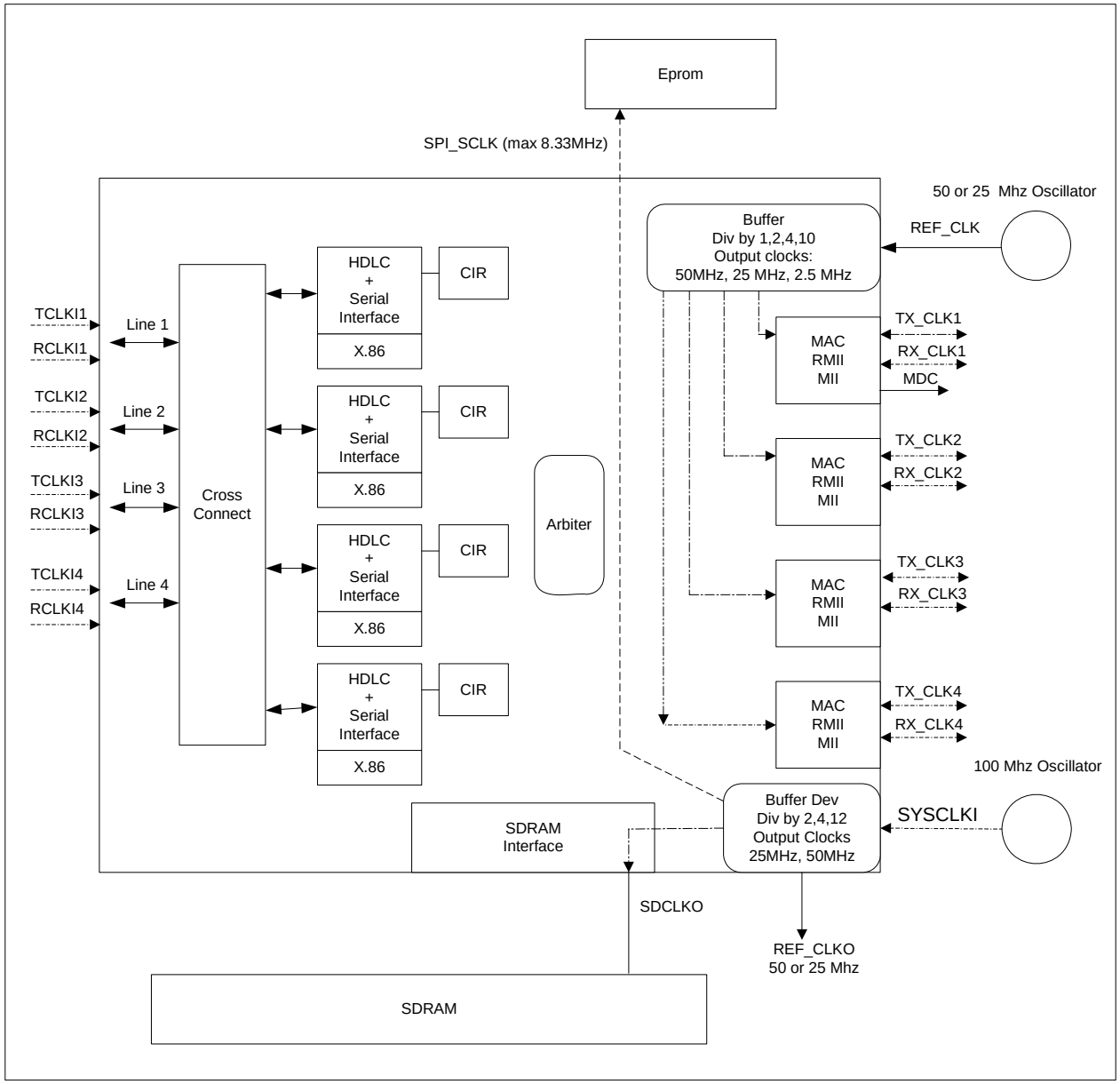
- Serial Transmit Data (TCLKI1-4) and Serial Receive Data (RCLKI1-4) clock inputs are used to transfer data from the serial interface. These clocks can be continuous or gapped.
- System Clock (SYSCLKI) input. Used for internal operation. This clock input cannot be a gapped clock. A clock supply with +/- 100 ppm frequency accuracy is suggested. A buffered version of this clock is provided on the SDCLKO pin for the operation of the SDRAM. A divided and buffered version of this clock is provided on the SPICK pin for Serial EEPROM operation. A divided and buffered version of this clock is provided on REFCLKO for the RMII/MII interface.
- Packet Interface Reference clock (REF_CLK) input that can be 25MHz or 50MHz. This clock is used as the timing reference for the RMII/MII interface. The user can utilize the built-in REFCLKO output clock to drive this input.
- The Transmit and Receive clocks for the MII Interface (TX_CLKn and RX_CLKn). In DTE mode, these are input pins and accept clocks provided by an Ethernet PHY. In the DCE mode, these are output pins and will output an internally generated clock to the Ethernet PHY. The output clocks are generated by the internal division of REF_CLK.
- REF_CLKO is an output clock that is generated by dividing the 100MHz System clock (SYSCLKI) by 2 or 4..
- A Management Data Clock (MDC) output is derived from SYSCLKI and is used for information transfer between the internal Ethernet MAC and external PHY. The MDC clock frequency is 1.67MHz.

The following table provides the different clocking options for the Ethernet interface.

Table 8-1. Clocking Options for the Ethernet Interface

RMII/MII Mode Selection	**MII**	**MII**	**RMII**	**RMII**	
10/100Mb Mode Selection	**100Mbps**	**10Mbps**	**100Mbps**	**10Mbps**	
RMIIMIIS Input Pin	0	0	1	1	Input
REF_CLKI Frequency	25MHz	25MHz	50MHz	50MHz	Input
TX_CLKn and RX_CLKn Divider Ratio (derived from REF_CLKI)	1	10	NA	NA	Divider Ratio
TX_CLKn, RX_CLKn Frequency	25MHz	2.5MHz	NA	NA	I/O
MDC Output Clock Frequency	1.67MHz	1.67MHz	1.67MHz	1.67MHz	Output
REFCLKO Divider Ratio (derived from SYSCLKI)	4	4	2	2	Divider Ratio
REF_CLKO Output Frequency	25MHz	25MHz	50MHz	50MHz	Output

Figure 8-1. Clocking for the DS33Z44



8.3.1 Serial Interface Clock Modes

Serial Interface timing is determined by the line clocks. Both the transmit and receive clocks (TCLKI1-4 and RCLKI1-4) are inputs, and can be gapped.

8.3.2 Ethernet Interface Clock Modes

The Ethernet interfaces can be configured for MII or RMII operation by setting the hardware pin RMIIMIIS. When in MII mode, 4 bits are sent and received every clock cycle. The MII clocks (TX_CLK1-4 and RX_CLK1-4) are derived from the REF_CLK, which must be 25MHz. The DS33Z44 can derive the 25MHz and 2.5MHz clocks from any external 25MHz reference. These derived clocks are output in the DCE Mode.

In RMII mode, the receive and transmit timing is synchronous to the 50MHz clock input on the REF_CLK pin. The selection for the reference frequency is controlled by RMIIMIIS pin. The user must set this selection in accordance with the REF_CLK input.

The REF_CLKO output is generated by a clock divider circuit utilizing the 100MHz system clock from SYSCLKI. The RMIIMIIS pin selects the divider ratio. The resulting clock is buffered and output on the REF_CLKO pin. The REF_CLKO function can be turned off with the GL.CR1.RFOO bit. Note that in DCE and RMII operating modes, the REF_CLKO signal should not be used to provide an input to REF_CLK, due to the reset requirements in these operating modes.

Table 8-2. LAN Interface Clock Selection

RMIIMIIS HARDWARE PIN STATE	REQUIRED REF_CLK FREQUENCY	ETHERNET INTERFACE MODE
0	25MHz ±100ppm	The interface is MII up to 100Mbps.
1	50MHz ±100ppm	The interface is RMII.

8.4 Resets and Low-Power Modes

The external $\overline{RST}$ pin and the global reset bit in GL.CR1 create an internal global reset signal. The global reset signal resets the status and control registers on the chip (except the GL.CR1.RST bit) to their default values and resets all the other flops to their reset values. The processor bus output signals are also placed in high-impedance mode when the $\overline{RST}$ pin is active (low). The global reset bit (GL.CR1.RST) stays set after a one is written to it, but is reset to zero when the external $\overline{RST}$ pin is active or when a zero is written to it. Allow 5 ms after initiating a reset condition for the reset operation to complete.

The Serial Interface reset bit in LI.RSTPD resets all the status and control registers on the Serial Interface to their default values, except for the LI.RSTPD.RST bit. The Serial Interface includes the HDLC encoder/decoder, X86 encoder and decoder and the corresponding serial port. The Serial Interface reset bit (LI.RSTPD.RST) stays set after a one is written to it, but is reset to zero when the global reset signal is active or when a zero is written to it.

If the DS33Z44 is configured to use an external EEPROM, the DS33Z44 will provide the startup sequence to read the device settings upon the rising edge of the external reset pin. When using the external EEPROM, the device is configured within 5ms. This is dependent on an EEPROM clock of 8.33MHz. The functional timing is provided by Figure 10-10.

Table 8-3. Reset Functions

RESET FUNCTION	LOCATION	COMMENTS
Hardware Device Reset	$\overline{RST}$ pin	Transition to a logic 0 to a logic 1 resets the device.
Hardware JTAG Reset	$\overline{JTRST}$ pin	Resets the JTAG test port.
Global Software Reset	GL.CR1	Writing to this bit resets the device.
Serial Interface Reset	LI.RSTPD	Writing to this bit resets a Serial Interface.
Queue Pointer Reset	GL.C1QPR, GL.C2QPR, GL.C3QPR, GL.C4QPR	Writing to this bit resets the associated Queue Pointer

There are several features in the DS33Z44 to reduce power consumption. The reset bit in the LI.RSTPD register minimizes power usage in the Serial Interface. Additionally, the $\overline{RST}$ pin or GL.CR1.RST bit may be held in reset indefinitely to keep the device in a low-power mode. Note that exiting a reset condition requires re-initialization and configuration. For the lowest possible standby current, clocks may be externally gated.

8.5 INITIALIZATION AND CONFIGURATION

EXAMPLE DEVICE INITIALIZATION SEQUENCE:

STEP 1: Reset the device by pulling the $\overline{RST}$ pin low or by using the software reset bits outlined in Section 8.4. Clear all reset bits. Allow 5ms for the reset recovery.

STEP 2: Check the Device ID in the GL.IDRL and GL.IDRH registers.

STEP 3: Configure the system clocks. Allow the clock system to properly adjust.

STEP 4: Initialize the entire remainder of the register space with 00h (or otherwise if specifically noted in the register's definition), including the reserved bits and reserved register locations.

STEP 5: Write FFFFFFFFh to the MAC indirect addresses 010Ch through 010Fh.

STEP 6: Setup connections in the GL.CON1-4 registers.

STEP 7: Configure the Serial Port register spaces as needed.

STEP 8: Configure the Ethernet Port register spaces as needed.

STEP 9: Configure the Ethernet MAC indirect registers as needed.

STEP 10: Configure the external Ethernet PHYs through the MDIO interface.

STEP 11: Clear all counters and latched status bits.

STEP 12: Set Queue sizes in the Arbiter and reset the queue pointers for all Ethernet and Serial Interfaces.

STEP 13: Enable Interrupts as needed.

STEP 14: Begin handling interrupts and latched status events.

8.6 Global Resources

A set of Global registers are located at 0F0h-0FFh. The global registers include Global resets, global interrupt status, interrupt masking, clock configuration, and the Device ID registers. See the Global Register Definitions in Table 9-2.

8.7 Per-Port Resources

The DS33Z44 contains a common set of global registers, BERT, and Arbiter. The four Serial (Line) Interfaces each have a set of registers for configuration and control, denoted in this document with the "LI." prefix. The four Ethernet (Subscriber) Interfaces each have a set of registers for configuration and control, denoted in this document with the "SU." prefix.

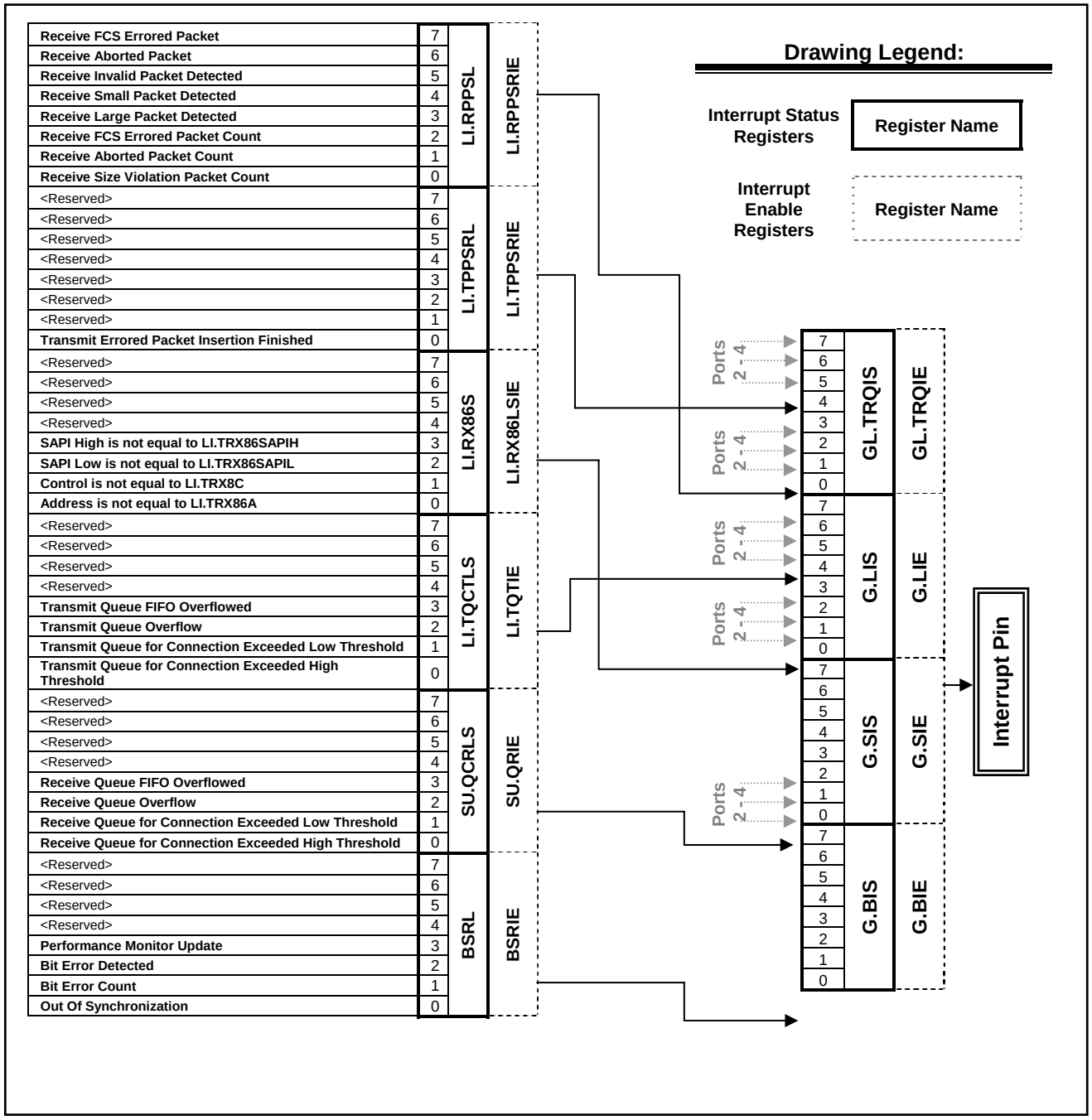
8.8 Device Interrupts

Figure 8-2 diagrams the flow of interrupt conditions from their source status bits through the multiple levels of information registers and mask bits to the interrupt pin. When an interrupt occurs, the host can read the Global Latched Status registers GL.LIS, GL.SIS, GL.BIS, and GL.TRQIS to initially determine the source of the interrupt. The host can then read the LI.TQCTLS, LI.TPPSRL, LI.RPPSRL, LI.RX86S, SU.QCRLS, or BSRL registers to further identify the source of the interrupt(s). In order to maintain software compatibility with the multiport devices in the product family, the global interrupt status and interrupt enable registers have been preserved, but do not need to be used. If GL.TRQIS is determined to be the interrupt source, the host will then read the LI.TPPSRL and LI.RPPSRL registers for the cause of the interrupt. If GL.LIS is determined to be the interrupt source, the host will then read the LI.TQCTLS, LI.TPPSRL, LI.RPPSRL, and LI.RX86S registers for the source of the interrupt. If GL.SIS is the source, the host will then read the SU.QCRLS register for the source of the interrupt. If GL.BIS is the source, the host will then read the BSRL register for the source of the interrupt. All Global Interrupt Status Register bits are real-time bits that will clear once the appropriate interrupt has been serviced and cleared, as long as no additional, enabled interrupt conditions are present in the associated status register. All Latched Status bits must be cleared by the host writing a “1” to the bit location of the interrupt condition that has been serviced. In order for individual status conditions to transmit their status to the next level of interrupt logic, they must be enabled by placing a “1” in the associated bit location of the correct Interrupt Enable Register. The Interrupt enable registers are LI.TPPSRIE, LI.RPPSRIE, LI.RX86LSIE, BSRIE, SU.QRIE, GL.LIE, GL.SIE, GL.BIE, and GL.TRQIE. Latched Status bits that have been enabled via Interrupt Enable registers are allowed to pass their interrupt conditions to the Global Interrupt Status Registers. The Interrupt enable registers allow individual Latched Status conditions to generate an interrupt, but when set to zero, they do not prevent the Latched Status bits from being set. Therefore, when servicing interrupts, the user should AND the Latched Status with the associated Interrupt Enable Register in order to exclude bits for which the user wished to prevent interrupt service. This architecture allows the application host to periodically poll the latched status bits for non-interrupt conditions, while using only one set of registers. Note the bit-orders of SU.QRIE and SU.QCRLS are different.

Note that the inactive state of the interrupt output pin is configurable. The INTM bit in GL.CR1 controls the inactive state of the interrupt pin, allowing selection of a pull-up resistor or active driver.

The interrupt structure is designed to efficiently guide the user to the source of an enabled interrupt source. The latched status bits for the interrupting entity must be read to clear the interrupt. Also reading the latched status bit will reset all bits in that register. During a reset condition, interrupts cannot be generated. The interrupts from any source can be blocked at a global level by the placing a zero in the global interrupt enable registers (GL.LIE, GL.SIE, GL.BIE, and GL.TRQIE). Reading the Latched Status bit for all interrupt generating events will clear the interrupt status bit and Interrupt signal will be deasserted.

Figure 8-2. Device Interrupt Information Flow Diagram



8.9 Serial Interfaces

The four Serial Interfaces support time-division multiplexed, serial data I/O up to 52Mbps. The Serial Interface receives and transmits encapsulated Ethernet packets. Each physical interface consists of a data pin, clock pin, and an enable/sync pin in both the transmit and receive directions. The Serial Interfaces can operate with a gapped clock, and can be connected to a framer, electrical LIU, optical transceiver, or T/E-Carrier transceiver for transmission to the WAN. The Serial Interface can be connected to the Dallas Semiconductor/Maxim T1/E1/J1 Framers, Line Interface Units (LIUs), and Single-Chip Transceivers (SCTs). The interface can also be connected to the Dallas Semiconductor/Maxim T3/E3/STS-1 Framers, LIUs, and SCTs to provide T3, E3, and STS1 connectivity.

8.10 Connections and Queues

The device provides bidirectional cross-connections between the multiple Ethernet ports and Serial ports when operating in software mode. Each connection has an associated transmit and receive queue. Note that the terms “Transmit Queue” and “Receive Queue” are with respect to the Ethernet Interface. The Receive queue is for data arriving from Ethernet interface to be transmitted to the WAN interface. The Transmit queue is for data arriving from the WAN Serial Interface to be transmitted to the Ethernet Interface. Hence the transmit and receive direction terminology is the same as is used for the Ethernet MAC Interface.

The user can define the connection and the size of the transmit and receive queues. The size is adjustable in units of 32 (by 2048 byte) packets. The external SDRAM can hold up to 8192 packets of data. The user must ensure that all the connection queues do no exceed this limit. The user also must ensure that the transmit and receive queues do not overlap each other. Uni-directional connections are not supported.

When the user needs to modify the queue sizes, all connections must be torn down and re-established. When a connection is disconnected all transmit and receive queues associated with the connection are flushed and a “1’ is sourced towards the Serial transmit and the HDLC receiver. The clocks to the HDLC are sourced a “0”. If multiple connections are established and a connection is disconnected, the other queue sizes cannot be adjusted to consume the free space of the disconnected queue. The established connections can continue to function as long as their associated queue sizes are not changed.

The user can also program high and low watermarks for each queue. If the queue size grows past the High watermark, an interrupt is generated if enabled. The registers of relevance are described in Table 8-4. AR.TQSC1-4 provide the size of the transmit queues for the connections. The High Watermark will set a latched status bit. The latched status bit will clear when the register is read. The status bit is indicated by LI.TQCTLS.TQHTS. Interrupts can be enabled on the latched bit events by LI.TQTIE. A latched status bit (LI.TQCTLS.TQLTS) is also set when the queue crosses a low watermark.

The Receive Queue functions in a similar manner. Note that the user must ensure that sizes and watermarks are set in accordance with the configuration speed of the Ethernet and Serial Interfaces. The DS33Z44 does not provide error indication if the user creates a connection and queue that overwrites data for another connection queue. The user must take care in setting the queue sizes and watermarks. The registers of relevance are AR.RQSC1-4 and SU.QCRLS. Queue size should never be set to 0.

It is recommended that the user reset the queue pointers for the connection after disconnection. The pointers must be reset before a connection is made. If this disconnect/connect procedure is not followed, incorrect data may be transmitted. The proper procedure for setting up a connection follows:

- Set up the queue sizes for both transmit and receive queue (AR.TQSC1-4 and AR.RQSC1-4).
- Set up the high/low thresholds and interrupt enables if desired (GL.TRQIE, LI.TQTIE, SU.QRIE)
- Reset all the pointers for the connection desired (GL.C1QPR–GL.C4QPR)
- Set up the connections (GL.CON1-4)
- If a connection is disconnected, reset the queue pointers after the disconnection.

Figure 8-3. Transmit Connection Diagram

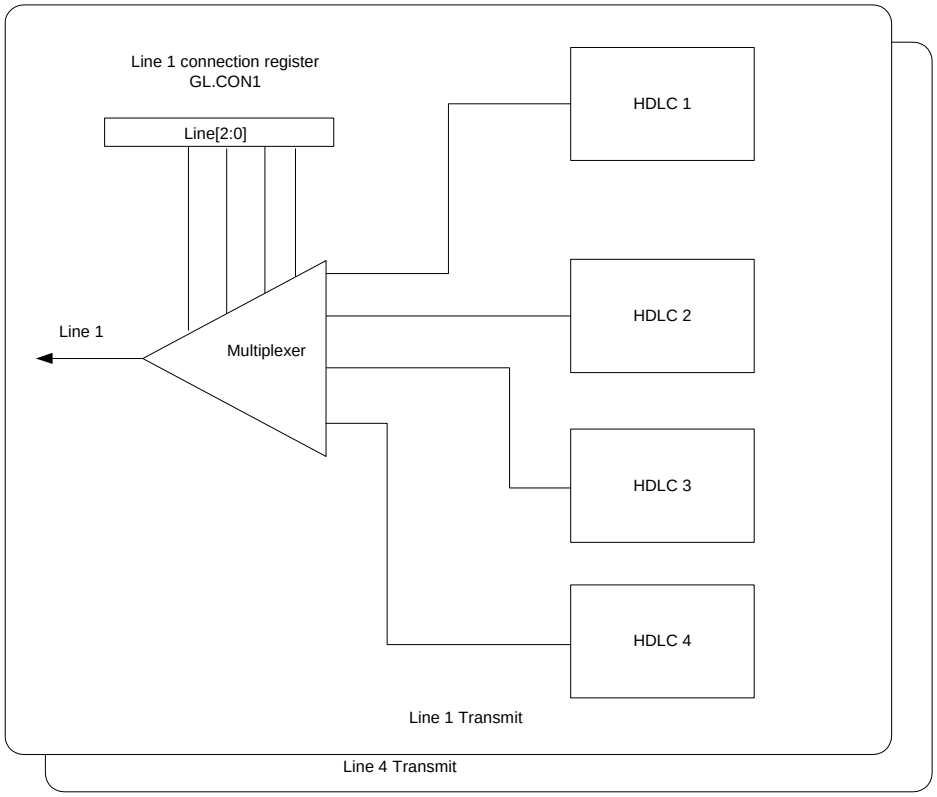


Figure 8-4. Receive Connection Diagram

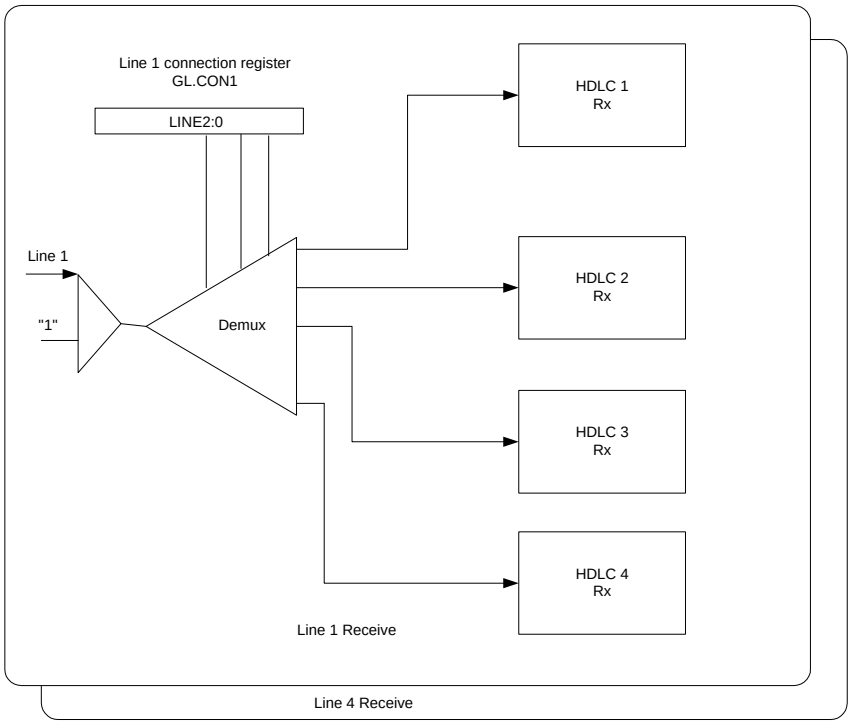


Table 8-4. Registers Related to Connections and Queues

REGISTER	FUNCTION
GL.CON1–4	Enable connection between the Ethernet Interfaces and the Serial Interfaces. Note that once connection is set up, then the queues and thresholds can be setup for that connection.
AR.TQSC1–4	Size for the Transmit Queue in Number of 32–2K packets.
AR.RQSC1–4	Size for the Receive Queue in Number of 32–2K packets.
GL.TRQIE	Interrupt enable for items related to the connections at the global level
GL.TRQIS	Interrupt enable status for items related to the connections at the global level
LI.TQTIE	Enables for the Transmit queue crossing high and low thresholds
LI.TQCTLS	Latched status bits for connection high and low thresholds for the transmit queue.
SU.QRIE	Enables for the receive queue crossing high and low thresholds
SU.QCRLS	Latched status bits for receive queue high and low thresholds.
GL.C1QPR–GL.C4QPR	Reset the connection pointers.

8.11 Arbiter

The Arbiter manages the transport between the Ethernet ports and the Serial ports. It is responsible for queuing and dequeuing packets to a single external SDRAM. The arbiter handles requests from the HDLC and MAC to transfer data to and from the SDRAM.

8.12 Flow Control

Flow control may be required to ensure that data queues do not overflow and packets are not lost. The DS33Z44 allows for optional flow control based on the queue high watermark or through host processor intervention. There are 2 basic mechanisms that are used for flow control:

- In half-duplex mode, a jam sequence is sent that causes collisions at the far end. The collisions cause the transmitting node to reduce the rate of transmission.
- In full-duplex mode, flow control is initiated by the receiving node sending a pause frame. The pause frame has a timer parameter that determines the pause timeout to be used by the transmitting node.

Note that the terms “transmit queue” and “receive queue” are with respect to the Ethernet Interface. The Receive Queue is the queue for the data that arrives on the MII/RMII interface, is processed by the MAC and stored in the SDRAM. Transmit queue is for data that arrives from the Serial port, is processed by the HDLC and stored in the SDRAM to be sent to the MAC transmitter.

The following flow control options are possible:

- Automatic flow control can be enabled in hardware mode by the AFCSn and FULLDSn pins
- Automatic flow control can be enabled in software mode with the SU.GCR.ATFLOW bit. Note that the user does not have control over SU.MACFCR.FCE and FCB bits if ATFLOW is set. The mechanism of sending pause or jam is dependent only on the receive queue high threshold.
- Manual flow control can be performed through software when SU.GCR.ATFLOW=0. The host processor must monitor the receive queues and generate pause frames (full-duplex) and/or jam bytes through the SU.MACFCR.FCB, SU.GCR.JAME, and SU.MACFCR FCE bits.

Note that in order to use flow control the minimum receive queue size must be set to at least 2 (AR.RQSC1-4) and the receive queue high threshold (SU.RQHT) must be set to 1. If the high threshold is set to the same value as the queue size, automatic flow control will not be effective. The high threshold must always be set to less than the corresponding queue size.

The following table provides all the options on flow control mechanism for DS33Z44.

Table 8-5. Options for Flow Control

	HARDWARE MODE			SOFTWARE MODE			
Configuration	No flow control	Half-duplex, Flow control With respect to SU.RQHT	Full-duplex, Flow control With respect to SU.RQHT	Half-duplex; Manual Flow Control	Half-duplex; Automatic Flow Control	Full-duplex; Manual Flow Control	Full-duplex; Automatic Flow Control
HWMODE Pin	1	1	1	0	0	0	0
AFCSn Pin	0	1	1	N/A	N/A	N/A	N/A
FULLDSn Pin	0	0	1	0	0	1	1
ATFLOW Bit	N/A	N/A	N/A	0	1	0	1
JAME Bit	N/A	N/A	N/A	Controlled By User	Controlled automatically	N/A	N/A
FCB Bit (Pause)	N/A	N/A	Controlled automatically	NA	NA	Controlled by user	Controlled automatically
FCE Bit	N/A	Set to AFCSn pin= Low	Set to AFCSn pin= High	Controlled By User	Controlled automatically	Controlled By User	Controlled Automatically
Pause Timer	N/A	N/A	Set to 140	N/A	N/A	Programmed by user	Programmed by user

8.12.1 Full-Duplex Flow Control

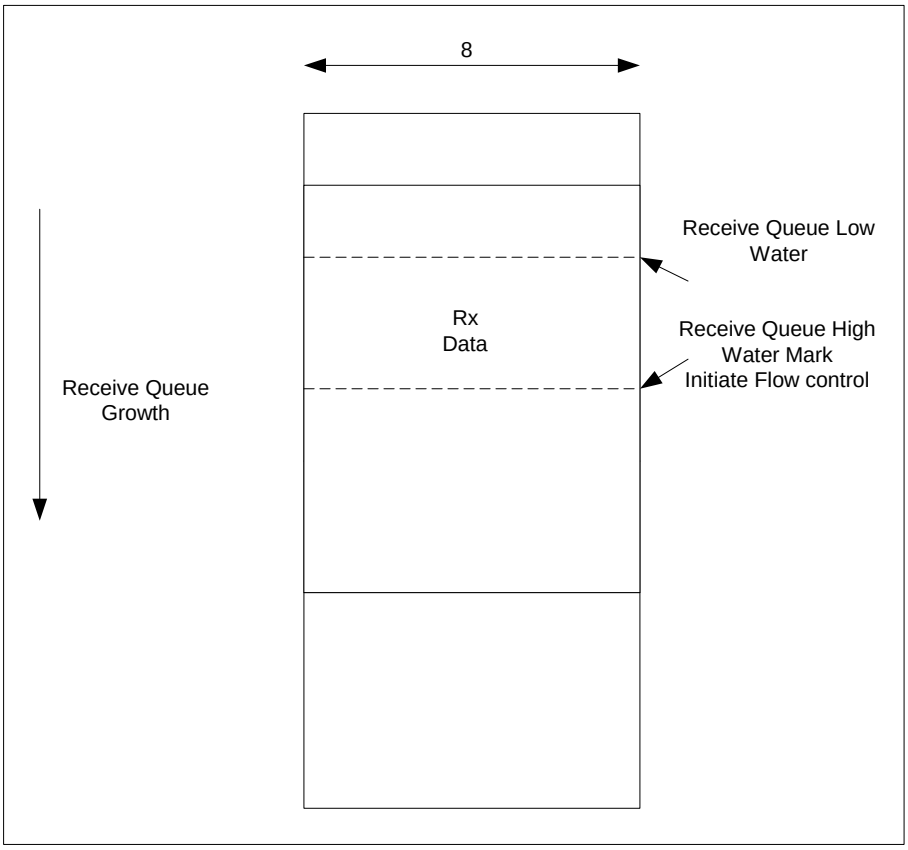
In the software mode automatic flow control is enabled by default. The host processor can disable this functionality with SU.GCR.ATFLOW. In hardware mode, the user must apply a logic high level to the AFCSn pins to enable automatic flow control. The flow control mechanism is governed by the high watermarks (SU.RQHT). The SU.RQLT low threshold can be used as indication that the network congestion is clearing up. The value of SU.RQLT does not affect the flow control. When the connection queue high threshold is exceeded the DS33Z44 will send a pause frame with the timer value programmed by the user. See Table 8-7 for more information. It is recommended that 140 slots (140 by 64 bytes or 5120 bytes) be used as the standard timer value.

The pause frame causes the distant transmitter to “pause for a time” before starting transmission again. The high and low thresholds for the receive queue are configurable by the user but it is recommended that the high threshold be set approximately 96 packets from the maximum size of the queue and the low threshold 96 packets lower than the high threshold. The DS33Z44 will send a pause frame as the queue has crossed the high threshold and a frame is received. Pause is sent every time a frame is received in the “high threshold state”. The receive queue could keep growing if the round trip delay is beyond 2800 bytes. Pause control will only take care of temporary congestion it does not take care of systems where the traffic throughput is too high for the queue sizes selected. If the flow control is not effective the receive queue will eventually overflow. This is indicated by SU.QCRLS.RQOVFL latched bit. If the receive queue is overflowed any new frames will not be received.

The user has the option of not enabling automatic flow control. In this case the thresholds and corresponding interrupt mechanism to send pause frame by writing to flow control busy bit in the MAC flow control registers SU.MACFCR.FCB, SU.GCR.JAME, and SU.MACFCR. This allows the user to set not only the watermarks but also to decide when to send a pause frame or not based on watermark crossings.

On the receive side the user has control over whether to respond to the pause frame sent by the distant end (PCF bit). Note that if automatic flow control is enabled the user cannot modify the FCE bit in the MAC flow control register. On the Transmit queue the user has the option of setting high and low thresholds and corresponding interrupts. **There is no automatic flow control mechanism for data received from the Serial side waiting for transmission over the Ethernet interface during times of heavy Ethernet congestion.**

Figure 8-5. Flow Control Using Pause Control Frame



8.12.2 Half-Duplex Flow Control

Half-duplex flow control uses a jamming sequence to exert backpressure on the transmitting node. The receiving node jams the first 4 bytes of a packet that are received from the MAC in order to cause collisions at the distant end. In both 100Mbps and 10Mbps MII/RMII modes, 4 bytes are jammed upon reception of a new frame. Note that the jamming mechanism does not jam the current frame that is being received during the watermark crossing, but will wait to jam the next frame after the SU.RQHT bit is set. If the queue remains above the high threshold, received frames will continue to be jammed. This jam sequence is stopped when the queue falls bellow the high threshold.

8.12.3 Host-Managed Flow Control

Although automatic flow control is recommended, flow control by the host processor is also possible. By utilizing the high watermark interrupts, the host processor can manually issue pause frames or jam incoming packets to exert backpressure on the transmitting node. Pause frames can be initiated with SU.MACFCR.FCB bit. Jam sequences can be initiated be setting SU.GCR.JAME. The host can detect pause frames by monitoring SU.RFSB3.UF and SU.RFSB3.CF. Jammed frames will be indistinguishable from packet collisions.

8.13 Ethernet Interfaces

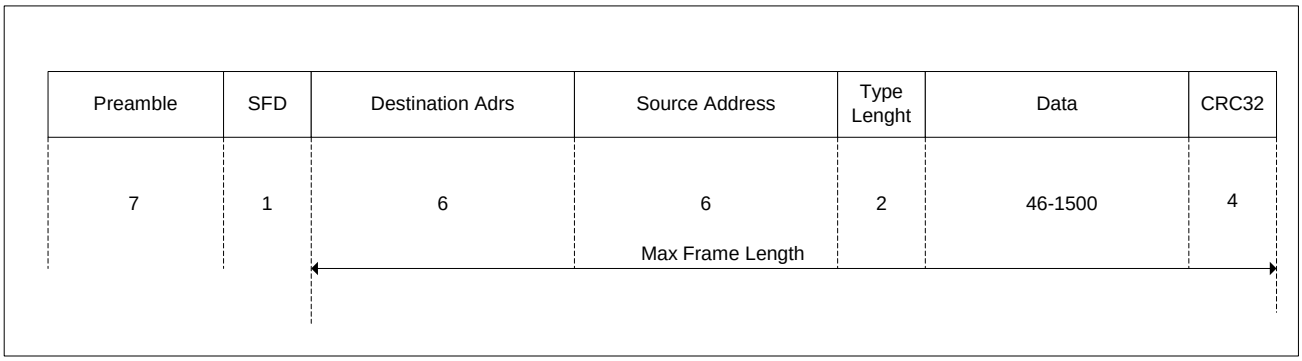
The four Ethernet Interfaces allow for direct connection to Ethernet PHYs. Each interface consists of a 10/100Mbps MII/RMII interface and an Ethernet MAC. In RMII operation, the interface contains 8 signals with a reference clock of 50MHz. In MII operation, the interface contains 12 signals and a clock reference of 25MHz. The DS33Z44 can be configured to RMII or MII interface by the Hardware pin RMIIMIIS. If the port is configured for MII in DCE mode, REF_CLK must be 25MHz. The DS33Z44 will internally generate the TX_CLKn and RX_CLKn outputs (at 25MHz for 100Mbps, 2.5MHz for 10Mbps) required for DCE mode from the REF_CLK input. In DTE mode of operation, the TX_CLKn and RX_CLKn signals are generated by the PHY and are inputs to the DS33Z44.

The data received from the MII or RMII interface is processed by the internal IEEE 802.3 compliant Ethernet MAC. The user can select the maximum frame size (up to 2016 bytes) that is received with the SU.RMFSRH and SU.RMFSRL registers. The maximum frame length (in bits) is the number specified in SU.RMFSRH and SU.RMFSRL multiplied by 8. **Any programmed value greater than 2016 bytes will result in unpredictable behavior and should be avoided.**

The length is shown in Figure 8-6. The length includes only destination address, source address, VLAN tag (2 bytes), type length field, data and CRC32. The frame size is different than the 802.3 length field shown in the figure.

Frames coming from the Ethernet PHY or received from the packet processor are rejected if greater than the maximum frame size specified. Each Ethernet frame sent or received generates status bits (SU.TFSH and SU.TFSL and SU.RFSB0 to SU.RFSB3). These are real time status registers and will change as each frame is sent or received. Hence they are useful to the user only when one frame is sent or received and the status is associated with the frame sent or received.

Figure 8-6. IEEE 802.3 Ethernet Frame



The distant end will normally reject the sent frames if jabber timeout, loss of carrier, excessive deferral, late collisions, excessive collisions, under run, deferred or collision errors occur. Transmission of a frame under any of theses errors will generate a status bit in SU.TFSL, SU.TFSH. The DS33Z44 provides user the option to automatically retransmit the frame if any of the errors have occurred through the bit settings in SU.TFRC. Deferred frames and heartbeat fail have separate resend control bits (SU.TFRC.TFBFCB and SU.TFRC.TPRHBC). If there is no carrier (indicated by the MAC Transmit Packet Status), the transmit queue (data from the Serial Interface to the SDRAM to Ethernet Interface) can be selectively flushed. This is controlled by SU.TFRC.NCFQ.

The MAC circuitry generates a frame status for every frame that is received. This real time status can be read by SU.RFSB0 to SU.RFSB3. Note the frame status is the “real time” status and hence the value will change as new frames are received. Hence the real time status reflects the status in time and may not correspond to the current received frame being processed. This is also true for the transmitted frames.

Frames with errors are usually rejected by the DS33Z44. The user has the option of accepting frames by settings in Receive Frame Rejection Control register (SU.RFRC). The user can program whether to reject or accept frames with the following errors:

- MII error asserted during the reception of the frame.
- Dribbling bits occurred in the frame.
- CRC error occurred.
- Length error occurred—the length indicated by the frame length is inconsistent with the number of bytes received.
- Control frame was received. The mode must be full-duplex.
- Unsupported control frame was received.

Note that frames received that are runt frames or frames with collision will automatically be rejected. In Hardware Mode any frame received with errors is rejected and any frame transmitted with an error is retransmitted

Table 8-6. Registers Related to the Ethernet Port

REGISTER	FUNCTION
SU.TFRC	This register determines if the current frame is retransmitted due to various transmit errors.
SU.TFSL and SU.TFSH	These two registers provide the real-time status of the transmit frame. Only apply to the last frame transmitted.
SU.RFSB0 to 3	These registers provide the real-time status for the received frame. Only apply to the last frame received.
SU.RFRC	This register provides settings for reception or rejection of frame based on errors detected by the MAC.
SU.RMFSRH and SU.RMFSRL	The settings for this register provide the maximum size of frames to be accepted from the MII/RMII receive interface.
SU.MACCR	This register provides configuration control for the MAC.

8.13.1 DTE and DCE Mode

The Ethernet MII/RMII interfaces can be configured for DCE or DTE Mode. When the ports are configured in DTE Mode, they can be connected to Ethernet PHYs. In DCE mode, the ports can be connected to MII/RMII MAC devices other than an Ethernet PHY. The DTE/DCE connections for the DS33Z44 in MII mode are shown in the following two figures.

In DCE Mode, the DS33Z44 transmitter is connected to an external receiver and DS33Z44 receiver is connected to an external MAC transmitter. The selection of DTE or DCE mode is done by the hardware pin DCEDTES.

Figure 8-7. Configured as DTE Connected to an Ethernet PHY in MII Mode

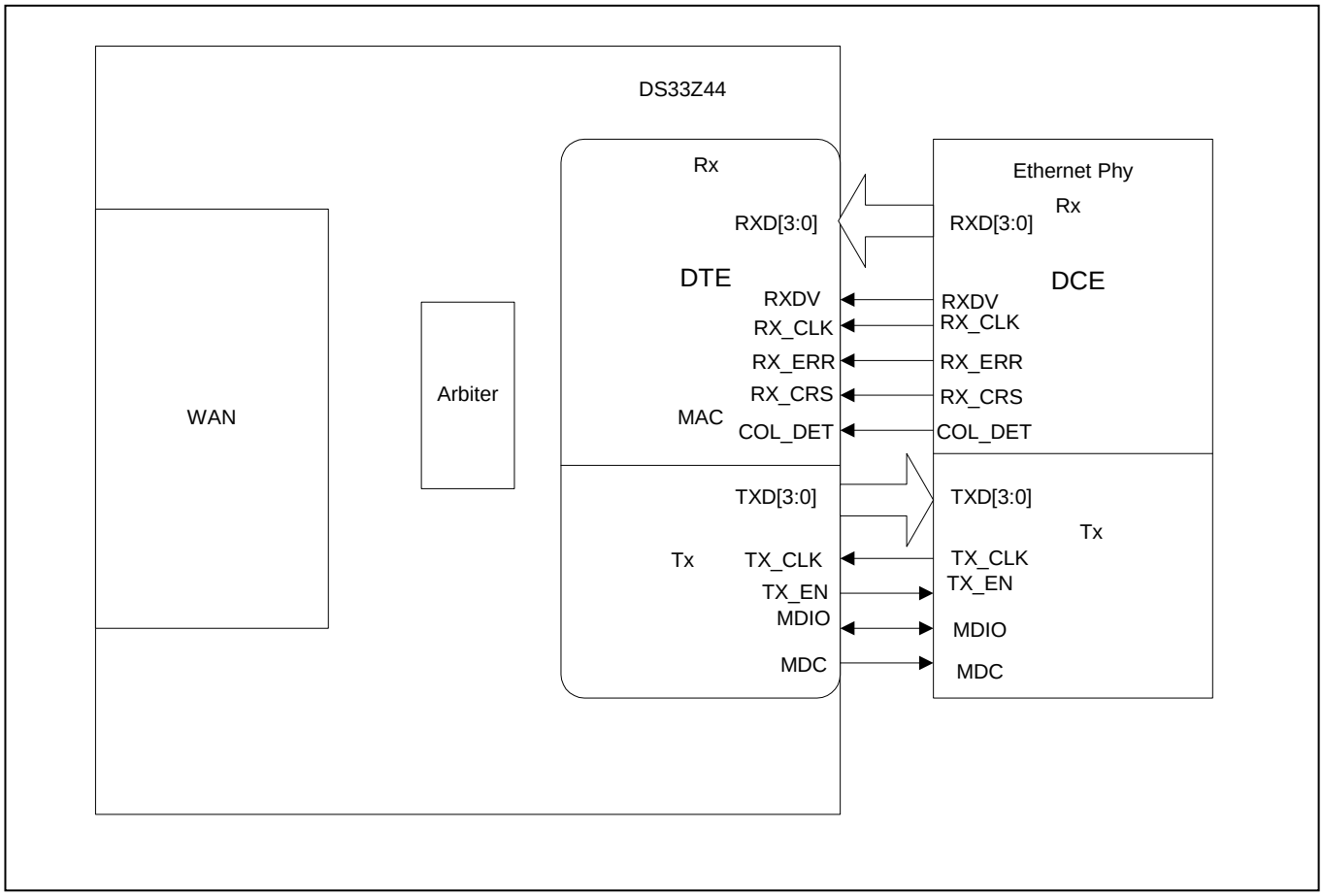
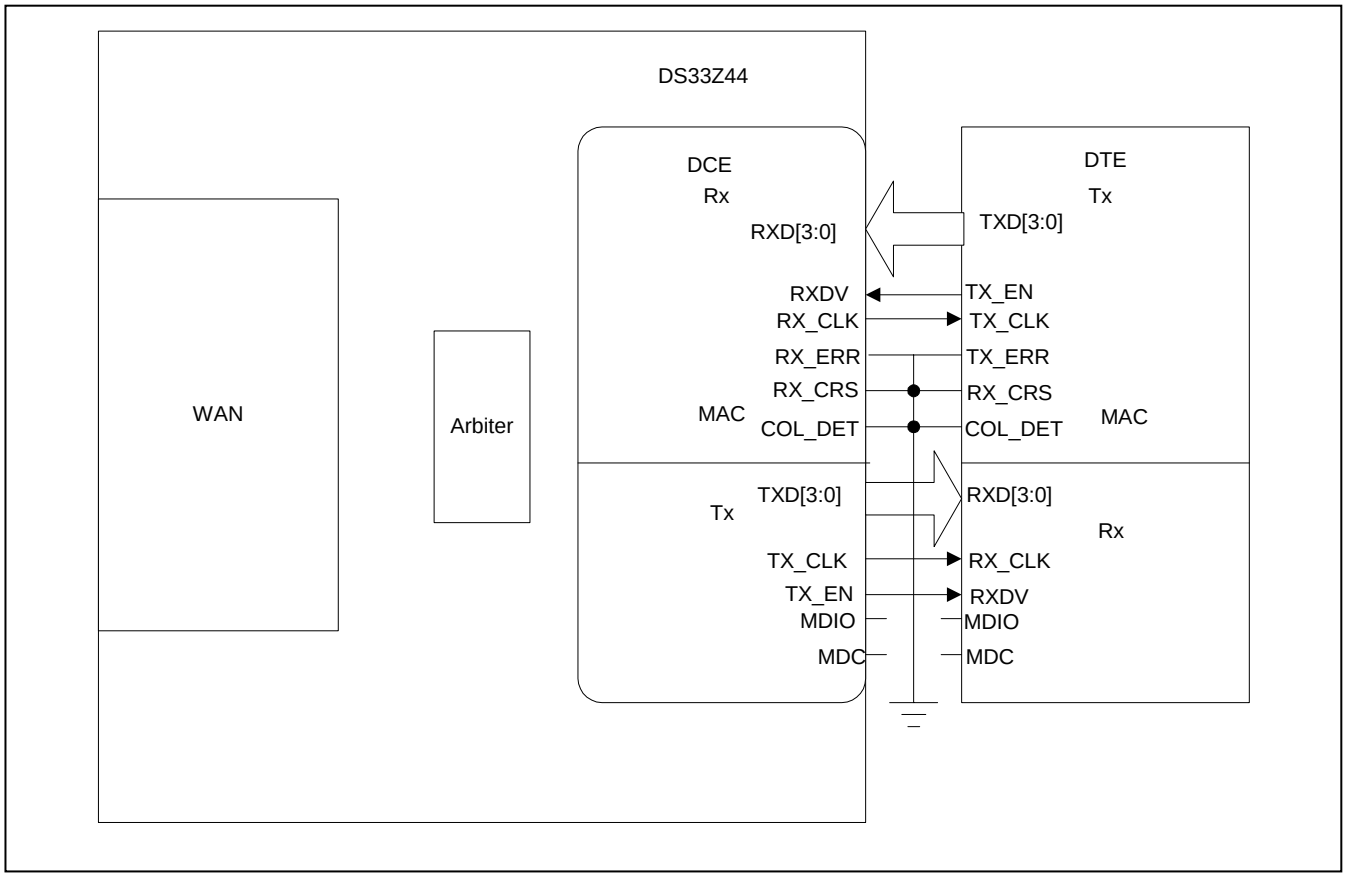


Figure 8-8. DS33Z44 Configured as a DCE in MII Mode



8.14 Ethernet MAC

Indirect addressing is required to access the MAC register settings. Writing to the MAC registers requires the SU.MACWD0-3 registers to be written with 4 bytes of data. The address must be written to SU.MACAWL and SU.MACAWH. A write command is issued by writing a zero to SU.MACRWC.MCRW and a one to MCS (MAC command status). MCS is cleared by the DS33Z44 when the operation is complete.

Reading from the MAC registers requires the SU.MACRADH and SU.MACRADL registers to be written with the address for the read operation. A read command is issued by writing a one to SU.MACRWC.MCRW and a zero to SU.MACRWC.MCS. SU.MACRWC.MCS is cleared by the DS33Z44 when the operation is complete. After MCS is clear, valid data is available in SU.MACRD0-SU.MACRD3. Note that only one operation can be initiated (read or write) at one time. Data cannot be written or read from the MAC registers until the MCS bit has been cleared by the device. The MAC Registers are detailed in the following table.

Table 8-7. MAC Control Registers

ADDRESS	REGISTER	DESCRIPTION
0000h–0003h	SU.MACCR	MAC Control Register. This register is used for programming full-duplex, half-duplex, promiscuous mode, and back-off limit for half-duplex. The transmit and receive enable bits must be set for the MAC to operate.
0004h–0007h	SU.MACAH	MAC Address High Register. This provides the physical address for this MAC.
0008h–000Bh	SU.MACAL	MAC Address Low Register. This provides the physical address for this MAC.
000Ch–000Fh	SU.MACMAH	Multicast Hash Table High Register.
0010h–0013h	SU.MACMAL	Multicast Hash Table Low Register.
0014h–0017h	SU.MACMIIA	MII Address Register (only available for MAC1). The user can specify the address for the access to the PHY through MDIO interface.
0018h–001Bh	SU.MACMIID	MII Data Register (only available for MAC1). The user can specify the data for the access to the PHY through MDIO interface.
001Ch–001Fh	SU.MACFCR	Flow Control Register.
0100h–0103h	SU.MMCCTRL	MMC Control Register bit 0 for resetting the status counters.

Table 8-8. MAC Status Registers

ADDRESS	REGISTER	DESCRIPTION
0200h–0203h	SU.RxFrmCntr	All Frames Received Counter.
0204h–0207h	SU.RxFrmOKCtr	Number of Received Frames that are Good.
0300h–0303h	SU.TxFrmCtr	Number of Frames Transmitted.
0308h–030Bh	SU.TxBytesCtr	Number of Bytes Transmitted.
030Ch–030Fh	SU.TxBytesOkCtr	Number of Bytes Transmitted with good frames.
0334h–0337h	SU.TxFrmUndr	Transmit FIFO underflow counter.
0338h–033Bh	SU.TxBdFrmsCtr	Transmit Number of Frames Aborted.

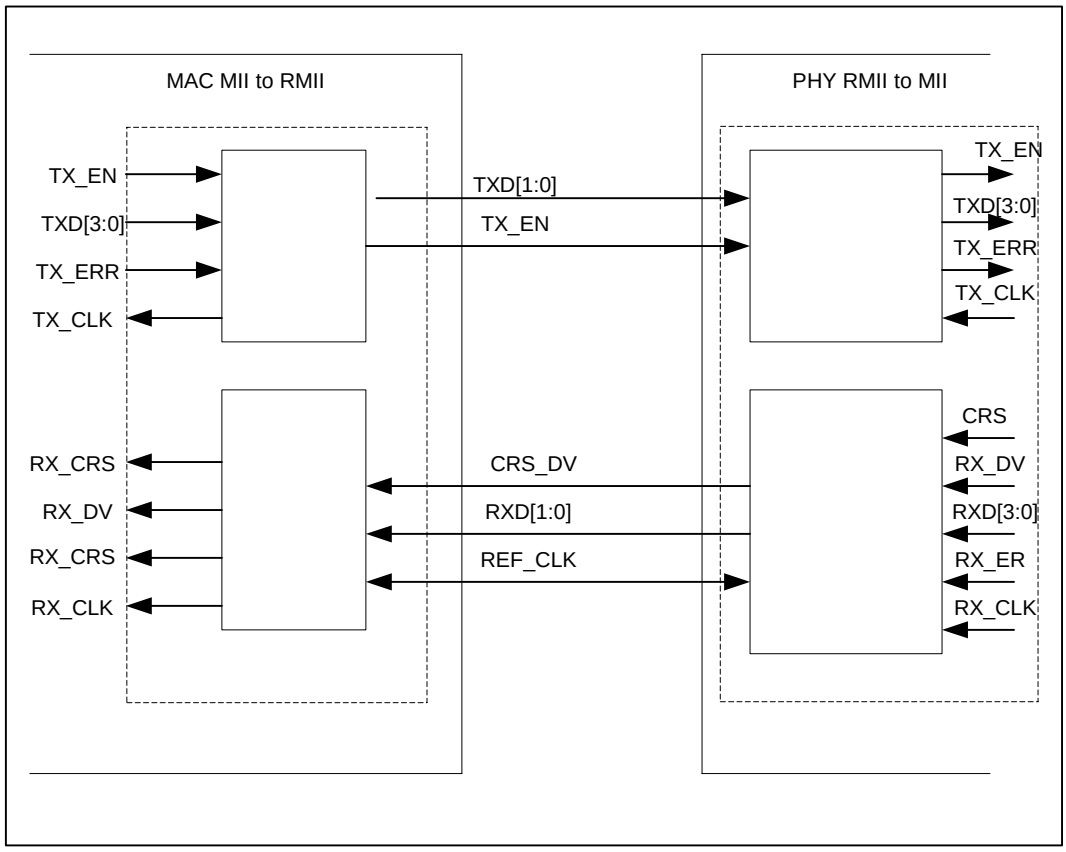
8.14.1 MII Mode Options

MODE/SPEED	FUNCTIONS
10Mbps half-duplex DTE with flow control off	Full-duplex/half-duplex is set through MAC registers. Hardware pin is used for DTE/DCE setting. In DTE the MII clocks are expected from the PHY interface. In DCE Mode the MII interface provides the clocks.
10Mbps half-duplex DTE with flow control	In half-duplex mode the flow control mechanism is backpressure. This is set by FCE bit in the MAC Control Register. The MAC will send JAM bits as required.
10Mbps full-duplex DTE Mode with no flow control	
100Mbps full-duplex, DTE with flow control	In full-duplex DTE mode the clocks are expected from the PHY. The flow control for a full-duplex operation is using control frames. If the MAC receives a pause command the Transmitter is disabled for the time specified in the pause command. The pause command has a multicast address 01-80-62-00-00-01. The MAC can also initiate a pause control frame by SU.GCR. The duration field in the pause control frame is determined by settings in the MAC Flow Control Register.
100Mbps half-duplex, DTE with no flow control	In half-duplex mode collisions are not ignored.
100Mbps half-duplex, DTE with flow control	In half-duplex mode collisions are not ignored. The flow control is through backpressure.
100Mbps full-duplex, DTE with no flow control	
100Mbps full-duplex DCE mode	In full-duplex DCE mode the clocks are provided by the DS33Z44. This clock is derived from the REF_CLK.
100Mbps half-duplex DCE mode with flow control	In full-duplex DCE mode the clocks are provided by the DS33Z44. The flow control for a full-duplex operation is using control frames. If the MAC receives a pause command the Transmitter is disabled for the time specified in the pause command. The pause command has a multicast address 01-80-62-00-00-01. The MAC can also initiate a pause control frame by SU.GCR. The duration field in the pause control frame is determined by settings in the MAC Flow Control Register.
100Mbps full-duplex DCE mode with flow control	In full-duplex DCE mode the clocks are provided by the DS33Z44. The flow control for a full-duplex operation is using control frames. If the MAC receives a pause command the Transmitter is disabled for the time specified in the pause command. The pause command has a multicast address 01-80-62-00-00-01. The MAC can also initiate a pause control frame by SU.GCR.The duration field in the pause control frame is determined by settings in the MAC Flow Control Register.

8.14.2 RMII Mode

RMII interface operates synchronously from the external 50MHz reference (REF_CLK). Only 8 signals are required. The following figure shows the RMII architecture. Note that DCE mode is not supported for RMII mode and RMII is valid only for full-duplex operation.

Figure 8-9. RMII Interface



8.14.3 PHY MII Management Block and MDIO Interface

The MII Management Block allows for the host to control up to 32 PHYs, each with 32 registers. The MII block communicates with the external PHY using 2-wire Serial Interface composed of MDC (serial clock) and MDIO for data. The MDIO data is valid on the rising edge of the MDC clock. The Frame format for the MII Management Interface is shown Figure 8-10. The read/write control of the MII Management is accomplished through the indirect SU.MACMIIA MII Management Address Register and data is passed through the indirect SU.MACMIID Data Register. These indirect registers are accessed through the MAC Control Registers defined in Table 8-7. The MDC clock is internally generated and runs at 1.67MHz. Note that the DS33Z44 provides a single MII Management port, and all control registers for this function are located in MAC 1.

Figure 8-10. MII Management Frame

	Preamble 32 bits	Start 2 bits	Opcode 2 bits	Phy Adrs 5 bits	Phy Reg 5 bits	Turnaround 2 bits	Data 16 bits	Idle 1 Bit
READ	111...111	01	10	PHYA[4:0]	PHYR[4:0]	ZZ	ZZZZZZZZZZ	Z
WRITE	111...111	01	01	PHYA[4:0]	PHYR[4:0]	10	PHYD[15:0]	Z

8.15 BERT

The BERT can be used for generation and detection of BERT patterns. The BERT is a software programmable test pattern generator and monitor capable of meeting most error performance requirements for digital transmission equipment. The following restrictions are related to the BERT:

- The RDEN1-4 and TDEN1-4 are inputs that can be used to “gap” bits.
- BERT will transmit even when the device is set for X.86 mode and TDENn is configured as an output
- The normal traffic flow is halted while the BERT is in operation.
- If the BERT is enabled for a Serial port, it will override the normal connection.
- If there is a connection overridden by the BERT, when BERT operation is terminated the normal operation is restored.

The transmit direction generates the programmable test pattern, and inserts the test pattern payload into the data stream. The receive direction extracts the test pattern payload from the receive data stream, and monitors the test pattern payload for the programmable test pattern.

8.15.1 BERT Features

- **PRBS and QRSS pattern** – 2^9-1, 2^{15}-1 2^{23}-1, and QRSS pattern support.
- **Programmable repetitive pattern** – The repetitive pattern length and pattern are programmable (length n = 1 to 32 and pattern = 0 to (2^n – 1).
- **24-bit error count and 32-bit bit count registers.**
- **Programmable bit error insertion** – Errors can be inserted individually.

8.15.2 Receive Data Interface

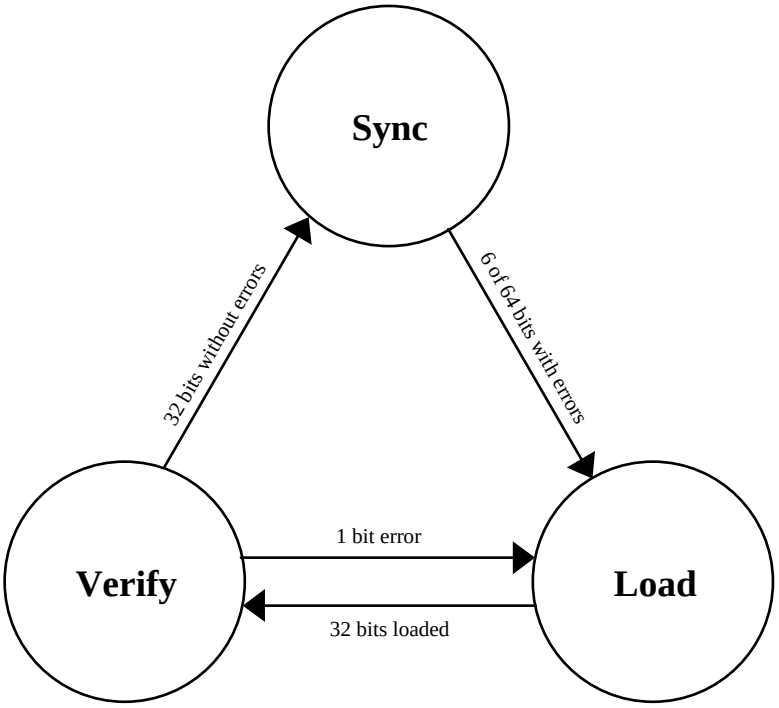
8.15.2.1 Receive Pattern Detection

The Receive BERT receives only the payload data and synchronizes the receive pattern generator to the incoming pattern. The receive pattern generator is a 32-bit shift register that shifts data from the least significant bit (LSB) or bit 1 to the most significant bit (MSB) or bit 32. The input to bit 1 is the feedback. For a PRBS pattern (generating polynomial $x^n + x^y + 1$), the feedback is an XOR of bit n and bit y. For a repetitive pattern (length n), the feedback is bit n. The values for n and y are individually programmable (1 to 32). The output of the receive pattern generator is the feedback. If QRSS is enabled, the feedback is an XOR of bits 17 and 20, and the output is forced to one if the next 14 bits are all zeros. QRSS is programmable (on or off). For PRBS and QRSS patterns, the feedback is forced to one if bits 1 through 31 are all zeros. Depending on the type of pattern programmed, pattern detection performs either PRBS synchronization or repetitive pattern synchronization.

8.15.2.2 PRBS Synchronization

PRBS synchronization synchronizes the receive pattern generator to the incoming PRBS or QRSS pattern. The receive pattern generator is synchronized by loading 32 data stream bits into the receive pattern generator, and then checking the next 32 data stream bits. Synchronization is achieved if all 32 bits match the incoming pattern. If at least is incoming bits in the current 64-bit window do not match the receive pattern generator, automatic pattern resynchronization is initiated. Automatic pattern resynchronization can be disabled.

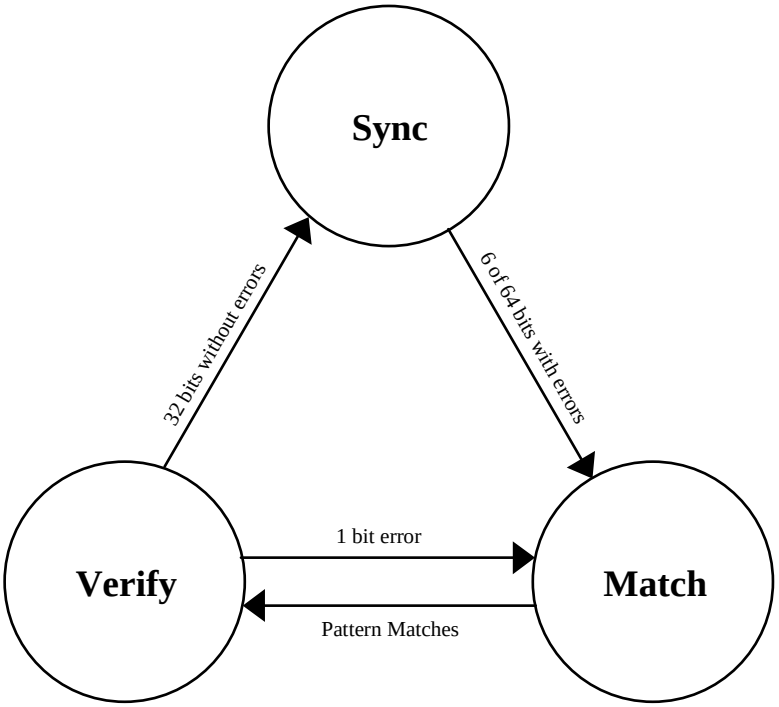
Figure 8-11. PRBS Synchronization State Diagram



8.15.3 Repetitive Pattern Synchronization

Repetitive pattern synchronization synchronizes the receive pattern generator to the incoming repetitive pattern. The receive pattern generator is synchronized by searching each incoming data stream bit position for the repetitive pattern, and then checking the next 32 data stream bits. Synchronization is achieved if all 32 bits match the incoming pattern. If at least sis incoming bits in the current 64-bit window do not match the receive PRBS pattern generator, automatic pattern resynchronization is initiated. Automatic pattern resynchronization can be disabled.

Figure 8-12. Repetitive Pattern Synchronization State Diagram



8.15.4 Pattern Monitoring

Pattern monitoring monitors the incoming data stream for Out Of Synchronization (OOS) condition, bit errors, and counts the incoming bits. An OOS condition is declared when the synchronization state machine is not in the “Sync” state. An OOS condition is terminated when the synchronization state machine is in the “Sync” state.

Bit errors are determined by comparing the incoming data stream bit to the receive pattern generator output. If they do not match, a bit error is declared, and the bit error and bit counts are incremented. If they match, only the bit count is incremented. The bit count and bit error count are not incremented when an OOS condition exists.

8.15.5 Pattern Generation

Pattern Generation generates the outgoing test pattern, and passes it onto Error Insertion. The transmit pattern generator is a 32-bit shift register that shifts data from the least significant bit (LSB) or bit 1 to the most significant bit (MSB) or bit 32. The input to bit 1 is the feedback. For a PRBS pattern (generating polynomial $x^n + x^y + 1$), the feedback is an XOR of bit n and bit y. For a repetitive pattern (length n), the feedback is bit n. The values for n and y are individually programmable. The output of the receive pattern generator is the feedback. If QRSS is enabled, the feedback is an XOR of bits 17 and 20, and the output is forced to one if the next 14 bits are all zeros. QRSS is programmable (on or off). For PRBS and QRSS patterns, the feedback is forced to one if bits 1 through 31 are all zeros. When a new pattern is loaded, the pattern generator is loaded with a pattern value before pattern generation starts. The pattern value is programmable ($0 – 2^n - 1$). When PRBS and QRSS patterns are generated the seed value is all ones.

8.15.5.1 Error Insertion

Error insertion inserts errors into the outgoing pattern data stream. Errors are inserted one at a time Single bit error insertion can be initiated from the microprocessor interface. If pattern inversion is enabled, the data stream is inverted before the overhead/stuff bits are inserted. Pattern inversion is programmable (on or off).

8.15.5.2 Performance Monitoring Update

All counters stop counting at their maximum count. A counter register is updated by asserting (low to high transition) the performance monitoring update signal (PMU). During the counter register update process, the performance monitoring status signal (PMS) is deasserted. The counter register update process consists of

loading the counter register with the current count, resetting the counter, forcing the zero count status indication low for one clock cycle, and then asserting PMS. No events shall be missed during an update procedure.

8.16 Serial Interfaces

The Serial Interfaces consist of a serial port and HDLC engine. The signals of the Serial Interface consist of Transmit Data, Transmit Clock, Transmit Enable, Receive Data, Receive Clock, and Receive Enable. The interface can be used to connect to T1/E1/T3/E3 framers and LIUs such as the D21458, DS3154, and DS3144. The following table outlines the registers that control the Serial Port.

Table 8-9. Serial Port Functions

REGISTER	FUNCTIONS
LI.TSLCR **LI.RSLCR**	These two registers are used for defining the settings of the Transmit and Receive Serial Interfaces. The enable signals for the data can be selected to have active high or low polarity. This is shown in LI.RSLCR and LI.TSLCR.

8.17 Transmit Packet Processor

The Transmit Packet Processor accepts data from the Transmit FIFO, and performs bit reordering, FCS processing, packet error insertion, stuffing, packet abort sequence insertion, interframe padding, and packet scrambling. The data output from the Transmit Packet Processor to the Transmit Serial Interface is a serial data stream (bit synchronous mode). HDLC processing can be disabled (clear channel enable). Disabling HDLC processing disables FCS processing, packet error insertion, stuffing, packet abort sequence insertion, and interframe padding. Only bit reordering and packet scrambling are not disabled.

Bit reordering changes the bit order of each byte. If bit reordering is disabled, the outgoing 8-bit data stream DT[1:8] with DT[1] being the MSB and DT[8] being the LSB is output from the Transmit FIFO with the MSB in TFD[7] (or 15, 23, or 31) and the LSB in TFD[0] (or 8, 16, or 24) of the transmit FIFO data TFD[7:0] 15:8, 23:16, or 31:24). If bit reordering is enabled, the outgoing 8-bit data stream DT[1:8] is output from the Transmit FIFO with the MSB in TFD[0] and the LSB in TFD[7] of the transmit FIFO data TFD[7:0]. In bit synchronous mode, DT [1] is the first bit transmitted. Bit Reordering can be controlled by address pin A0 in Hardware Mode.

FCS processing calculates an FCS and appends it to the packet. FCS calculation is a CRC-16 or CRC-32 calculation over the entire packet. The polynomial used for FCS-16 is $x^{16} + x^{12} + x^5 + 1$. The polynomial used for FCS-32 is $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$. The FCS is inverted after calculation. The FCS type is programmable. If FCS append is enabled, the calculated FCS is appended to the packet. If FCS append is disabled, the packet is transmitted without an FCS. The FCS append mode is programmable. If packet processing is disabled, FCS processing is not performed.

Packet error insertion inserts errors into the FCS bytes. A single FCS bit is corrupted in each errored packet. The FCS bit corrupted is changed from errored packet to errored packet. Error insertion can be controlled by a register or by the manual error insertion input (LI.TMEI.TMEI). The error insertion initiation type (register or input) is programmable. If a register controls error insertion, the number and frequency of the errors are programmable. If FCS append is disabled, packet error insertion will not be performed. If packet processing is disabled, packet error insertion is not performed.

Stuffing inserts control data into the packet to prevent packet data from mimicking flags. A packet start indication is received, and stuffing is performed until, a packet end indication is received. Bit stuffing consists of inserting a zero directly following any five contiguous oness. If packet processing is disabled, stuffing is not performed.

There is at least one flag plus a programmable number of additional flags between packets. The interframe fill can be flags or all ones followed by a start flag. If the interframe fill is all ones, the number of ones between the end and start flags does not need to be an integer number of bytes, however, there must be at least 15 consecutive ones between the end and start flags. The interframe padding type is programmable. If packet processing is disabled, interframe padding is not performed.

Packet abort insertion inserts a packet abort sequences as necessary. If a packet abort indication is detected, a packet abort sequence is inserted and interframe padding is done until a packet start flag is detected. The abort sequence is FFh. If packet processing is disabled, packet abort insertion is not performed.

The packet scrambler is a $x^{43} + 1$ scrambler that scrambles the entire packet data stream. The packet scrambler runs continuously, and is never reset. In bit synchronous mode, scrambling is performed one bit at a time. In byte synchronous mode, scrambling is performed 8 bits at a time. Packet scrambling is programmable. Note in Hardware Mode, the scrambling is controlled by A1/SD.

Once all packet processing has been completed serial data stream is passed on to the Transmit Serial Interface.

8.18 Receive Packet Processor

The Receive Packet Processor accepts data from the Receive Serial Interface performs packet descrambling, packet delineation, interframe fill filtering, packet abort detection, destuffing, packet size checking, FCS error monitoring, FCS byte extraction, and bit reordering. The data coming from the Receive Serial Interface is a serial data stream. Packet processing can be disabled (clear channel enable). Disabling packet processing disables packet delineation, interframe fill filtering, packet abort detection, destuffing, packet size checking, FCS error monitoring, and FCS byte extraction. Only packet descrambling and bit reordering are not disabled.

The packet descrambler is a self-synchronous $x^{43} + 1$ descrambler that descrambles the entire packet data stream. Packet descrambling is programmable. The descrambler runs continuously, and is never reset. The descrambling is performed one bit at a time. Packet descrambling is programmable. If packet processing is disabled, the serial data stream is demultiplexed in to an 8-bit data stream before being passed on. Note in Hardware Mode, the scrambling is controlled by A1/SD.

If packet processing is disabled, a packet boundary is arbitrarily chosen and the data is divided into "packets" of programmable size (dependent on maximum packet size setting). These packets are then passed on to bit reordering with packet start and packet end indications. Data then bypasses packet delineation, interframe fill filtering, packet abort detection, destuffing, packet size checking, FCS error monitoring, and FCS byte extraction.

Packet delineation determines the packet boundary by identifying a packet start or end flag. Each time slot is checked for a flag sequence (7Eh). Once a flag is found, it is identified as a start/end flag and the packet boundary is set. The flag check is performed one bit at a time. If packet processing is disabled, packet delineation is not performed.

Interframe fill filtering removes the interframe fill between packets. When a packet end flag is detected, all data is discarded until a packet start flag is detected. The interframe fill can be flags or all ones. The number of ones between flags does not need to be an integer number of bytes, and if at least seven ones are detected in the first 16 bits after a flag, all data after the flag is discarded until a start flag is detected. There may be only one flag between packets. When the interframe fill is flags, the flags may have a shared zero (0111111101111110). If there is less than 16 bits between two flags, the data is discarded. If packet processing is disabled, interframe fill filtering is not performed.

Packet abort detection searches for a packet abort sequence. Between a packet start flag and a packet end flag, if an abort sequence is detected, the packet is marked with an abort indication, the aborted packet count is incremented, and all subsequent data is discarded until a packet start flag is detected. The abort sequence is seven consecutive ones. If packet processing is disabled, packet abort detection is not performed.

Destuffing removes the extra data inserted to prevent data from mimicking a flag or an abort sequence. A start flag is detected, a packet start is set, the flag is discarded, destuffing is performed until an end flag is detected, a packet end is set, and the flag is discarded. In bit synchronous mode, bit destuffing is performed. Bit destuffing consists of discarding any zero that directly follows five contiguous ones. After destuffing is completed, the serial bit stream is demultiplexed into an 8-bit parallel data stream and passed on with packet start, packet end, and packet abort indications. If there is less than eight bits in the last byte, an invalid packet flag is raised, the packet is tagged with an abort indication, and the packet size violation count is incremented. If packet processing is disabled, destuffing is not performed.

Packet size checking checks each packet for a programmable maximum and programmable minimum size. As the packet data comes in, the total number of bytes is counted. If the packet length is below the minimum size limit, the packet is marked with an aborted indication, and the packet size violation count is incremented. If the packet length is above the maximum size limit, the packet is marked with an aborted indication, the packet size violation count is incremented, and all packet data is discarded until a packet start is received. The minimum and maximum lengths include the FCS bytes, and are determined after destuffing has occurred. If packet processing is disabled, packet size checking is not performed.

FCS error monitoring checks the FCS and aborts errored packets. If an FCS error is detected, the FCS errored packet count is incremented and the packet is marked with an aborted indication. If an FCS error is not detected, the receive packet count is incremented. The FCS type (16-bit or 32-bit) is programmable. If FCS processing or packet processing is disabled, FCS error monitoring is not performed.

FCS byte extraction discards the FCS bytes. If FCS extraction is enabled, the FCS bytes are extracted from the packet and discarded. If FCS extraction is disabled, the FCS bytes are stored in the receive FIFO with the packet. If FCS processing or packet processing is disabled, FCS byte extraction is not performed.

Bit reordering changes the bit order of each byte. If bit reordering is disabled, the incoming 8-bit data stream DT[1:8] with DT[1] being the MSB and DT[8] being the LSB is output to the Receive FIFO with the MSB in RFD[7] (or 15, 23, or 31) and the LSB in RFD[0] (or 8, 16, or 24) of the receive FIFO data RFD[7:0] (or 15:8, 23:16, or 31:24). If bit reordering is enabled, the incoming 8-bit data stream DT[1:8] is output to the Receive FIFO with the MSB in RFD[0] and the LSB in RFD[7] of the receive FIFO data RFD[7:0]. DT[1] is the first bit received from the incoming data stream. Bit reordering can be controlled by pin A0 in Hardware Mode.

Once all of the packet processing has been completed, the 8-bit parallel data stream is demultiplexed into a 32-bit parallel data stream. The Receive FIFO data is passed on to the Receive FIFO with packet start, packet end, packet abort, and modulus indications. At a packet end, the 32-bit word may contain 1, 2, 3, or 4 bytes of data depending on the number of bytes in the packet. The modulus indications indicate the number of bytes in the last data word of the packet.

8.19 X.86 Encoding and Decoding

X.86 protocol provides a method for encapsulating Ethernet Frame onto LAPS. LAPS provides a HDLC-type framing structure for encapsulation of Ethernet frames, but does not inflict dynamic bandwidth expansion as HDLC does. LAPS encapsulated frames can be used to send data onto a SONET/SDH network. The DS33Z44 expects a byte synchronization signal to provide the byte boundary for the X.86 receiver. This is provided by the RBSYN pin. The functional timing is shown in Figure 10-4. The X.86 transmitter provides a byte boundary indicator with the signal TBSYN. The functional timing is shown in Figure 10-3. Note that in some cases, additional logic may be required to meet RBSYNC/TBSYNC sychronization timing requirements when operating in X.86 mode.

Figure 8-13. LAPS Encoding of MAC Frames Concept

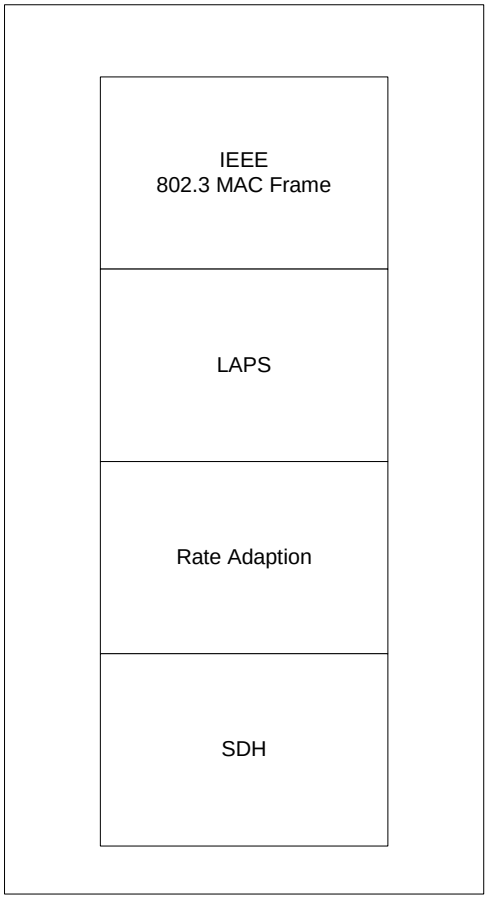
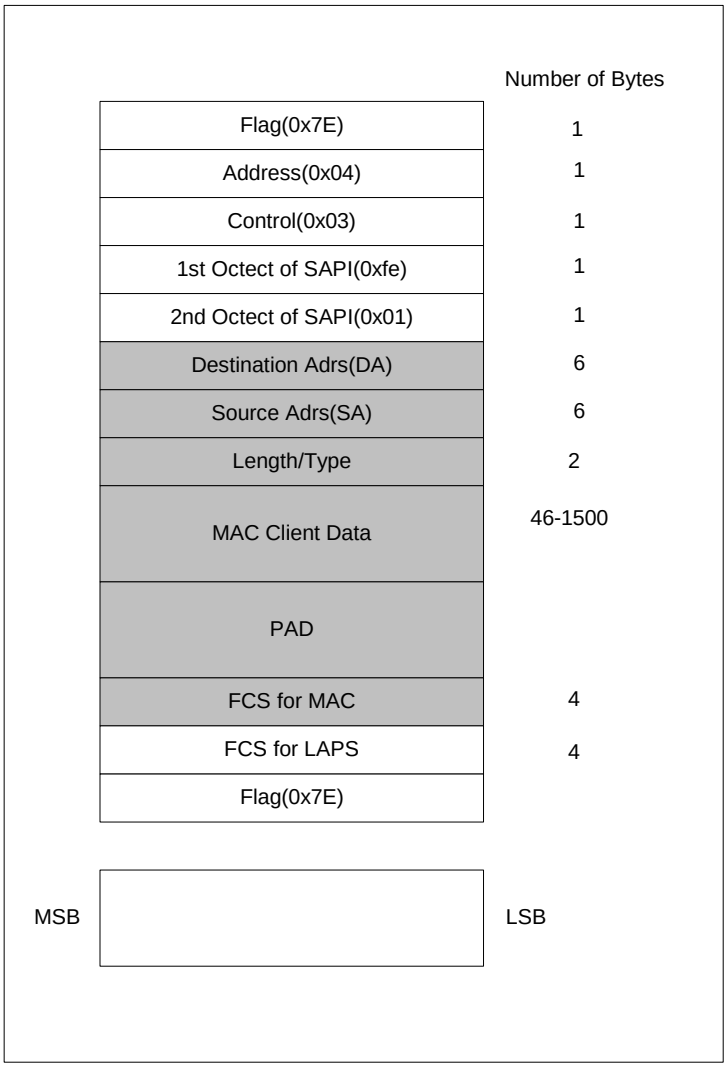


Figure 8-14. X.86 Encapsulation of the MAC Field



The DS33Z44 will encode the MAC Frame with the LAPS encapsulation on a complete serial stream if configured for X.86 mode in the register LI.TX86E. The DS33Z44 provides the following functions:

- Control Registers for Address, SAPI, Destination Address, Source Address.
- 32 bit FCS enabled.
- Programmable $X^{43}+1$ scrambling.

The sequence of processing performed by the receiver is as follows:

- Programmable octets $X^{43}+1$ descrambling.
- Detect the Start Flag (7E).
- Remove Rate adaptation octets 7d, dd.
- Perform transparency-processing 7d, 5e is converted to 7e and 7d, 5d is converted to 7d.
- Check for a valid Address, Control, and SAPI fields (LI.TRX86A to LI.TRX86SAPIL).
- Perform FCS checking.
- Detect the closing flag.

The X86 received frame is aborted if:

- If 7d, 7E is detected. This is an abort packet sequence in X.86.
- Invalid FCS is detected.
- The received frame has less than 6 octets.
- Control, SAPI, an d address field are mismatched to the programmed value.
- Octet 7d and octet other than 5d, 5e, 7e, or dd is detected.

For the transmitter if X.86 is enabled the sequence of processing is as follows:

- Construct frame including start flag SAPI, Control and MAC frame.
- Calculate FCS.
- Perform transparency processing - 7E is translated to 7D5E, 7D is translated to 7D5D.
- Append the end flag (7E).
- Scramble the sequence $X^{43}+1$.

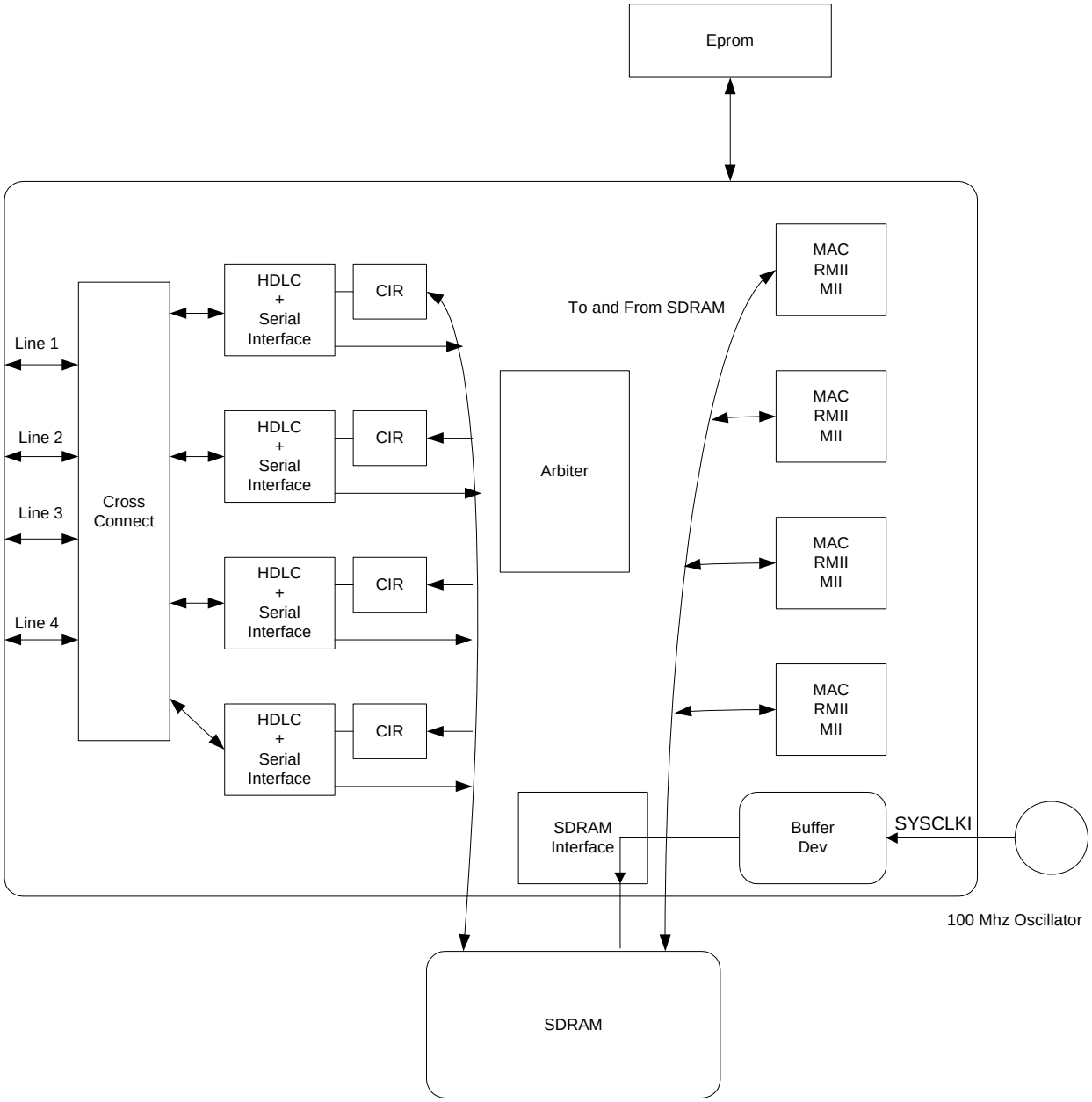
Note that the Serial transmit and receive registers apply to the X.86 implementations with specific exceptions. The exceptions are outlined in the Serial Interface transmit and receive register sections.

8.20 Committed Information Rate Controller

The DS33Z44 provides a CIR provisioning facility. The CIR can be used restricts the transport of received MAC data to a programmable rate. This is shown in Figure 8-15. The CIR will restrict the data flow from the Receive MAC to Transmit HDLC. This can be used for provisioning and billing functions towards the WAN. The user must set the CIR register to control the amount of data throughput from the MAC to HDLC transmit. The CIR register is in granularity of 500kbps with a range of 0 to 52Mbps. The operation of the CIR is as follows:

- The CIR block counts the credits that are accumulated at the end of every 125ms.
- If data is received and stored in the SDRAM to be sent to the Serial Interface, the interface will request the data if there is a positive credit balance. If the credit balance is negative, transmit interface does not request data.
- New credit balance is calculated credit balance = old credit balance – frame size in bytes after the frame is sent.
- The credit balance is incremented every 125ms by CIR/8.
- Credit balances not used in 250ms are reset to 0.
- The maximum value of CIR can not exceed the transmit line rate.
- If the data rate received from the Ethernet interface is higher than the CIR, the receive queue buffers will fill and the high threshold water mark will invoke flow control to reduce the incoming traffic rate.
- The CIR function is only available for software mode of operation only.
- CIR function is only available in data received at the Ethernet Interface to be sent to WAN. There is not CIR functionality for data arriving from the WAN to be sent to the Ethernet Interface.
- Negative credits are not allowed, if there is not a credit balance, no frames are sent until there is a credit balance again.

Figure 8-15. CIR in the WAN Transmit Path



8.21 Hardware Mode

The hardware mode settings are provided for users who do not want to utilize a microprocessor or EEPROM. The hardware mode default queue sizes and watermark thresholds can be selected for various line rates using the MODEC pins. The user can control the DTE/DCE, RMII/MII and Half-Duplex/Full-Duplex and setting with hardware pins DCEDTES, RMIIMIIS, and FULLDS1-4 selection. The flow control (pause and back pressure) can be configured with the AFCS1-4 hardware pins. The user can also control bit order, data scrambling, and X.86 encapsulation using the A0, A1, and A2 pins, respectively.

The DS33Z44 has three different default hardware settings. This is outlined in the following tables. The typical applications for each of the Hardware Modes are outlined in following tables. Note that in the hardware only mode the following restrictions apply:

- The ports are powered up and ready to transmit/receive after reset.
- BERT functionality is not supported in Hardware Mode.
- Queue size and watermarks are fixed.
- Receive and Transmit HDLC FCS are 16 bits.
- Transmit Packets are resent if errors occur, Receive Packets are rejected if errors occur.
- Transmission of errored packets is not supported in hardware mode.
- MII, RMII, Full- and Half-Duplex, Automatic flow control, DTE, DCE, 100Mbps, or 10Mbps can be selected through Hardware Pins.
- TDENn and RDENn are not supported and should be tied high.
- CIR function is not supported in Hardware Mode.

Table 8-10. Hardware Modes and Applications

MODEC PIN SETTINGS	APPLICATIONS
00	Serial Interfaces 1 to 4 connected to T1/E1 Lines or T3/E3 and Ethernet Interfaces 1 to 4 set to 10Mbps or 100Mbps LAN MII or RMII. All transmitters and receivers are enabled for communication.
01	Serial Interfaces 1 to 3 connected to T1/E1 Lines and Serial Interface 4 to T3/E3 and Ethernet Interfaces 1 to 4 set to 10Mbps or 100Mbps LAN MII or RMII. All transmitters and receivers are enabled for communication.
10	Serial Interfaces 1 and 2 are connected to T3/E3 lines and Serial Interfaces 3 and 4 are connected to T1/E1 Lines and Ethernet Interfaces 1 to 4 Setup to 10Mbps or 100Mbps LAN MII or RMII. All transmitters and receivers are enabled for communication.

The specific registers and detailed functions for each of the hardware modes are detailed in the following tables.

Table 8-11. Specific Functional Default Values for Hardware Mode

FUNCTIONAL BLOCK	REGISTER REFERENCE	DEFAULT VALUE IN HARDWARE MODE	DESCRIPTION
Global			
Connections Between Serial Ports and Ethernet Interfaces	GL.CON1 GL.CON2 GL.CON3 GL.CON4	0000 0001b 0000 0010b 0000 0011b 0000 0100b	Connection established for Serial 1 to Ethernet 1, Serial 2 to Ethernet 2, Serial 3 to Ethernet 3, and Serial 4 to Ethernet 4.
Serial Data			
Transmit Serial Interface Configuration	LI.TSLCR	0000 0000b	Transmit Data enable is not supported and should be tied high. The user must provide gapped clocks to mask bits if needed. The Transmit Serial data will output on the rising edge of TCLKI1-4.
Serial Interface Reset and Power-Down	LI.RSTPD	0000 0000b	In default hardware mode the Serial Interface Transmitter is powered up and ready to go.
Transmit FCS	LI.TPPCL	0001 0000*	FCS is 16 bits for HDLC Transmitter
Transmit Interfame Gap	LI.TIFGC	0000 0001b	Transmit inter frame gap is one byte. The value is 7E.
Receive FCS	LI.RPPCL	0001 0000b*	Receive HDLC FCS is set to 16 bits. Receive scrambling and bit ordering controlled by hardware pins
Receive Maximum Packet Length	LI.RMPSC	2016 bytes	The receive maximum packet length is set to 2016 bytes not including the HDLC FCS. Any packets greater than 2016 bytes are rejected.
Receive Serial Port Configuration	LI.RSLCR	0000 0000b	Receive RDENn enable will not be supported and should be tied high. The Received data is sampled on the falling edge and gapped clock is supported.
Transmit Packet Resend Criteria	SU.TFRC	0000 0000b	Any error: Jabber timeout, Loss of carrier, Excessive deferral, Late collision, Excessive collisions, Under run, collision, deferred, heartbeat fail will result in resending of packets
Receive Packet Rejection Control	SU.RFRC	0000 0000b	Received packets are rejected if any receive errors occur
Receiver Maximum Frame Size	SU.RMFSRH SU.RMFSRL	0000 0111 1110 0000b	The maximum receiver packet size is 2016 bytes including the MAC FCS. Any packet larger that 2016 is rejected
Ethernet			
MAC Control Register	SU.MACCR	1001 0000 0000 0100 0000 0000 0000 0000b*	Duplex mode(bit 20) is determined by the FULLDS pin (MSB to LSB)
MAC Flow Control Register	SU.MACFCR	0000 0001 0100 0000 0000 0000 0000 0000b*	Flow control is determined by the AFCSn pin. Pause Timer = 140 Slots (MSB to LSB)
Queue Size and Thresholds			

FUNCTIONAL BLOCK	REGISTER REFERENCE	DEFAULT VALUE IN HARDWARE MODE	DESCRIPTION
Connection Transmit Queue Size	AR.TQSC1-4	640 packets	Modec[1:0] = 00
	AR.TQSC1-3	512 packets	Modec[1:0] = 01
	AR.TQSC4	640 packets	Modec[1:0] = 01
	AR.TQSC1-2	768 packets	Modec[1:0] = 10
	AR.TQSC3-4	640 packets	Modec[1:0] = 10
Transmit Queue High Threshold	LI.TQHT (ports 1-4)	384 packets	Modec[1:0] = 00
	LI.TQHT (ports 1-4)	384 packets	Modec[1:0] = 01
	LI.TQHT (ports 1-4)	384 packets	Modec[1:0] = 01
Transmit Queue Low Threshold	LI.TQLT (ports 1-4)	192 packets*	Modec[1:0] = 00
	LI.TQLT (ports 1-4)	192 packets*	Modec[1:0] = 01
	LI.TQLT (ports 1-4)	192 packets*	Modec[1:0] = 10
Receive Queue Size	AR.RQSC1-4	1408 packets*	Modec[1:0] = 00
	AR.RQSC1-3	1536 packets*	Modec[1:0] = 01
	AR.RQSC4	1408 packets*	Modec[1:0] = 01
	AR.RQSC1-2	1280 packets*	Modec[1:0] = 10
	AR.RQSC3-4	1408 packets*	Modec[1:0] = 10
Receive Queue Low Threshold	SU.RQLT (ports 1-4)	480 packets*	Modec[1:0] = 00
	SU.RQLT (ports 1-4)	512 packets*	Modec[1:0] = 01
	SU.RQLT (ports 1-2)	384 packets*	Modec[1:0] = 10
	SU.RQLT (ports 3-4)	480 packets*	Modec[1:0] = 10
Receive Queue High Threshold	SU.RQHT (ports 1-4)	960 packets*	Modec[1:0] = 00
	SU.RQHT (ports 1-4)	1024 packets*	Modec[1:0] = 01
	SU.RQHT (ports 1-2)	768 packets*	Modec[1:0] = 10
	SU.RQHT (ports 3-4)	960 packets*	Modec[1:0] = 10

** The default values for these registers are different than in the Software mode.*

Note: *Each "packet" above is 2048 bytes.*

Table 8-12. Hardware Mode Pins

PIN	HARDWARE MODE FUNCTION
HWMODE	0 = Hardware Mode disabled. 1 = Hardware Mode enabled.
MODEC[1:0]	Select the hardware mode default settings.
RMIIMIIS	0 = MII Operation. Applies to all four ports. 1 = RMII operation. Applies to all four ports.
DCEDTES	1 = DCE Operation 0 = DTE Operation
FULLDSn	0 = Half-Duplex Mode. 1 = Full-Duplex Mode.
A2/X86ED	0 = X.86 mode is disabled. 1 = X.86 mode is enabled for transmit and receive.
A1/SCD	0 = X^{43}+1 scrambling/descrambling is enabled. 1 = X^{43}+1 scrambling/descrambling is disabled.
A0/BREO	0 = HDLC transmit and receive bits are normal. The MSB is transmitted and received first. 1 = HDLC transmit and receive bits are reversed. The LSB is transmitted and received first.

9 DEVICE REGISTERS

Ten address lines are used to address the register space. Table 9-1 shows the register map for the DS33Z44. The addressable range for the device is 0000h to 08FFh. Each Register Section is 64 bytes deep. Global Registers are preserved for software compatibility with multiport devices. The Serial Interface (Line) Registers are used to configure the serial port and the associated transport protocol. The Ethernet Interface (Subscriber) registers are used to control and observe each of the Ethernet ports. The registers associated with the MAC must be configured through indirect register write /read access due to the architecture of the device.

When writing to a register input values for unused bits and registers (those designated with "–") should be zero unless specifically noted otherwise, as these bits and registers are reserved. When a register is read from, the values of the unused bits and registers should be ignored. A latched status bit is set when an event happens and is cleared when read.

The register details are provided in the following tables.

Table 9-1. Register Address Map

	GLOBAL REGISTERS	ARBITER	BERT	SERIAL INTERFACE	ETHERNET INTERFACE
	0000h – 003Fh	0040h – 007Fh	0080h – 00BFh	-	-
Port 1	-	-	-	00C0h – 013Fh	0140h – 017Fh
Port 2	-	-	-	0180h – 01FFh	0200h – 023Fh
Port 3	-	-	-	0240h – 02BFh	02C0h – 02FFh
Port 4	-	-	-	0300h – 037Fh	0380h – 03BFh

Reserved address space: 03C0h-07FFh

9.1 Register Bit Maps

9.1.1 Global Register Bit Map

Table 9-2. Global Register Bit Map

ADDR	Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
000h	GL.IDRL	ID07	ID06	ID05	ID04	ID03	ID02	ID01	ID00
001h	GL.IDRH	ID15	ID14	ID13	ID12	ID11	ID10	ID09	ID08
002h	GL.CR1	-	-	-	-	-	REF_CLKO	INTM	RST
003h	GL.BLR	-	-	-	-	GL.BLC4	GL.BLC3	GL.BLC2	GL.BLC1
004h	GL.RTCAL	RLCALS4	RLCALS3	RLCALS2	RLCALS1	TLCALS4	TLCALS3	TLCALS2	TLCALS1
005h	GL.SRCALS	-	-	-	-	-	-	REFCLKS	SYSCLS
006h	GL.LIE	LIN4TIE	LIN3TIE	LIN2TIE	LIN1TIE	LIN4RIE	LIN3RIE	LIN2RIE	LIN1RIE
007h	GL.LIS	LIN4TIS	LIN3TIS	LIN2TIS	LIN1TIS	LIN4RIS	LIN3RIS	LIN2RIS	LIN1RIS
008h	GL.SIE	-	-	-	-	SUB4IE	SUB3IE	SUB2IE	SUB1IE
009h	GL.SIS	-	-	-	-	SUB4IS	SUB3IS	SUB2IS	SUB1IS
00Ah	GL.TRQIE	TQ4IE	TQ3IE	TQ2IE	TQ1IE	RQ4IE	RQ3IE	RQ2IE	RQ1IE
00Bh	GL.TRQIS	TQ4IS	TQ3IS	TQ2IS	TQ1IS	RQ4IS	RQ3IS	RQ2IS	RQ1IS
00Ch	GL.BIE	-	-	-	-	-	-	-	BIE
00Dh	GL.BIS	-	-	-	-	-	-	-	BIS
00Eh	GL.CON1	-	-	-	-	-	LINE1[2]	LINE1[1]	LINE1[0]
00Fh	**GL.CON2**	-	-	-	-	-	LINE2[2]	LINE2[1]	LINE2[0]
010h	**GL.CON3**	-	-	-	-	-	LINE3[2]	LINE3[1]	LINE3[0]
011h	**GL.CON4**	-	-	-	-	-	LINE4[2]	LINE4[1]	LINE4[0]
012h	GL.C1QPR	-	-	-	-	C1MRPRR	C1HWPRR	C1MHPR	C1HRPR
013h	**GL.C2QPR**	-	-	-	-	C2MRPRR	C2HWPRR	C2MHPR	C2HRPR
014h	**GL.C3QPR**	-	-	-	-	C3MRPRR	C3HWPRR	C3MHPR	C3HRPR
015h	**GL.C4QPR**	-	-	-	-	C4MRPRR	C4HWPRR	C4MHPR	C4HRPR
020h	GL.BISTEN	-	-	-	-	-	-	-	BISTE
021h	GL.BISTPF	-	-	-	-	-	-	BISTDN	BISTPF
03Ah	**GL.SDMODE1**	-	-	-	-	WT	BL2	BL1	BL0
03Bh	**GL.SDMODE2**	-	-	-	-	-	LTMOD2	LTMOD1	LTMOD0
03Ch	**GL.SDMODEWS**	-	-	-	-	-	-	-	SDMW
03Dh	**GL.SDRFTC**	SREFT7	SREFT6	SREFT5	SREFT4	SREFT3	SREFT2	SREFT1	SREFT0

All address locations not listed are reserved.

9.1.2 Arbiter Register Bit Map

Table 9-3 contains the Arbiter registers of the DS33Z44. Bits that are reserved are noted with a single dash "-". All registers not listed are reserved and should be initialized with a value of 00h for proper operation.

Table 9-3. Arbiter Register Bit Map

ADDR	NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
040h	**AR.RQSC1**	RQSC1[7]	RQSC1[6]	RQSC1[5]	RQSC1[4]	RQSC1[3]	RQSC1[2]	RQSC1[1]	RQSC1[0]
041h	**AR.TQSC1**	TQSC1[7]	TQSC1[6]	TQSC1[5]	TQSC1[4]	TQSC1[3]	TQSC1[2]	TQSC1[1]	TQSC1[0]
042h	**AR.RQSC2**	RQSC2[7]	RQSC2[6]	RQSC2[5]	RQSC2[4]	RQSC2[3]	RQSC2[2]	RQSC2[1]	RQSC2[0]
043h	**AR.TQSC2**	TQSC2[7]	TQSC2[6]	TQSC2[5]	TQSC2[4]	TQSC2[3]	TQSC2[2]	TQSC2[1]	TQSC2[0]
044h	**AR.RQSC3**	RQSC3[7]	RQSC3[6]	RQSC3[5]	RQSC3[4]	RQSC3[3]	RQSC3[2]	RQSC3[1]	RQSC3[0]
045h	**AR.TQSC3**	TQSC3[7]	TQSC3[6]	TQSC3[5]	TQSC3[4]	TQSC3[3]	TQSC3[2]	TQSC3[1]	TQSC3[0]
046h	**AR.RQSC4**	RQSC4[7]	RQSC4[6]	RQSC4[5]	RQSC4[4]	RQSC4[3]	RQSC4[2]	RQSC4[1]	RQSC4[0]
047h	**AR.TQSC4**	TQSC4[7]	TQSC4[6]	TQSC4[5]	TQSC4[4]	TQSC4[3]	TQSC4[2]	TQSC4[1]	TQSC4[0]

9.1.3 BERT Register Bit Map

Table 9-4. BERT Register Bit Map

ADDR	NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
080h	**BCR**	-	PMU	RNPL	RPIC	MPR	APRD	TNPL	TPIC
081h	**Reserved**	-	-	-	-	-	-	-	-
082h	**BPCLR**	-	QRSS	PTS	PLF4	PLF3	PLF2	PLF1	PLF0
083h	**BPCHR**	-	-	-	PTF4	PTF3	PTF2	PTF1	PTF0
084h	**BSPB0R**	BSP7	BSP6	BSP5	BSP4	BSP3	BSP2	BSP1	BSP0
085h	**BSPB1R**	BSP15	BSP14	BSP13	BSP12	BSP11	BSP10	BSP9	BSP8
086h	**BSPB2R**	BSP23	BSP22	BSP21	BSP20	BSP19	BSP18	BSP17	BSP16
087h	**BSPB3R**	BSP31	BSP30	BSP29	BSP28	BSP27	BSP26	BSP25	BSP24
088h	**TEICR**	-	-	TIER2	TIER1	TIER0	BEI	TSEI	-
08Ah	**Reserved**	-	-	-	-	-	-	-	-
08Bh	**Reserved**	-	-	-	-	-	-	-	-
08Ch	**BSR**	-	-	-	-	PMS	-	BEC	OOS
08Dh	**Reserved**	-	-	-	-	-	-	-	-
08Eh	**BSRL**	-	-	-	-	PMSL	BEL	BECL	OOSL
08Fh	**Reserved**	-	-	-	-	-	-	-	-
090h	**BSRIE**	-	-	-	-	PMSIE	BEIE	BECIE	OOSIE
091h	**Reserved**	-	-	-	-	-	-	-	-
092h	**Reserved**	-	-	-	-	-	-	-	-
093h	**Reserved**	-	-	-	-	-	-	-	-
094h	**RBECB0R**	BEC7	BEC6	BEC5	BEC4	BEC3	BEC2	BEC1	BEC0
095h	**RBECB1R**	BEC15	BEC14	BEC13	BEC12	BEC11	BEC10	BEC9	BEC8
096h	**RBECB2R**	BEC23	BEC22	BEC21	BEC20	BEC19	BEC18	BEC17	BEC16
097h	**Reserved**	-	-	-	-	-	-	-	-
098h	**RBCB0**	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0
099h	**RBCB1**	BC15	BC14	BC13	BC12	BC11	BC10	BC9	BC8
09Ah	**RBCB2**	BC23	BC22	BC21	BC20	BC19	BC18	BC17	BC16
09Bh	**RBCB3**	BC31	BC30	BC29	BC28	BC27	BC26	BC25	BC24
09Ch	**Reserved**	-	-	-	-	-	-	-	-
09Dh	**Reserved**	-	-	-	-	-	-	-	-
09Eh	**Reserved**	-	-	-	-	-	-	-	-
09Fh	**Reserved**	-	-	-	-	-	-	-	-

9.1.4 Serial Interface Register Bit Map

Table 9-5. Serial Interface Register Bit Map

ADDR	NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0C0h	LI.TSLCR	-	-	-	-	-	-	-	TDENPLT
0C1h	LI.RSTPD	-	-	-	-	-	-	RESET	-
0C2h	LI.LPBK	-	-	-	-	-	-	-	QLP
0C3h	**Reserved**								
0C4h	LI.TPPCL	-	-	TFAD	TF16	TIFV	TSD	TBRE	-
0C5h	LI.TIFGC	TIFG7	TIFG6	TIFG5	TIFG4	TIFG3	TIFG2	TIFG1	TIFG0
0C6h	LI.TEPLC	TPEN7	TPEN6	TPEN5	TPEN4	TPEN3	TPEN2	TPEN1	TPEN0
0C7h	LI.TEPHC	MEIMS	TPER6	TPER5	TPER4	TPER3	TPER2	TPER1	TPER0
0C8h	LI.TPPSR	-	-	-	-	-	-	-	TEPF
0C9h	LI.TPPSRL	-	-	-	-	-	-	-	TEPFL
0CAh	LI.TPPSRIE	-	-	-	-	-	-	-	TEPFIE
0CBh	**Reserved**	-	-	-	-	-	-	-	-
0CCh	LI.TPCR0	TPC7	TPC6	TPC5	TPC4	TPC3	TPC2	TPC1	TPC0
0CDh	LI.TPCR1	TPC15	TPC14	TPC13	TPC12	TPC11	TPC10	TPC9	TPC8
0CEh	LI.TPCR2	TPC23	TPC22	TPC21	TPC20	TPC19	TPC18	TPC17	TPC16
0CFh	**Reserved**	-	-	-	-	-	-	-	-
0D0h	LI.TBCR0	TBC7	TBC6	TBC5	TBC4	TBC3	TBC2	TBC1	TBC0
0D1h	LI.TBCR1	TBC15	TBC14	TBC13	TBC12	TBC11	TBC10	TBC9	TBC8
0D2h	LI.TBCR2	TBC23	TBC22	TBC21	TBC20	TBC19	TBC18	TBC17	TBC16
0D3h	LI.TBCR3	TBC31	TBC30	TBC29	TBC28	TBC27	TBC26	TBC25	TBC24
0D4h	LI.TMEI	-	-	-	-	-	-	-	TMEI
0D5h	**Reserved**	-	-	-	-	-	-	-	-
0D6h	LI.THPMUU	-	-	-	-	-	-	-	TPMUU
0D7h	LI.THPMUS	-	-	-	-	-	-	-	TPMUS
0D8h	LI.TX86EDE	-	-	-	-	-	-	-	X86ED
0D9h	LI.TRX86A	X86TRA7	X86TRA6	X86TRA5	X86TRA4	X86TRA3	X86TRA2	X86TRA1	X86TRA0
0DAh	LI.TRX8C	X86TRC7	X86TRC6	X86TRC5	X86TRC4	X86TRC3	X86TRC2	X86TRC1	X86TRC0
0DBh	LI.TRX86SAPIH	TRSAPIH7	TRSAPIH6	TRSAPIH5	TRSAPIH4	TRSAPIH3	TRSAPIH2	TRSAPIH1	TRSAPIH0
0DCh	LI.TRX86SAPIL	TRSAPIL7	TRSAPIL6	TRSAPIL5	TRSAPIL4	TRSAPIL3	TRSAPIL2	TRSAPIL1	TRSAPIL0
0DDh	LI.CIR	CIRE	CIR6	CIR5	CIR4	CIR3	CIR2	CIR1	CIR0
100h	LI.RSLCR	-	-	-	-	-	-	-	RDENPLT
101h	LI.RPPCL	-	-	RFPD	RF16	RFED	RDD	RBRE	RCCE
102h	LI.RMPSCL	RMX7	RMX6	RMX5	RMX4	RMX3	RMX2	RMX1	RMX0
103h	LI.RMPSCH	RMX15	RMX14	RMX13	RMX12	RMX11	RMX10	RMX9	RMX8
104h	LI.RPPSR	-	-	-	-	-	REPC	RAPC	RSPC
105h	LI.RPPSRL	REPL	RAPL	RIPDL	RSPDL	RLPDL	REPCL	RAPCL	RSPCL
106h	LI.RPPSRIE	REPIE	RAPIE	RIPDIE	RSPDIE	RLPDIE	REPCIE	RAPCIE	RSPCIE
107h	**Reserved**								
108h	LI.RPCB0	RPC7	RPC6	RPC5	RPC4	RPC3	RPC2	RPC1	RPC0
109h	LI.RPCB1	RPC15	RPC14	RPC13	RPC12	RPC11	RPC10	RPC09	RPC08
10Ah	LI.RPCB2	RPC23	RPC22	RPC21	RPC20	RPC19	RPC18	RPC17	RPC16
10Ch	LI.RFPCB0	RFPC7	RFPC6	RFPC5	RFPC4	RFPC3	RFPC2	RFPC1	RFPC0
10Dh	LI.RFPCB1	RFPC15	RFPC14	RFPC13	RFPC12	RFPC11	RFPC10	RFPC9	RFPC8
10Eh	LI.RFPCB2	RFPC23	RFPC22	RFPC21	RFPC20	RFPC19	RFPC18	RFPC17	RFPC16
10Fh	**Reserved**								
110h	LI.RAPCB0	RAPC7	RAPC6	RAPC5	RAPC4	RAPC3	RAPC2	RAPC1	RAPC0
111h	LI.RAPCB1	RAPC15	RAPC14	RAPC13	RAPC12	RAPC11	RAPC10	RAPC9	RAPC8

ADDR	NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
112h	**LI.RAPCB2**	RAPC23	RAPC22	RAPC21	RAPC20	RAPC19	RAPC18	RAPC17	RAPC16
113h	**Reserved**	-	-	-	-	-	-	-	-
114h	**LI.RSPCB0**	RSPC7	RSPC6	RSPC5	RSPC4	RSPC3	RSPC2	RSPC1	RSPC0
115h	**LI.RSPCB1**	RSPC15	RSPC14	RSPC13	RSPC12	RSPC11	RSPC10	RSPC9	RSPC8
116h	**LI.RSPCB2**	RSPC23	RSPC22	RSPC21	RSPC20	RSPC19	RSPC18	RSPC17	RSPC16
118h	**LI.RBC0**	RBC7	RBC6	RBC5	RBC4	RBC3	RBC2	RBC1	RBC0
119h	**LI.RBC1**	RBC15	RBC14	RBC13	RBC12	RBC11	RBC10	RBC9	RBC8
11Ah	**LI.RBC2**	RBC23	RBC22	RBC21	RBC20	RBC19	RBC18	RBC17	RBC16
11Bh	**LI.RBC3**	RBC31	RBC30	RBC29	RBC28	RBC27	RBC26	RBC25	RBC24
11Ch	**LI.RAC0**	REBC7	REBC6	REBC5	REBC4	REBC3	REBC2	REBC1	REBC0
11Dh	**LI.RAC1**	REBC15	REBC14	REBC13	REBC12	REBC11	REBC10	REBC9	REBC8
11Eh	**LI.RAC2**	REBC23	REBC22	REBC21	REBC20	REBC19	REBC18	REBC17	REBC16
11Fh	**LI.RAC3**	REBC31	REBC30	REBC29	REBC28	REBC27	REBC26	REBC25	REBC24
120h	**LI.RHPMUU**	-	-	-	-	-	-	-	RPMUU
121h	**LI.RHPMUS**	-	-	-	-	-	-	-	RPMUUS
122h	**LI.RX86S**	-	-	-	-	SAPIHNE	SAPILNE	CNE	ANE
123h	**LI.RX86LSIE**	-	-	-	-	SAPINE01IM	SAPINEFEIM	CNE3LIM	ANE4IM
124h	**LI.TQLT**	TQLT7	TQLT6	TQLT5	TQLT4	TQLT3	TQLT2	TQLT1	TQLT0
125h	**LI.TQHT**	TQHT7	TQHT6	TQHT5	TQHT4	TQHT3	TQHT2	TQHT1	TQHT0
126h	**LI.TQTIE**	-	-	-	-	TFOVFIE	TQOVFIE	TQHTIE	TQLTIE
127h	**LI.TQCTLS**	-	-	-	-	TFOVFLS	TQOVFLS	TQHTLS	TQLTLS

0DEh–0FFh and 128h–13Fh are reserved.

Note: *the address locations in the above table are for Serial Interface 1. The address locations for Serial Interfaces 2 through 4 can be found with the following formula:*

Address for Port n = Address for Serial Port 1 + [0C0h x (n-1)]; for n = 1 to 4.

9.1.5 Ethernet Interface Register Bit Map

Table 9-6. Ethernet Interface Register Bit Map

ADDR	NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
140h	SU.MACRADL	MACRA7	MACRA6	MACRA5	MACRA4	MACRA3	MACRA2	MACRA1	MACRA0
141h	SU.MACRADH	MACRA15	MACRA14	MACRA13	MACRA12	MACRA11	MACRA10	MACRA09	MACRA08
142h	SU.MACRD0	MACRD7	MACRD6	MACRD5	MACRD4	MACRD3	MACRD2	MACRD1	MACRD0
143h	SU.MACRD1	MACRD15	MACRD14	MACRD13	MACRD12	MACRD11	MACRD10	MACRD9	MACRD8
144h	Error! Reference source not found.	MACRD23	MACRD22	MACRD21	MACRD20	MACRD19	MACRD18	MACRD17	MACRD16
145h	SU.MACRD3	MACRD31	MACRD30	MACRD29	MACRD28	MACRD27	MACRD26	MACRD25	MACRD24
146h	SU.MACWD0	MACWD7	MACWD6	MACWD5	MACWD4	MACWD3	MACWD2	MACWD1	MACWD0
147h	SU.MACWD1	MACWD15	MACWD14	MACWD13	MACWD12	MACWD11	MACWD10	MACWD09	MACWD08
148h	SU.MACWD2	MACWD23	MACWD22	MACWD21	MACWD20	MACWD19	MACWD18	MACWD17	MACWD16
149h	SU.MACWD3	MACD31	MACD30	MACD29	MACD28	MACD27	MACD26	MACD25	MACD24
14Ah	SU.MACAWL	MACAW 7	MACAW 6	MACAW 5	MACAW4	MACAW3	MACAW2	MACAW1	MACAW0
14Bh	SU.MACAWH	MACAW 15	MACAW 14	MACAW 13	MACAW12	MACAW11	MACAW10	MACAW9	MACAW8
14Ch	SU.MACRWC	-	-	-	-	-	-	MCRW	MCS
14Fh	SU.LPBK	-	-	-	-	-	-	-	QLP
150h	SU.GCR	-	-	-	-	CRCS	H10S	ATFLOW	JAME
151h	SU.TFRC	-	-	-	-	NCFQ	TPDFCB	TPRHBC	TPRCB
152h	SU.TFSL	UR	EC	LC	ED	LOC	NOC	-	FABORT
153h	SU.TFSH	PR	HBF	CC3	CC2	CC1	CC0	LCO	DEF
154h	SU.RFSB0	FL7	FL6	FL5	FL4	FL3	FL2	FL1	Fl0
155h	SU.RFSB1	RF	WT	FL13	FL12	FL11	FL10	FL9	Fl8
156h	SU.RFSB2	-	-	CRCE	DB	MIIE	FT	CS	FTL
157h	SU.RFSB3	MF	-	-	BF	MCF	UF	CF	LE
158h	SU.RMFSRL	RMPS7	RMPS6	RMPS5	RMPS4	RMPS3	RMPS2	RMPS1	RMPS0
159h	SU.RMFSRH	RMPS15	RMPS14	RMPS13	RMPS12	RMPS11	RMPS10	RMPS09	RMPS08
15Ah	SU.RQLT	RQLT7	RQLT6	RQLT5	RQLT4	RQLT3	RQLT2	RQLT1	RQLT0
15Bh	SU.RQHT	RQHT7	RQHT6	RQHT5	RQHT4	RQHT3	RQHT2	RQHT1	RQHT0
15Ch	SU.QRIE	-	-	-	-	RFOVFIE	RQVFIE	RQLTIE	RQHTIE
15Dh	SU.QCRLS	-	-	-	-	RFOVFLS	RQOVFLS	RQHTLS	RQLTLS
15Eh	SU.RFRC	-	UCFRB	CFRRB	LERRB	CRCERRB	DBRB	MIIERB	BERRB

15Fh–17Fh are reserved.

Note: *the address locations in the above table are for Ethernet Interface 1. The address locations for Ethernet Interfaces 2 through 4 can be found with the following formula:*

Address for Port n = Address for Ethernet Port 1 + [0C0h x (n-1)]; for n = 1 to 4.

9.1.6 MAC Register Bit Map

Table 9-7. MAC Indirect Register Bit Map

ADDR	NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0000h	**SU.MACCR 31:24**	RA	Reserved	Reserved	HDB	PS	Reserved	Reserved	Reserved
0001h	**23:16**	DRO	OML1	OML0	F	PM	PAM	Reserved	Reserved
0002h	**15:8**	HO	Reserved	HP	LCC	DBF	DRTY	Reserved	ASTP
0003h	**7:0**	BOLMT1	BOLMT0	DC	Reserved	TE	RE	Reserved	Reserved
0004h	**SU.MACAH 31:24**	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0005h	**23:16**	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0006h	**15:8**	PADR47	PADR46	PADR45	PADR44	PADR43	PADR42	PADR41	PADR40
0007h	**7:0**	PADR39	PADR38	PADR37	PADR36	PADR35	PADR34	PADR33	PADR32
0008h	**SU.MACAL 31:24**	PADR31	PADR30	PADR29	PADR28	PADR27	PADR26	PADR25	PADR24
0009h	**23:16**	PADR23	PADR22	PADR21	PADR20	PADR19	PADR18	PADR17	PADR16
000Ah	**15:8**	PADR15	PADR14	PADR13	PADR12	PADR11	PADR10	PADR09	PADR08
000Bh	**7:0**	PADR07	PADR06	PADR05	PADR04	PADR03	PADR02	PADR01	PADR00
000Ch	**SU.MACMAH 31:24**	MMA63	MMA62	MMA61	MMA60	MMA59	MMA58	MMA57	MMA56
000Dh	**23:16**	MMA55	MMA54	MMA53	MMA52	MMA51	MMA50	MMA49	MMA48
000Eh	**15:8**	MMA47	MMA46	MMA45	MMA44	MMA43	MMA42	MMA41	MMA40
000Fh	**7:0**	MMA39	MMA38	MMA37	MMA36	MMA35	MMA34	MMA33	MMA32
0010h	**SU.MACMAL 31:24**	MMA31	MMA30	MMA29	MMA28	MMA27	MMA26	MMA25	MMA24
0011h	**23:16**	MMA23	MMA22	MMA21	MMA20	MMA19	MMA18	MMA17	MMA16
0012h	**15:8**	MMA15	MMA14	MMA13	MMA12	MMA11	MMA10	MMA09	MMA08
0013h	**7:0**	MMA07	MMA06	MMA05	MMA04	MMA03	MMA02	MMA01	MMA00
0014h	**SU.MACMIIA 31:24**	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0015h	**23:16**	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0016h	**15:8**	PHYA4	PHYA3	PHYA2	PHYA1	PHYA0	MIIA4	MIIA3	MIIA2
0017h	**7:0**	MIIA1	MIIA0	Reserved	Reserved	Reserved	Reserved	MIIW	MIIB
0018h	**SU.MACMIID 31:24**	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0019h	**23:16**	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
001Ah	**15:8**	MIID15	MIID14	MIID13	MIID12	MIID11	MIID10	MIID09	MIID08
001Bh	**7:0**	MIID07	MIID06	MIID05	MIID04	MIID03	MIID02	MIID01	MIID00
001Ch	**SU.MACFCR 31:24**	PT15	PT14	PT13	PT12	PT11	PT10	PT09	PT08
001Dh	**23:16**	PT07	PT06	PT05	PT04	PT03	PT02	PT01	PT00
001Eh	**15:8**	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
001Fh	**7:0**	Reserved	Reserved	Reserved	Reserved	Reserved	PCF	FCE	FCB
100h	**SU.MMCCTRL 31:24**	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
101h	**23:16**	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
102h	**15:8**	Reserved	Reserved	MXFRM10	MXFRM9	MXFRM8	MXFRM7	MXFRM6	MXFRM5
103h	**7:0**	MXFRM4	MXFRM3	MXFRM2	MXFRM1	MXFRM0	Reserved	Reserved	Reserved
10Ch	**RESERVED – initialize to FF**	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
10Dh	**RESERVED – initialize to FF**	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
10Eh	**RESERVED – initialize to FF**	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
10Fh	**RESERVED – initialize to FF**	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

ADDR	NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
110h	**RESERVED – initialize to FF**	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
111h	**RESERVED – initialize to FF**	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
112h	**RESERVED – initialize to FF**	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
113h	**RESERVED – initialize to FF**	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
200h	**SU.RxFrmCtr 31:24**	RXFRMC31	RXFRMC30	RXFRMC29	RXFRMC28	RXFRMC27	RXFRMC26	RXFRMC25	RXFRMC24
201h	**23:16**	RXFRMC23	RXFRMC22	RXFRMC21	RXFRMC20	RXFRMC19	RXFRMC18	RXFRMC17	RXFRMC16
202h	**15:8**	RXFRMC15	RXFRMC14	RXFRMC13	RXFRMC12	RXFRMC11	RXFRMC10	RXFRMC9	RXFRMC8
203h	**7:0**	RXFRMC7	RXFRMC6	RXFRMC5	RXFRMC4	RXFRMC3	RXFRMC2	RXFRMC1	RXFRMC0
204h	**SU.RxFrmOKCtr 31:24**	RXFRMOK31	RXFRMOK30	RXFRMOK29	RXFRMOK28	RXFRMOK27	RXFRMOK26	RXFRMOK25	RXFRMOK24
205h	**23:16**	RXFRMOK23	RXFRMOK22	RXFRMOK21	RXFRMOK20	RXFRMOK19	RXFRMOK18	RXFRMOK17	RXFRMOK16
206h	**15:8**	RXFRMOK15	RXFRMOK14	RXFRMOK13	RXFRMOK12	RXFRMOK11	RXFRMOK10	RXFRMOK9	RXFRMOK8
207h	**7:0**	RXFRMOK7	RXFRMOK6	RXFRMOK5	RXFRMOK4	RXFRMOK3	RXFRMOK2	RXFRMOK1	RXFRMOK0
300h	**SU.TxFrmCtr**	TXFRMC31	TXFRMC30	TXFRMC29	TXFRMC28	TXFRMC27	TXFRMC26	TXFRMC25	TXFRMC24
301h	**23:16**	TXFRMC23	TXFRMC22	TXFRMC21	TXFRMC20	TXFRMC19	TXFRMC18	TXFRMC17	TXFRMC16
302h	**15:8**	TXFRMC15	TXFRMC14	TXFRMC13	TXFRMC12	TXFRMC11	TXFRMC10	TXFRMC9	TXFRMC8
303h	**7:0**	TXFRMC7	TXFRMC6	TXFRMC5	TXFRMC4	TXFRMC3	TXFRMC2	TXFRMC1	TXFRMC0
308h	**SU.TxBytesCtr**	TXBYTEC31	TXBYTEC30	TXBYTEC29	TXBYTEC28	TXBYTEC27	TXBYTEC26	TXBYTEC25	TXBYTEC24
309h	**23:16**	TXBYTEC23	TXBYTEC22	TXBYTEC21	TXBYTEC20	TXBYTEC19	TXBYTEC18	TXBYTEC17	TXBYTEC16
30Ah	**15:8**	TXBYTEC15	TXBYTEC14	TXBYTEC13	TXBYTEC12	TXBYTEC11	TXBYTEC10	TXBYTEC9	TXBYTEC8
30Bh	**7:0**	TXBYTEC7	TXBYTEC6	TXBYTEC5	TXBYTEC4	TXBYTEC3	TXBYTEC2	TXBYTEC1	TXBYTEC0
30Ch	**SU.TxBytesOkCtr**	TXBYTEOK31	TXBYTEOK30	TXBYTEOK29	TXBYTEOK28	TXBYTEOK27	TXBYTEOK26	TXBYTEOK25	TXBYTEOK24
30Dh	**23:16**	TXBYTEOK23	TXBYTEOK22	TXBYTEOK21	TXBYTEOK20	TXBYTEOK19	TXBYTEOK18	TXBYTEOK17	TXBYTEOK16
30Eh	**15:8**	TXBYTEOK15	TXBYTEOK14	TXBYTEOK13	TXBYTEOK12	TXBYTEOK11	TXBYTEOK10	TXBYTEOK9	TXBYTEOK8
30Fh	**7:0**	TXBYTEOK7	TXBYTEOK6	TXBYTEOK5	TXBYTEOK4	TXBYTEOK3	TXBYTEOK2	TXBYTEOK1	TXBYTEOK0
334h	**SU.TxFrmUndr**	TXFRMU31	TXFRMU30	TXFRMU29	TXFRMU28	TXFRMU27	TXFRMU26	TXFRMU25	TXFRMU24
335h	**23:16**	TXFRMU23	TXFRMU22	TXFRMU21	TXFRMU20	TXFRMU19	TXFRMU18	TXFRMU17	TXFRMU16
336h	**15:8**	TXFRMU15	TXFRMU14	TXFRMU13	TXFRMU12	TXFRMU11	TXFRMU10	TXFRMU9	TXFRMU8
337h	**7:0**	TXFRMU7	TXFRMU6	TXFRMU5	TXFRMU4	TXFRMU3	TXFRMU2	TXFRMU1	TXFRMU0
338h	**SU.TxBdFrmCtr**	TXFRMBD31	TXFRMBD30	TXFRMBD29	TXFRMBD28	TXFRMBD27	TXFRMBD26	TXFRMBD25	TXFRMBD24
339h	**23:16**	TXFRMBD23	TXFRMBD22	TXFRMBD21	TXFRMBD20	TXFRMBD19	TXFRMBD18	TXFRMBD17	TXFRMBD16
33Ah	**15:8**	TXFRMBD15	TXFRMBD14	TXFRMBD13	TXFRMBD12	TXFRMBD11	TXFRMBD10	TXFRMBD9	TXFRMBD8
33Bh	**7:0**	TXFRMBD7	TXFRMBD6	TXFRMBD5	TXFRMBD4	TXFRMBD3	TXFRMBD2	TXFRMBD1	TXFRMBD0

Note that the addresses in the table above are the indirect addresses that must be provided to the SU.MACAWH and SU.MACAWL. All unused and reserved locations must be initialized to zero for proper operation unless specifically noted otherwise.

9.2 Global Register Definitions

Functions contained in the global registers include: framer reset, LIU reset, device ID, BERT interrupt status, framer interrupt status, IBO configuration, MCLK configuration, and BPCLK configuration. These registers are preserved to provide code compatibility with the multiport devices in this product family. The global registers bit descriptions are presented below.

Register Name: **GL.IDRL**
Register Description: **Global ID Low Register**
Register Address: **00h**

Bit #	7	6	5	4	3	2	1	0
Name	ID07	ID06	ID05	ID04	ID03	ID02	ID01	ID00
Default	0	0	1	1	0	0	0	0

Bit 7: (ID07). Reserved for future use.

Bit 6: (ID06). Reserved for future use.

Bit 5: RMII Interface (ID05). If this bit is set the device contains a RMII interface.

Bit 4: MII Interface (ID04). If this bit is set the device contains a MII interface.

Bit 3: PHY (ID04). If this bit is set the device contains an Ethernet PHY.

Bits 2 to 0: Device Revision (ID02 to ID00). A three-bit count that is equal to 000b for the first die revision, and is incremented with each successive die revision. May not match the two-letter die revision code on the top brand of the device.

Register Name: **GL.IDRH**
Register Description: **Global ID High Register**
Register Address: **01h**

Bit #	7	6	5	4	3	2	1	0
Name	ID15	ID14	ID13	ID12	ID11	ID10	ID09	ID08
Default	0	1	1	0	0	0	1	1

Bits 7 to 5: (ID15 to ID13). Number of ports in the device: 1.

Bit 4: LIU (ID12) . If this bit is set the device has LIU functionality.

Bit 3: Framer (ID011). If this bit is set the device has a framer.

Bit 2: (ID10). Reserved for future use.

Bit 1: HDLC Interface or X.86 (ID09). If this bit is set the device has HDLC or X.86 encapsulation.

Bit 0: IMUX (ID08). If this bit is set the device has Inverse mux functionality.

Register Name: **GL.CR1**
Register Description: **Global Control Register 1**
Register Address: **02h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	REF_CLKO	INTM	RST
Default	—	—	—	—	—	0	0	0

Bit 2: REF_CLKO OFF (REF_CLKO). This bit determines the REF_CLKO output mode.
1 = REF_CLKO is disabled and outputs an active low signal.
0 = REF_CLKO is active and in accordance with RMII/MII Selection

Bit 1: $\overline{\text{INT}}$ Pin Mode (INTM). This bit determines the inactive mode of the $\overline{\text{INT}}$ pin. The $\overline{\text{INT}}$ pin always drives low when active.
1 = Pin is high impedance when not active
0 = Pin drives high when not active

Bit 0: Reset (RST). When this bit is set to 1, all of the internal data path and status and control registers (except this RST bit), on all ports, are reset to their default state. This bit must be set high for a minimum of 100ns.
0 = Normal operation
1 = Reset and force all internal registers to their default values

Register Name: **GL.BLR**
Register Description: **Global BERT Connect Register**
Register Address: **03h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	GL.BLC4	GL.BLC3	GL.BLC2	GL.BLC1
Default	0	0	0	0	0	0	0	0

Bit 3: BERT Connect 4 (GL.BLC4). If this bit is set to 1, the BERT is connected to Serial Interface 4.

Bit 2: BERT Connect 3 (GL.BLC3). If this bit is set to 1, the BERT is connected to Serial Interface 3.

Bit 1: BERT Connect 2 (GL.BLC2). If this bit is set to 1, the BERT is connected to Serial Interface 2.

Bit 0: BERT Connect 1 (GL.BLC1). If this bit is set to 1, the BERT is connected to Serial Interface 1.

The BERT transmitter is connected to the transmit serial port and the BERT receive to the receive serial port. When the BERT is connected, normal data transfer is interrupted. Note that connecting the BERT overrides a connection to the Serial Interface, if a connection exists. When the BERT is disconnected, the connection is restored. The BERT is unavailable in Hardware Mode. Do not assign more than one bit in this register to “1” at the same time.

Register Name: **GL.RTCAL**
Register Description: **Global Receive and Transmit Serial Port Clock Activity Latched Status**
Register Address: **04h**

Bit #	7	6	5	4	3	2	1	0
Name	RLCALS4	RLCALS3	RLCALS2	RLCALS1	TLCALS4	TLCALS3	TLCALS2	TLCALS1
Default	0	0	0	0	0	0	0	0

Bit 7: Receive Serial Interface Clock Activity Latched Status 4 (RLCALS4). This bit is set to 1 if the receive clock for Serial Interface 4 has activity. This bit is cleared upon read.

Bit 6: Receive Serial Interface Clock Activity Latched Status 3 (RLCALS3). This bit is set to 1 if the receive clock for Serial Interface 3 has activity. This bit is cleared upon read.

Bit 5: Receive Serial Interface Clock Activity Latched Status 2 (RLCALS2). This bit is set to 1 if the receive clock for Serial Interface 2 has activity. This bit is cleared upon read.

Bit 4: Receive Serial Interface Clock Activity Latched Status 1 (RLCALS1). This bit is set to 1 if the receive clock for Serial Interface 1 has activity. This bit is cleared upon read.

Bit 3: Transmit Serial Interface Clock Activity Latched Status 4 (TLCALS4). This bit is set to 1 if the transmit clock for Serial Interface 4 has activity. This bit is cleared upon read.

Bit 2: Transmit Serial Interface Clock Activity Latched Status 3 (TLCALS3). This bit is set to 1 if the transmit clock for Serial Interface 3 has activity. This bit is cleared upon read.

Bit 1: Transmit Serial Interface Clock Activity Latched Status 2 (TLCALS2). This bit is set to 1 if the transmit clock for Serial Interface 2 has activity. This bit is cleared upon read.

Bit 0: Transmit Serial Interface Clock Activity Latched Status 1 (TLCALS1). This bit is set to 1 if the transmit clock for Serial Interface 1 has activity. This bit is cleared upon read.

Register Name: **GL.SRCALS**
Register Description: **Global SDRAM Reference Clock Activity Latched Status**
Register Address: **05h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	REFCLKS	SYSCLS
Default	0	0	0	0	0	0	0	0

Bit 1: Reference Clock Activity Latched Status (REFCLKS). This bit is set to 1 if REF_CLK has activity. This bit is cleared upon read.

Bit 0: System Clock Input Latched Status (SYSCLS). This bit is set to 1 if SYSCLKI has activity. This bit is cleared upon read.

Register Name: **GL.LIE**
Register Description: **Global Serial Interface Interrupt Enable**
Register Address: **06h**

Bit #	7	6	5	4	3	2	1	0
Name	LIN4TIE	LIN3TIE	LIN2TIE	LIN1TIE	LIN4RIE	LIN3RIE	LIN2RIE	LIN1RIE
Default	0	0	0	0	0	0	0	0

Bit 7: Serial Interface 4 Tx Interrupt Enable (LIN4TIE). Setting this bit to 1 enables an interrupt on LIN4TIS.

Bit 6: Serial Interface 3 Tx Interrupt Enable (LIN3TIE). Setting this bit to 1 enables an interrupt on LIN3TIS.

Bit 5: Serial Interface 2 Tx Interrupt Enable (LIN2TIE). Setting this bit to 1 enables an interrupt on LIN2TIS.

Bit 4: Serial Interface 1 Tx Interrupt Enable (LIN1TIE). Setting this bit to 1 enables an interrupt on LIN1TIS.

Bit 3: Serial Interface 4 Rx Interrupt Enable (LIN4RIE). Setting this bit to 1 enables an interrupt on LIN4RIS.

Bit 2: Serial Interface 3 Rx Interrupt Enable (LIN3RIE). Setting this bit to 1 enables an interrupt on LIN3RIS.

Bit 1: Serial Interface 2 Rx Interrupt Enable (LIN2RIE). Setting this bit to 1 enables an interrupt on LIN2RIS.

Bit 0: Serial Interface 1 Rx Interrupt Enable (LIN1RIE). Setting this bit to 1 enables an interrupt on LIN1RIS.

Register Name: **GL.LIS**
Register Description: **Global Serial Interface Interrupt Status**
Register Address: **07h**

Bit #	7	6	5	4	3	2	1	0
Name	LIN4TIS	LIN3TIS	LIN2TIS	LIN1TIS	LIN4RIS	LIN3RIS	LIN2RIS	LIN1RIS
Default	0	0	0	0	0	0	0	0

Bit 7: Serial Interface 4 Tx Interrupt Status (LIN4TIS). This bit is set if Serial Interface 4 Transmit has an enabled interrupt generating event. Serial Interface interrupts consist of HDLC interrupts and X.86 interrupts.

Bit 6: Serial Interface 3 Tx Interrupt Status (LIN3TIS). This bit is set if Serial Interface 3 Transmit has an enabled interrupt generating event. Serial Interface interrupts consist of HDLC interrupts and X.86 interrupts.

Bit 5: Serial Interface 2 Tx Interrupt Status (LIN2TIS). This bit is set if Serial Interface 2 Transmit has an enabled interrupt generating event. Serial Interface interrupts consist of HDLC interrupts and X.86 interrupts.

Bit 4: Serial Interface 1 Tx Interrupt Status (LIN1TIS). This bit is set if Serial Interface 1 Transmit has an enabled interrupt generating event. Serial Interface interrupts consist of HDLC interrupts and X.86 interrupts.

Bit 3: Serial Interface 4 Rx Interrupt Status (LIN4RIS). This bit is set if Serial Interface 4 Receive has an enabled interrupt generating event. Serial Interface interrupts consist of HDLC interrupts and X.86 interrupts.

Bit 2: Serial Interface 3 Rx Interrupt Status (LIN3RIS). This bit is set if Serial Interface 3 Receive has an enabled interrupt generating event. Serial Interface interrupts consist of HDLC interrupts and X.86 interrupts.

Bit 1: Serial Interface 2 Rx Interrupt Status (LIN2RIS). This bit is set if Serial Interface 2 Receive has an enabled interrupt generating event. Serial Interface interrupts consist of HDLC interrupts and X.86 interrupts.

Bit 0: Serial Interface 1 Rx Interrupt Status (LIN1RIS). This bit is set if Serial Interface 1 Receive has an enabled interrupt generating event. Serial Interface interrupts consist of HDLC interrupts and X.86 interrupts.

Register Name: **GL.SIE**
Register Description: **Global Ethernet Interface Interrupt Enable**
Register Address: **08h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	SUB4IE	SUB3IE	SUB2IE	SUB1IE
Default	0	0	0	0	0	0	0	0

Bit 3: Ethernet Interface 4 Interrupt Enable (SUB4IE). Setting this bit to 1 enables an interrupt on SUB4S.

Bit 2: Ethernet Interface 3 Interrupt Enable (SUB3IE). Setting this bit to 1 enables an interrupt on SUB3S.

Bit 1: Ethernet Interface 2 Interrupt Enable (SUB2IE). Setting this bit to 1 enables an interrupt on SUB2S.

Bit 0: Ethernet Interface 1 Interrupt Enable (SUB1IE). Setting this bit to 1 enables an interrupt on SUB1S.

Register Name: **GL.SIS**
Register Description: **Global Ethernet Interface Interrupt Status**
Register Address: **09h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	SUB4IS	SUB3IS	SUB2IS	SUB1IS
Default	0	0	0	0	0	0	0	0

Bit 4: Ethernet Interface 4 Interrupt Status (SUB4IS). This bit is set to 1 if Ethernet Interface 4 has an enabled interrupt-generating event. The Ethernet Interface consists of the MAC and The RMII/MII port.

Bit 3: Ethernet Interface 3 Interrupt Status (SUB3IS). This bit is set to 1 if Ethernet Interface 3 has an enabled interrupt-generating event. The Ethernet Interface consists of the MAC and The RMII/MII port.

Bit 2: Ethernet Interface 2 Interrupt Status (SUB2IS). This bit is set to 1 if Ethernet Interface 2 has an enabled interrupt-generating event. The Ethernet Interface consists of the MAC and The RMII/MII port.

Bit 0: Ethernet Interface 1 Interrupt Status (SUB1IS). This bit is set to 1 if Ethernet Interface 1 has an enabled interrupt-generating event. The Ethernet Interface consists of the MAC and The RMII/MII port.

Register Name: **GL.TRQIE**
Register Description: **Global Transmit Receive Queue Interrupt Enable**
Register Address: **0Ah**

Bit #	7	6	5	4	3	2	1	0
Name	TQ4IE	TQ3IE	TQ2IE	TQ1IE	RQ4IE	RQ3IE	RQ2IE	RQ1IE
Default	0	0	0	0	0	0	0	0

Bit 7: Transmit Queue 4 Interrupt Enable (TQ4IE). Setting this bit to 1 enables an interrupt on TQ4IS.

Bit 6: Transmit Queue 3 Interrupt Enable (TQ3IE). Setting this bit to 1 enables an interrupt on TQ3IS.

Bit 5: Transmit Queue 2 Interrupt Enable (TQ2IE). Setting this bit to 1 enables an interrupt on TQ2IS.

Bit 4: Transmit Queue 1 Interrupt Enable (TQ1IE). Setting this bit to 1 enables an interrupt on TQ1IS.

Bit 3: Receive Queue 4 Interrupt Enable (RQ4IE). Setting this bit to 1 enables an interrupt on RQ4IS.

Bit 2: Receive Queue 3 Interrupt Enable (RQ3IE). Setting this bit to 1 enables an interrupt on RQ3IS.

Bit 1: Receive Queue 2 Interrupt Enable (RQ2IE). Setting this bit to 1 enables an interrupt on RQ2IS.

Bit 0: Receive Queue 1 Interrupt Enable (RQ1IE). Setting this bit to 1 enables an interrupt on RQ1IS.

Register Name: **GL.TRQIS**
Register Description: **Global Transmit Receive Queue Interrupt Status**
Register Address: **0Bh**

Bit #	7	6	5	4	3	2	1	0
Name	TQ4IS	TQ3IS	TQ2IS	TQ1IS	RQ4IS	RQ3IS	RQ2IS	RQ1IS
Default	0	0	0	0	0	0	0	0

Bit 7: Transmit Queue 4 Interrupt Enable (TQ4IS). If this bit is set to 1, the Transmit Queue 4 has interrupt status event. Transmit queue events are transmit queue crossing thresholds and queue overflows.

Bit 6: Transmit Queue 3 Interrupt Enable (TQ3IS). If this bit is set to 1, the Transmit Queue 3 has interrupt status event. Transmit queue events are transmit queue crossing thresholds and queue overflows.

Bit 5: Transmit Queue 2 Interrupt Enable (TQ2IS). If this bit is set to 1, the Transmit Queue 2 has interrupt status event. Transmit queue events are transmit queue crossing thresholds and queue overflows.

Bit 4: Transmit Queue 1 Interrupt Enable (TQ1IS). If this bit is set to 1, the Transmit Queue 1 has interrupt status event. Transmit queue events are transmit queue crossing thresholds and queue overflows.

Bit 3: Receive Queue 4 Interrupt Status (RQ4IS). If this bit is set to 1, the Receive Queue 4 has interrupt status event. Receive queue events are transmit queue crossing thresholds and queue overflows.

Bit 2: Receive Queue 3 Interrupt Status (RQ3IS). If this bit is set to 1, the Receive Queue 3 has interrupt status event. Receive queue events are transmit queue crossing thresholds and queue overflows.

Bit 1: Receive Queue 2 Interrupt Status (RQ2IS). If this bit is set to 1, the Receive Queue 2 has interrupt status event. Receive queue events are transmit queue crossing thresholds and queue overflows.

Bit 0: Receive Queue 1 Interrupt Status (RQ1IS). If this bit is set to 1, the Receive Queue 1 has interrupt status event. Receive queue events are transmit queue crossing thresholds and queue overflows.

Register Name: **GL.BIE**
Register Description: **Global BERT Interrupt Enable**
Register Address: **0Ch**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	BIE
Default	0	0	0	0	0	0	0	0

Bit 0: BERT Interrupt Enable (BIE). Setting this bit to 1 enables an interrupt on BIS.

Register Name: **GL.BIS**
Register Description: **Global BERT Interrupt Status**
Register Address: **0Dh**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	BIS
Default	0	0	0	0	0	0	0	0

Bit 0: BERT Interrupt Status (BIS). This bit is set to 1 if the BERT has an enabled interrupt generating event.

Register Name: **GL.CON1**
Register Description: **Connection Register for Ethernet Interface 1**
Register Address: **0Eh**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	LINE1[2]	LINE1[1]	LINE1[0]
Default	0	0	0	0	0	0	0	1

Bits 2 to 0: LINE1[2] to LINE1[0]. The LINE1[0:2] bits select the Serial port that is to be connected to Ethernet Interface 1. Note that bidirectional connection is assumed between the Serial and Ethernet Interfaces. The connection register and corresponding queue size must be defined for proper operation. Writing a 0 to this register will disconnect the connection. When a connection is disconnected, “1”s are sourced to the Serial Interface transmit and to the HDLC receiver. The clocks to the HDLC transmitter and receiver are turned off (0). A LINE1[0:2] value of 1 connects Ethernet Interface 1 to Serial Interface 1. A LINE1[0:2] value of 2 connects Ethernet Interface 1 to Serial Interface 2. A LINE1[0:2] value of 3 connects Ethernet Interface 1 to Serial Interface 3. A LINE1[0:2] value of 4 connects Ethernet Interface 1 to Serial Interface 4. The user must reset the queue pointers before a connection is made and after a connection is disconnected.

Register Name: **GL.CON2**
Register Description: **Connection Register for Ethernet Interface 2**
Register Address: **0Fh**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	LINE2[2]	LINE2[1]	LINE2[0]
Default	0	0	0	0	0	0	1	0

Bits 2 to 0: LINE2[2] to LINE2[0]. The LINE2[0:2] bits select the Serial port that is to be connected to Ethernet Interface 2. Note that bidirectional connection is assumed between the Serial and Ethernet Interfaces. The connection register and corresponding queue size must be defined for proper operation. Writing a 0 to this register will disconnect the connection. When a connection is disconnected, “1”s are sourced to the Serial Interface transmit and to the HDLC receiver. The clocks to the HDLC transmitter and receiver are turned off (0). A LINE2[0:2] value of 1 connects Ethernet Interface 2 to Serial Interface 1. A LINE2[0:2] value of 2 connects Ethernet Interface 2 to Serial Interface 2. A LINE2[0:2] value of 3 connects Ethernet Interface 2 to Serial Interface 3. A LINE2[0:2] value of 4 connects Ethernet Interface 2 to Serial Interface 4. The user must reset the queue pointers before a connection is made and after a connection is disconnected.

Register Name: **GL.CON3**
Register Description: **Connection Register for Ethernet Interface 3**
Register Address: **10h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	LINE3[2]	LINE3[1]	LINE3[0]
Default	0	0	0	0	0	0	1	1

Bits 2 to 0: LINE3[2] to LINE3[0]. The LINE3[0:2] bits select the Serial port that is to be connected to Ethernet Interface 3. Note that bidirectional connection is assumed between the Serial and Ethernet Interfaces. The connection register and corresponding queue size must be defined for proper operation. Writing a 0 to this register will disconnect the connection. When a connection is disconnected, “1”s are sourced to the Serial Interface transmit and to the HDLC receiver. The clocks to the HDLC transmitter and receiver are turned off (0). A LINE3[0:2] value of 1 connects Ethernet Interface 3 to Serial Interface 1. A LINE3[0:2] value of 2 connects Ethernet Interface 3 to Serial Interface 2. A LINE3[0:2] value of 3 connects Ethernet Interface 3 to Serial Interface 3. A LINE3[0:2] value of 4 connects Ethernet Interface 3 to Serial Interface 4. The user must reset the queue pointers before a connection is made and after a connection is disconnected.

Register Name: **GL.CON4**
Register Description: **Connection Register for Ethernet Interface 4**
Register Address: **11h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	LINE4[2]	LINE4[1]	LINE4[0]
Default	0	0	0	0	0	1	0	0

Bits 2 to 0: LINE4[2] to LINE4[0]. The LINE4[0:2] bits select the Serial port that is to be connected to Ethernet Interface 4. Note that bidirectional connection is assumed between the Serial and Ethernet Interfaces. The connection register and corresponding queue size must be defined for proper operation. Writing a 0 to this register will disconnect the connection. When a connection is disconnected, “1”s are sourced to the Serial Interface transmit and to the HDLC receiver. The clocks to the HDLC transmitter and receiver are turned off (0). A LINE4[0:2] value of 1 connects Ethernet Interface 4 to Serial Interface 1. A LINE4[0:2] value of 2 connects Ethernet Interface 4 to Serial Interface 2. A LINE4[0:2] value of 3 connects Ethernet Interface 4 to Serial Interface 3. A LINE4[0:2] value of 4 connects Ethernet Interface 4 to Serial Interface 4. The user must reset the queue pointers before a connection is made and after a connection is disconnected.

Register Name: **GL.C1QPR**
Register Description: **Connection 1 Queue Pointer Reset**
Register Address: **12h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	C1MRPR	C1HWPR	C1MHPR	C1HRPR
Default	0	0	0	0	0	0	0	0

Bit 3: MAC Read Pointer Reset (C1MRPR). Setting this bit to 1 resets the receive queue read pointer for connection 1. This queue pointer must be reset after a disconnect and before a connection. The user must clear the bit before subsequent reset operations.

Bit 2: HDLC Write Pointer Reset (C1HWPR). Setting this bit to 1 resets the receive queue write pointer for connection 1. This queue pointer must be reset after a disconnect and before a connection. The user must clear the bit before subsequent reset operations.

Bit 1: HDLC Read Pointer Reset (C1MHPR). Setting this bit to 1 resets the transmit queue read pointer for connection 1. This queue pointer must be reset after a disconnect and before a connection. The user must clear the bit before subsequent reset operations.

Bit 0: MAC Transmit Write Pointer Reset (C1HRPR). Setting this bit to 1 resets the transmit queue write pointer for connection 1. This queue pointer must be reset after a disconnect and before a connection. The user must clear the bit before subsequent reset operations.

Register Name: **GL.C2QPR**
Register Description: **Connection 2 Queue Pointer Reset**
Register Address: **13h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	C2MRPR	C2HWPR	C2MHPR	C2HRPR
Default	0	0	0	0	0	0	0	0

Bit 3: MAC Read Pointer Reset (C2MRPR). Setting this bit to 1 resets the receive queue read pointer for connection 2. This queue pointer must be reset after a disconnect and before a connection. The user must clear the bit before subsequent reset operations.

Bit 2: HDLC Write Pointer Reset (C2HWPR). Setting this bit to 1 resets the receive queue write pointer for connection 2. This queue pointer must be reset after a disconnect and before a connection. The user must clear the bit before subsequent reset operations.

Bit 1: HDLC Read Pointer Reset (C2MHPR). Setting this bit to 1 resets the transmit queue read pointer for connection 2. This queue pointer must be reset after a disconnect and before a connection. The user must clear the bit before subsequent reset operations.

Bit 0: MAC Transmit Write Pointer Reset (C2HRPR). Setting this bit to 1 resets the transmit queue write pointer for connection 2. This queue pointer must be reset after a disconnect and before a connection. The user must clear the bit before subsequent reset operations.

Register Name: **GL.C3QPR**
Register Description: **Connection 3 Queue Pointer Reset**
Register Address: **14h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	C3MRPR	C3HWPR	C3MHPR	C3HRPR
Default	0	0	0	0	0	0	0	0

Bit 3: MAC Read Pointer Reset (C3MRPR). Setting this bit to 1 resets the receive queue read pointer for connection 3. This queue pointer must be reset after a disconnect and before a connection. The user must clear the bit before subsequent reset operations.

Bit 2: HDLC Write Pointer Reset (C3HWPR). Setting this bit to 1 resets the receive queue write pointer for connection 3. This queue pointer must be reset after a disconnect and before a connection. The user must clear the bit before subsequent reset operations.

Bit 1: HDLC Read Pointer Reset (C3MHPR). Setting this bit to 1 resets the transmit queue read pointer for connection 3. This queue pointer must be reset after a disconnect and before a connection. The user must clear the bit before subsequent reset operations.

Bit 0: MAC Transmit Write Pointer Reset (C3HRPR). Setting this bit to 1 resets the transmit queue write pointer for connection 3. This queue pointer must be reset after a disconnect and before a connection. The user must clear the bit before subsequent reset operations.

Register Name: **GL.C4QPR**
Register Description: **Connection 4 Queue Pointer Reset**
Register Address: **15h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	C4MRPR	C4HWPR	C4MHPR	C4HRPR
Default	0	0	0	0	0	0	0	0

Bit 3: MAC Read Pointer Reset (C4MRPR). Setting this bit to 1 resets the receive queue read pointer for connection 4. This queue pointer must be reset after a disconnect and before a connection. The user must clear the bit before subsequent reset operations.

Bit 2: HDLC Write Pointer Reset (C4HWPR). Setting this bit to 1 resets the receive queue write pointer for connection 4. This queue pointer must be reset after a disconnect and before a connection. The user must clear the bit before subsequent reset operations.

Bit 1: HDLC Read Pointer Reset (C4MHPR). Setting this bit to 1 resets the transmit queue read pointer for connection 4. This queue pointer must be reset after a disconnect and before a connection. The user must clear the bit before subsequent reset operations.

Bit 0: MAC Transmit Write Pointer Reset (C4HRPR). Setting this bit to 1 resets the transmit queue write pointer for connection 4. This queue pointer must be reset after a disconnect and before a connection. The user must clear the bit before subsequent reset operations.

Register Name: **GL.BISTEN**
Register Description: **BIST Enable**
Register Address: **20h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	BISTE
Default	0	0	0	0	0	0	0	0

Bit 0: BIST Enable (BISTE). If this bit is set the DS33Z44 performs BIST test on the SDRAM. Normal data communication is halted while BIST enable is high. The user must reset the DS33Z44 after completion of BIST test before normal dataflow can begin.

Register Name: **GL.BISTPF**
Register Description: **BIST Pass-Fail**
Register Address: **21h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	BISTDN	BISTPF
Default	0	0	0	0	0	0	0	0

Bit 1: BIST DONE (BISTDN). If this bit is set to 1, the DS33Z44 has completed the BIST Test initiated by BISTE. The pass fail result is available in BISTPF.

Bit 0: BIST Pass-Fail (BISTPF). This bit is equal to 0 after the DS33Z44 performs BIST testing on the SDRAM and the test passes. This bit is set to 1 if the test failed. This bit is valid only after the BIST test is complete and the BIST DN bit is set. If set this bit can only be cleared by resetting the DS33Z44.

Register Name: **GL.SDMODE1**
Register Description: **Global SDRAM Mode Register 1**
Register Address: **3Ah**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	WT	BL2	BL1	BL0
Default	0	0	0	0	0	0	1	1

Bit 3: Wrap Type (WT). This bit is used to configure the wrap mode.

0 = Sequential
1 = Interleave

Bits 2 to 0: Burst Length 2 to 0 (BL2 to BL0). These bits are used to determine the Burst Length.

Note: This register has a non-zero default value. This should be taken into consideration when initializing the device.

Note: After changing the value of this register, the user must toggle the GL.SDMODEWS.SDMW bit to write the new values to the SDRAM.

Register Name: **GL.SDMODE2**
Register Description: **Global SDRAM Mode Register 2**
Register Address: **3Bh**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	LTMOD2	LTMOD1	LTMOD0
Default	0	0	0	0	0	0	1	0

Bits 2 to 0: CAS Latency Mode (LTMOD2 to LTMOD0). These bits are used to setup CAS latency. Note: Only CAS latency of 2 or 3 is allowed.

Note 1: This register has a non-zero default value. This should be taken into consideration when initializing the device.

Note 2: After changing the value of this register, the user must toggle the GL.SDMODEWS.SDMW bit to write the new values to the SDRAM.

Register Name: **GL.SDMODEWS**
Register Description: **Global SDRAM Mode Register Write Status**
Register Address: **3Ch**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	SDMW
Default	0	0	0	0	0	0	0	0

Bit 0: SDRAM Mode Write (SDMW). Setting this bit to 1 will write the current values of the mode control and refresh time control registers to the SDRAM. The user must clear this bit and set it again for subsequent write operations.

Register Name: **GL.SDRFTC**
Register Description **Global SDRAM Refresh Time Control**
Register Address: **3Dh**

Bit #	7	6	5	4	3	2	1	0
Name	SREFT7	SREFT6	SREFT5	SREFT4	SREFT3	SREFT2	SREFT1	SREFT0
Default	0	1	0	0	0	1	1	0

Bits 7 to 0: SDRAM Refresh Time Control (SREFT7 to SREFT0) These 8 bits are used to control the SDRAM refresh frequency. The refresh rate will be equal to this register value x 8 x 100MHz.

Note 1: This register has a non-zero default value. This should be taken into consideration when initializing the device.

Note 2: After changing the value of this register, the user must toggle the GL.SDMODEWS.SDMW bit to write the new values to the SDRAM.

9.3 Arbiter Registers

The Arbiter manages the transport between the Ethernet port and the Serial Interface. It is responsible for queuing and dequeuing data to an external SDRAM. The arbiter handles requests from the HDLC and MAC to transfer data to/from the SDRAM. The base address of the Arbiter register space is 0040h.

9.3.1 Arbiter Register Bit Descriptions

Register Name: **AR.RQSC1**
Register Description: **Arbiter Receive Queue Size Connection 1**
Register Address: **40h**

Bit #	7	6	5	4	3	2	1	0
Name	RQSC1[7]	RQSC1[6]	RQSC1[5]	RQSC1[4]	RQSC1[3]	RQSC1[2]	RQSC1[1]	RQSC1[0]
Default	0	0	1	1	1	1	0	1

Bits 7 to 0: Receive Queue Size Connection 1 (RQSC1[7] to RQSC1[0]). These 7 bits of the size of receive queue associated with connection 1. Receive queue is for data arriving from the MAC to be sent to the WAN. The Queue address size is defined in increments of 32 x 2048 bytes. The queue size is AR.RQSC1 multiplied by 32 to determine the number of 2048 byte packets that can be stored in the queue. This queue is constructed in the external SDRAM**. Note: Queue size of 0 is not allowed and should never be set.**

Register Name: **AR.TQSC1**
Register Description: **Arbiter Transmit Queue Size Connection 1**
Register Address: **41h**

Bit #	7	6	5	4	3	2	1	0
Name	TQSC1[7]	TQSC1[6]	TQSC1[5]	TQSC1[4]	TQSC1[3]	TQSC1[2]	TQSC1[1]	TQSC1[0]
Default	0	0	0	0	0	0	1	1

Bits 7 to 0: Transmit Queue Size Connection 1 (TQSC1[7] to TQSC1[0]). These 7 bits of the size of transmit queue associated with connection 1. The queue address size is defined in increments of 32 packets. The queue size is AR.TQSC1 multiplied by 32 to determine the number of 2048 byte packets that can be stored in the queue. The range of bytes will depend on the external SDRAM connected to the DS33Z44. Transmit queue is the data queue for data arriving on the WAN that is sent to the MAC. **Note that queue size of 0 is not allowed and should never be set.**

Register Name: **AR.RQSC2**
Register Description: **Arbiter Receive Queue Size Connection 2**
Register Address: **42h**

Bit #	7	6	5	4	3	2	1	0
Name	RQSC2[7]	RQSC2[6]	RQSC2[5]	RQSC2[4]	RQSC2[3]	RQSC2[2]	RQSC2[1]	RQSC2[0]
Default	0	0	1	1	1	1	0	1

Bits 7 to 0: Receive Queue Size Connection 2 (RQSC2[7] to RQSC2[0]). These 7 bits of the size of receive queue associated with connection 2. Receive queue is for data arriving from the MAC to be sent to the WAN. The Queue address size is defined in increments of 32 x 2048 bytes. The queue size is AR.RQSC2 multiplied by 32 to determine the number of 2048 byte packets that can be stored in the queue. This queue is constructed in the external SDRAM**. Note: Queue size of 0 is not allowed and should never be set.**

Register Name: **AR.TQSC2**
Register Description: **Arbiter Transmit Queue Size Connection 2**
Register Address: **43h**

Bit #	7	6	5	4	3	2	1	0
Name	TQSC2[7]	TQSC2[6]	TQSC2[5]	TQSC2[4]	TQSC2[3]	TQSC2[2]	TQSC2[1]	TQSC2[0]
Default	0	0	0	0	0	0	1	1

Bits 7 to 0: Transmit Queue Size Connection 2 (TQSC2[7] to TQSC2[0]). These 7 bits of the size of transmit queue associated with connection 2. The queue address size is defined in increments of 32 packets. The queue size is AR.TQSC2 multiplied by 32 to determine the number of 2048 byte packets that can be stored in the queue. The range of bytes will depend on the external SDRAM connected to the DS33Z44. Transmit queue is the data queue for data arriving on the WAN that is sent to the MAC. **Note that queue size of 0 is not allowed and should never be set.**

Register Name: **AR.RQSC3**
Register Description: **Arbiter Receive Queue Size Connection 3**
Register Address: **44h**

Bit #	7	6	5	4	3	2	1	0
Name	RQSC3[7]	RQSC3[6]	RQSC3[5]	RQSC3[4]	RQSC3[3]	RQSC3[2]	RQSC3[1]	RQSC3[0]
Default	0	0	1	1	1	1	0	1

Bits 7 to 0: Receive Queue Size Connection 3 (RQSC3[7] to RQSC3[0]). These 7 bits of the size of receive queue associated with connection 3. Receive queue is for data arriving from the MAC to be sent to the WAN. The Queue address size is defined in increments of 32 x 2048 bytes. The queue size is AR.RQSC3 multiplied by 32 to determine the number of 2048 byte packets that can be stored in the queue. This queue is constructed in the external SDRAM**. Note: Queue size of 0 is not allowed and should never be set.**

Register Name: **AR.TQSC3**
Register Description: **Arbiter Transmit Queue Size Connection 3**
Register Address: **45h**

Bit #	7	6	5	4	3	2	1	0
Name	TQSC3[7]	TQSC3[6]	TQSC3[5]	TQSC3[4]	TQSC3[3]	TQSC3[2]	TQSC3[1]	TQSC3[0]
Default	0	0	0	0	0	0	1	1

Bits 7 to 0: Transmit Queue Size Connection 3 (TQSC3[7] to TQSC3[0]). These 7 bits of the size of transmit queue associated with connection 3. The queue address size is defined in increments of 32 packets. The queue size is AR.TQSC3 multiplied by 32 to determine the number of 2048 byte packets that can be stored in the queue. The range of bytes will depend on the external SDRAM connected to the DS33Z44. Transmit queue is the data queue for data arriving on the WAN that is sent to the MAC. **Note that queue size of 0 is not allowed and should never be set.**

Register Name: **AR.RQSC4**
Register Description: **Arbiter Receive Queue Size Connection 4**
Register Address: **46h**

Bit #	7	6	5	4	3	2	1	0
Name	RQSC4[7]	RQSC4[6]	RQSC4[5]	RQSC4[4]	RQSC4[3]	RQSC4[2]	RQSC4[1]	RQSC4[0]
Default	0	0	1	1	1	1	0	1

Bits 7 to 0: Receive Queue Size Connection 4 (RQSC4[7] to RQSC4[0]). These 7 bits of the size of receive queue associated with connection 4. Receive queue is for data arriving from the MAC to be sent to the WAN. The Queue address size is defined in increments of 32 x 2048 bytes. The queue size is AR.RQSC4 multiplied by 32 to determine the number of 2048 byte packets that can be stored in the queue. This queue is constructed in the external SDRAM**. Note: Queue size of 0 is not allowed and should never be set.**

Register Name: **AR.TQSC4**
Register Description: **Arbiter Transmit Queue Size Connection 4**
Register Address: **47h**

Bit #	7	6	5	4	3	2	1	0
Name	TQSC4[7]	TQSC4[6]	TQSC4[5]	TQSC4[4]	TQSC4[3]	TQSC4[2]	TQSC4[1]	TQSC4[0]
Default	0	0	0	0	0	0	1	1

Bits 7 to 0: Transmit Queue Size Connection 4 (TQSC4[7] to TQSC4[0]). These 7 bits of the size of transmit queue associated with connection 4. The queue address size is defined in increments of 32 packets. The queue size is AR.TQSC4 multiplied by 32 to determine the number of 2048 byte packets that can be stored in the queue. The range of bytes will depend on the external SDRAM connected to the DS33Z44. Transmit queue is the data queue for data arriving on the WAN that is sent to the MAC. **Note that queue size of 0 is not allowed and should never be set.**

9.4 BERT Registers

Register Name: **BCR**
Register Description: **BERT Control Register**
Register Address: **80h**

Bit #	7	6	5	4	3	2	1	0
Name	—	PMU	RNPL	RPIC	MPR	APRD	TNPL	TPIC
Default	0	0	0	0	0	0	0	0

Bit 7: This bit must be kept low for proper operation.

Bit 6: Performance Monitoring Update (PMU). This bit causes a performance monitoring update to be initiated A 0 to 1 transition causes the performance monitoring registers to be updated with the latest data, and the counters reset (0 or 1). For a second performance monitoring update to be initiated, this bit must be set to 0, and back to 1. If PMU goes low before the PMS bit goes high, an update might not be performed.

Bit 5: Receive New Pattern Load (RNPL). A zero to one transition of this bit will cause the programmed test pattern (QRSS, PTS, PLF [4:0}, PTF [4:0], and BSP [31:0]) to be loaded in to the receive pattern generator. This bit must be changed to zero and back to one for another pattern to be loaded. Loading a new pattern will forces the receive pattern generator out of the “Sync” state which causes a resynchronization to be initiated. Note: QRSS, PTS, PLF [4:0}, PTF [4:0], and BSP [31:0] must not change from the time this bit transitions from 0 to 1 until four RXCK clock cycle after this bit transitions from 0 to 1.

Bit 4: Receive Pattern Inversion Control (RPIC). When 0, the receive incoming data stream is not altered. When 1, the receive incoming data stream is inverted.

Bit 3: Manual Pattern Resynchronization (MPR). A zero to one transition of this bit will cause the receive pattern generator to resynchronize to the incoming pattern. This bit must be changed to zero and back to one for another resynchronization to be initiated. Note: A manual resynchronization forces the receive pattern generator out of the “Sync” state.

Bit 2: Automatic Pattern Resynchronization Disable (APRD). When 0, the receive pattern generator will automatically resynchronize to the incoming pattern if six or more times during the current 64-bit window the incoming data stream bit and the receive pattern generator output bit did not match. When 1, the receive pattern generator will not automatically resynchronize to the incoming pattern. Note: Automatic synchronization is prevented by not allowing the receive pattern generator to automatically exit the “Sync” state.

Bit 1: Transmit New Pattern Load (TNPL). A zero to one transition of this bit will cause the programmed test pattern (QRSS, PTS, PLF[4:0], PTF[4:0], and BSP[31:0]) to be loaded in to the transmit pattern generator. This bit must be changed to zero and back to one for another pattern to be loaded. Note: QRSS, PTS, PLF[4:0], PTF[4:0], and BSP[31:0] must not change from the time this bit transitions from 0 to 1 until four TXCK clock cycle after this bit transitions from 0 to 1.

Bit 0: Transmit Pattern Inversion Control (TPIC). When 0, the transmit outgoing data stream is not altered. When 1, the transmit outgoing data stream is inverted.

Register Name: **BPCLR**
Register Description: **BERT Pattern Configuration Low Register**
Register Address: **82h**

Bit #	7	6	5	4	3	2	1	0
Name	—	QRSS	PTS	PLF4	PLF3	PLF2	PLF1	PLF0
Default	0	0	0	0	0	0	0	0

The BERT's BPCLR, BPCHR, and BSPB registers are used for polynomial-based pattern generation, with a formula of $x^n + x^y + 1$. The initial value for x (the seed) is placed in the BSPB (bert seed/pattern) register. The BERT generates a series of bits by iteration of the formula.

Bit 6: QRSS Enable (QRSS). When 0, the pattern generator configuration is controlled by PTS, PLF[0:4], and PTF[0:4], and BSP[0:31]. When 1, the pattern generator configuration is forced to a QRSS pattern with a generating polynomial of $x^{20} + x^{17} + 1$. The output of the pattern generator is forced to one if the next fourteen output bits are all zero.

Bit 5: Pattern Type Select (PTS). When 0, the pattern is a PRBS pattern. When 1, the pattern is a repetitive pattern.

Bits 4 to 0: Pattern Length Feedback (PLF4 to PLF0). These five bits control the "length" feedback of the pattern generator. The "length" feedback will be from bit n of the pattern generator (n = PLF[4:0] +1). For a PRBS signal, the feedback is an XOR of bit n and bit y. For a repetitive pattern the feedback is bit n. The values possible are outlined in Section 8.15.

Register Name: **BPCHR**
Register Description: **BERT Pattern Configuration High Register**
Register Address: **83h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	PTF4	PTF3	PTF2	PTF1	PTF0
Default	0	0	0	0	0	0	0	0

Bits 4 to 0: Pattern Tap Feedback (PTF4 to PTF0). These five bits control the PRBS "tap" feedback of the pattern generator. The "tap" feedback will be from bit y of the pattern generator (y = PTF[4:0] +1). These bits are ignored when programmed for a repetitive pattern. For a PRBS signal, the feedback is an XOR of bit n and bit y. The values possible are outlined in Section 8.15.

Register Name: **BSPB0R**
Register Description: **BERT Pattern Byte 0 Register**
Register Address: **84h**

Bit #	7	6	5	4	3	2	1	0
Name	BSP7	BSP6	BSP5	BSP4	BSP3	BSP2	BSP1	BSP0
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: BERT Pattern (BSP7 to BSP]). Lower eight bits of 32 bits. Register description follows next register.

Register Name: **BSPB1R**
Register Description: **BERT Pattern Byte 1 Register**
Register Address: **85h**

Bit #	7	6	5	4	3	2	1	0
Name	BSP15	BSP14	BSP13	BSP12	BSP11	BSP10	BSP9	BSP8
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: BERT Pattern (BSP15 to BSP8). 8 bits of 32 bits. Register description below.

Register Name: **BSPB2R**
Register Description: **BERT Pattern Byte 2 Register**
Register Address: **86h**

Bit #	7	6	5	4	3	2	1	0
Name	BSP23	BSP22	BSP21	BSP20	BSP19	BSP18	BSP17	BSP16
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: BERT Pattern (BSP23 to BSP16). 8 bits of 32 bits. Register description below.

Register Name: **BSPB3R**
Register Description: **BERT Seed/Pattern Byte 3 Register**
Register Address: **87h**

Bit #	7	6	5	4	3	2	1	0
Name	BSP31	BSP30	BSP29	BSP28	BSP27	BSP26	BSP25	BSP24
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: BERT Pattern (BSP31 to BSP24]). Upper 8 bits of 32 bits. Register description below.

BERT Pattern (BSP[31:0]). These 32 bits are the programmable seed for a transmit PRBS pattern, or the programmable pattern for a transmit or receive repetitive pattern. BSP(31) is the first bit output on the transmit side for a 32-bit repetitive pattern or 32-bit length PRBS. BSP(31) is the first bit input on the receive side for a 32-bit repetitive pattern.

Register Name: **TEICR**
Register Description: **Transmit Error Insertion Control Register**
Register Address: **88h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	TEIR2	TEIR1	TEIR0	BEI	TSEI	—
Default	0	0	0	0	0	0	0	0

Bits 5 to 3: Transmit Error Insertion Rate (TEIR2 to TEIR0). These three bits indicate the rate at which errors are inserted in the output data stream. One out of every 10^n bits is inverted. TEIR[2:0] is the value n. A TEIR[2:0] value of 0 disables error insertion at a specific rate. A TEIR[2:0] value of 1 result in every 10^{th} bit being inverted. A TEIR[2:0] value of 2 results in every 100^{th} bit being inverted. Error insertion starts when this register is written to with a TEIR[2:0] value that is non-zero. If this register is written to during the middle of an error insertion process, the new error rate is started after the next error is inserted.

Bit 2: Bit Error Insertion Enable (BEI). When 0, single bit error insertion is disabled. When 1, single bit error insertion is enabled.

Bit 1: Transmit Single Error Insert (TSEI). This bit causes a bit error to be inserted in the transmit data stream if and single bit error insertion is enabled. A 0 to 1 transition causes a single bit error to be inserted. For a second bit error to be inserted, this bit must be set to 0, and back to 1. Note: If this bit transitions more than once between error insertion opportunities, only one error is inserted.

All other bits in this register besides BEI and TSEI and TIER must be reset to 0 for proper operation.

Register Name: **BSR**
Register Description: **BERT Status Register**
Register Address: **8Ch**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	PMS	—	BEC	OOS
Default	0	0	0	0	0	0	0	0

Bit 3: Performance Monitoring Update Status (PMS). This bit indicates the status of the receive performance monitoring register (counters) update. This bit will transition from low to high when the update is completed. PMS is asynchronously forced low when the PMU bit goes low.

Bit 1: Bit Error Count (BEC). When 0, the bit error count is zero. When 1, the bit error count is one or more.

Bit 0: Out Of Synchronization (OOS). When 0, the receive pattern generator is synchronized to the incoming pattern. When 1, the receive pattern generator is not synchronized to the incoming pattern.

Register Name: **BSRL**
Register Description: **BERT Status Register Latched**
Register Address: **8Eh**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	PMSL	BEL	BECL	OOSL
Default	0	0	0	0	0	0	0	0

Bit 3: Performance Monitor Update Status Latched (PMSL). This bit is set when the PMS bit transitions from 0 to 1.

Bit 2: Bit Error Detected Latched (BEL). This bit is set when a bit error is detected.

Bit 1: Bit Error Count Latched (BECL). This bit is set when the BEC bit transitions from 0 to 1.

Bit 0: Out Of Synchronization Latched (OOSL). This bit is set when the OOS bit changes state.

Register Name: **BSRIE**
Register Description: **BERT Status Register Interrupt Enable**
Register Address: **90h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	PMSIE	BEIE	BECIE	OOSIE
Default	0	0	0	0	0	0	0	0

Bit 3: Performance Monitoring Update Status Interrupt Enable (PMSIE). This bit enables an interrupt if the PMSL bit is set.

0 = Interrupt disabled
1 = Interrupt enabled

Bit 2: Bit Error Interrupt Enable (BEIE). This bit enables an interrupt if the BEL bit is set.

0 = Interrupt disabled
1 = Interrupt enabled

Bit 1: Bit Error Count Interrupt Enable (BECIE). This bit enables an interrupt if the BECL bit is set.

0 = Interrupt disabled
1 = Interrupt enabled

Bit 0: Out Of Synchronization Interrupt Enable (OOSIE). This bit enables an interrupt if the OOSL bit is set.

0 = Interrupt disabled
1 = Interrupt enabled

Register Name: **RBECB0R**
Register Description: **Receive Bit Error Count Byte 0 Register**
Register Address: **94h**

Bit #	7	6	5	4	3	2	1	0
Name	BEC7	BEC6	BEC5	BEC4	BEC3	BEC2	BEC1	BEC0
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Bit Error Count (BEC[7:0]). Lower eight bits of 24 bits. Register description below.

Register Name: **RBECB1R**
Register Description: **Receive Bit Error Count Byte 1 Register**
Register Address: **95h**

Bit #	7	6	5	4	3	2	1	0
Name	BEC15	BEC14	BEC13	BEC12	BEC11	BEC10	BEC9	BEC8
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Bit Error Count (BEC[15:8]). Eight bits of a 24-bit value. Register description below.

Register Name: **RBECR2**
Register Description: **Receive Bit Error Count Byte 2 Register**
Register Address: **96h**

Bit #	7	6	5	4	3	2	1	0
Name	BEC23	BEC22	BEC21	BEC20	BEC19	BEC18	BEC17	BEC16
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Bit Error Count (BEC[23:16]). Upper 8 bits of the register.

Bit Error Count (BEC[23:0]). These 24 bits indicate the number of bit errors detected in the incoming data stream. This count stops incrementing when it reaches a count of FF FFFFh. The associated bit error counter will not incremented when an OOS condition exists.

Register Name: **RBCB0**
Register Description: **Receive Bit Count Byte 0 Register**
Register Address: **98h**

Bit #	7	6	5	4	3	2	1	0
Name	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0
Default	0	0	0	0	0	0	0	0

Bits 0 to 7: Bit Count (BC[7:0]). Eight bits of a 32-bit value. Register description below.

Register Name: **RBCB1**
Register Description: **Receive Bit Count Byte 1 Register #1**
Register Address: **99h**

Bit #	7	6	5	4	3	2	1	0
Name	BC15	BC14	BC13	BC12	BC11	BC10	BC9	BC8
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Bit Count (BC[15:8]). Eight bits of a 32-bit value. Register description below.

Register Name: **RBCB2**
Register Description: **Receive Bit Count Byte 2 Register**
Register Address: **9Ah**

Bit #	7	6	5	4	3	2	1	0
Name	BC23	BC22	BC21	BC20	BC19	BC18	BC17	BC16
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Bit Count (BC[23:16]). Eight bits of a 32-bit value. Register description below.

Register Name: **RBCB3**
Register Description: **Receive Bit Count Byte 3 Register**
Register Address: **9Bh**

Bit #	7	6	5	4	3	2	1	0
Name	BC31	BC30	BC29	BC28	BC27	BC26	BC25	BC24
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Bit Count (BC[31:24]). These 32 bits indicate the number of bits in the incoming data stream. This count stops incrementing when it reaches a count of FFFF FFFFh. The associated bit counter will not incremented when an OOS condition exists.

9.5 Serial Interface Registers

The Serial Interface contains the serial HDLC transport circuitry and the associated serial port. The Serial Interface register map consists of registers that are common functions, transmit functions, and receive functions.

Bits that are underlined are read-only; all other bits can be written. All reserved registers and bits with "—" designation should be written to zero, unless specifically noted in the register definition. When read, the information from reserved registers and bits designated with "—" should be discarded.

Counter registers are updated by asserting (low to high transition) the associated performance monitoring update signal (xxPMU). During the counter register update process, the associated performance monitoring status signal (xxPMS) is deasserted. The counter register update process consists of loading the counter register with the current count, resetting the counter, forcing the zero count status indication low for one clock cycle, and then asserting xxPMS. No events are missed during this update procedure.

A latched bit is set when the associated event occurs, and remains set until it is cleared by reading. Once cleared, a latched bit will not be set again until the associated event occurs again. Reserved configuration bits and registers should be written to zero.

9.5.1 Serial Interface Transmit and Common Registers

Serial Interface Transmit registers are used to control the HDLC transmitter associated with each serial interface. Note that throughout this document the HDLC processor is also referred to as a "packet processor."

9.5.2 Serial Interface Transmit Register Bit Descriptions

Register Name: **LI.TSLCR**
Register Description: **Transmit Serial Interface Configuration Register**
Register Address: **0C0h, 180h, 240h, 300h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	TDENPLT
Default	0	0	0	0	0	0	0	0

Bit 0: Transmit Data Enable Polarity (TDENPLT). If set to 1, TDENn is an active-low enable. In the default mode, when TDEN is logic high, the data is enabled and output by the DS33Z44.

Register Name: **LI.RSTPD**
Register Description: **Serial Interface Reset Register**
Register Address: **0C1h, 181h, 241h, 301h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	RESET	—
Default	0	0	0	0	0	0	0	0

Bit 1: Reset (RESET). If this bit set to 1, the Data Path and Control and Status for this interface are reset. The Serial Interface is held in reset as long as this bit is high. This bit must be high for a minimum of 200ns for a valid reset to occur.

Register Name: **LI.LPBK**
Register Description: **Serial Interface Loopback Control Register**
Register Address: **0C2h, 182h, 242h, 302h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	QLP
Default	0	0	0	0	0	0	0	0

Bit 0: Queue Loopback Enable (QLP). If this bit set to 1, data received on the Serial Interface is looped back to the Serial Interface transmitter. Received data will not be sent from the Serial Interface to the Ethernet Interface. Buffered packet data will remain in queue until the loopback is removed.

9.5.3 Transmit HDLC Processor Registers

Register Name: **LI.TPPCL**
Register Description: **Transmit Packet Processor Control Low Register**
Register Address: **0C4h, 184h, 244h, 304h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	TFAD	TF16	TIFV	TSD	TBRE	TIAEI
Default	0	0	0	0	0	0	0	0

Note: *The user should take care not to modify this register value during packet error insertion.*

Bit 5 : Transmit FCS Append Disable (TFAD). This bit controls whether or not an FCS is appended to the end of each packet. When equal to 0, the calculated FCS bytes are appended to packets. When set to 1, packets are transmitted without FCS. In X.86 Mode, FCS is always 32 bits and is always appended to the packet.

Bit 4: Transmit FCS-16 Enable (TF16). When 0, the FCS processing uses a 32-bit FCS. When 1, the FCS processing uses a 16-bit FCS. In X.86 Mode 32-bit FCS processing is enabled.

Bit 3: Transmit Bit Synchronous Interframe Fill Value (TIFV). When 0, interframe fill is done with the flag sequence (7Eh). When 1, interframe fill is done with all ones. This bit is ignored in byte synchronous mode. In X.86 mode the interframe flag is always 7E.

Bit 2: Transmit Scrambling Disable (TSD). When equal to 0, $X^{43}+1$ scrambling is performed. When set to 1, scrambling is disabled. Note that in hardware mode, transmit scrambling is controlled by the SCD hardware pin.

Bit 1: Transmit Bit Reordering Enable (TBRE). When equal to 0, bit reordering is disabled (The first bit transmitted is from the MSB of the transmit FIFO byte TFD [7]). When set to 1, bit reordering is enabled (The first bit transmitted is from the LSB of the transmit FIFO byte TFD [0]). Note that this function can be controlled in Hardware mode with the BREO hardware pin.

Bit 0: Transmit Initiate Automatic Error Insertion (TIAEI). This write-only bit initiates error insertion. See the LI.TEPHC register definition for details of usage.

Register Name: **LI.TIFGC**
Register Description: **Transmit Interframe Gapping Control Register**
Register Address: **0C5h, 185h, 245h, 305h**

Bit #	7	6	5	4	3	2	1	0
Name	TIFG7	TIFG6	TIFG5	TIFG4	TIFG3	TIFG2	TIFG1	TIFG0
Default	0	0	0	0	0	0	0	1

Bits 7 to 0: Transmit Interframe Gapping (TIFG[7:0]). These eight bits indicate the number of additional flags and bytes of interframe fill to be inserted between packets. The number of flags and bytes of interframe fill between packets is at least the value of TIFG[7:0] plus 1. Note: If interframe fill is set to all ones, a TFIG value of 2 or 3 will result in a flag, two bytes of ones, and an additional flag between packets.

Register Name: **LI.TEPLC**
Register Description: **Transmit Errored Packet Low Control Register**
Register Address: **0C6h, 186h, 246h, 306h**

Bit #	7	6	5	4	3	2	1	0
Name	TPEN7	TPEN6	TPEN5	TPEN4	TPEN3	TPEN2	TPEN1	TPEN0
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Transmit Errored Packet Insertion Number (TPEN[7:0]). These eight bits indicate the total number of errored packets to be transmitted when triggered by TIAEI. Error insertion will end after this number of errored packets has been transmitted. A value of FFh results in continuous errored packet insertion at the specified rate.

Register Name: **LI.TEPHC**
Register Description: **Transmit Errored Packet High Control Register**
Register Address: **0C7h, 187h, 247h, 307h**

Bit #	7	6	5	4	3	2	1	0
Name	MEIMS	TPER6	TPER5	TPER4	TPER3	TPER2	TPER1	TPER0
Default	0	0	0	0	0	0	0	0

Bit 7: Manual Error Insert Mode Select (MEIMS). When 0, the transmit manual error insertion signal (TMEI) will not cause errors to be inserted. When 1, TMEI will cause an error to be inserted when it transitions from a 0 to a 1. Note: Enabling TMEI does not disable error insertion using TCER[6:0] and TCEN[7:0].

Bits 6 to 0: Transmit Errored Packet Insertion Rate (TPER[6:0]). These seven bits indicate the rate at which errored packets are to be output. One out of every $x * 10^y$ packets is to be an errored packet. TPER[3:0] is the value x, and TPER[6:4] is the value y, which has a maximum value of 6. If TPER[3:0] has a value of 0h, errored packet insertion is disabled. If TPER[6:4] has a value of 6xh or 7xh the errored packet rate is $x * 10^6$. A TPER[6:0] value of 01h results in every packet being errored. A TPER[6:0] value of 0Fh results in every 15^{th} packet being errored. A TPER[6:0] value of 11h results in every 10^{th} packet being errored.

To initiate automatic error insertion, use the following routine:

1) Configure LI.TEPLC and LI.TEPHC for the desired error insertion mode.
2) Write the LI.TPPCL.TIAEI bit to 1. Note that this bit is write-only.
3) If not using continuous error insertion (LI.TPELC is not equal to FFh), the user should monitor the LI.TPPSR.TEPF bit for completion of the error insertion. If interrupt on completion of error insertion is enabled (LI.TPPSRIE.TEPFIE = 1), the user only needs to wait for the interrupt condition.
4) Proceed with the cleanup routine listed below.

Cleanup routine:

1) Write LI.TEPLC and LI.TEPHC each to 00h.
2) Write the LI.TPPCL.TIAEI bit to 0.

Register Name: **LI.TPPSR**
Register Description: **Transmit Packet Processor Status Register**
Register Address: **0C8h, 188h, 248h, 308h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	TEPF
Default	0	0	0	0	0	0	0	0

Bit 0: Transmit Errored Packet Insertion Finished (TEPF). This bit is set when the number of errored packets indicated by the TPEN[7:0] bits in the TEPC register have been transmitted. This bit is cleared when errored packet insertion is disabled, or a new errored packet insertion process is initiated.

Register Name: **LI.TPPSRL**
Register Description: **Transmit Packet Processor Status Register Latched**
Register Address: **0C9h, 189h, 249h, 309h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	TEPFL
Default	0	0	0	0	0	0	0	0

Bit 0: Transmit Errored Packet Insertion Finished Latched (TEPFL). This bit is set when the TEPF bit in the TPPSR register transitions from zero to one.

Register Name: **LI.TPPSRIE**
Register Description: **Transmit Packet Processor Status Register Interrupt Enable**
Register Address: **0CAh, 18Ah, 24Ah, 30Ah**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	TEPFIE
Default	0	0	0	0	0	0	0	0

Bit 0: Transmit Errored Packet Insertion Finished Interrupt Enable (TEPFIE). This bit enables an interrupt if the TEPFL bit in the LI.TPPSRL register is set.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **LI.TPCR0**
Register Description: **Transmit Packet Count Byte 0**
Register Address: **0CCh, 18Ch, 24Ch, 30Ch**

Bit #	7	6	5	4	3	2	1	0
Name	TPC7	TPC6	TPC5	TPC4	TPC3	TPC2	TPC1	TPC0
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Transmit Packet Count (TPC[7:0]). Eight bits of 24-bit value. Register description below.

Register Name: **LI.TPCR1**
Register Description: **Transmit Packet Count Byte 1**
Register Address: **0CDh, 18Dh, 24Dh, 30Dh**

Bit #	7	6	5	4	3	2	1	0
Name	TPC15	TPC14	TPC13	TPC12	TPC11	TPC10	TPC9	TPC8
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Transmit Packet Count (TPC[15:8]). Eight bits of 24-bit value. Register description below.

Register Name: **LI.TPCR2**
Register Description: **Transmit Packet Count Byte 2**
Register Address: **0CEh, 18Eh, 24Eh, 30Eh**

Bit #	7	6	5	4	3	2	1	0
Name	TPC23	TPC22	TPC21	TPC20	TPC19	TPC18	TPC17	TPC16
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Transmit Packet Count (TPC[23:16]). These 24 bits indicate the number of packets extracted from the Transmit FIFO and output in the outgoing data stream.

Register Name: **LI.TBCR0**
Register Description: **Transmit Byte Count Byte 0**
Register Address: **0D0h, 190h, 250h, 310h**

Bit #	7	6	5	4	3	2	1	0
Name	TBC7	TBC6	TBC5	TBC4	TBC3	TBC2	TBC1	TBC0
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Transmit Byte Count (TBC[0:7]). Eight bits of 32-bit value. Register description below.

Register Name: **LI.TBCR1**
Register Description: **Transmit Byte Count Byte 1**
Register Address: **0D1h, 191h, 251h, 311h**

Bit #	7	6	5	4	3	2	1	0
Name	TBC15	TBC14	TBC13	TBC12	TBC11	TBC10	TBC9	TBC8
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Transmit Byte Count (TBC[15:8]). Eight bits of 32-bit value. Register description below.

Register Name: **LI.TBCR2**
Register Description: **Transmit Byte Count Byte 2**
Register Address: **0D2h, 192h, 252h, 312h**

Bit #	7	6	5	4	3	2	1	0
Name	TBC23	TBC22	TBC21	TBC20	TBC19	TBC18	TBC17	TBC16
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Transmit Byte Count (TBC[23:16]). Eight bits of 32-bit value. Register description below.

Register Name: **LI.TBCR3**
Register Description: **Transmit Byte Count Byte 3**
Register Address: **0D3h, 193h, 253h, 313h**

Bit #	7	6	5	4	3	2	1	0
Name	TBC31	TBC30	TBC29	TBC28	TBC27	TBC26	TBC25	TBC24
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Transmit Byte Count (TBC[31:24]). These 32 bits indicate the number of packet bytes inserted in the outgoing data stream.

Register Name: **LI.TMEI**
Register Description: **Transmit Manual Error Insertion**
Register Address: **0D4h, 194h, 254h, 314h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	TMEI
Default	0	0	0	0	0	0	0	0

Bit 0: Transmit Manual Error Insertion (TMEI). A 0-to-1 transition will insert a single error in the transmit direction.

Register Name: **LI.THPMUU**
Register Description: **Serial Interface Transmit HDLC PMU Update Register**
Register Address: **0D6h, 196h, 256h, 316h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	TPMUU
Default	0	0	0	0	0	0	0	0

Bit 0: Transmit PMU Update (TPMUU). This signal causes the transmit cell/packet processor block performance monitoring registers (counters) to be updated. A 0-to-1 transition causes the performance monitoring registers to be updated with the latest data, and the counters reset (0 or 1). This update updates performance monitoring counters for the serial interface.

Register Name: **LI.THPMUS**
Register Description: **Serial Interface Transmit HDLC PMU Update Status Register**
Register Address: **0D7h, 197h, 257h, 317h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	TPMUS
Default	0	0	0	0	0	0	0	0

Bit 0: Transmit PMU Update Status (TPMUS). This bit is set when the Transmit PMU Update is completed. This bit is cleared when TPMUU is reset.

9.5.4 X.86 Registers

X.86 transmit and common registers are used to control the operation of the X.86 encoder and decoder.

Register Name: **LI.TX86EDE**
Register Description: **X.86 Encoding Decoding Enable**
Register Address: **0D8h, 198h, 258h, 318h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	X86ED
Default	0	0	0	0	0	0	0	0

Bit 0: X.86 Encoding Decoding (X86ED). If this bit is set to 1, X.86 encoding and decoding is enabled for the Transmit and Receive paths. The MAC Frame is encapsulated in the X.86 Frame for Transmit and the X.86 headers are checked for in the received data. If X.86 functionality is selected, the X.86 receiver byte boundary is provided by the RBSYNCn signal and the DS33Z44 provides the transmit byte synchronization TBSYNCn. No HDLC encapsulation is performed.

Register Name: **LI.TRX86A**
Register Description: **Transmit Receive X.86 Address**
Register Address: **0D9h, 199h, 259h, 319h**

Bit #	7	6	5	4	3	2	1	0
Name	X86TRA7	X86TRA6	X86TRA5	X86TRA4	X86TRA3	X86TRA2	X86TRA1	X86TRA0
Default	0	0	0	0	0	1	0	0

Bits 7 to 0: X86 Transmit Receive Address (X86TRA[7:0]). This is the address field for the X.86 transmitter and for the receiver. The register default value is 0x04.

Register Name: **LI.TRX8C**
Register Description: **Transmit Receive X.86 Control**
Register Address: **0DAh, 19Ah, 25Ah, 31Ah**

Bit #	7	6	5	4	3	2	1	0
Name	X86TRC7	X86TRC6	X86TRC5	X86TRC4	X86TRC3	X86TRC2	X86TRC1	X86TRC0
Default	0	0	0	0	0	0	1	1

Bits 7 to 0: X86 Transmit Receive Control (X86TRC[7:0]). This is the control field for the X.86 transmitter and expected value for the receiver. The register is reset to 0x03.

Register Name: **LI.TRX86SAPIH**
Register Description: **Transmit Receive X.86 SAPIH**
Register Address: **0DBh, 19Bh, 25Bh, 31Bh**

Bit #	7	6	5	4	3	2	1	0
Name	TRSAPIH7	TRSAPIH6	TRSAPIH5	TRSAPIH4	TRSAPIH3	TRSAPIH2	TRSAPIH1	TRSAPIH0
Default	1	1	1	1	1	1	1	0

Bits 7 to 0: X86 Transmit Receive Address (TRSAPIH[7:0]). This is the address field for the X.86 transmitter and expected for the receiver. The register is reset to 0xfe.

Register Name: **LI.TRX86SAPIL**
Register Description: **Transmit Receive X.86 SAPIL**
Register Address: **0DCh, 19Ch, 25Ch, 31Ch**

Bit #	7	6	5	4	3	2	1	0
Name	TRSAPIL7	TRSAPIL6	TRSAPIL5	TRSAPIL4	TRSAPIL3	TRSAPIL2	TRSAPIL1	TRSAPIL0
Default	0	0	0	0	0	0	0	1

Bits 7 to 0: X86 Transmit Receive Control (TRSAPIL[7:0]). This is the address field for the X.86 transmitter and expected value for the receiver. The register is reset to 0x01.

Register Name: **LI.CIR**
Register Description: **Committed Information Rate**
Register Address: **0DDh, 19Dh, 25Dh, 31Dh**

Bit #	7	6	5	4	3	2	1	0
Name	CIRE	CIR6	CIR5	CIR4	CIR3	CIR2	CIR1	CIR0
Default	0	0	0	0	0	0	0	1

Bit 7: Committed Information Rate Enable (CIRE). Set this bit to 1 to enable the Committed Information Rate Controller feature.

Bits 6 to 0: Committed Information Rate (CIR[6:0]). These bits provide the value for the committed information rate. The value is multiplied by 500kbps to get the CIR value. The user must ensure that the CIR value is less than or equal to the maximum Serial Interface transmit rate. The valid range is from 1 to 104. Any values outside this range will result in unpredictable behavior. Note that a value of 104 translates to a 52Mbps line rate. Hence if the CIR is above the line rate, the rate is not restricted by the CIR. For instance, if using a T1 line and the CIR is programmed with a value of 104, it has no effect in restricting the rate.

9.5.5 Receive Serial Interface

Serial Receive registers are used to control the HDLC Receiver associated with each Serial Interface. Note that throughout this document HDLC Processor is also referred to as “Packet Processor.” The receive packet processor block has seventeen registers.

9.5.5.1 Register Bit Descriptions

Register Name: **LI.RSLCR**
Register Description: **Receive Serial Interface Configuration Register**
Register Address: **100h, 1C0h, 280h, 340h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	RDENPLT
Default	0	0	0	0	0	0	0	0

Bit 0: Receive Data Enable Polarity (RDENPLT). Receive Data Enable Polarity. If set to 1, RDENn low enables reception of the bit.

Register Name: **LI.RPPCL**
Register Description: **Receive Packet Processor Control Low Register**
Register Address: **101h, 1C1h, 281h, 341h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	RFPD	RF16	RFED	RDD	RBRE	RCCE
Default	0	0	0	0	0	0	0	0

Bit 5: Receive FCS Processing Disable (RFPD). When equal to 0, FCS processing is performed and FCS is appended to packets. When set to 1, FCS processing is disabled (the packets do not have an FCS appended). In X.86 mode, FCS processing is always enabled.

Bit 4: Receive FCS-16 Enable (RF16). When 0, the error checking circuit uses a 32-bit FCS. When 1, the error checking circuit uses a 16-bit FCS. This bit is ignored when FCS processing is disabled. In X.86 mode, the FCS is always 32 bits.

Bit 3: Receive FCS Extraction Disable (RFED). When 0, the FCS bytes are discarded. When 1, the FCS bytes are passed on. This bit is ignored when FCS processing is disabled. In X.86 mode, FCS bytes are discarded.

Bit 2: Receive Descrambling Disable (RDD). When equal to 0, $X^{43}+1$ descrambling is performed. When set to 1, descrambling is disabled.

Bit 1: Receive Bit Reordering Enable (RBRE). When equal to 0, reordering is disabled and the first bit received is expected to be the MSB DT [7] of the byte. When set to 1, bit reordering is enabled and the first bit received is expected to be the LSB DT [0] of the byte. Note that function is controlled by the BREO in Hardware Mode.

Bit 0: Receive Clear-Channel Enable (RCCE). When equal to 0, packet processing is enabled. When set to 1, the device is in clear-channel mode and all packet-processing functions except descrambling and bit reordering are disabled.

Register Name: **LI.RMPSCL**
Register Description: **Receive Maximum Packet Size Control Low Register**
Register Address: **102h, 1C2h, 282h, 342h**

Bit #	7	6	5	4	3	2	1	0
Name	RMX7	RMX6	RMX5	RMX4	RMX3	RMX2	RMX1	RMX0
Default	1	1	1	0	0	0	0	0

Bits 7 to 0: Receive Maximum Packet Size (RMX[7:0]). Eight bits of a 16-bit value. Register description below.

Register Name: **LI.RMPSCH**
Register Description: **Receive Maximum Packet Size Control High Register**
Register Address: **103h, 1C3h, 283h, 343h**

Bit #	7	6	5	4	3	2	1	0
Name	RMX15	RMX14	RMX13	RMX12	RMX11	RMX10	RMX9	RMX8
Default	0	0	0	0	0	1	1	1

Bits 7 to 0: Receive Maximum Packet Size (RMX[15:8]). These 16 bits indicate the maximum allowable packet size in bytes. The size includes the FCS bytes, but excludes bit/byte stuffing. Note: If the maximum packet size is less than the minimum packet size, all packets are discarded. When packet processing is disabled, these sixteen bits indicate the "packet" size the incoming data is to be broken into.

The maximum packet size allowable is 2016 bytes plus the FCS bytes. Any values programmed that are greater than 2016 + FCS will have the same effect as 2016+ FCS value.

In X.86 mode, the X.86 encapsulation bytes are included in maximum size control.

Register Name: **LI.RPPSR**
Register Description: **Receive Packet Processor Status Register**
Register Address: **104h, 1C4h, 284h, 344h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	REPC	RAPC	RSPC
Default	0	0	0	0	0	0	0	0

Bit 2: Receive FCS Errored Packet Count (REPC). This read-only bit indicates that the receive FCS errored packet count is non-zero.

Bit 1: Receive Aborted Packet Count (RAPC). This read-only bit indicates that the receive aborted packet count is non-zero.

Bit 0: Receive Size Violation Packet Count (RSPC). This read-only bit indicates that the receive size violation packet count is non-zero.

Register Name: **LI.RPPSRL**
Register Description: **Receive Packet Processor Status Register Latched**
Register Address: **105h, 1C5h, 285h, 345h**

Bit #	7	6	5	4	3	2	1	0
Name	REPL	RAPL	RIPDL	RSPDL	RLPDL	REPCL	RAPCL	RSPCL
Default	0	0	0	0	0	0	0	0

Bit 7: Receive FCS Errored Packet Latched (REPL). This bit is set when a packet with an errored FCS is detected.

Bit 6: Receive Aborted Packet Latched (RAPL). This bit is set when a packet with an abort indication is detected.

Bit 5: Receive Invalid Packet Detected Latched (RIPDL). This bit is set when a packet with a non-integer number of bytes is detected.

Bit 4: Receive Small Packet Detected Latched (RSPDL). This bit is set when a packet smaller than the minimum packet size is detected.

Bit 3: Receive Large Packet Detected Latched (RLPDL). This bit is set when a packet larger than the maximum packet size is detected.

Bit 2: Receive FCS Errored Packet Count Latched (REPCL). This bit is set when the REPC bit in the RPPSR register transitions from zero to one.

Bit 1: Receive Aborted Packet Count Latched (RAPCL). This bit is set when the RAPC bit in the RPPSR register transitions from zero to one.

Bit 0: Receive Size Violation Packet Count Latched (RSPCL). This bit is set when the RSPC bit in the RPPSR register transitions from zero to one.

Register Name: **LI.RPPSRIE**
Register Description: **Receive Packet Processor Status Register Interrupt Enable**
Register Address: **106h, 1C6h, 286h, 346h**

Bit #	7	6	5	4	3	2	1	0
Name	REPIE	RAPIE	RIPDIE	RSPDIE	RLPDIE	REPCIE	RAPCIE	RSPCIE
Default	0	0	0	0	0	0	0	0

Bit 7: Receive FCS Errored Packet Interrupt Enable (REPIE). This bit enables an interrupt if the REPL bit in the LI.RPPSRL register is set.

0 = Interrupt disabled
1 = Interrupt enabled

Bit 6: Receive Aborted Packet Interrupt Enable (RAPIE). This bit enables an interrupt if the RAPL bit in the LI.RPPSRL register is set.

0 = Interrupt disabled
1 = Interrupt enabled

Bit 5: Receive Invalid Packet Detected Interrupt Enable (RIPDIE). This bit enables an interrupt if the RIPDL bit in the LI.RPPSRL register is set.

0 = Interrupt disabled
1 = Interrupt enabled

Bit 4: Receive Small Packet Detected Interrupt Enable (RSPDIE). This bit enables an interrupt if the RSPDL bit in the LI.RPPSRL register is set.

0 = Interrupt disabled
1 = Interrupt enabled

Bit 3: Receive Large Packet Detected Interrupt Enable (RLPDIE). This bit enables an interrupt if the RLPDL bit in the LI.RPPSRL register is set.

0 = Interrupt disabled
1 = Interrupt enabled

Bit 2: Receive FCS Errored Packet Count Interrupt Enable (REPCIE). This bit enables an interrupt if the REPCL bit in the LI.RPPSRL register is set. Must be set low when the packets do not have an FCS appended.

0 = Interrupt disabled
1 = Interrupt enabled

Bit 1: Receive Aborted Packet Count Interrupt Enable (RAPCIE). This bit enables an interrupt if the RAPCL bit in the LI.RPPSRL register is set.

0 = Interrupt disabled
1 = Interrupt enabled

Bit 0: Receive Size Violation Packet Count Interrupt Enable (RSPCIE). This bit enables an interrupt if the RSPCL bit in the LI.RPPSRL register is set.

0 = Interrupt disabled
1 = Interrupt enabled

Register Name: **LI.RPCB0**
Register Description: **Receive Packet Count Byte 0 Register**
Register Address: **108h, 1C8h, 288h, 348h**

Bit #	7	6	5	4	3	2	1	0
Name	RPC7	RPC6	RPC5	RPC4	RPC3	RPC2	RPC1	RPC0
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive Packet Count (RPC[7:0]). Eight bits of a 24-bit value. Register description below.

Register Name: **LI.RPCB1**
Register Description: **Receive Packet Count Byte 1 Register**
Register Address: **109h, 1C9h, 289h, 349h**

Bit #	7	6	5	4	3	2	1	0
Name	RPC15	RPC14	RPC13	RPC12	RPC11	RPC10	RPC09	RPC08
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive Packet Count (RPC[15:8]). Eight bits of a 24-bit value. Register description below.

Register Name: **LI.RPCB2**
Register Description: **Receive Packet Count Byte 2 Register**
Register Address: **10Ah, 1CAh, 28Ah, 34Ah**

Bit #	7	6	5	4	3	2	1	0
Name	RPC23	RPC22	RPC21	RPC20	RPC19	RPC18	RPC17	RPC16
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive Packet Count (RPC[23:16]). These 24 bits indicate the number of packets stored in the receive FIFO without an abort indication. Note: Packets discarded due to system loopback or an overflow condition are included in this count. This register is valid when clear channel is enabled.

Register Name: **LI.RFPCB0**
Register Description: **Receive FCS Errored Packet Count Byte 0 Register**
Register Address: **10Ch, 1CCh, 28Ch, 34Ch**

Bit #	7	6	5	4	3	2	1	0
Name	RFPC7	RFPC6	RFPC5	RFPC4	RFPC3	RFPC2	RFPC1	RFPC0
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive FCS Errored Packet Count (RFPC[7:0]). Eight bits of a 24-bit value. Register description below.

Register Name: **LI.RFPCB1**
Register Description: **Receive FCS Errored Packet Count Byte 1 Register**
Register Address: **10Dh, 1CDh, 28Dh, 34Dh**

Bit #	7	6	5	4	3	2	1	0
Name	RFPC15	RFPC14	RFPC13	RFPC12	RFPC11	RFPC10	RFPC9	RFPC8
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive FCS Errored Packet Count (RFPC[15:8]). Eight bits of a 24-bit value. Register description below.

Register Name: **LI.RFPCB2**
Register Description: **Receive FCS Errored Packet Count Byte 2 Register**
Register Address: **10Eh, 1CEh, 28Eh, 34Eh**

Bit #	7	6	5	4	3	2	1	0
Name	RFPC23	RFPC22	RFPC21	RFPC20	RFPC19	RFPC18	RFPC17	RFPC16
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive FCS Errored Packet Count (RFPC[23:16]). These 24 bits indicate the number of packets received with an FCS error. The byte count for these packets is included in the receive aborted byte count register REBCR.

Register Name: **LI.RAPCB0**
Register Description: **Receive Aborted Packet Count Byte 0 Register**
Register Address: **110h, 1D0h, 290h, 350h**

Bit #	7	6	5	4	3	2	1	0
Name	RAPC7	RAPC6	RAPC5	RAPC4	RAPC3	RAPC2	RAPC1	RAPC0
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive Aborted Packet Count (RAPC[7:0]). Eight bits of a 24-bit value. Register description below.

Register Name: **LI.RAPCB1**
Register Description: **Receive Aborted Packet Count Byte 1 Register**
Register Address: **111h, 1D1h, 291h, 351h**

Bit #	7	6	5	4	3	2	1	0
Name	RAPC15	RAPC14	RAPC13	RAPC12	RAPC11	RAPC10	RAPC9	RAPC8
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive Aborted Packet Count (RAPC[15:8]). Eight bits of a 24-bit value. Register description below.

Register Name: **LI.RAPCB2**
Register Description: **Receive Aborted Packet Count Byte 2 Register**
Register Address: **112h, 1D2h, 292h, 352h**

Bit #	7	6	5	4	3	2	1	0
Name	RAPC23	RAPC22	RAPC21	RAPC20	RAPC19	RAPC18	RAPC17	RAPC16
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive Aborted Packet Count (RAPC[23:16]). The 24 bit value from these three registers indicates the number of packets received with a packet abort indication. The byte count for these packets is included in the receive aborted byte count register REBCR.

Register Name: **LI.RSPCB0**
Register Description: **Receive Size Violation Packet Count Byte 0 Register**
Register Address: **114h, 1D4h, 294h, 354h**

Bit #	7	6	5	4	3	2	1	0
Name	RSPC7	RSPC6	RSPC5	RSPC4	RSPC3	RSPC2	RSPC1	RSPC0
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive Size Violation Packet Count (RSPC[7:0]). Eight bits of a 24-bit value. Register description below.

Register Name: **LI.RSPCB1**
Register Description: **Receive Size Violation Packet Count Byte 1 Register**
Register Address: **115h, 1D5h, 295h, 355h**

Bit #	7	6	5	4	3	2	1	0
Name	RSPC15	RSPC14	RSPC13	RSPC12	RSPC11	RSPC10	RSPC9	RSPC8
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive Size Violation Packet Count (RSPC[15:8]). Eight bits of a 24-bit value. Register description below.

Register Name: **LI.RSPCB2**
Register Description: **Receive Size Violation Packet Count Byte 2 Registers**
Register Address: **116h, 1D6h, 296h, 356h**

Bit #	7	6	5	4	3	2	1	0
Name	RSPC23	RSPC22	RSPC21	RSPC20	RSPC19	RSPC18	RSPC17	RSPC16
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive Size Violation Packet Count (RSPC[23:16]). These 24 bits indicate the number of packets received with a packet size violation (below minimum, above maximum, or non-integer number of bytes). The byte count for these packets is included in the receive aborted byte count register REBCR.

Register Name: **LI.RBC0**
Register Description: **Receive Byte Count 0 Register**
Register Address: **118h, 1D8h, 298h, 358h**

Bit #	7	6	5	4	3	2	1	0
Name	RBC7	RBC6	RBC5	RBC4	RBC3	RBC2	RBC1	RBC0
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive Byte Count (RBC[7:0]). Eight bits of a 32-bit value. Register description below.

Register Name: **LI.RBC1**
Register Description: **Receive Byte Count 1 Register**
Register Address: **119h, 1D9h, 299h, 359h**

Bit #	7	6	5	4	3	2	1	0
Name	RBC15	RBC14	RBC13	RBC12	RBC11	RBC10	RBC9	RBC8
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive Byte Count (RBC[15:8]). Eight bits of a 32-bit value. Register description below.

Register Name: **LI.RBC2**
Register Description: **Receive Byte Count 2 Register**
Register Address: **11Ah, 1DAh, 29Ah, 35Ah**

Bit #	7	6	5	4	3	2	1	0
Name	RBC23	RBC22	RBC21	RBC20	RBC19	RBC18	RBC17	RBC16
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive Byte Count (RBC[23:16]). Eight bits of a 32-bit value. Register description below.

Register Name: **LI.RBC3**
Register Description: **Receive Byte Count 3 Register**
Register Address: **11Bh, 1DBh, 29Dh, 35Bh**

Bit #	7	6	5	4	3	2	1	0
Name	RBC31	RBC30	RBC29	RBC28	RBC27	RBC26	RBC25	RBC24
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive Byte Count (RBC[31:24]). These 32 bits indicate the number of bytes contained in packets stored in the receive FIFO without an abort indication. Note: Bytes discarded due to FCS extraction, system loopback, FIFO reset, or an overflow condition may be included in this count.

Register Name: **LI.RAC0**
Register Description: **Receive Aborted Byte Count 0 Register**
Register Address: **11Ch, 1DCh, 29Ch, 35Ch**

Bit #	7	6	5	4	3	2	1	0
Name	REBC7	REBC6	REBC5	REBC4	REBC3	REBC2	REBC1	REBC0
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive Aborted Byte Count (RBC[7:0]). Eight bits of a 32-bit value. Register description below.

Register Name: **LI.RAC1**
Register Description: **Receive Aborted Byte Count 1 Register**
Register Address: **11Dh, 1DDh, 29Dh, 35Dh**

Bit #	7	6	5	4	3	2	1	0
Name	REBC15	REBC14	REBC13	REBC12	REBC11	REBC10	REBC9	REBC8
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive Aborted Byte Count (RBC[15:8]). Eight bits of a 32-bit value. Register description below.

Register Name: **LI.RAC2**
Register Description: **Receive Aborted Byte Count 2 Register**
Register Address: **11Eh, 1DEh, 29Eh, 35Eh**

Bit #	7	6	5	4	3	2	1	0
Name	REBC23	REBC22	REBC21	REBC20	REBC19	REBC18	REBC17	REBC16
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive Aborted Byte Count (RBC[16:23]). Eight bits of a 32-bit value. Register description below.

Register Name: **LI.RAC3**
Register Description: **Receive Aborted Byte Count 3 Register**
Register Address: **11Fh, 1DFh, 29Fh, 35Fh**

Bit #	7	6	5	4	3	2	1	0
Name	REBC31	REBC30	REBC29	REBC28	REBC27	REBC26	REBC25	REBC24
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive Aborted Byte Count (REBC[31:24]). These 32 bits indicate the number of bytes contained in packets stored in the receive FIFO with an abort indication. Note: Bytes discarded due to FCS extraction, system loopback, FIFO reset, or an overflow condition may be included in this count.

Register Name: **LI.RHPMUU**
Register Description: **Serial Interface Receive HDLC PMU Update Register**
Register Address: **120h, 1E0h, 2A0h, 360h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	RPMUU
Default	0	0	0	0	0	0	0	0

Bit 0: Receive PMU Update (RPMUU). This signal causes the receive cell/packet processor block performance monitoring registers (counters) to be updated. A 0-to-1 transition causes the performance monitoring registers to be updated with the latest data, and the counters reset (0 or 1). This update updates performance monitoring counters for the Serial Interface.

Register Name: **LI.RHPMUS**
Register Description: **Serial Interface Receive HDLC PMU Update Status Register**
Register Address: **121h, 1E1h, 2A1h, 361h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	RPMUUS
Default	0	0	0	0	0	0	0	0

Bit 0: Receive PMU Update Status (RPMUUS). This bit is set when the Transmit PMU Update is completed. This bit is cleared when RPMUU is set to 0.

Register Name: **LI.RX86S**
Register Description: **Receive X.86 Latched Status Register**
Register Address: **122h, 1E2h, 2A2h, 362h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	SAPIHNE	SAPILNE	CNE	ANE
Default	0	0	0	0	0	0	0	0

Bit 3: SAPI High is Not Equal to LI.TRX86SAPIH Latched Status (SAPIHNE). This latched status bit is set if SAPIH is not equal to LI.TRX86SAPIH. This latched status bit is cleared upon read.

Bit 2: SAPI Low is Not Equal to LI.TRX86SAPIL Latched Status (SAPILNE). This latched status bit is set if SAPIL is not equal to LI.TRX86SAPIL. This latched status bit is cleared upon read.

Bit 1: Control is Not Equal to LI.TRX8C (CNE). This latched status bit is set if the control field is not equal to LI.TRX8C. This latched status bit is cleared upon read.

Bit 0: Address is Not Equal to LI.TRX86A (ANE). This latched status bit is set if the X.86 Address field is not equal to LI.TRX86A. This latched status bit is cleared upon read.

Register Name: **LI.RX86LSIE**
Register Description: **Receive X.86 Interrupt Enable**
Register Address: **123h, 1E3h, 2A3h, 363h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	SAPINE01IM	SAPINEFEIM	CNE3LIM	ANE4IM
Default	0	0	0	0	0	0	0	0

Bit 3: SAPI Octet Not Equal to LI.TRX86SAPIH Interrupt Enable (SAPINE01IM). If this bit is set to 1, LI.RX86S.SAPIHNE will generate an interrupt.

Bit 2: SAPI Octet Not Equal to LI.TRX86SAPIL Interrupt Enable (SAPINEFEIM). If this bit is set to 1, LI.RX86S.SAPILNE will generate an interrupt.

Bit 1: Control Not Equal to LI.TRX8C Interrupt Enable (CNE3LIM). If this bit is set to 1, LI.RX86S.CNE will generate an interrupt.

Bit 0: Address Not Equal to LI.TRX86A Interrupt Enable (ANE4IM). If this bit is set to 1, LI.RX86S.ANE will generate an interrupt.

Register Name: **LI.TQLT**
Register Description: **Serial Interface Transmit Queue Low Threshold (Watermark)**
Register Address: **124h, 1E4h, 2A4h, 364h**

Bit #	7	6	5	4	3	2	1	0
Name	TQLT7	TQLT6	TQLT5	TQLT4	TQLT3	TQLT2	TQLT1	TQLT0
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Transmit Queue Low Threshold (TQLT[7:0]). The transmit queue low threshold for the connection, in increments of 32 packets of 2048 bytes each. The value of this register is multiplied by 32 x 2048 bytes to determine the byte location of the threshold. Note that the transmit queue is for data that was received from the Serial Interface to be sent to the Ethernet Interface.

Register Name: **LI.TQHT**
Register Description: **Serial Interface Transmit Queue High Threshold (Watermark)**
Register Address: **125h, 1E5h, 2A5h, 365h**

Bit #	7	6	5	4	3	2	1	0
Name	TQHT7	TQHT6	TQHT5	TQHT4	TQHT3	TQHT2	TQHT1	TQHT0
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Transmit Queue High Threshold (TQHT[7:0]). The transmit queue high threshold for the connection, in increments of 32 packets of 2048 bytes each. The value of this register is multiplied by 32 x 2048 bytes to determine the byte location of the threshold. Note that the transmit queue is for data that was received from the Serial Interface to be sent to the Ethernet Interface.

Register Name: **LI.TQTIE**
Register Description: **Serial Interface Transmit Queue Cross Threshold Interrupt Enable**
Register Address: **126h, 1E6h, 2A6h, 366h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	TFOVFIE	TQOVFIE	TQHTIE	TQLTIE
Default	0	0	0	0	0	0	0	0

Bit 3: Transmit FIFO Overflow for Connection Interrupt Enable (TFOVFIE). If this bit is set, the watermark interrupt is enabled for TFOVFLS.

Bit 2: Transmit Queue Overflow for Connection Interrupt Enable (TQOVFIE). If this bit is set, the watermark interrupt is enabled for TQOVFLS.

Bit 1: Transmit Queue for Connection High Threshold Interrupt Enable (TQHTIE). If this bit is set, the watermark interrupt is enabled for TQHTS.

Bit 0: Transmit Queue for Connection Low Threshold Interrupt Enable (TQLTIE). If this bit is set, the watermark interrupt is enabled for TQLTS.

Register Name: **LI.TQCTLS**
Register Description: **Serial Interface Transmit Queue Cross Threshold Latched Status**
Register Address: **127h, 1E7h, 2A7h, 367h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	TFOVFLS	TQOVFLS	TQHTLS	TQLTLS
Default	0	0	0	0	0	0	0	0

Bit 3: Transmit Queue FIFO Overflowed Latched Status (TFOVFLS). This bit is set if the transmit queue FIFO has overflowed. This register is cleared after a read. This FIFO is for data to be transmitted from the HDLC to be sent to the SDRAM.

Bit 2: Transmit Queue Overflow Latched Status (TQOVFLS). This bit is set if the transmit queue has overflowed. This register is cleared after a read.

Bit 1: Transmit Queue for Connection Exceeded High Threshold Latched Status (TQHTLS). This bit is set if the transmit queue crosses the high watermark. This register is cleared after a read.

Bit 0: Transmit Queue for Connection Exceeded Low Threshold Latched Status (TQLTLS). This bit is set if the transmit queue crosses the low watermark. This register is cleared after a read.

9.6 Ethernet Interface Registers

The Ethernet Interface registers are used to configure RMII/MII bus operation and establish the MAC parameters as required by the user. The MAC Registers cannot be addressed directly from the processor port. The registers below are used to perform indirect read or write operations to the MAC registers. The MAC Status registers are shown in Table 9-7. Accessing the MAC registers is described in the Section 8.14.

9.6.1 Ethernet Interface Register Bit Descriptions

Register Name: **SU.MACRADL**
Register Description: **MAC Read Address Low Register**
Register Address: **140h, 200h, 2C0h, 380h**

Bit #	7	6	5	4	3	2	1	0
Name	MACRA7	MACRA6	MACRA5	MACRA4	MACRA3	MACRA2	MACRA1	MACRA0
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: MAC Read Address (MACRA[7:0]). Low byte of the MAC address. Used only for read operations.

Register Name: **SU.MACRADH**
Register Description: **MAC Read Address High Register**
Register Address: **141h, 201h, 2C1h, 381h**

Bit #	7	6	5	4	3	2	1	0
Name	MACRA15	MACRA14	MACRA13	MACRA12	MACRA11	MACRA10	MACRA9	MACRA8
Default	0	0	0	0	0	0	0	0

Bits 0 to 7: MAC Read Address (MACRA8-15). High byte of the MAC address. Used only for read operations.

Register Name: **SU.MACRD0**
Register Description: **MAC Read Data Byte 0**
Register Address: **142h, 202h, 2C2h, 382h**

Bit #	7	6	5	4	3	2	1	0
Name	MACRD7	MACRD6	MACRD5	MACRD4	MACRD3	MACRD2	MACRD1	MACRD0
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: MAC Read Data (MACRD[7:0]). One of four bytes of data read from the MAC. Valid after a read command has been issued and the SU.MACRWC.MCS bit is zero.

Register Name: **SU.MACRD1**
Register Description: **MAC Read Data Byte 1**
Register Address: **143h, 203h, 2C3h, 383h**

Bit #	7	6	5	4	3	2	1	0
Name	MACRD15	MACRD14	MACRD13	MACRD12	MACRD11	MACRD10	MACRD9	MACRD8
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: MAC Read Data 1 (MACRD[15:8]). One of four bytes of data read from the MAC. Valid after a read command has been issued and the SU.MACRWC.MCS bit is zero.

Register Name: **SU.MACRD2**
Register Description: **MAC Read Data Byte 2**
Register Address: **144h, 204h, 2C4h, 384h**

Bit #	7	6	5	4	3	2	1	0
Name	MACRD23	MACRD22	MACRD21	MACRD20	MACRD19	MACRD18	MACRD17	MACRD16
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: MAC Read Data 2 (MACRD[23:16]). One of four bytes of data read from the MAC. Valid after a read command has been issued and the SU.MACRWC.MCS bit is zero.

Register Name: **SU.MACRD3**
Register Description: **MAC Read Data Byte 3**
Register Address: **145h, 205h, 2C5h, 385h**

Bit #	7	6	5	4	3	2	1	0
Name	MACRD31	MACRD30	MACRD29	MACRD28	MACRD27	MACRD26	MACRD25	MACRD24
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: MAC Read Data 3 (MACRD[31:24]). One of four bytes of data read from the MAC. Valid after a read command has been issued and the SU.MACRWC.MCS bit is zero.

Register Name: **SU.MACWD0**
Register Description: **MAC Write Data Byte 0**
Register Address: **146h, 206h, 2C6h, 386h**

Bit #	7	6	5	4	3	2	1	0
Name	MACWD7	MACWD6	MACWD5	MACWD4	MACWD3	MACWD2	MACWD1	MACWD0
	0	0	0	0	0	0	0	0

Bits 7 to 0: MAC Write Data 0 (MACWD[7:0]). One of four bytes of data to be written to the MAC. Data has been written after a write command has been issued and the SU.MACRWC.MCS bit is zero.

Register Name: **SU.MACWD1**
Register Description: **MAC Write Data Byte 1**
Register Address: **147h, 207h, 2C7h, 387h**

Bit #	7	6	5	4	3	2	1	0
Name	MACWD15	MACWD14	MACWD13	MACWD12	MACWD11	MACWD10	MACWD09	MACWD08
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: MAC Write Data 1 (MACWD[15:8]). One of four bytes of data to be written to the MAC. Data has been written after a write command has been issued and the SU.MACRWC.MCS bit is zero.

Register Name: **SU.MACWD2**
Register Description: **MAC Write Data Byte 2**
Register Address: **148h, 208h, 2C8h, 388h**

Bit #	7	6	5	4	3	2	1	0
Name	MACWD23	MACWD22	MACWD21	MACWD20	MACWD19	MACWD18	MACWD17	MACWD16
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: MAC Write Data 2 (MACWD[23:16]). One of four bytes of data to be written to the MAC. Data has been written after a write command has been issued and the SU.MACRWC.MCS bit is zero.

Register Name: **SU.MACWD3**
Register Description: **MAC Write Data Byte 3**
Register Address: **149h, 209h, 2C9h, 389h**

Bit #	7	6	5	4	3	2	1	0
Name	MACD31	MACD30	MACD29	MACD28	MACD27	MACD26	MACD25	MACD24
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: MAC Write Data 3 (MACD[31:24]). One of four bytes of data to be written to the MAC. Data has been written after a write command has been issued and the SU.MACRWC.MCS bit is zero.

Register Name: **SU.MACAWL**
Register Description: **MAC Address Write Low**
Register Address: **14Ah, 20Ah, 2CAh, 38Ah**

Bit #	7	6	5	4	3	2	1	0
Name	MACAW7	MACAW6	MACAW5	MACAW4	MACAW3	MACAW2	MACAW1	MACAW0
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: MAC Write Address (MACAW[7:0]). Low byte of the MAC address. Used only for write operations.

Register Name: **SU.MACAWH**
Register Description: **MAC Address Write High**
Register Address: **14Bh, 20Bh, 2CBh, 38Bh**

Bit #	7	6	5	4	3	2	1	0
Name	MACAW15	MACAW14	MACAW13	MACAW12	MACAW11	MACAW10	MACAW9	MACAW8
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: MAC Write Address (MACAW[15:8]). High byte of the MAC address. Used only for write operations.

Register Name: **SU.MACRWC**
Register Description: **MAC Read Write Command Status**
Register Address: **14Ch, 20Ch, 2CCh, 38Ch**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	MCRW	MCS
Default	0	0	0	0	0	0	0	0

Bit 1: MAC Command RW (MCRW). If this bit is written to 1, a read is performed from the MAC. If this bit is written to 0, a write operation is performed. Address information for write operations must be located in SU.MACAWH and SU.MACAWL. Address information for read operations must be located in SU.MACRADH and SU.MACRADL. The user must also write a 1 to the MCS bit, and the DS33Z44 will clear MCS when the operation is complete.

Bit 0: MAC Command Status (MCS). Setting MCS in conjunction with MCRW will initiate a read or write to the MAC registers. Upon completion of the read or write this bit is cleared. Once a read or write command has been initiated the host must poll this bit to see when the operation is complete.

Register Name: **SU.LPBK**
Register Description: **Ethernet Interface Loopback Control Register**
Register Address: **14Fh, 20Fh, 2CFh, 38Fh**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	QLP
Default	0	0	0	0	0	0	0	0

Bit 0: Queue Loopback Enable (QLP). If this bit is set to 1, data from the Ethernet Interface receive queue is looped back to the transmit queue. Buffered data from the Serial Interface will remain until the loopback is removed.

Register Name: **SU.GCR**
Register Description: **Ethernet Interface General Control Register**
Register Address: **150h, 210h, 2D0h, 390h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	CRCS	H10S	ATFLOW	JAME
Default	0	0	0	0	0	0	1	0

Bit 3: CRCS. If this bit is zero (default), the MAC or Ethernet CRC is stripped before the data is encapsulated and transmitted. If this bit is set to 1, the CRC is not stripped before transport, it is recalculated and added to the received data that arrives on the WAN before retransmission. It is assumed that CRC has been stripped before transport. Note that the maximum packet size supported by the Ethernet interface is still 2016 (this includes the 4 bytes of CRC).

Bit 2: H10S. This bit controls the 10/100 selection for RMII and DCE Mode. **When in RMII mode, setting** this bit to 1 will cause the MAC will operate at 100 Mbps and setting this bit to zero will cause the MAC to operate at 10 Mbps. When in DCE mode, the bit function is inverted—setting this bit to 1 will cause the MAC to operate at 10 Mbps. In DTE and MII mode, the MAC determines the data rate from the incoming TX_CLK and RX_CLK.

Bit 1: Automatic Flow Control Enable (ATFLOW). If this bit is set to 1, automatic flow control is enabled based on the connection receive queue size and high watermarks. Pause frames are sent automatically in full-duplex mode. The pause time must be programmed through SU.MACFCR. The jam sequence will not be sent automatically in half-duplex mode unless the JAME bit is set. This bit is applicable only in software mode.

Bit 0: Jam Enable (JAME). If this bit is set to 1, a Jam sequence is sent for a duration of 4 bytes. This function is only valid in half-duplex mode, and will only function if Automatic Flow Control is disabled. Note that if the receive queue size is less than receive high threshold, setting a JAME will JAM one received frame. If JAME is set and the receiver queue size is higher than the high threshold, all received frames are jammed until the queue empties below the threshold.

Note that SU.GCR is only valid in the software mode. In hardware mode, pins are used to control Automatic flow control and 100/10-speed selection.

Register Name: **SU.TFRC**
Register Description: **Transmit Frame Resend Control**
Register Address: **151h, 211h, 2D1h, 391h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	NCFQ	TPDFCB	TPRHBC	TPRCB
Default	0	0	0	0	0	0	0	0

Bit 3: No Carrier Queue Flush Bar (NCFQ). If this bit is set to 1, the queue for data passing from Serial Interface to Ethernet Interface will not be flushed when loss of carrier is detected.

Bit 2: Transmit Packet Deferred Fail Control Enable (TPDFCB). If this bit if set to 1, the current frame is transmitted immediately instead of being deferred. If this bit is set to 0, the frame is deferred if CRS is asserted and sent when the CRS is unasserted indicating the media is idle.

Bit 1: Transmit Packet HB Fail Control Bar (TPRHBC). If this bit is set to 1, the current frame will not be retransmitted if a heartbeat failure is detected.

Bit 0: Transmit Packet Resend Control Bar (TPRCB). If this bit is set to 1, the current frame will not be retransmitted if any of the following errors have occurred:

- Jabber timeout
- Loss of carrier
- Excessive deferral
- Late collision
- Excessive collisions
- Under run
- Collision

Note that blocking retransmission due to collision (applicable in MIII/Half-Duplex Mode) can result in unpredictable system level behavior.

Register Name: **SU.TFSL**
Register Description: **Transmit Frame Status Low**
Register Address: **152h, 212h, 2D2h, 392h**

Bit #	7	6	5	4	3	2	1	0
Name	UR	EC	LC	ED	LOC	NOC	—	FABORT
Default	0	0	0	0	0	0	0	0

Bit 7: Under Run (UR). When this bit is set to 1, the frame was aborted due to a data under run condition of the transmit buffer.

Bit 6: Excessive Collisions (EC). When this bit is set to 1, a frame has been aborted after 16 successive collisions while attempting to transmit the current frame. If the Disable Retry bit is set to 1, then Excessive Collisions will be set to 1 after the first collision.

Bit 5: Late Collision (LC). When this bit is set to 1, a frame was aborted by collision after the 64 bit collision window. Not valid if an under run has occurred.

Bit 4: Excessive Deferral (ED). When this bit is set to 1, a frame was aborted due to excessive deferral.

Bit 3: Loss Of Carrier (LOC). When this bit is set to 1, a frame was aborted due to loss of carrier for one or more bit times. Valid only for non-collided frames. Valid only in half-duplex operation.

Bit 2: No Carrier (NOC). When this bit is set to 1, a frame was aborted because no carrier was found for transmission.

Bit 0: Frame Abort (FABORT). When this bit is set to 1, the MAC has aborted a frame for one of the above reasons. When this bit is clear, the previous frame has been transmitted successfully.

Register Name: **SU.TFSH**
Register Description: **Transmit Frame Status High**
Register Address: **153h, 213h, 2D3h, 393h**

Bit #	7	6	5	4	3	2	1	0
Name	PR	HBF	CC3	CC2	CC1	CC0	LCO	DEF
Default	0	0	0	0	0	0	0	0

Bit 7: Packet Resend (PR). When this bit is set, the current packet must be retransmitted due to a collision.

Bit 6: Heartbeat Failure (HBF). When this bit is set, the device failed to detect a heart beat after transmission. This bit is not valid if an under run has occurred.

Bits 5 to 2: Collision Count (CC[3:0]). These four bits indicate the number of collisions that occurred prior to successful transmission of the previous frame. Not valid if Excessive Collisions is set to 1.

Bit 1: Late Collision (LCO). When set to 1, the MAC observed a collision after the 64-byte collision window.

Bit 0: Deferred Frame (DEF). When set to 1, the current frame was deferred due to carrier assertion by another node after being ready to transmit.

Register Name: **SU.RFSB0**
Register Description: **Receive Frame Status Byte 0**
Register Address: **154h, 214h, 2D4h, 394h**

Bit #	7	6	5	4	3	2	1	0
Name	FL7	FL6	FL5	FL4	FL3	FL2	FL1	FL0
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Frame Length (FL[7:0]). These eight bits are the low byte of the length (in bytes) of the received frame, with FCS and Padding. If Automatic Pad Stripping is enabled, this value is the length of the received packet without PCS or Pad bytes. The upper six bits are contained in SU.RFSB1.

Register Name: **SU.RFSB1**
Register Description: **Receive Frame Status Byte 1**
Register Address: **155h, 215h, 2D5h, 395h**

Bit #	7	6	5	4	3	2	1	0
Name	RF	WT	FL13	FL12	FL11	FL10	FL9	FL8
Default	0	0	0	0	0	0	0	0

Bit 7: Runt Frame (RF). This bit is set to 1 if the received frame was altered by a collision or terminated within the collision window.

Bit 6: Watchdog Timeout (WT). This bit is set to 1 if a packet receive time exceeds 2048 byte times. After 2048 byte times the receiver is disabled and the received frame will fail CRC check.

Bits 5 to 0: Frame Length (FL[13:8]). These six bits are the upper bits of the length (in bytes) of the received frame, with FCS and Padding. If Automatic Pad Stripping is enabled, this value is the length of the received packet without PCS or Pad bytes.

Register Name: **SU.RFSB2**
Register Description: **Receive Frame Status Byte 2**
Register Address: **156h, 216h, 2D6h, 396h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	CRCE	DB	MIIE	FT	CS	FTL
Default	0	0	0	0	0	0	0	0

Bit 5: CRC Error (CRCE). This bit is set to 1 if the received frame does not contain a valid CRC value.

Bit 4: Dribbling Bit (DB). This bit is set to 1 if the received frame contains a non-integer multiple of 8 bits. It does not indicate that the frame is invalid. This bit is not valid for runt or collided frames.

Bit 3: MII Error (MIIE). This bit is set to 1 if an error was found on the MII bus.

Bit 2: Frame Type (FT). This bit is set to 1 if the received frame exceeds 1536 bytes. It is equal to zero if the received frame is an 802.3 frame. This bit is not valid for runt frames.

Bit 1: Collision Seen (CS). This bit is set to 1 if a late collision occurred on the received packet. A late collision is one that occurs after the 64 byte collision window.

Bit 0: Frame Too Long (FTL). This bit is set to 1 if a frame exceeds the 1518 byte maximum standard Ethernet frame. This bit is only an indication, and causes no frame truncation.

Register Name: **SU.RFSB3**
Register Description: **Receive Frame Status Byte 3**
Register Address: **157h, 217h, 2D7h, 397h**

Bit #	7	6	5	4	3	2	1	0
Name	MF	—	—	BF	MCF	UF	CF	LE
Default	0	0	0	0	0	0	0	0

Bit 7: Missed Frame (MF). This bit is set to 1 if the packet is not successfully received from the MAC by the packet Arbiter.

Bit 4: Broadcast Frame (BF). This bit is set to 1 if the current frame is a broadcast frame.

Bit 3: Multicast Frame (MCF). This bit is set to 1 if the current frame is a multicast frame.

Bit 2: Unsupported Control Frame (UF). This bit is set to 1 if the frame received is a control frame with an opcode that is not supported. If the Control Frame bit is set, and the Unsupported Control Frame bit is clear, then a pause frame has been received and the transmitter is paused.

Bit 1: Control Frame (CF). This bit is set to 1 when the current frame is a control frame. This bit is only valid in full-duplex mode.

Bit 0: Length Error (LE). This bit is set to 1 when the frames length field and the actual byte count are unequal. This bit is only valid for 802.3 frames.

Register Name: **SU.RMFSRL**
Register Description: **Receiver Maximum Frame Low Register**
Register Address: **158h, 218h, 2D8h, 398h**

Bit #	7	6	5	4	3	2	1	0
Name	RMPS7	RMPS6	RMPS5	RMPS4	RMPS3	RMPS2	RMPS1	RMPS0
Default	1	1	1	0	0	0	0	0

Bits 7 to 0: Receiver Maximum Frame (RMPS[7:0]). Eight bits of 16-bit value. Register description below.

Register Name: **SU.RMFSRH**
Register Description: **Receiver Maximum Frame High Register**
Register Address: **159h, 219h, 2D9h, 399h**

Bit #	7	6	5	4	3	2	1	0
Name	RMPS15	RMPS14	RMPS13	RMPS12	RMPS11	RMPS10	RMPS9	RMPS8
Default	0	0	0	0	0	1	1	1

Bits 7 to 0: Receiver Maximum Frame (RMPS[15:8]). This value is the receiver's maximum frame size (in bytes), up to a maximum of 2016 bytes. Any frame received greater than this value is rejected. The frame size includes destination address, source address, type/length, data and CRC-32. The frame size is not the same as the frame length encoded within the IEEE 802.3 frame. **Any values programmed that are greater than 2016 will have unpredictable behavior and should be avoided.**

Register Name: **SU.RQLT**
Register Description: **Receive Queue Low Threshold (Watermark)**
Register Address: **15Ah, 21Ah, 2DAh, 39Ah**

Bit #	7	6	5	4	3	2	1	0
Name	RQLT7	RQLT6	RQLT5	RQLT4	RQLT3	RQLT2	RQLT1	RQLT0
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive Queue Low Threshold (RQLT[7:0]). The receive queue low threshold for the connection, in increments of 32 packets of 2048 bytes each. The value of this register is multiplied by 32 x 2048 bytes to determine the byte location of the threshold. Note that the receive queue is for data that was received from the Ethernet Interface to be sent to the Serial Interface.

Register Name: **SU.RQHT**
Register Description: **Receive Queue High Threshold (Watermark)**
Register Address: **15Bh, 21Bh, 2DBh, 39Bh**

Bit #	7	6	5	4	3	2	1	0
Name	RQHT7	RQHT6	RQHT5	RQHT4	RQHT3	RQHT2	RQHT1	RQHT0
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive Queue High Threshold (RQTH[7:0]). The receive queue high threshold for the connection, in increments of 32 packets of 2048 bytes each. The value of this register is multiplied by 32 x 2048 bytes to determine the byte location of the threshold. Note that the receive queue is for data that was received from the Ethernet Interface to be sent to the Serial Interface.

Register Name: **SU.QRIE**
Register Description: **Receive Queue Cross Threshold enable**
Register Address: **15Ch, 21Ch, 2DCh, 39Ch**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	RFOVFIE	RQVFIE	RQLTIE	RQHTIE
Default	0	0	0	0	0	0	0	0

Bit 3: Receive FIFO Overflow Interrupt Enable (RFOVFIE). If this bit is set, the interrupt is enabled for RFOVFLS.

Bit 2: Receive Queue Overflow Interrupt Enable (RQVFIE). If this bit is set, the interrupt is enabled for RQOVFLS.

Bit 1: Receive Queue Crosses Low Threshold Interrupt Enable (RQLTIE). If this bit is set, the watermark interrupt is enabled for RQLTS.

Bit 0: Receive Queue Crosses High Threshold Interrupt Enable (RQHTIE). If this bit is set, the watermark interrupt is enabled for RQHTS.

Register Name: **SU.QCRLS**
Register Description: **Queue Cross Threshold Latched Status**
Register Address: **15Dh, 21Dh, 2DDh, 39Dh**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	RFOVFLS	RQOVFLS	RQHTLS	RQLTLS
Default	0	0	0	0	0	0	0	0

Bit 3: Receive FIFO Overflow latched Status (RFOVFLS). This bit is set if the receive FIFO overflows for the data to be transmitted from the MAC to the SDRAM.

Bit 2: Receive Queue Overflow Latched Status (RQOVFLS). This bit is set if the receive queue has overflowed. This register is cleared after a read.

Bit 1: Receive Queue for Connection Crossed High Threshold Latched Status (RQHTLS). This bit is set if the receive queue crosses the high watermark. This register is cleared after a read.

Bit 0: Receive Queue for Connection Crossed Low Threshold Latched Status (RQLTLS). This bit is set if the receive queue crosses the low watermark. This register is cleared after a read.

Note the bit order differences in the high/low threshold indications in SU.QCRLS and the interrupt enables in SU.QRIE.

Register Name: **SU.RFRC**
Register Description: **Receive Frame Rejection Control**
Register Address: **15Eh, 21Eh, 2DEh, 39Eh**

Bit #	7	6	5	4	3	2	1	0
Name—	UCFR	CFRR	LERR	CRCERR	DBR	MIIER	BERR	
Default	0	0	0	0	0	0	0	0

Bit 6: Uncontrolled Control Frame Reject (UCFR). When set to 1, Control Frames other than Pause Frames are allowed. When this bit is equal to zero, non-pause control frames are rejected.

Bit 5: Control Frame Reject (CFRR). When set to 1, control frames are allowed. When this bit is equal to zero, all control frames are rejected.

Bit 4: Length Error Reject (CRCERR). When set to 1, frames with an unmatched frame length field and actual number of bytes received are allowed. When equal to zero, only frames with matching length fields and actual bytes received will be allowed.

Bit 3: CRC Error Reject (CRCERR). When set to 1, frames received with a CRC error or MII error are allowed. When equal to zero, frames with CRC or MII errors are rejected.

Bit 2: Dribbling Bit Reject (DBR). When set to 1, frames with lengths of non-integer multiples of 8 bits are allowed. When equal to zero, frames with dribbling bits are rejected. The dribbling bit setting is only valid only if there is not a collision or runt frame.

Bit 1: MII Error Reject (MIIER). When set to 1, frames are allowed with MII Receive Errors. When equal to zero, frames with MII errors are rejected.

Bit 0: Broadcast Frame Reject (BERR). When set to 1, broadcast frames are allowed. When equal to zero, broadcast frames are rejected.

9.6.2 MAC Registers

The control registers related to the control of the individual MACs are shown in the following table. The DS33Z44 keeps statistics for the packet traffic sent and received. The register address map is shown in the following table. Note that the addresses listed are the indirect addresses that must be provided to SU.MACRADH/SU.MACRADL or SU.MACAWH/SU.MACAWL.

Register Name: **SU.MACCR**
Register Description: **MAC Control Register**
Register Address: **0000h (indirect)**

0000h:

Bit #	31	30	29	28	27	26	25	24
Name	RA	Reserved	Reserved	HDB	PS	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

0001h:

Bit #	23	22	21	20	19	18	17	16
Name	DRO	Reserved	OML0	F	PM	PAM	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

0002h:

Bit #	15	14	13	12	11	10	09	08
Name	Reserved	Reserved	Reserved	LCC	Reserved	DRTY	Reserved	ASTP
Default	0	0	0	0	0	0	0	0

0003h:

Bit #	07	06	05	04	03	02	01	00
Name	BOLMT1	BOLMT0	DC	Reserved	TE	RE	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

Bit 31: Receive All Mode Select (RA). When set to 1, address filtering is performed on all incoming packets. When equal to 0, only packets that pass Destination Address filtering will be received.

Bit 28: Heartbeat Disable (HDB). When set to 1, the heartbeat (SQE) function is disabled. This bit should be set to 1 when operating in MII mode.

Bit 27: Port Select (PS). This bit should be equal to 0 for proper operation.

Bit 23: Disable Receive Own (DRO). When set to 1, the MAC disables the reception of frames while TX_ENn is asserted. When this bit equals zero, transmitted frames are also received by the MAC. This bit should be cleared when operating in full-duplex mode. This bit must be set to 1 for half-duplex operation.

Bit 21: Loopback Operating Mode (OML0). When set to 1, data is looped from the transmit side, back to the receive side, without being transmitted to the PHY.

Bit 20: Full-Duplex Mode Select (F). When set to 1, the MAC transmits and receives data simultaneously. When in full-duplex mode, the heartbeat check is disabled and the heartbeat fail status should be ignored.

Bit 19: Promiscuous Mode (PM). When set to 1, the MAC is in Promiscuous Mode and forwards all frames. Note that the default value is 1.

Bit 18: Pass All Multicast (PAM). When set to 1, the MAC forwards Multicast Frames.

Bit 12: Late Collision Control (LCC). When set to 1, enables retransmission of a collided packet even after the collision period. When this bit is clear, retransmission of late collisions is disabled.

Bit 10: Disable Retry (DRTY). When set to 1, the MAC makes only a single attempt to transmit each frame. If a collision occurs, the MAC ignores the current frame and proceeds to the next frame. When this bit equals 0, the MAC will retry collided packets 16 times before signaling a retry error.

Bit 8: Automatic Pad Stripping (ASTP). When set to 1, all incoming frames with less than 46 byte length are automatically stripped of the pad characters and FCS.

Bits 7 and 6: Back-Off Limit (BOLMT[1:0]). These two bits allow the user to set the back-off limit used for the maximum retransmission delay for collided packets. Default operation limits the maximum delay for retransmission to a countdown of 10 bits from a random number generator. The user can reduce the maximum number of counter bits as described in the table below. See IEEE 802.3 for details of the back-off algorithm.

Bit 7	Bit 6	Random Number Generator Bits Used
0	0	**10**
0	1	**8**
1	0	**4**
1	1	**1**

Bit 5: Deferral Check (DC). When set to 1, the MAC will abort packet transmission if it has deferred for more than 24,288 bit times. The deferral counter starts when the transmitter is ready to transmit a packet, but is prevented from transmission because CRS is active. If the MAC begins transmission but a collision occurs after the beginning of transmission, the deferral counter is reset again. If this bit is equal to zero, then the MAC will defer indefinitely.

Bit 3: Transmitter Enable (TE). When set to 1, packet transmission is enabled. When equal to zero, transmission is disabled.

Bit 2: Receiver Enable (RE). When set to 1, packet reception is enabled. When equal to zero, packets are not received.

Register Name: **SU.MACAH**
Register Description: **MAC Address High Register**
Register Address: **0004h (indirect)**

0004h:

Bit #	31	30	29	28	27	26	25	24
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	1	1	1	1	1	1	1	1

0005h:

Bit #	23	22	21	20	19	18	17	16
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	1	1	1	1	1	1	1	1

0006h:

Bit #	15	14	13	12	11	10	09	08
Name	PADR47	PADR46	PADR45	PADR44	PADR43	PADR42	PADR41	PADR40
Default	1	1	1	1	1	1	1	1

0007h:

Bit #	07	06	05	04	03	02	01	00
Name	PADR39	PADR38	PADR37	PADR36	PADR35	PADR34	PADR33	PADR32
Default	1	1	1	1	1	1	1	1

These 32 bits should be initialized with the upper 4 bytes of the Physical Address for this MAC device.

Register Name: **SU.MACAL**
Register Description: **MAC Address Low Register**
Register Address: **0008h (indirect)**

0008h:

Bit #	31	30	29	28	27	26	25	24
Name	PADR31	PADR30	PADR29	PADR28	PADR27	PADR26	PADR25	PADR24
Default	1	1	1	1	1	1	1	1

0009h:

Bit #	23	22	21	20	19	18	17	16
Name	PADR23	PADR22	PADR21	PADR20	PADR19	PADR18	PADR17	PADR16
Default	1	1	1	1	1	1	1	1

000Ah:

Bit #	15	14	13	12	11	10	09	08
Name	PADR15	PADR14	PADR13	PADR12	PADR11	PADR10	PADR09	PADR08
Default	1	1	1	1	1	1	1	1

000Bh:

Bit #	07	06	05	04	03	02	01	00
Name	PADR07	PADR06	PADR05	PADR04	PADR03	PADR02	PADR01	PADR00
Default	1	1	1	1	1	1	1	1

These 32 bits should be initialized with the lower 4 bytes of the Physical Address for this MAC device.

Register Name: **SU.MACMAH**
Register Description: **MAC Multicast Address High Register**
Register Address: **000Ch (indirect)**

000Ch:

Bit #	31	30	29	28	27	26	25	24
Name	MMA63	MMA62	MMA61	MMA60	MMA59	MMA58	MMA57	MMA56
Default	1	1	1	1	1	1	1	1

000Dh:

Bit #	23	22	21	20	19	18	17	16
Name	MMA55	MMA54	MMA53	MMA52	MMA51	MMA50	MMA49	MMA48
Default	1	1	1	1	1	1	1	1

000Eh:

Bit #	15	14	13	12	11	10	09	08
Name	MMA47	MMA46	MMA45	MMA44	MMA43	MMA42	MMA41	MMA40
Default	1	1	1	1	1	1	1	1

000Fh:

Bit #	07	06	05	04	03	02	01	00
Name	MMA39	MMA38	MMA37	MMA36	MMA35	MMA34	MMA33	MMA32
Default	1	1	1	1	1	1	1	1

These registers can be initialized with the upper 4 bytes of a 64-bit hash table for group address filtering.

Register Name: **SU.MACMAL**
Register Description: **MAC Multicast Address Low Register**
Register Address: **0010h (indirect)**

0010h:

Bit #	31	30	29	28	27	26	25	24
Name	MMA31	MMA30	MMA29	MMA28	MMA27	MMA26	MMA25	MMA24
Default	0	0	0	0	0	0	0	0

0011h:

Bit #	23	22	21	20	19	18	17	16
Name	MMA23	MMA22	MMA21	MMA20	MMA19	MMA18	MMA17	MMA16
Default	0	0	0	0	0	0	0	0

0012h:

Bit #	15	14	13	12	11	10	09	08
Name	MMA15	MMA14	MMA13	MMA12	MMA11	MMA10	MMA09	MMA08
Default	0	0	0	0	0	0	0	0

0013h:

Bit #	07	06	05	04	03	02	01	00
Name	MMA07	MMA06	MMA05	MMA04	MMA03	MMA02	MMA01	MMA00
Default	0	0	0	0	0	0	0	0

These registers can be initialized with the lower 4 bytes of a 64-bit hash table for group address filtering.

Register Name: **SU.MACMIIA**
Register Description: **MAC MII Management (MDIO) Address Register**
Register Address: **0014h (indirect)**

0014h:

Bit #	31	30	29	28	27	26	25	24
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

0015h:

Bit #	23	22	21	20	19	18	17	16
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

0016h:

Bit #	15	14	13	12	11	10	09	08
Name	PHYA4	PHYA3	PHYA2	PHYA1	PHYA0	MIIA4	MIIA3	MIIA2
Default	0	1	0	1	1	0	1	0

0017h:

Bit #	07	06	05	04	03	02	01	00
Name	MIIA1	MIIA0	Reserved	Reserved	Reserved	Reserved	MIIW	MIIB
Default	1	1	0	0	0	0	0	0

Bits 15 to 11: PHY Address (PHYA[4:0]). These five bits select one of the 32 available PHY address locations to access through the PHY management (MDIO) bus.

Bits 10 to 6: MII Address (MIIA[4:0]). These five bits are the address location within the PHY that is being accessed.

Bit 1: MII Write (MIIW). Write this bit to 1 in order to execute a write instruction over the MDIO interface. Write the bit to zero to execute a read instruction.

Bit 0: MII Busy (MIIB). This bit is set to 1 by the DS33Z44 during execution of a MII management instruction through the MDIO interface, and is set to zero when the DS33Z44 has completed the instruction. The user should read this bit and ensure that it is equal to zero prior to beginning a MDIO instruction.

Note that this register is only valid for MAC 1.

Register Name: **SU.MACMIID**
Register Description: **MAC MII (MDIO) Data Register**
Register Address: **0018h (indirect)**

0018h:

Bit #	31	30	29	28	27	26	25	24
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

0019h:

Bit #	23	22	21	20	19	18	17	16
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

001Ah:

Bit #	15	14	13	12	11	10	09	08
Name	MIID15	MIID14	MIID13	MIID12	MIID11	MIID10	MIID09	MIID08
Default	0	0	0	0	0	0	0	0

001Bh:

Bit #	07	06	05	04	03	02	01	00
Name	MIID07	MIID06	MIID05	MIID04	MIID03	MIID02	MIID01	MIID00
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: MII (MDIO) Data (MIID[15:00]. These two bytes contain the data to be written to or the data read from the MII management interface (MDIO).

Note that this register is only valid for MAC 1.

Register Name: **SU.MACFCR**
Register Description: **MAC Flow Control Register**
Register Address: **001Ch (indirect)**

001Ch:

Bit #	31	30	29	28	27	26	25	24
Name	PT15	PT14	PT13	PT12	PT11	PT10	PT09	PT08
Default	0	0	0	0	0	0	0	0

001Dh:

Bit #	23	22	21	20	19	18	17	16
Name	PT07	PT06	PT05	PT04	PT03	PT02	PT01	PT00
Default	0	1	0	1	0	0	0	0

001Eh:

Bit #	15	14	13	12	11	10	09	08
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

001Fh:

Bit #	07	06	05	04	03	02	01	00
Name	Reserved	Reserved	Reserved	Reserved	Reserved	PCF	FCE	FCB
Default	0	0	0	0	0	0	1	0

Bits 31 to 16: Pause Time (PT[15:00]. These bits are used for the Pause Time Field in transmitted Pause Frames. This value is the number of time slots the remote node should wait prior to transmission.

Bit 2: Pass Control Frames (PCF). When set to 1, the MAC will set the Packet Filter bit to indicate that it has received a control or pause frame. When FCE is also set to 1, the MAC will respond to control and pause frames, but also passes them. When this bit equals zero, all frames, including control and pause frames are passed. The other address filtering modes take precedence over this bit.

Bit 1: Flow Control Enable (FCE). When set to 1, the MAC automatically detects pause frames and will disable the transmitter for the requested pause time.

Bit 0: Flow Control Busy (FCB). The host can set this bit to 1 in order to initiate transmission of a pause frame. During transmission of a pause frame, this bit remains set. The DS33Z44 will clear this bit when transmission of the pause frame has been completed. The user should read this bit and ensure that this bit is equal to zero prior to initiating a pause frame.

Register Name: **SU.MMCCTRL**
Register Description: **MAC MMC Control Register**
Register Address: **0100h (indirect)**

0100h:

Bit #	31	30	29	28	27	26	25	24
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

0101h:

Bit #	23	22	21	20	19	18	17	16
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

0102h:

Bit #	15	14	13	12	11	10	09	08
Name	Reserved	Reserved	MXFRM10	MXFRM9	MXFRM8	MXFRM7	MXFRM6	MXFRM5
Default	0	0	1	0	1	1	1	1

0103h:

Bit #	07	06	05	04	03	02	01	00
Name	MXFRM4	MXFRM3	MXFRM2	MXFRM1	MXFRM0	Reserved	Reserved	Reserved
Default	0	1	1	1	0	0	1	0

Bits 13 to 3: Maximum Frame Size (MXFRM[10:0]). These bits indicate the maximum packet size value. All transmitted frames larger than this value are counted as long frames.

Register Name: **Reserved**
Register Description: **MAC Reserved Control Register**
Register Address: **010Ch (indirect)**

010Ch:

Bit #	31	30	29	28	27	26	25	24
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

010Dh:

Bit #	23	22	21	20	19	18	17	16
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

010Eh:

Bit #	15	14	13	12	11	10	09	08
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

010Fh:

Bit #	07	06	05	04	03	02	01	00
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

Note: Addresses 10Ch through 10Fh must each be initialized with all ones (FFh) for proper operation.

Register Name: **Reserved**
Register Description: **MAC Reserved Control Register**
Register Address: **0110h (indirect)**

0110h:

Bit #	31	30	29	28	27	26	25	24
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

0111h:

Bit #	23	22	21	20	19	18	17	16
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

0112h:

Bit #	15	14	13	12	11	10	09	08
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

0113h:

Bit #	07	06	05	04	03	02	01	00
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

Note: Addresses 110h through 113h must each be initialized with all ones (FFh) for proper operation.

Register Name: **SU.RxFrmCtr**
Register Description: **MAC All Frames Received Counter**
Register Address: **0200h (indirect)**

0200h:

Bit #	31	30	29	28	27	26	25	24
Name	RXFRMC31	RXFRMC30	RXFRMC29	RXFRMC28	RXFRMC27	RXFRMC26	RXFRMC25	RXFRMC24
Default	0	0	0	0	0	0	0	0

0201h:

Bit #	23	22	21	20	19	18	17	16
Name	RXFRMC23	RXFRMC22	RXFRMC21	RXFRMC20	RXFRMC19	RXFRMC18	RXFRMC17	RXFRMC16
Default	0	0	0	0	0	0	0	0

0202h:

Bit #	15	14	13	12	11	10	09	08
Name	RXFRMC15	RXFRMC14	RXFRMC13	RXFRMC12	RXFRMC11	RXFRMC10	RXFRMC9	RXFRMC8
Default	0	0	0	0	0	0	0	0

0203h:

Bit #	07	06	05	04	03	02	01	00
Name	RXFRMC7	RXFRMC6	RXFRMC5	RXFRMC4	RXFRMC3	RXFRMC2	RXFRMC1	RXFRMC0
Default	0	0	0	0	0	0	0	0

Bits 31 to 0: All Frames Received Counter (RXFRMC[31:0]): 32-bit value indicating the number of frames received. Each time a frame is received, this counter is incremented by 1. This counter resets only upon device reset, does not saturate, and rolls over to zero upon reaching the maximum value. The user should ensure that the measurement period is less than the minimum length of time required for the counter to increment 2^32-1 times at the maximum frame rate. The user should store the value from the beginning of the measurement period for later calculations, and take into account the possibility of a roll-over to occurring.

Register Name: **SU.RxFrmOkCtr**
Register Description: **MAC Frames Received OK Counter**
Register Address: **0204h (indirect)**

0204h:

Bit #	31	30	29	28	27	26	25	24
Name	RXFRMOK31	RXFRMOK30	RXFRMOK29	RXFRMOK28	RXFRMOK27	RXFRMOK26	RXFRMOK25	RXFRMOK24
Default	0	0	0	0	0	0	0	0

0205h:

Bit #	23	22	21	20	19	18	17	16
Name	RXFRMOK23	RXFRMOK22	RXFRMOK21	RXFRMOK20	RXFRMOK19	RXFRMOK18	RXFRMOK17	RXFRMOK16
Default	0	0	0	0	0	0	0	0

0206h:

Bit #	15	14	13	12	11	10	09	08
Name	RXFRMOK15	RXFRMOK14	RXFRMOK13	RXFRMOK12	RXFRMOK11	RXFRMOK10	RXFRMOK9	RXFRMOK8
Default	0	0	0	0	0	0	0	0

0207h:

Bit #	07	06	05	04	03	02	01	00
Name	RXFRMOK7	RXFRMOK6	RXFRMOK5	RXFRMOK4	RXFRMOK3	RXFRMOK2	RXFRMOK1	RXFRMOK0
Default	0	0	0	0	0	0	0	0

Bits 31 to 0: Frames Received OK Counter (RXFRMOK[31:0]). 32-bit value indicating the number of frames received and determined to be valid. Each time a valid frame is received, this counter is incremented by 1. This counter resets only upon device reset, does not saturate, and rolls over to zero upon reaching the maximum value. The user should ensure that the measurement period is less than the minimum length of time required for the counter to increment 2^32-1 times at the maximum frame rate. The user should store the value from the beginning of the measurement period for later calculations, and take into account the possibility of a roll-over to occurring.

Register Name: **SU.TxFrmCtr**
Register Description: **MAC All Frames Transmitted Counter**
Register Address: **0300h (indirect)**

0300h:

Bit #	31	30	29	28	27	26	25	24
Name	TXFRMC31	TXFRMC30	TXFRMC29	TXFRMC28	TXFRMC27	TXFRMC26	TXFRMC25	TXFRMC24
Default	0	0	0	0	0	0	0	0

0301h:

Bit #	23	22	21	20	19	18	17	16
Name	TXFRMC23	TXFRMC22	TXFRMC21	TXFRMC20	TXFRMC19	TXFRMC18	TXFRMC17	TXFRMC16
Default	0	0	0	0	0	0	0	0

0302h:

Bit #	15	14	13	12	11	10	09	08
Name	TXFRMC15	TXFRMC14	TXFRMC13	TXFRMC12	TXFRMC11	TXFRMC10	TXFRMC9	TXFRMC8
Default	0	0	0	0	0	0	0	0

0303h:

Bit #	07	06	05	04	03	02	01	00
Name	TXFRMC7	TXFRMC6	TXFRMC5	TXFRMC4	TXFRMC3	TXFRMC2	TXFRMC1	TXFRMC0
Default	0	0	0	0	0	0	0	0

Bits 31 to 0: All Frames Transmitted Counter (TXFRMC[31:0]). 32-bit value indicating the number of frames transmitted. Each time a frame is transmitted, this counter is incremented by 1. This counter resets only upon device reset, does not saturate, and rolls over to zero upon reaching the maximum value. The user should ensure that the measurement period is less than the minimum length of time required for the counter to increment 2^32-1 times at the maximum frame rate. The user should store the value from the beginning of the measurement period for later calculations, and take into account the possibility of a roll-over to occurring.

Register Name: **SU.TxBytesCtr**
Register Description: **MAC All Bytes Transmitted Counter**
Register Address: **0308h (indirect)**

0308h:

Bit #	31	30	29	28	27	26	25	24
Name	TXBYTEC31	TXBYTEC30	TXBYTEC29	TXBYTEC28	TXBYTEC27	TXBYTEC26	TXBYTEC25	TXBYTEC24
Default	0	0	0	0	0	0	0	0

0309h:

Bit #	23	22	21	20	19	18	17	16
Name	TXBYTEC23	TXBYTEC22	TXBYTEC21	TXBYTEC20	TXBYTEC19	TXBYTEC18	TXBYTEC17	TXBYTEC16
Default	0	0	0	0	0	0	0	0

030Ah:

Bit #	15	14	13	12	11	10	09	08
Name	TXBYTEC15	TXBYTEC14	TXBYTEC13	TXBYTEC12	TXBYTEC11	TXBYTEC10	TXBYTEC9	TXBYTEC8
Default	0	0	0	0	0	0	0	0

030Bh:

Bit #	07	06	05	04	03	02	01	00
Name	TXBYTEC7	TXBYTEC6	TXBYTEC5	TXBYTEC4	TXBYTEC3	TXBYTEC2	TXBYTEC1	TXBYTEC0
Default	0	0	0	0	0	0	0	0

Bits 31 to 0: All Bytes Transmitted Counter (TXBYTEC[31:0]). 32-bit value indicating the number of bytes transmitted. Each time a byte is transmitted, this counter is incremented by 1. This counter resets only upon device reset, does not saturate, and rolls over to zero upon reaching the maximum value. The user should ensure that the measurement period is less than the minimum length of time required for the counter to increment 2^32-1 times at the maximum data rate. The user should store the value from the beginning of the measurement period for later calculations, and take into account the possibility of a roll-over to occurring.

Register Name: **SU.TxBytesOkCtr**
Register Description: **MAC Bytes Transmitted OK Counter**
Register Address: **030Ch (indirect)**

030Ch:

Bit #	31	30	29	28	27	26	25	24
Name	TXBYTEOK31	TXBYTEOK30	TXBYTEOK29	TXBYTEOK28	TXBYTEOK27	TXBYTEOK26	TXBYTEOK25	TXBYTEOK24
Default	0	0	0	0	0	0	0	0

030Dh:

Bit #	23	22	21	20	19	18	17	16
Name	TXBYTEOK23	TXBYTEOK22	TXBYTEOK21	TXBYTEOK20	TXBYTEOK19	TXBYTEOK18	TXBYTEOK17	TXBYTEOK16
Default	0	0	0	0	0	0	0	0

030Eh:

Bit #	15	14	13	12	11	10	09	08
Name	TXBYTEOK15	TXBYTEOK14	TXBYTEOK13	TXBYTEOK12	TXBYTEOK11	TXBYTEOK10	TXBYTEOK9	TXBYTEOK8
Default	0	0	0	0	0	0	0	0

030Fh:

Bit #	07	06	05	04	03	02	01	00
Name	TXBYTEOK7	TXBYTEOK6	TXBYTEOK5	TXBYTEOK4	TXBYTEOK3	TXBYTEOK2	TXBYTEOK1	TXBYTEOK0
Default	0	0	0	0	0	0	0	0

Bits 31 to 0: Bytes Transmitted OK Counter (TXBYTEOK[31: 0]). 32-bit value indicating the number of bytes transmitted and determined to be valid. Each time a valid byte is transmitted, this counter is incremented by 1. This counter resets only upon device reset, does not saturate, and rolls over to zero upon reaching the maximum value. The user should ensure that the measurement period is less than the minimum length of time required for the counter to increment 2^32-1 times at the maximum frame rate. The user should store the value from the beginning of the measurement period for later calculations, and take into account the possibility of a roll-over to occurring.

Register Name: **SU.TXFRMUNDR**
Register Description: **MAC Transmit Frame Underrun Counter**
Register Address: **0334h (indirect)**

0334h:

Bit #	31	30	29	28	27	26	25	24
Name	TXFRMU31	TXFRMU30	TXFRMU29	TXFRMU28	TXFRMU27	TXFRMU26	TXFRMU25	TXFRMU24
Default	0	0	0	0	0	0	0	0

0335h:

Bit #	23	22	21	20	19	18	17	16
Name	TXFRMU23	TXFRMU22	TXFRMU21	TXFRMU20	TXFRMU19	TXFRMU18	TXFRMU17	TXFRMU16
Default	0	0	0	0	0	0	0	0

0336h:

Bit #	15	14	13	12	11	10	09	08
Name	TXFRMU15	TXFRMU14	TXFRMU13	TXFRMU12	TXFRMU11	TXFRMU10	TXFRMU9	TXFRMU8
Default	0	0	0	0	0	0	0	0

0337h:

Bit #	07	06	05	04	03	02	01	00
Name	TXFRMU7	TXFRMU6	TXFRMU5	TXFRMU4	TXFRMU3	TXFRMU2	TXFRMU1	TXFRMU0
Default	0	0	0	0	0	0	0	0

Bits 31 to 0: Frames Aborted Due to FIFO Underrun Counter (TXFRMU[31:0]). 32-bit value indicating the number of frames aborted due to FIFO under run. Each time a frame is aborted due to FIFO under run, this counter is incremented by 1. This counter resets only upon device reset, does not saturate, and rolls over to zero upon reaching the maximum value. The user should ensure that the measurement period is less than the minimum length of time required for the counter to increment 2^32-1 times at the maximum frame rate. The user should store the value from the beginning of the measurement period for later calculations, and take into account the possibility of a rollover to occurring.

Register Name: **SU.TxBdFrmCtr**
Register Description: **MAC All Frames Aborted Counter**
Register Address: **0338h (indirect)**

0338h:

Bit #	31	30	29	28	27	26	25	24
Name	TXFRMBD31	TXFRMBD30	TXFRMBD29	TXFRMBD28	TXFRMBD27	TXFRMBD26	TXFRMBD25	TXFRMBD24
Default	0	0	0	0	0	0	0	0

0339h:

Bit #	23	22	21	20	19	18	17	16
Name	TXFRMBD23	TXFRMBD22	TXFRMBD21	TXFRMBD20	TXFRMBD19	TXFRMBD18	TXFRMBD17	TXFRMBD16
Default	0	0	0	0	0	0	0	0

033Ah:

Bit #	15	14	13	12	11	10	09	08
Name	TXFRMBD15	TXFRMBD14	TXFRMBD13	TXFRMBD12	TXFRMBD11	TXFRMBD10	TXFRMBD9	TXFRMBD8
Default	0	0	0	0	0	0	0	0

033Bh:

Bit #	07	06	05	04	03	02	01	00
Name	TXFRMBD7	TXFRMBD6	TXFRMBD5	TXFRMBD4	TXFRMBD3	TXFRMBD2	TXFRMBD1	TXFRMBD0
Default	0	0	0	0	0	0	0	0

Bits 31 to 0: All Frames Aborted Counter (TXFRMBD[31:0]). 32-bit value indicating the number of frames aborted due to any reason. Each time a frame is aborted, this counter is incremented by 1. This counter resets only upon device reset, does not saturate, and rolls over to zero upon reaching the maximum value. The user should ensure that the measurement period is less than the minimum length of time required for the counter to increment 2^32-1 times at the maximum frame rate. The user should store the value from the beginning of the measurement period for later calculations, and take into account the possibility of a roll-over to occurring.

10 FUNCTIONAL TIMING

10.1 Functional Serial I/O Timing

The Serial Interface provides flexible timing to interconnect with a wide variety of serial interfaces. TDENn is an input signal that can be used to enable or block the TSERn data. The “shaded bits” are not clocked by the DS33Z44. The TDENn must occur one bit before the effected bit in the TSERn stream. Note that polarity of the TDENn is selectable through LI.TSLCR. In the figure below, TDENn is active low, allowing the bits to clock, and inactive high, causing the next data bit not to be clocked. TCLK can be gapped as shown in the following figure. Similarly, the receiver function is governed by RCLKIn, RDENn and RSERn. RSERn data will not be provided to the receiver for the bits blocked when RDENn is inactive. The RDENn polarity can be programmed by LI.RSLCR. The RDENn signal must be coincident with the RSERn bit that needs to be blocked.

Figure 10-1. Tx Serial Interface Functional Timing

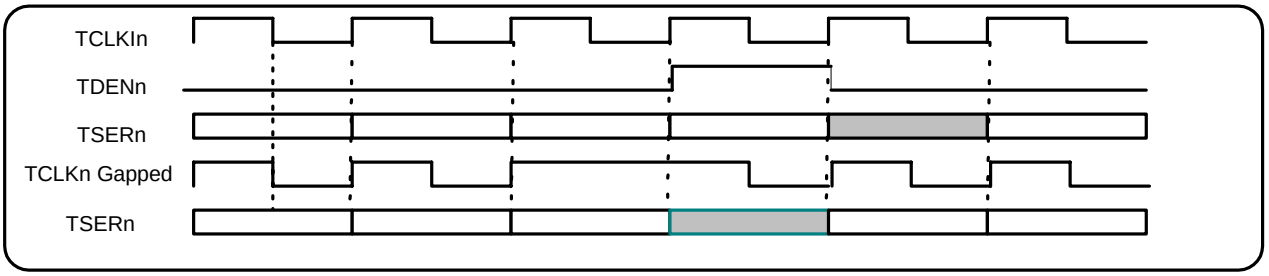
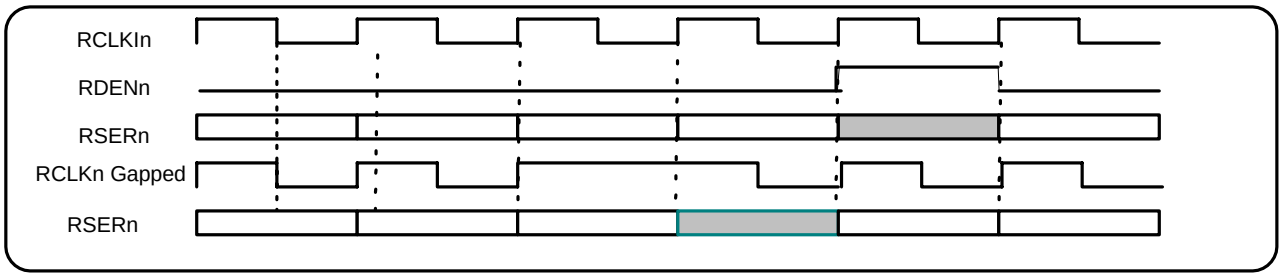


Figure 10-2. Rx Serial Interface Functional Timing



The DS33Z44 provides the TBSYNC1-4 signals as a byte boundary indication to an external interface when X.86 (LAPS) functionality is selected. The functional timing of TBSYNCn is shown in the following figure. TBSYNCn is active high on the last bit of the byte being shifted out, and occurs every 8 bits. For the serial receiver interface, RBSYNCn is used to provide byte boundary indication to the DS33Z44 when X.86 (LAPS) mode is used. The functional timing is shown in Figure 10-3. In X.86 Mode, the receiver expects the RBSYNCn byte indicator as shown in Figure 10-4.

Figure 10-3. Transmit Byte Sync Functional timing

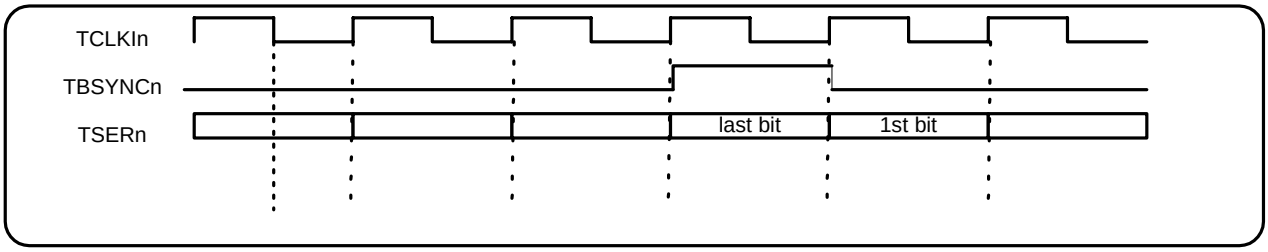
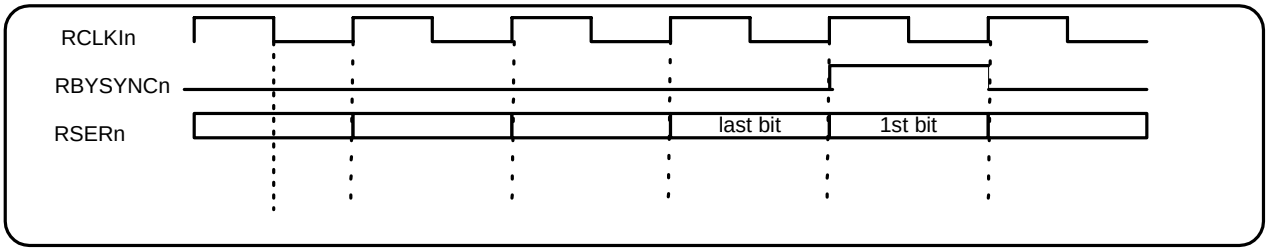


Figure 10-4. Receive Byte Sync Functional Timing



10.2 MII and RMII Interfaces

The MII Interface Transmit Port has its own transmit clock and data interface. The data bus TXDn[3:0] operates synchronously with TX_CLKn. The LSB is presented first. TX_CLKn should be 2.5MHz for 10Mbps operation and 25MHz for 100Mbps operation. TX_ENn is valid at the same time as the first byte of the preamble. In DTE Mode TX_CLKn is input from the external PHY. In DCE Mode, the DS33Z44 provides TX_CLKn, derived from an external reference (SYSCLKI).

In Half-Duplex (DTE) Mode, the DS33Z44 supports CRS and COL signals. CRS is active when the PHY detects transmit or receive activity. If there is a collision as indicated by the COL input, the DS33Z44 will replace the data nibbles with jam nibbles. After a “random“ time interval, the packet is retransmitted. The MAC will try to send the packet a maximum of 16 times. The jam sequence consists of 55555555h. Note that the COL signal and CRS can be asynchronous to TX_CLKn and are only valid in half-duplex mode.

Figure 10-5. MII Transmit Functional Timing

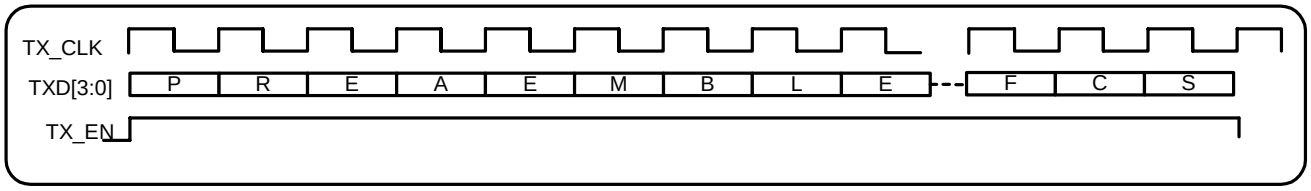
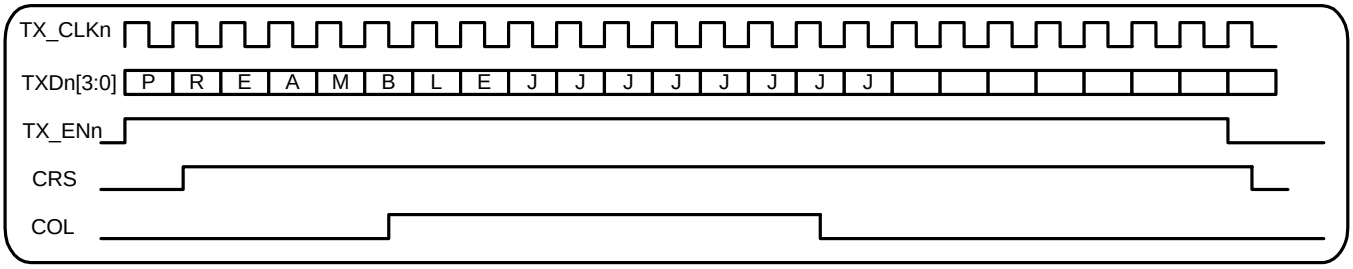
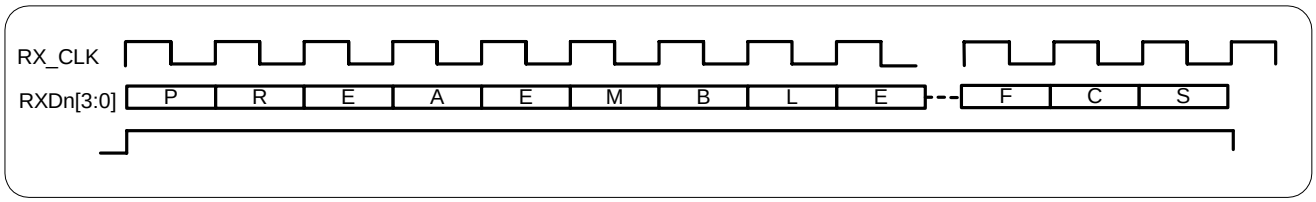


Figure 10-6. MII Transmit Half-Duplex with a Collision Functional Timing



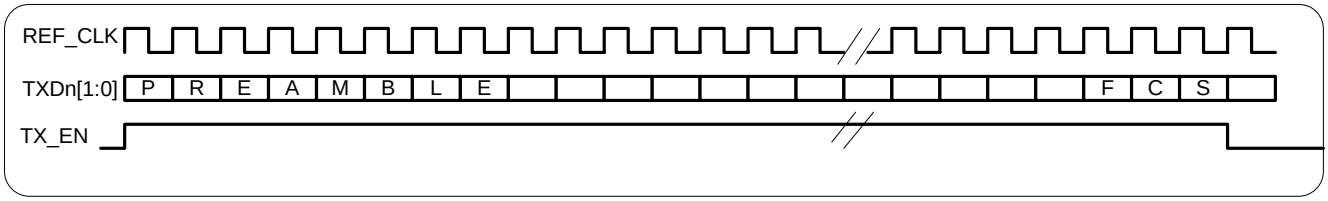
Receive Data (RXDn[3:0]) is clocked from the external PHY synchronously with RX_CLKn. The RX_CLKn signal is 2.5MHz for 10Mbps operation and 25MHz for 100Mbps operation. RX_DVn is asserted by the PHY from the first Nibble of the preamble in 100Mbps operation or first nibble of SFD for 10Mbps operation. The data on RXDn[3:0] is not accepted by the MAC if RX_DVn is low or RX_ERRn is high (in DTE mode). RX_ERRn should be tied low when in DCE Mode.

Figure 10-7. MII Receive Functional Timing



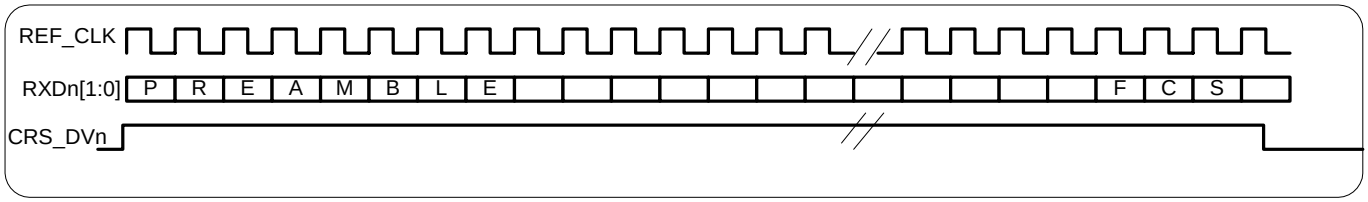
In RMII Mode, TX_ENn is high with the first bit of the preamble. The TXDn[1:0] is synchronous with the 50MHz REFCLK. For 10Mbps operation, the data bit outputs are updated every 10 clocks.

Figure 10-8. RMII Transmit Interface Functional Timing



RMII Receive data on RXDn[1:0] is expected to be synchronous with the rising edge of the 50MHz REFCLK. The data is only valid if CRS_DVn is high. The external PHY asynchronously drives CRS_DVn low during carrier loss.

Figure 10-9. RMII Receive Interface Functional Timing



10.3 SPI Interface Mode and EEPROM Program Sequence

The DS33Z44 will act as an SPI Master when configured with MODEC[1:0] to read the configuration from an external Serial EEPROM, such as the Atmel AT25160A. The EEPROM must be programmed with the data structure shown in Table 10-1. The MOSI (Master Out-Slave In) signal can be selectively output on the rising or falling edge of SPICK. The MISO data can be sampled on rising or falling edge of SPICK based on the CKPHA pin input. The SPICK is generated by the DS33Z44 at a frequency of 8.33MHz, derived from an external SYSCLKI of 100MHz. The initialization sequence is commenced immediately after power-up reset or a rising edge of the $\overline{RST}$ input pin. The SPI master initiates a read with the instruction code 0000x011b; followed by the address location. The $\overline{SPI\_CS}$ is held low until the data addressed is read and latched. The DS33Z44 begins reading the EEPROM at address 0000h. Data is sequentially latched until the last data byte is read and latched.

The indirect MAC registers require a special program sequence at the end of the EEPROM file. Four MAC registers can be programmed in the EEPROM Mode: SU.MACCR, SU.MACMIIA, SU.MACMIID, and SU.MACFCR. The indirect MAC registers are programmed using four separate seven-byte records from the EEPROM. An example is shown in Table 10-2.

Figure 10-10. SPI Master Functional Timing

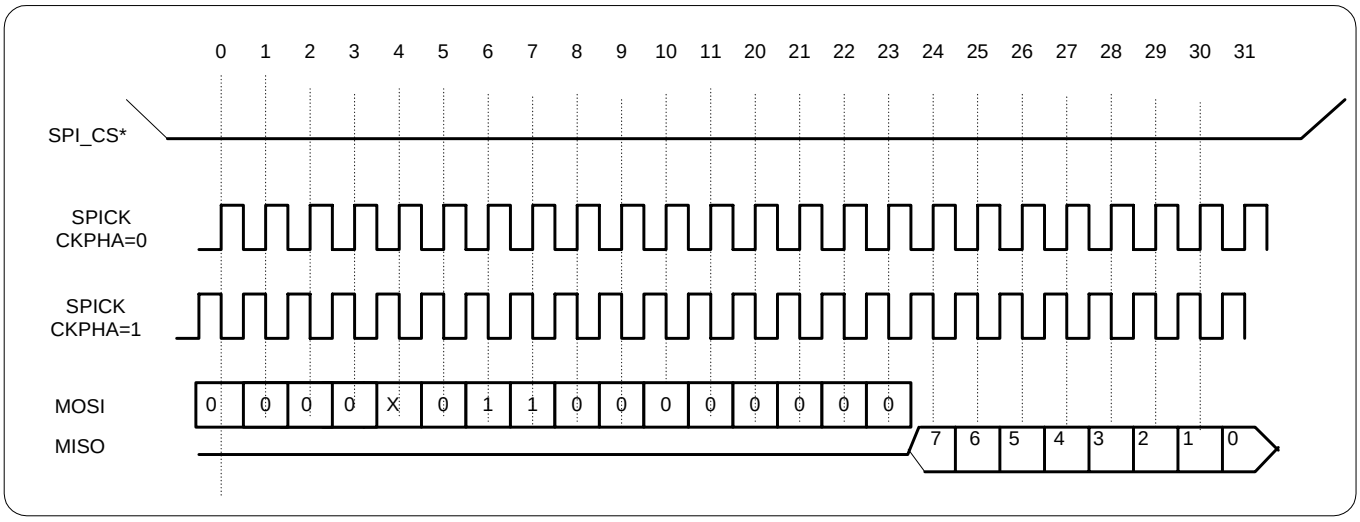


Table 10-1. EEPROM Program Memory Map

FUNCTIONAL BLOCK	ADDRESS RANGE FOR DATA IN EEPROM (IN HEX)
Global Registers	000h to 03Fh
Arbiter Registers	040h to 07Fh
BERT Registers	080h to 0BFh
Serial Interface 1 Tx Registers	0C0h to 0FFh
Serial Interface 1 Rx Registers	100h to 13Fh
Ethernet Interface 1 Registers	140h to 17Fh
Serial Interface 2 Tx Registers	180h to 1BFh
Serial Interface 2 Rx Registers	1C0h to 1FFh
Ethernet Interface 2 Registers	200h to 23Fh
Serial Interface 3 Tx Registers	240h to 27Fh
Serial Interface 3 Rx Registers	280h to 2BFh
Ethernet Interface 3 Registers	2C0h to 2FFh
Serial Interface 4 Tx Registers	300h to 33Fh
Serial Interface 4 Rx Registers	340h to 37Fh
Ethernet Interface 4 Registers	380h to 3BFh
MAC 1 Register 1 (MAC Control Register)	3C0h to 3C6h (special for indirect addresses)
MAC 1 Register 2 (MII Address Register)	3C7h to 3CDh (special for indirect addresses)
MAC 1 Register 3 (MII Data Register)	3CEh to 3D4h (special for indirect addresses)
MAC 1 Register 4 (Flow Control Register)	3D5h to 3DBh (special for indirect addresses)
MAC 2 Register 1 (MAC Control Register)	3DCh to 3E2h (special for indirect addresses)
MAC 2 Register 4 (Flow Control Register)	3E3h to 3E9h (special for indirect addresses)
MAC 3 Register 1 (MAC Control Register)	3EAh to 3F0h (special for indirect addresses)
MAC 3 Register 4 (Flow Control Register)	3F1h to 3F7h (special for indirect addresses)
MAC 4 Register 1 (MAC Control Register)	3F8h to 3FEh (special for indirect addresses)
MAC 4 Register 4 (Flow Control Register)	3FFh to 405h (special for indirect addresses)

Table 10-2 shows the MAC Addresses for MAC1 that can be programmed in the EEPROM mode. The MII Address and Data is not available for MAC2 to 4 since only one MDC/MDIO port is available for the DS33Z44.

Table 10-2. MAC Registers That Can Be Programmed from the EEPROM

EEPROM FILE BYTE FUNCTION	EEPROM MEMORY LOCATION*	EXAMPLE EEPROM ADDRESS LOCATION	EXAMPLE DATA USING MAC REGISTER WRITE 1 TO INITIALIZE MACCR
MAC Data Byte 1	Base + 00h	**3C0h**	**2Ch—**written to SU.MACWD0
MAC Data Byte 2	Base + 01h	**3C1h**	**00h**—written to SU.MACWD1
MAC Data Byte 3	Base + 02h	**3C2h**	**04h**—written to SU.MACWD2
MAC Data Byte 4	Base + 03h	**3C3h**	**90h—**written to SU.MACWD3
MAC Address Low	Base + 04h	**3C4h**	**00h—**written to SU.MACAWL
MAC Address High	Base + 05h	**3C5h**	**00h—** written to SU.MACAWH
MAC Write Command	Base + 06h	**3C6h**	**01h—**written to SU.MACRWC to initiate the indirect write

** Base EEPROM address of MAC instructions = 3C0h.*

11 OPERATING PARAMETERS

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Lead with Respect to V_{SS} (except V_{DD})……-0.5V to +5.5V
Supply Voltage Range ($V_{DD3.3}$) with Respect to V_{SS}……-0.3V to +3.6V
Supply Voltage Range ($V_{DD1.8}$) with Respect to V_{SS}……-0.3V to +2.0V
Ambient Operating Temperature Range……-40°C to +85°C
Junction Operating Temperature Range……-40°C to +125°C
Storage Temperature……-55°C to +125°C
Soldering Temperature……See IPC/JEDEC J-STD-020 Specification

These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect reliability. Ambient Operating Temperature Range is assuming the device is mounted on a JEDEC-standard test board in a convection-cooled JEDEC test enclosure.

Note: The "typ" values listed below are not production tested.

Table 11-1. Recommended DC Operating Conditions

($V_{DD3.3}$ = 3.3V ±5%, $V_{DD1.8}$ = 1.8V ±5%, T_j = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logic 1	V_{IH}		2.0		3.465	V
Logic 0	V_{IL}		-0.3		+0.8	V
Supply ($V_{DD3.3}$) ±5%	$V_{DD3.3}$		3.135	3.300	3.465	V
Supply ($V_{DD1.8}$) ±5%	$V_{DD1.8}$		1.71	1.8	1.89	V

Table 11-2. DC Electrical Characteristics

(T_j = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current ($V_{DD3.3}$ = 3.465V)	I_{DDIO}	(Notes 1, 2)		50	150	mA
Supply Current ($V_{DD1.8}$ = 1.89V)	I_{DDCORE}	(Notes 1, 2)		50	150	mA
I/O Standby Current in Reset ($V_{DD3.3}$ = 3.465V)	I_{DDD}	(Notes 2, 3)		20		mA
Core Standby Current in Reset ($V_{DD1.8}$ = 1.89V)	$I_{DDDCORE}$	(Notes 2, 3)		35		mA
I/O Static Current ($V_{DD3.3}$ = 3.465V)	I_{DDD}	(Notes 2, 4)		15	30	mA
Core Static Current ($V_{DD1.8}$ = 1.89)	$I_{DDDCORE}$	(Notes 2, 4)		0.2	2	mA
Lead Capacitance	C_{IO}			7		pF
Input Leakage	I_{IL}		-10		+10	µA
Input Leakage	I_{ILP}		-50		-10	µA
Output Leakage (when High Impedance)	I_{LO}		-10		+10	µA
Output Voltage (I_{OH} = -4.0mA)	V_{OH}	4mA outputs	2.4			V
Output Voltage (I_{OL} = +4.0mA)	V_{OL}	4mA outputs			0.4	V
Output Voltage (I_{OH} = -8.0mA)	V_{OH}	8mA outputs	2.4			V
Output Voltage (I_{OL} = +12.0mA)	V_{OL}	12mA outputs			0.4	V
Input Voltage	V_{IL}				0.8	V
	V_{IH}		2.0			V

Note 1: Typical power is 330mW.

Note 2: All outputs loaded with rated capacitance; all inputs between V_{DD} and V_{SS}; inputs with pullups connected to V_{DD}.

Note 3: RST pin held low, or RST bit set.

Note 4: RST pin held low, or RST bit set. All clocks stopped

Table 11-3. Typical Output Pin Drive Currents

NAME	TYPE	DRIVE CURRENT (mA)
TSER1-4	O	12
TDEN1-4/ TBSYNC1-4	IO	4
REF_CLKO	O	8
TX_CLK1-4	IO	4
TX_ENn	O	4
TXDn[3:0]	O	4
RX_CLK1-4	IO	4
MDC	O	4
MDIO	IO	4
D7 to D3, D2/SPICK, D1/MISO, D0/MOSI	IOZ	4
$\overline{\text{SPI\_CS}}$	O	4
$\overline{\text{INT}}$	Oz	4
SDATA [31:0]	IOz	4
SDA[11:0]	O	4
SBA[1:0]	O	4
$\overline{\text{SRAS}}$	O	4
$\overline{\text{SCAS}}$	O	4
$\overline{\text{SWE}}$	O	4
SDMask [3:0]	O	4
SDCLKO	O	4
$\overline{\text{SDCS}}$	O	4
QOVF1-4	O	4
JTDO	OZ	4

11.1 Thermal Characteristics

Table 11-4. Thermal Characteristics

PARAMETER	MIN	TYP	MAX
Ambient Temperature (Note 1)	-40°C	—	+85°C
Junction Temperature	—	—	+125°C
Theta-JA (θ_{JA}) in Still Air for 256-Pin CSBGA (Note 2)	—	+29.9°C/W	—

Note 1: The package is mounted on a four-layer JEDEC standard test board.

Note 2: Theta-JA (θ_{JA}) is the junction-to-ambient thermal resistance, when the package is mounted on a four-layer JEDEC standard test board.

11.2 MII Interface

Table 11-5. Transmit MII Interface

PARAMETER	SYMBOL	10Mbps			100Mbps			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TX_CLKn Period	t1		400			40		ns
TX_CLKn Low Time	t2	140		260	14		26	ns
TX_CLKn High Time	t3	140		260	14		26	ns
TX_CLKn to TXDn[3:0], TX_ENn Delay	t4	0		20	0		20	ns

Figure 11-1. Transmit MII Interface Timing

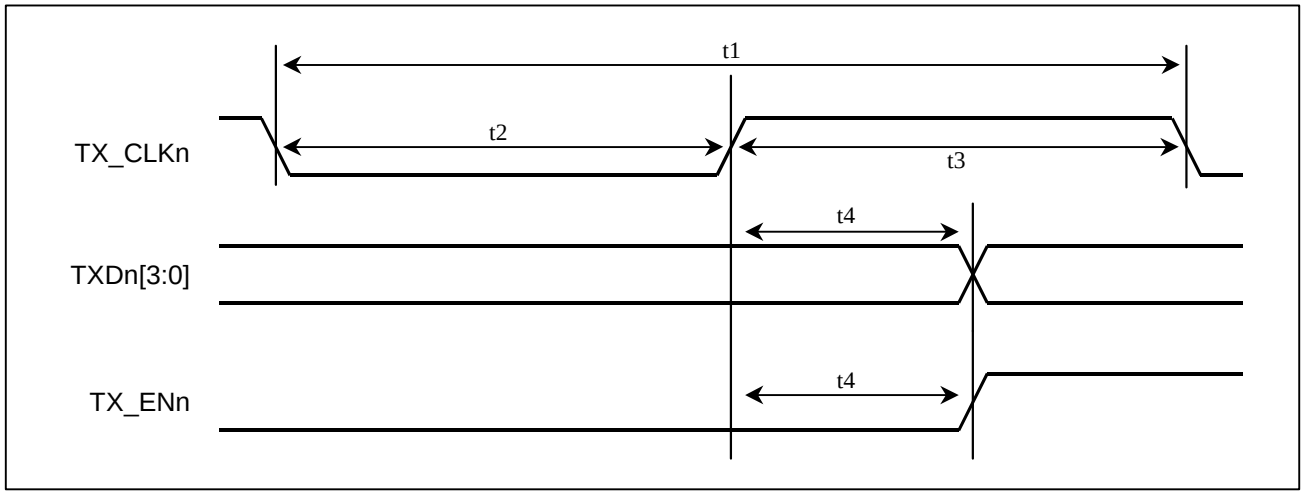
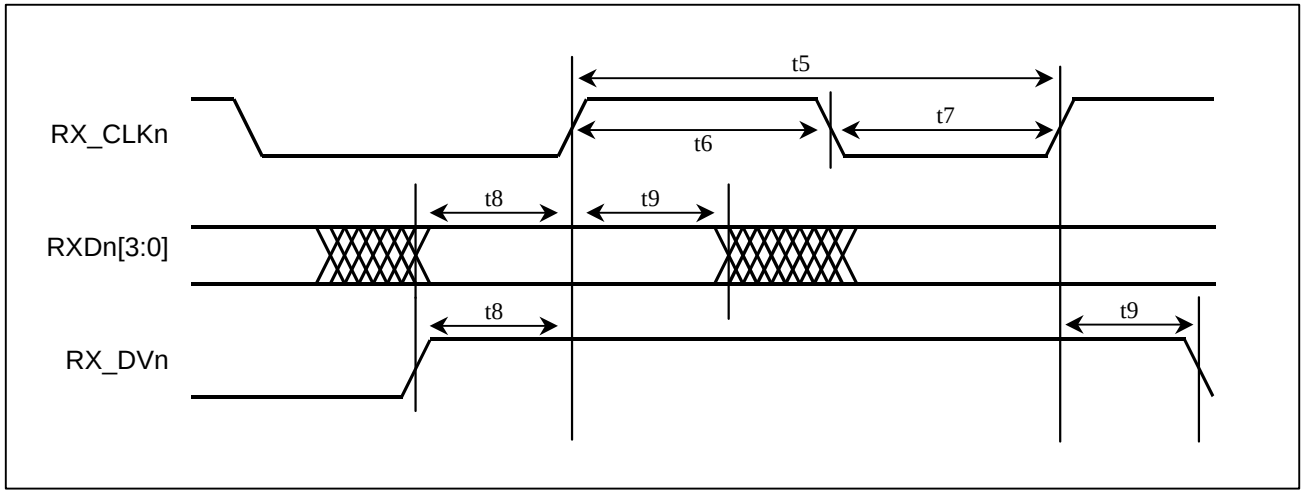


Table 11-6. Receive MII Interface

PARAMETER	SYMBOL	10Mbps			100Mbps			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RX_CLKn Period	t5		400			40		ns
RX_CLKn Low Time	t6	140		260	14		26	ns
RX_CLKn High Time	t7	140		260	14		26	ns
RXDn[3:0], RX_DVn to RX_CLKn Setup Time	t8	5			5			ns
RX_CLKn to RXDn[3:0], RX_DVn Hold Time	t9	5			5			ns

Figure 11-2. Receive MII Interface Timing



11.3 RMII Interface

Table 11-7. Transmit RMII Interface

PARAMETER	SYMBOL	10Mbps			100Mbps			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
REF_CLK Frequency			50MHz ±50ppm			50MHz ±50ppm		
REF_CLK Period	t1		20			20		ns
REF_CLK Low Time	t2	7		13	7		13	ns
REF_CLK High Time	t3	7		13	7		13	ns
TX_CLKn to TXDn[1:0], TX_ENn Delay	t4	5		10	5		10	ns

Figure 11-3. Transmit RMII Interface

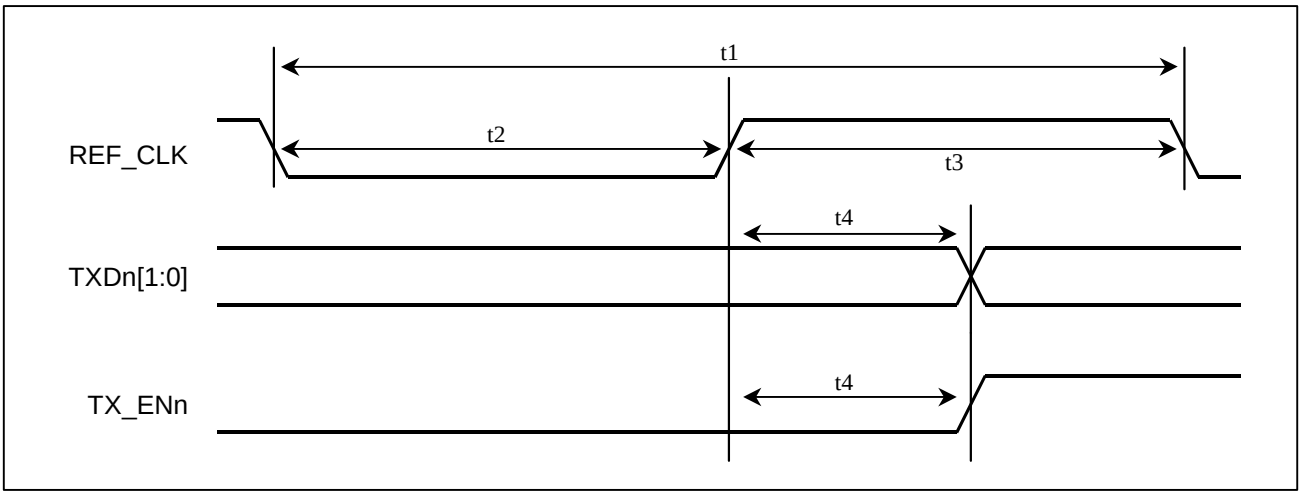
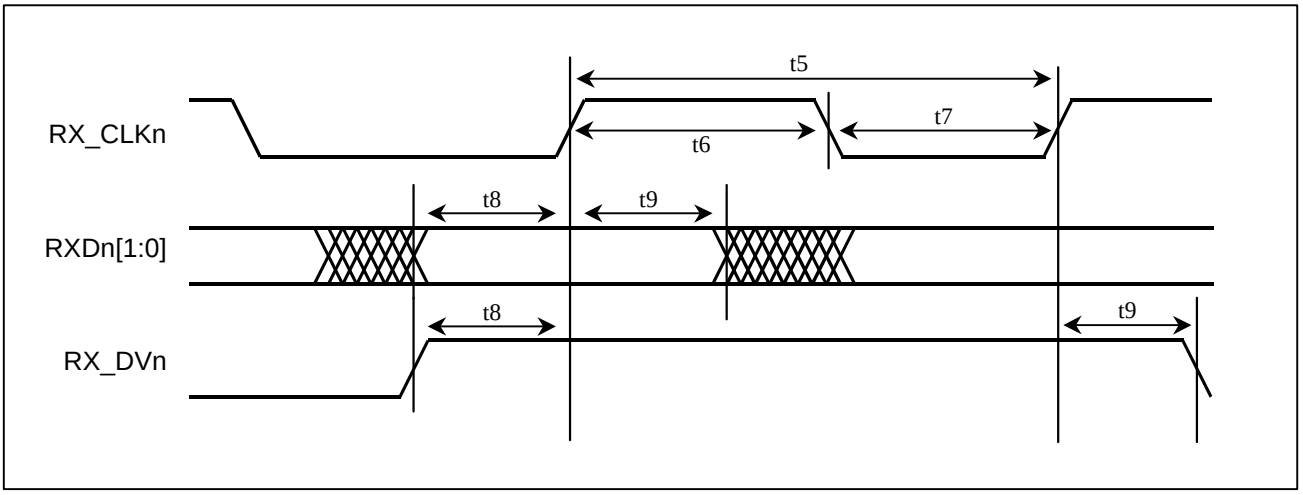


Table 11-8. Receive RMII Interface

PARAMETER	SYMBOL	10Mbps			100Mbps			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
REF_CLK Frequency			50MHz ±50ppm			50MHz ±50ppm		MHz
REF_CLK Period	t1		20			20		ns
REF_CLK Low Time	t2	7		13	7		13	ns
REF_CLK High Time	t3	7		13	7		13	ns
RXDn[3:0], RX_DVn to RX_CLKn Setup Time	t8	5			5			ns
RX_CLKn to RXDn[1:0], RX_DVn Hold Time	t9	5			5			ns

Figure 11-4. Receive RMII Interface Timing

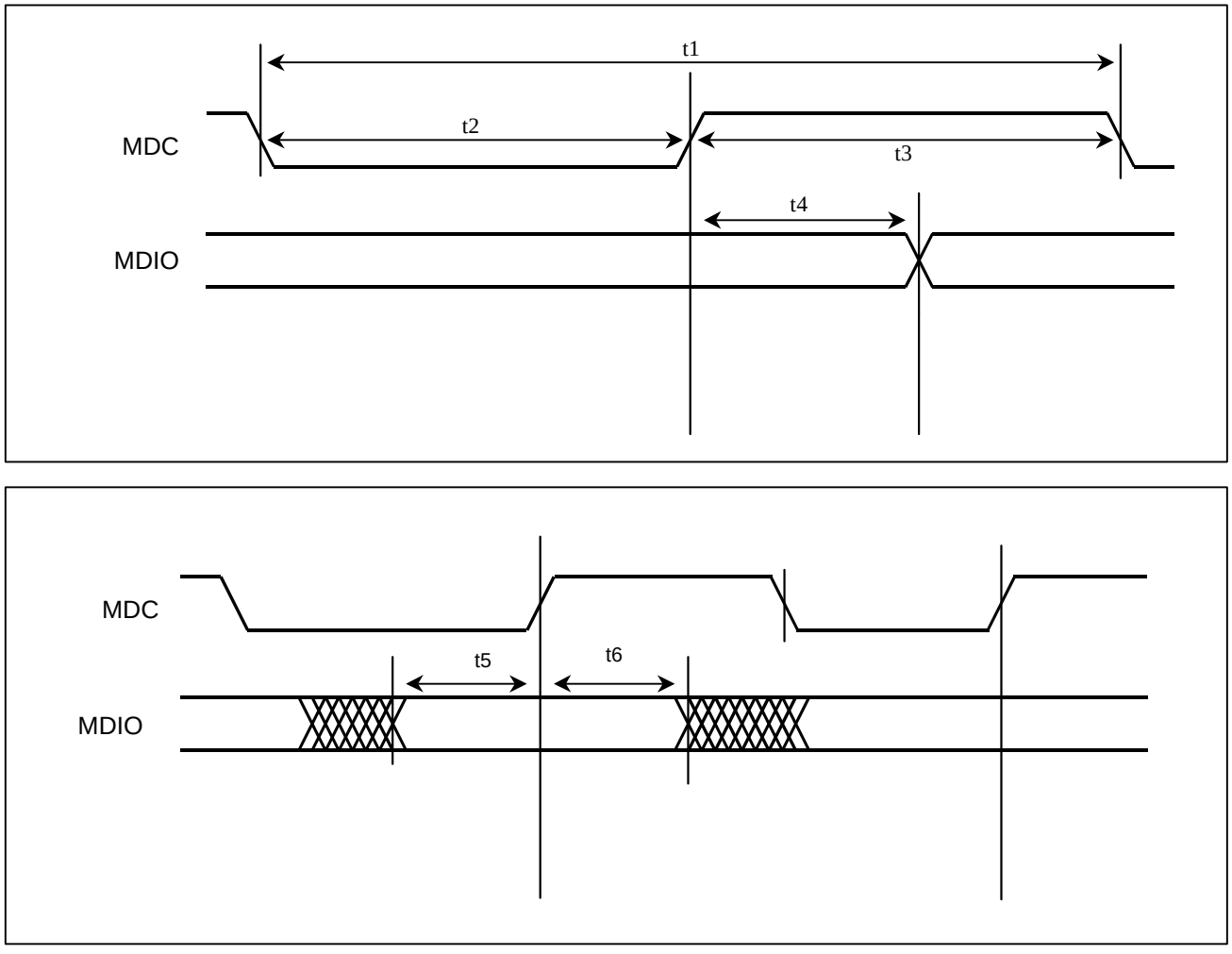


11.4 MDIO Interface

Table 11-9. MDIO Interface

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
MDC Frequency			1.67		MHz
MDC Period	t1	540	600	660	ns
MDC Low Time	t2	270	300	330	ns
MDC High Time	t3	270	300	330	ns
MDC to MDIO Output Delay	t4	20		10	ns
MDIO Setup Time	t5	10			ns
MDIO Hold Time	t6	20			ns

Figure 11-5. MDIO Interface Timing

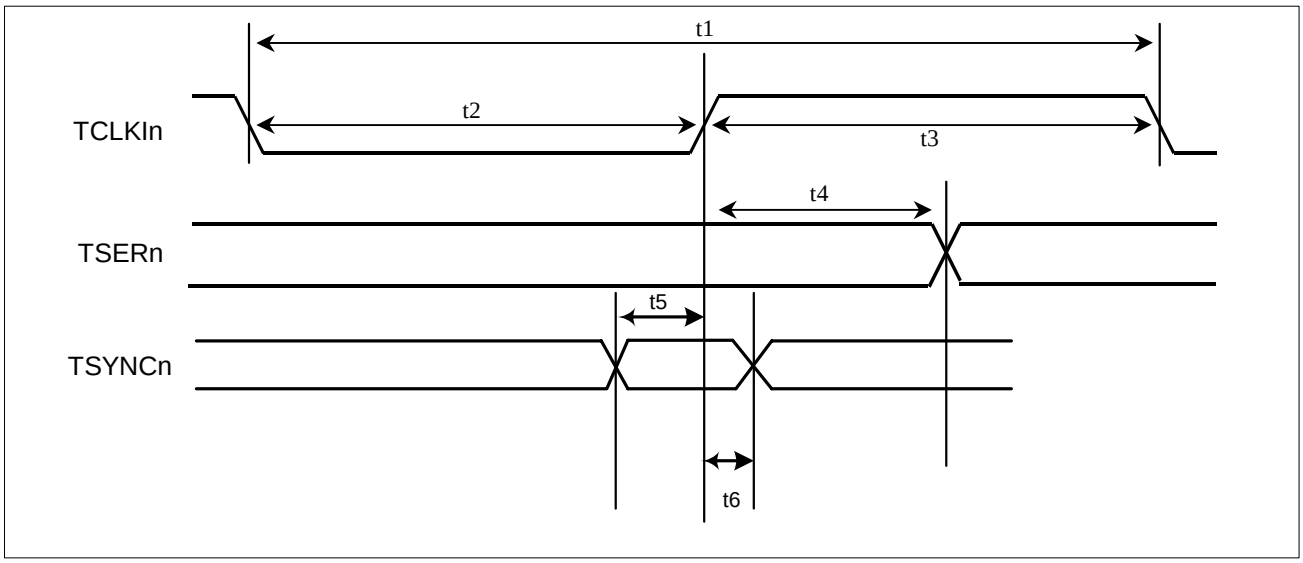


11.5 Transmit WAN Interface

Table 11-10. Transmit WAN Interface

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
TCLKIn Frequency				52	MHz
TCLKIn Period	t1	19.2		1000	ns
TCLKIn Low Time	t2	8		550	ns
TCLKIn High Time	t3	8		550	ns
TCLKIn to TSERn Output Delay	t4	3		10	ns
TBSYNCn Setup Time	t5	3.5			ns
TBSYNCn Hold Time	t6	7			ns

Figure 11-6. Transmit WAN Interface Timing

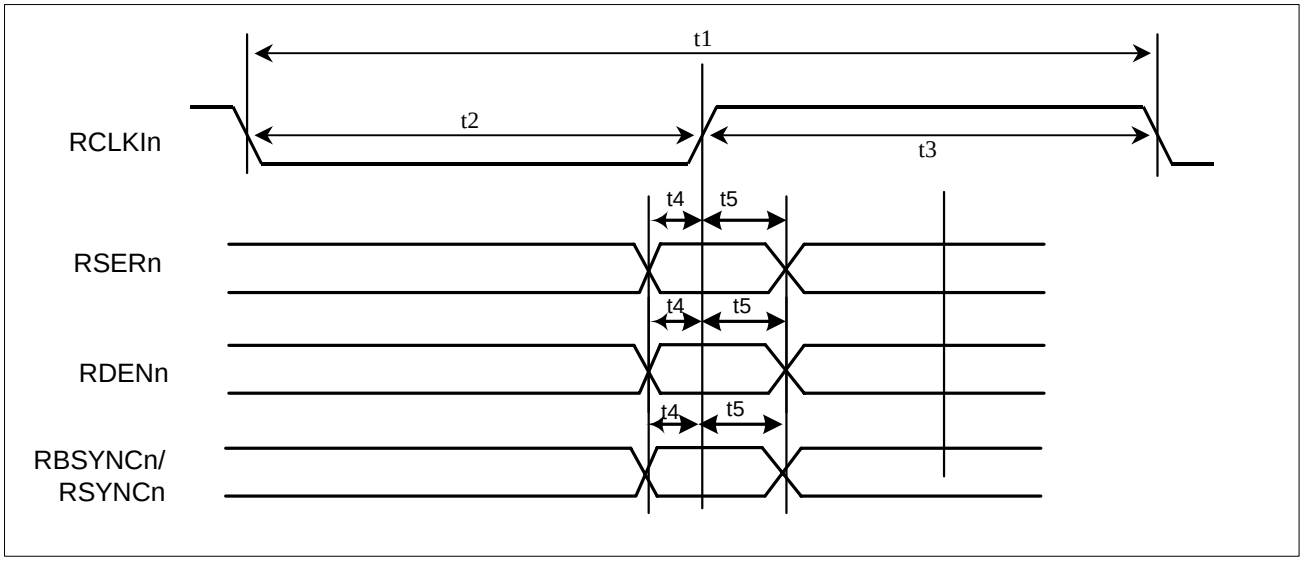


11.6 Receive WAN Interface

Table 11-11. Receive WAN Interface

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
RCLKIn Frequency				52	MHz
RCLKIn Period	t1	19.2		1000	ns
RCLKIn Low Time	t2	8		1000	ns
RCLKIn High Time	t3	8		1000	ns
RSERn Setup Time	t4	7			ns
RDENn Setup Time	t4	7			ns
RBSYNCn Setup Time	t4	7			
RDENn Setup Time	t4	7			ns
RSYNCn Setup Time	t4	7			ns
RSERn Hold Time	t5	2			ns
RSYNCn Hold Time	t5	2			ns
RDENn hold Time	t5	2			ns
RBSYNn Hold Time	t5	2			ns

Figure 11-7. Receive WAN Interface Timing

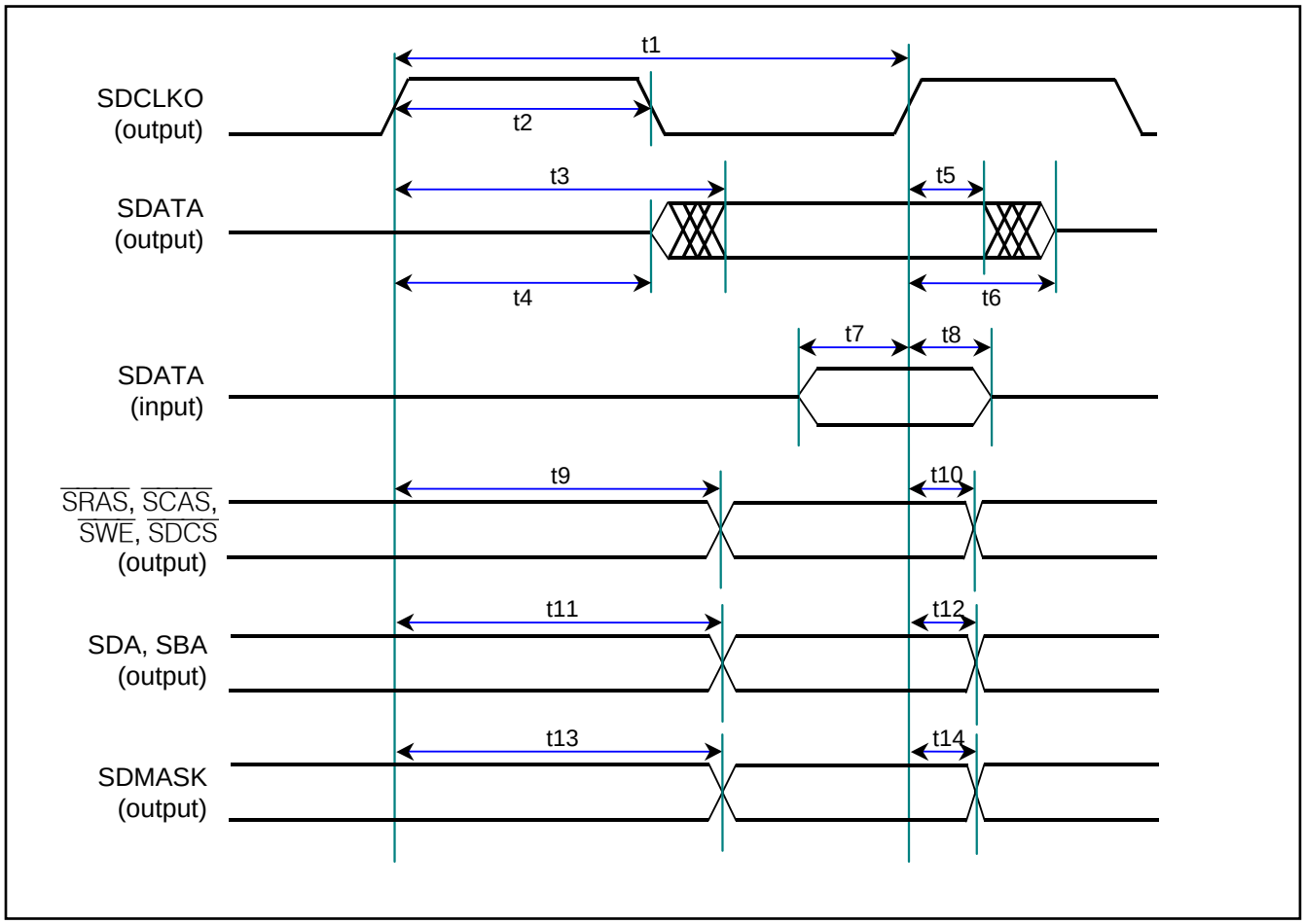


11.7 SDRAM Timing

Table 11-12. SDRAM Interface Timing

PARAMETER	SYMBOL	100MHz			UNITS
		MIN	TYP	MAX	
SDCLKO Period	t1	9.7	10	10.3	ns
SDCLKO Duty Cycle	t2	4		6	ns
SDCLKO to SDATA Valid Write to SDRAM	t3			7	ns
SDCLKO to SDATA Drive On Write to SDRAM	t4	4			ns
SDCLKO to SDATA Invalid Write to SDRAM	t5	3			ns
SDCLKO to SDATA Drive Off Write to SDRAM	t6			4	ns
SDATA to SDCLKO Setup Time Read from SDRAM	t7	2			ns
SDCLKO to SDATA Hold Time Read from SDRAM	t8			2	ns
SDCLKO to $\overline{\text{SRAS}}$, $\overline{\text{SCAS}}$, $\overline{\text{SWE}}$, $\overline{\text{SDCS}}$ Active Read or Write to SDRAM	t9			5	ns
SDCLKO TO $\overline{\text{SRAS}}$, $\overline{\text{SCAS}}$, $\overline{\text{SWE}}$, $\overline{\text{SDCS}}$ Inactive Read or Write to SDRAM	t10	2			ns
SDCLKO to SDA, SBA Valid Read or Write to SDRAM	t11			7	ns
SDCLKO TO SDA, SBA Invalid Read or Write to SADRAM	t12	2			ns
SDCLKO to SDMASK Valid Read or Write to SDRAM	t13			5	ns
SDCLKO to SDMASK Invalid Read or Write to SDRAM	t14	2			ns

Figure 11-8. SDRAM Interface Timing



11.8 Microprocessor Bus AC Characteristics

Table 11-13. AC Characteristics—Microprocessor Bus Timing

(V_{DD} = 3.3V ±5%, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Setup Time for A[12:0] Valid to $\overline{CS}$ Active	t1	0			ns
Setup Time for $\overline{CS}$ Active to either $\overline{RD}$, or $\overline{WR}$ Active	t2	0			ns
Delay Time from Either $\overline{RD}$ or $\overline{DS}$ Active to DATA[7:0] Valid	t3			75	ns
Hold Time from Either $\overline{RD}$ or $\overline{WR}$ Inactive to $\overline{CS}$ Inactive	t4	0			ns
Hold Time from $\overline{CS}$ or $\overline{RD}$ or $\overline{DS}$ Inactive to DATA[7:0] Tri-State	t5	5		20	ns
Wait Time from R$\overline{W}$ Active to Latch Data	t6	80			ns
Data Setup Time to $\overline{DS}$ Inactive	t7	10			ns
Data Hold Time from R$\overline{W}$ Inactive	t8	2			ns
Address Hold from R$\overline{W}$ inactive	t9	0			ns
Write Access to Subsequent Write/Read Access Delay Time	t10	80			ns

Figure 11-9. Intel Bus Read Timing (HWMODE = 0, MODEC = 00)

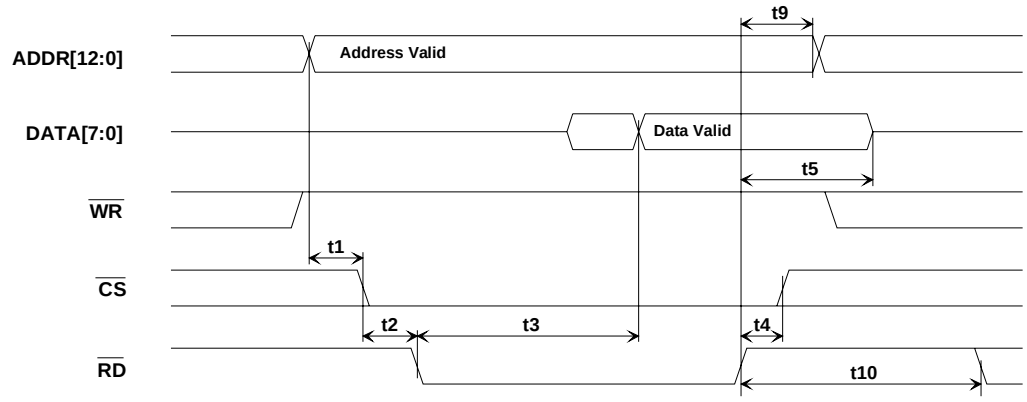


Figure 11-10. Intel Bus Write Timing (HWMODE = 0, MODEC = 00)

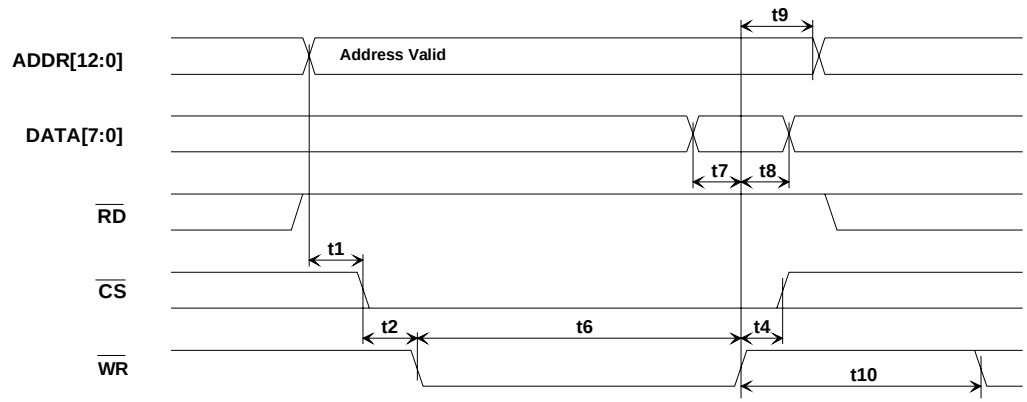


Figure 11-11. Motorola Bus Read Timing (HWMODE = 0, MODEC = 01)

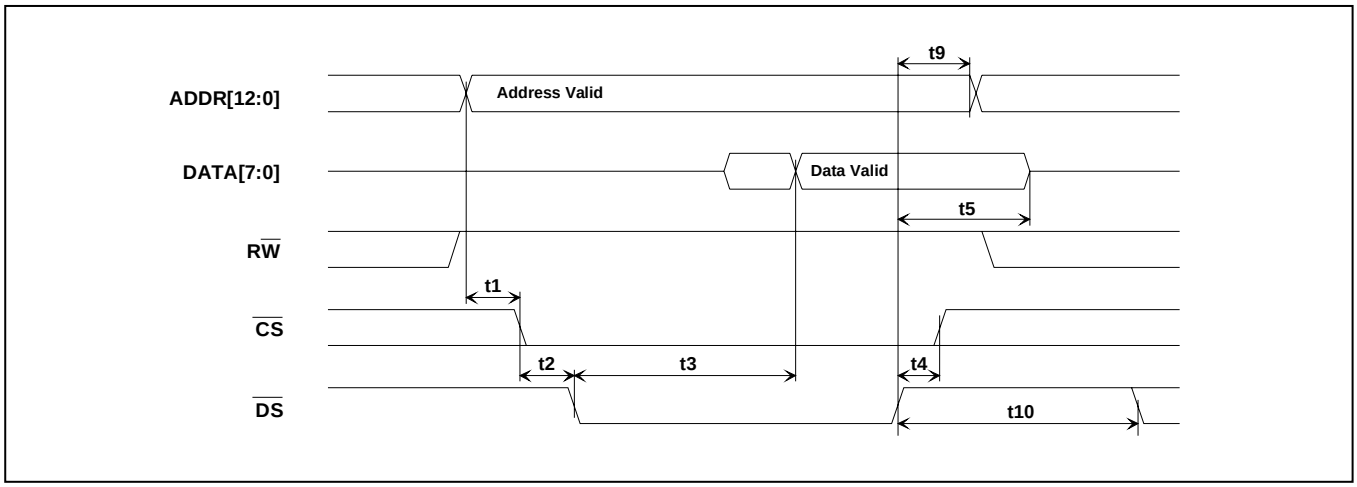
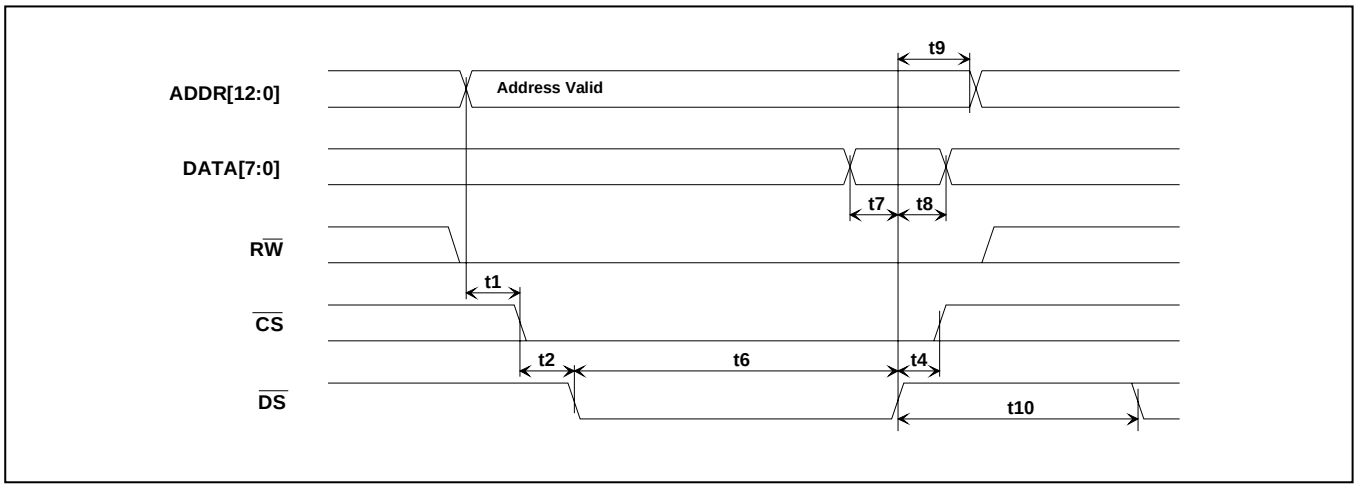


Figure 11-12. Motorola Bus Write Timing (HWMODE = 0, MODEC = 01)

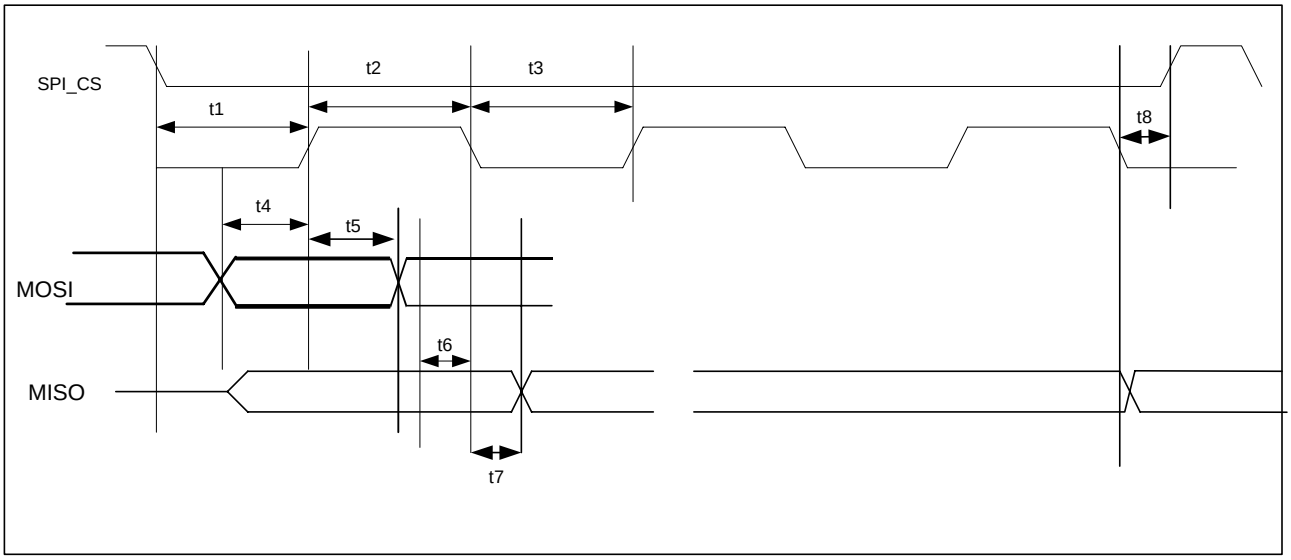


11.9 EEPROM Interface Timing

Table 11-14. EEPROM Interface Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SPI_CK Period	t1		120		ns
SPI_CK Low Time	t2	55		65	ns
SPI_CK High Time	t3	55		65	ns
MOSI Setup Delay	t4	50			ns
MISO Hold	t5	50			ns
MISO Setup	T6	10			ns
MISO Hold	T7	10			ns
$\overline{\text{SPI\_CS}}$ Hold	T8	60			ns

Figure 11-13. EEPROM Interface Timing



11.10 JTAG Interface Timing

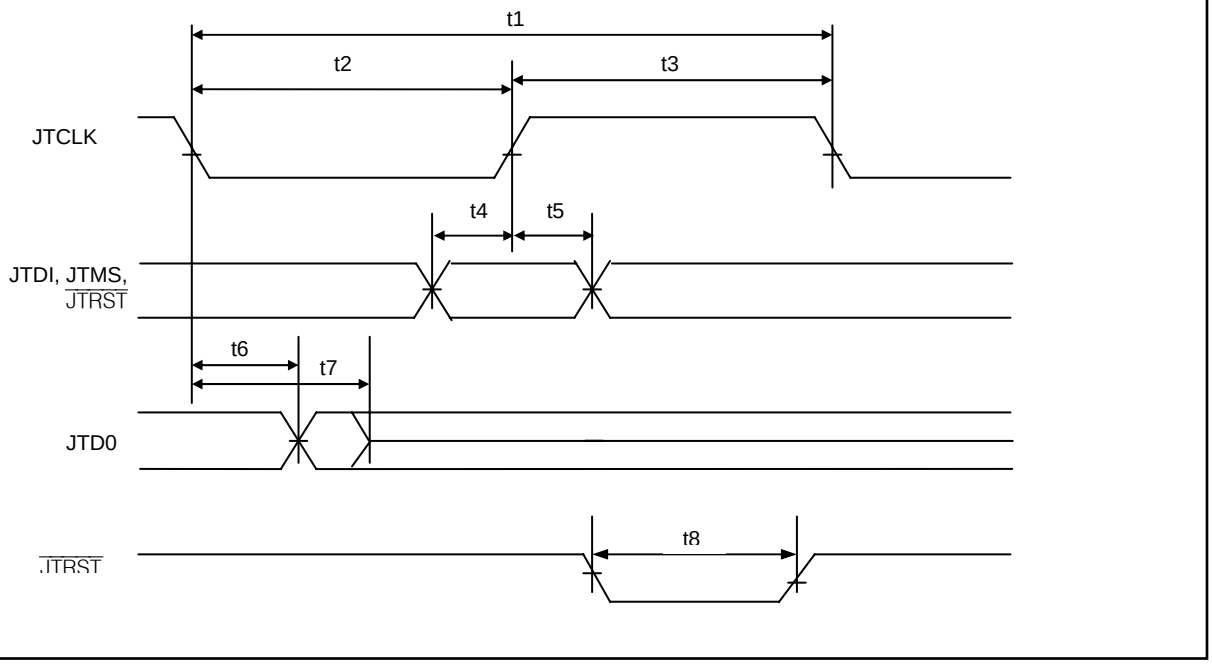
Table 11-15. JTAG Interface Timing

(V_{DD} = 3.3V ±5%, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
JTCLK Clock Period	t1			1000		ns
JTCLK Clock High:Low Time	t2:t3	(Note 1)	50	500		ns
JTCLK to JTDI, JTMS Setup Time	t4		2			ns
JTCLK to JTDI, JTMS Hold Time	t5		2			ns
JTCLK to JTDO Delay	t6		2		50	ns
JTCLK to JTDO HIZ Delay	t7		2		50	ns
$\overline{\text{JTRST}}$ Width Low Time	t8		100			ns

Note 1: Clock can be stopped high or low.

Figure 11-14. JTAG Interface Timing Diagram



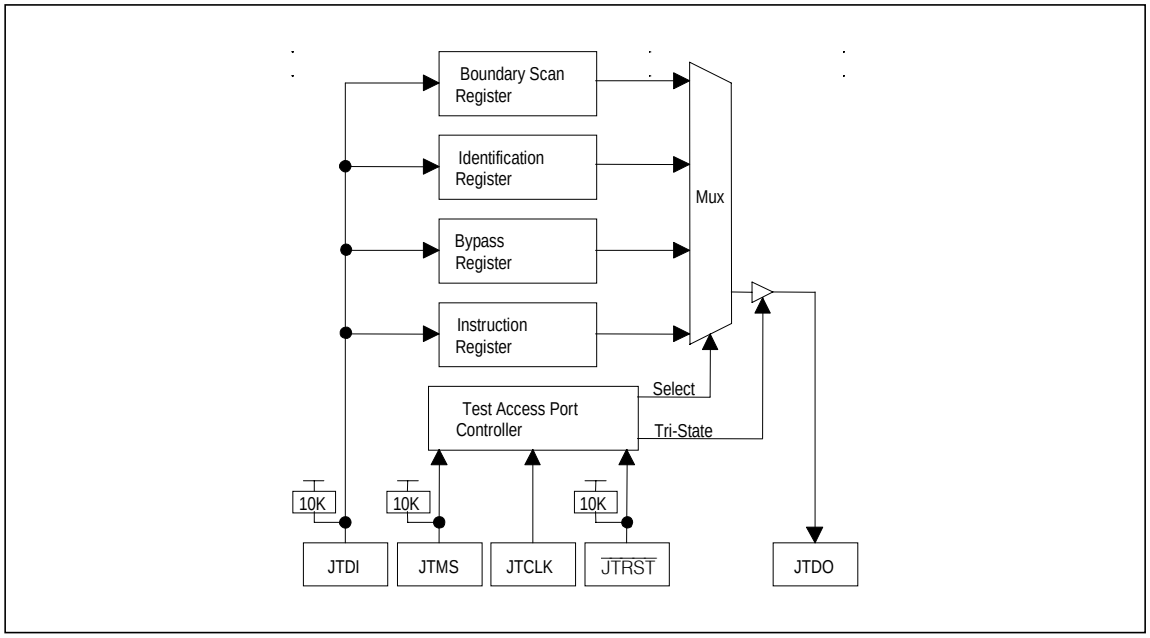
12 JTAG INFORMATION

The DS33Z44 supports the standard instruction codes SAMPLE:PRELOAD, BYPASS, and EXTEST. Optional public instructions included are HIGHZ, CLAMP, and IDCODE. See Table 12-1. The DS33Z44 contains the following as required by IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture.

- Test Access Port (TAP)
- TAP Controller
- Instruction Register
- Bypass Register
- Boundary Scan Register
- Device Identification Register

The Test Access Port has the necessary interface pins: $\overline{\text{JTRST}}$, JTCLK, JTMS, JTDI, and JTDO. See the pin descriptions for details. Refer to IEEE 1149.1-1990, IEEE 1149.1a-1993, and IEEE 1149.1b-1994 for details about the Boundary Scan Architecture and the Test Access Port.

Figure 12-1. JTAG Functional Block Diagram



12.1 JTAG/TAP Controller State Machine Description

This section covers the details on the operation of the Test Access Port (TAP) Controller State Machine. The TAP controller is a finite state machine that responds to the logic level at JTMS on the rising edge of JTCLK.

12.2 TAP Controller State Machine

The TAP controller is a finite state machine that responds to the logic level at JTMS on the rising edge of JTCLK. See Figure 12-2 for a diagram of the state machine operation.

12.2.1 Test-Logic-Reset

Upon power up, the TAP Controller is in the Test-Logic-Reset state. The Instruction register will contain the IDCODE instruction. All system logic of the device will operate normally.

12.2.2 Run-Test-Idle

The Run-Test-Idle is used between scan operations or during specific tests. The Instruction register and test registers will remain idle.

12.2.3 Select-DR-Scan

All test registers retain their previous state. With JTMS LOW, a rising edge of JTCLK moves the controller into the Capture-DR state and will initiate a scan sequence. JTMS HIGH during a rising edge on JTCLK moves the controller to the Select-IR-Scan state.

12.2.4 Capture-DR

Data may be parallel-loaded into the test data registers selected by the current instruction. If the instruction does not call for a parallel load or the selected register does not allow parallel loads, the test register will remain at its current value. On the rising edge of JTCLK, the controller will go to the Shift-DR state if JTMS is LOW or it will go to the Exit1-DR state if JTMS is HIGH.

12.2.5 Shift-DR

The test data register selected by the current instruction is connected between JTDI and JTDO and will shift data one stage towards its serial output on each rising edge of JTCLK. If a test register selected by the current instruction is not placed in the serial path, it will maintain its previous state.

12.2.6 Exit1-DR

While in this state, a rising edge on JTCLK will put the controller in the Update-DR state, which terminates the scanning process, if JTMS is HIGH. A rising edge on JTCLK with JTMS LOW will put the controller in the Pause-DR state.

12.2.7 Pause-DR

Shifting of the test registers is halted while in this state. All test registers selected by the current instruction will retain their previous state. The controller will remain in this state while JTMS is LOW. A rising edge on JTCLK with JTMS HIGH will put the controller in the Exit2-DR state.

12.2.8 Exit2-DR

A rising edge on JTCLK with JTMS HIGH while in this state will put the controller in the Update-DR state and terminate the scanning process. A rising edge on JTCLK with JTMS LOW will enter the Shift-DR state.

12.2.9 Update-DR

A falling edge on JTCLK while in the Update-DR state will latch the data from the shift register path of the test registers into the data output latches. This prevents changes at the parallel output due to changes in the shift register.

12.2.10 Select-IR-Scan

All test registers retain their previous state. The instruction register will remain unchanged during this state. With JTMS LOW, a rising edge on JTCLK moves the controller into the Capture-IR state and will initiate a scan sequence for the instruction register. JTMS HIGH during a rising edge on JTCLK puts the controller back into the Test-Logic-Reset state.

12.2.11 Capture-IR

The Capture-IR state is used to load the shift register in the instruction register with a fixed value. This value is loaded on the rising edge of JTCLK. If JTMS is HIGH on the rising edge of JTCLK, the controller will enter the Exit1-IR state. If JTMS is LOW on the rising edge of JTCLK, the controller will enter the Shift-IR state.

12.2.12 Shift-IR

In this state, the shift register in the instruction register is connected between JTDI and JTDO and shifts data one stage for every rising edge of JTCLK towards the serial output. The parallel register, as well as all test registers, remains at their previous states. A rising edge on JTCLK with JTMS HIGH will move the controller to the Exit1-IR state. A rising edge on JTCLK with JTMS LOW will keep the controller in the Shift-IR state while moving data one stage thorough the instruction shift register.

12.2.13 Exit1-IR

A rising edge on JTCLK with JTMS LOW will put the controller in the Pause-IR state. If JTMS is HIGH on the rising edge of JTCLK, the controller will enter the Update-IR state and terminate the scanning process.

12.2.14 Pause-IR

Shifting of the instruction shift register is halted temporarily. With JTMS HIGH, a rising edge on JTCLK will put the controller in the Exit2-IR state. The controller will remain in the Pause-IR state if JTMS is LOW during a rising edge on JTCLK.

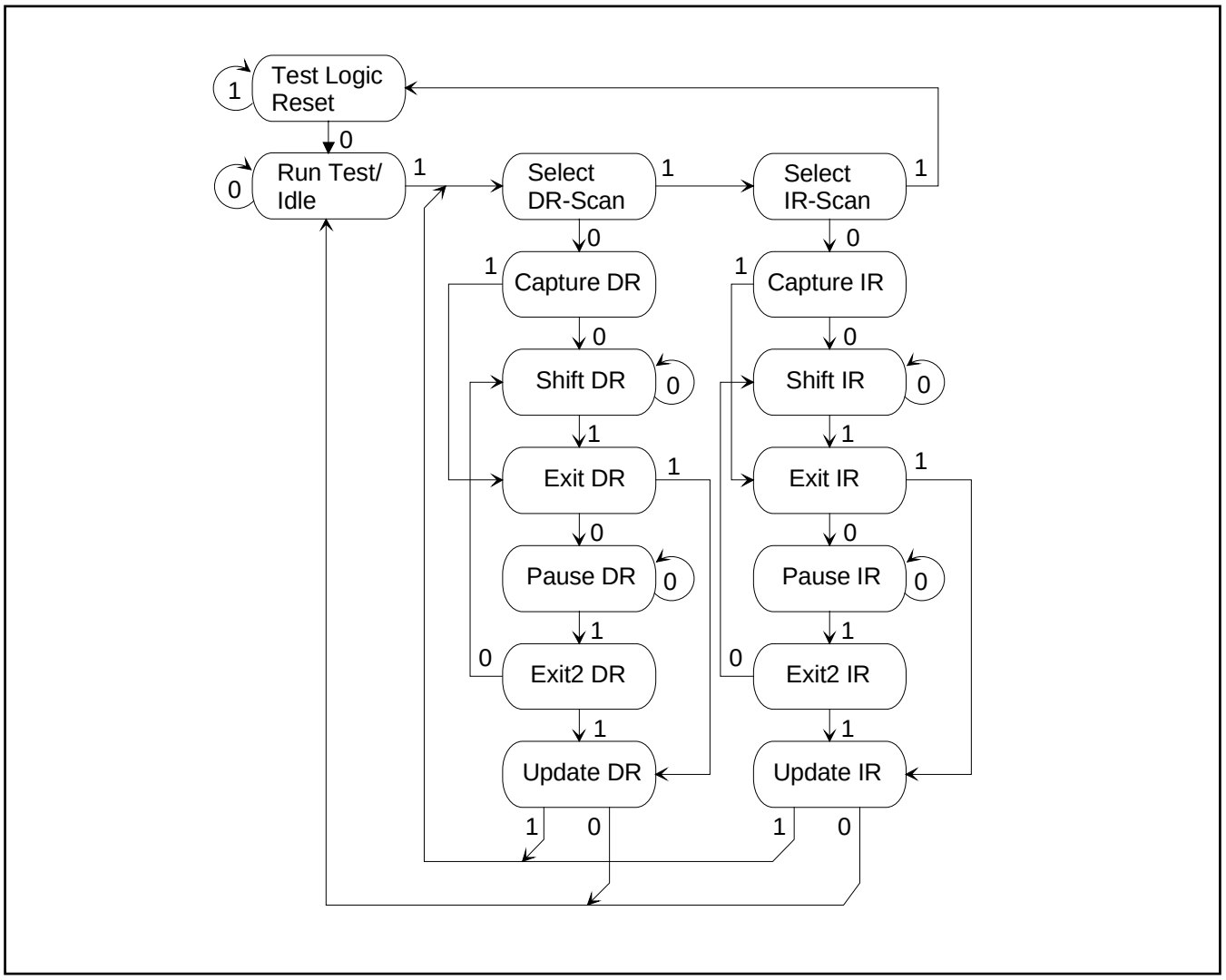
12.2.15 Exit2-IR

A rising edge on JTCLK with JTMS LOW will put the controller in the Update-IR state. The controller will loop back to Shift-IR if JTMS is HIGH during a rising edge of JTCLK in this state.

12.2.16 Update-IR

The instruction code shifted into the instruction shift register is latched into the parallel output on the falling edge of JTCLK as the controller enters this state. Once latched, this instruction becomes the current instruction. A rising edge on JTCLK with JTMS held low will put the controller in the Run-Test-Idle state. With JTMS HIGH, the controller will enter the Select-DR-Scan state.

Figure 12-2. TAP Controller State Diagram



12.3 Instruction Register

The instruction register contains a shift register as well as a latched parallel output and is 3 bits in length. When the TAP controller enters the Shift-IR state, the instruction shift register is connected between JTDI and JTDO. While in the Shift-IR state, a rising edge on JTCLK with JTMS LOW will shift the data one stage towards the serial output at JTDO. A rising edge on JTCLK in the Exit1-IR state or the Exit2-IR state with JTMS HIGH will move the controller to the Update-IR state. The falling edge of that same JTCLK will latch the data in the instruction shift register to the instruction parallel output. Instructions supported by the DS33Z44 and its respective operational binary codes are shown in Table 12-1.

Table 12-1. Instruction Codes for IEEE 1149.1 Architecture

INSTRUCTION	SELECTED REGISTER	INSTRUCTION CODES
SAMPLE:PRELOAD	Boundary Scan	010
BYPASS	Bypass	111
EXTEST	Boundary Scan	000
CLAMP	Bypass	011
HIGHZ	Bypass	100
IDCODE	Device Identification	001

12.3.1 SAMPLE:PRELOAD

This is a mandatory instruction for the IEEE 1149.1 specification. This instruction supports two functions. The digital I/Os of the device can be sampled at the boundary scan register without interfering with the normal operation of the device by using the Capture-DR state. SAMPLE:PRELOAD also allows the device to shift data into the boundary scan register via JTDI using the Shift-DR state.

12.3.2 BYPASS

When the BYPASS instruction is latched into the parallel instruction register, JTDI connects to JTDO through the one-bit bypass test register. This allows data to pass from JTDI to JTDO not affecting the device's normal operation.

12.3.3 EXTEST

This allows testing of all interconnections to the device. When the EXTEST instruction is latched in the instruction register, the following actions occur. Once enabled via the Update-IR state, the parallel outputs of all digital output pins are driven. The boundary scan register is connected between JTDI and JTDO. The Capture-DR will sample all digital inputs into the boundary scan register.

12.3.4 CLAMP

All digital outputs of the device will output data from the boundary scan parallel output while connecting the bypass register between JTDI and JTDO. The outputs will not change during the CLAMP instruction.

12.3.5 HIGHZ

All digital outputs of the device are placed in a high-impedance state. The BYPASS register is connected between JTDI and JTDO.

12.3.6 IDCODE

When the IDCODE instruction is latched into the parallel instruction register, the identification test register is selected. The device identification code is loaded into the identification register on the rising edge of JTCLK following entry into the Capture-DR state. Shift-DR can be used to shift the identification code out serially via JTDO. During Test-Logic-Reset, the identification code is forced into the instruction register's parallel output. The ID code will always have a one in the LSB position. The next 11 bits identify the manufacturer's JEDEC number and number of continuation bytes followed by 16 bits for the device and 4 bits for the version.

12.4 JTAG ID Codes

Table 12-2. ID Code Structure

DEVICE	REVISION ID[31:28]	DEVICE CODE ID[27:12]	MANUFACTURER'S CODE ID[11:1]	REQUIRED ID[0]
DS33Z44	0000	0000 0000 0110 0011	000 1010 0001	1

12.5 Test Registers

IEEE 1149.1 requires a minimum of two test registers: the bypass register and the boundary scan register. An optional test register has been included with the DS33Z44 design. This test register is the identification register and is used in conjunction with the IDCODE instruction and the Test-Logic-Reset state of the TAP controller.

12.5.1 Boundary Scan Register

This register contains both a shift register path and a latched parallel output for all control cells and digital I/O cells and is n bits in length.

12.5.2 Bypass Register

This is a single one-bit shift register used in conjunction with the BYPASS, CLAMP, and HIGHZ instructions, which provides a short path between JTDI and JTDO.

12.5.3 Identification Register

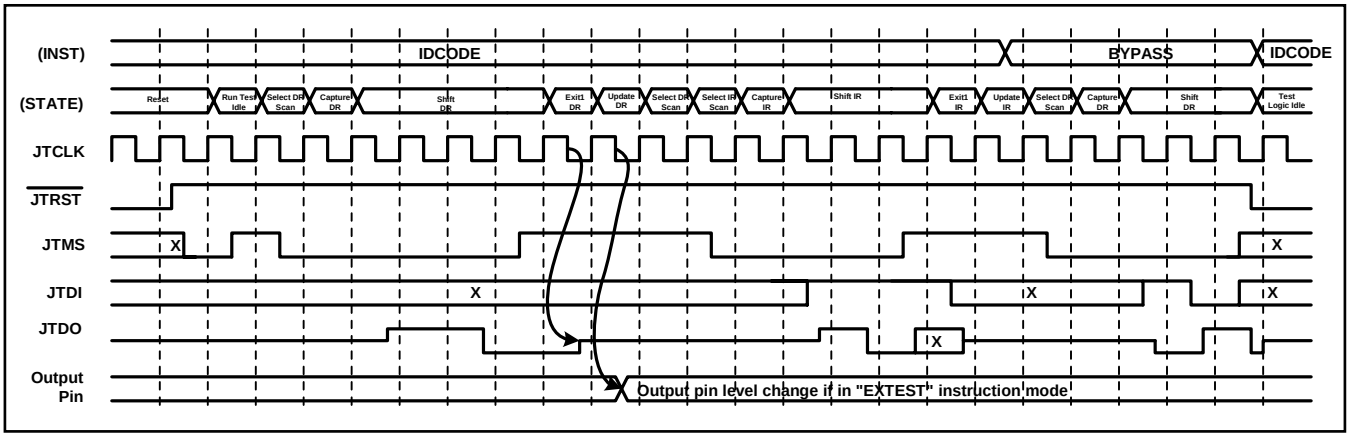
The identification register contains a 32-bit shift register and a 32-bit latched parallel output. This register is selected during the IDCODE instruction and when the TAP controller is in the Test-Logic-Reset state.

12.6 JTAG Functional Timing

This functional timing for the JTAG circuits shows:

- The JTAG controller starting from reset state.
- Shifting out the first 4 LSB bits of the IDCODE.
- Shifting in the BYPASS instruction (111) while shifting out the mandatory X01 pattern.
- Shifting the TDI pin to the TDO pin through the bypass shift register.
- An asynchronous reset occurs while shifting.

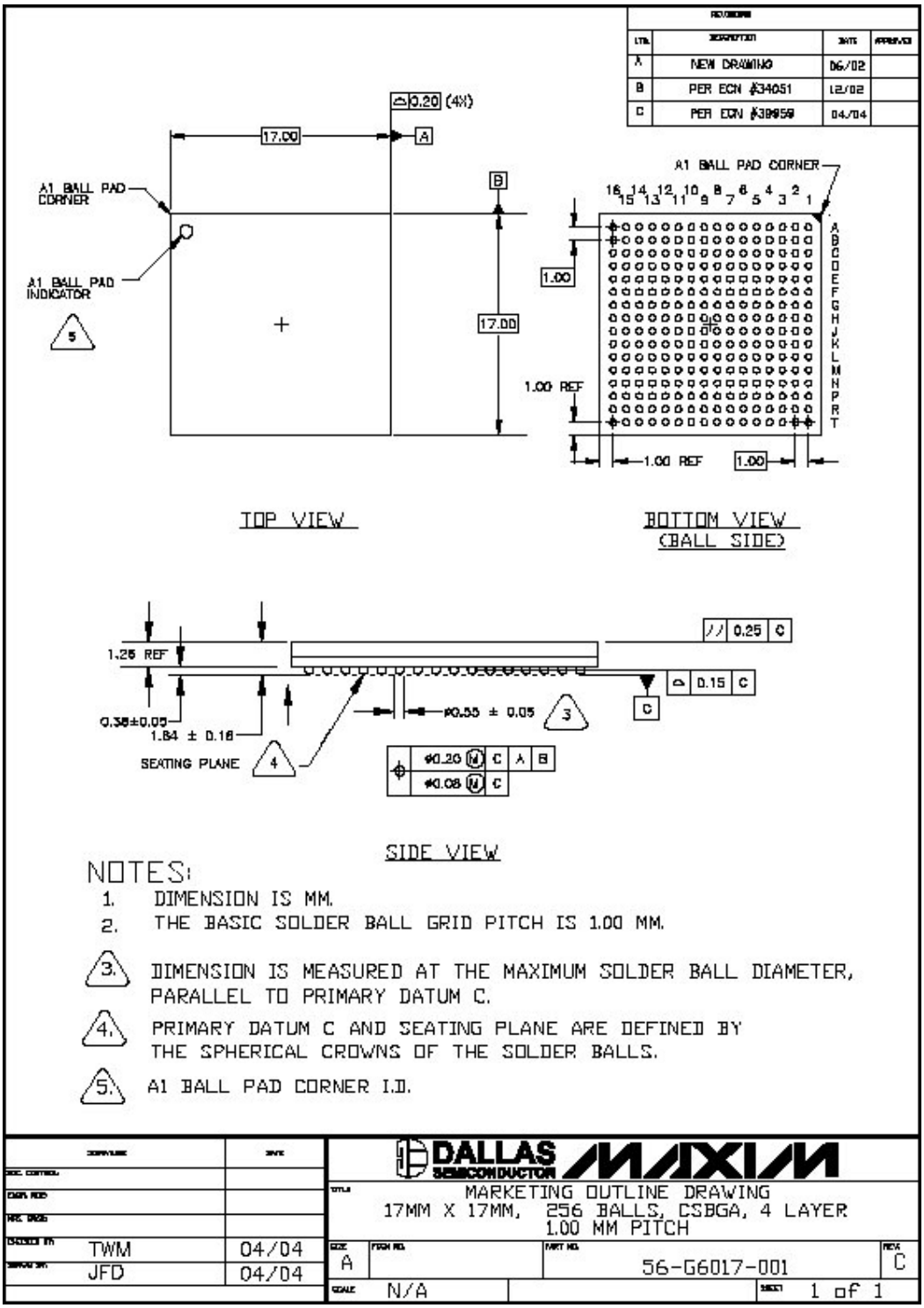
Figure 12-3. JTAG Functional Timing



13 PACKAGE INFORMATION

(The package drawing(s) in this data sheet may not reflect the most current specifications. The package number provided for each package is a link to the latest package outline information.)

13.1 256-CSBGA (17mm x 17mm) (56-G6017-001)



14 REVISION HISTORY

REVISION	DESCRIPTION
120304	New Product Release
122006	Added TCLKI to TSER Output Delay Minimum of 3ns. Corrected instances of “TSYNC” to “TBSYNC”. Added TCLKI to TBSYNC Setup Time Minimum of 3.5ns. Added definition for BPCLR.PLF[4:0]. Corrected pin description of MDC. Corrected default value listed in the SU.RMFSRL register definition. Added GL.SDMODE1, GL.SDMODE2, GL.SDMODEWS, and GL.SDRFTC register definitions. Added GL.SDMODE1, GL.SDMODE2, GL.SDMODEWS, and GL.SDRFTC registers to the register bit map. Clarified the GL.C1QPR – GL.C4QPR register definitions. Corrected SU.MACCR.PM and SU.MACCR.PAM bit definitions. Corrected pin description of RST. Corrected pin description of REF_CLK. Clarified text regarding use of REF_CLKO in DCE and RMII modes. Corrected pin assignment in the pin descriptions for RXD1[3] to E11. Corrected SU.GCR.H10S bit definition. Corrected the SU.RQLT and SU.RQHT default values to zero. Corrected SU.MACCR register definition. Corrected Addresses on the last 3 rows of *Table 10-1. EEPROM Program Memory Map*. Clarified section 8.19 on X.86 mode synchronization. Corrected value of “Receiver Maximum Frame Size” listed in table 8-11. Corrected low-power mode information in section 8.4. Added D/C operating current maximum values. Updated D/C operating current typical values. Added D/C Characteristic entries for Supply currents in “standby” conditions. Removed references to the SU.RSTPD register. Register reserved for future use. Changed bits 15 and 13 to Reserved for the SU.MACCR register. Updated package drawing.