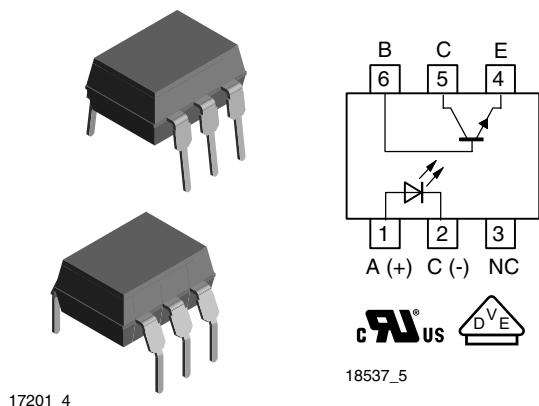


Optocoupler, Phototransistor Output, with Base Connection



DESCRIPTION

The CNY75A, CNY75B, CNY75C, CNY75GA, CNY75GB, CNY75GC consists of a phototransistor optically coupled to a gallium arsenide infrared-emitting diode in a 6 pin plastic dual inline package.

AGENCY APPROVALS

- UL1577, file no. E52744, double protection
- BSI: BS EN 41003, BS EN 60095 (BS 415), BS EN 60950 (BS 7002), pending
- DIN EN 60747-5-5 (VDE 0884)
- FIMKO (SETI): EN 60950, certificate no. FI25155

FEATURES

- Isolation materials according to UL 94-VO
- Pollution degree 2 (DIN/VDE 0110/resp. IEC 60664)
- Climatic classification 55/110/21 (IEC 60068 part 1)
- Low temperature coefficient of CTR
- CTR offered in 3 groups
- Rated isolation voltage (RMS includes DC) $V_{IOWM} = 600 V_{RMS}$ (848 V peak)
- Rated recurring peak voltage (repetitive) $V_{IORM} = 600 V_{RMS}$
- Rated impulse voltage (transient overvoltage) $V_{IOTM} = 6 kV_{peak}$
- Isolation test voltage (partial discharge test voltage) $V_{pd} = 1.6 kV$
- Creepage current resistance according to VDE 0303/IEC 60112 comparative tracking index: CTI ≥ 325
- Thickness through insulation ≥ 0.4 mm
- Compliant to RoHS directive 2002/95/EC and in accordance to WEEE 2002/96/EC


RoHS
COMPLIANT

APPLICATIONS

- Switch-mode power supplies
- Line receiver
- Computer peripheral interface
- Microprocessor system interface
- Circuits for safe protective separation against electrical shock according to safety class II (reinforced isolation):
 - for appl. class I - IV at mains voltage ≤ 300 V
 - for appl. class I - III at mains voltage ≤ 600 V according to DIN EN 60747-5-5 (VDE 0884)

ORDER INFORMATION ⁽¹⁾

PART	REMARKS
CNY75A	CTR 63 % to 125 %, DIP-6
CNY75B	CTR 100 % to 200 %, DIP-6
CNY75C	CTR 160 % to 320 %, DIP-6
CNY75GA	CTR 63 % to 125 %, DIP-6, 400 mil
CNY75GB	CTR 100 % to 200 %, DIP-6, 400 mil
CNY75GC	CTR 160 % to 320 %, DIP-6, 400 mil

Note

⁽¹⁾ G = leadform 10.16 mm; G is not marked on the body.



CNY75A, CNY75B, CNY75C, CNY75GA, CNY75GB, CNY75GC

Optocoupler, Phototransistor Output, Vishay Semiconductors
with Base Connection

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾				
PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
INPUT				
Reverse voltage		V_R	5	V
Forward current		I_F	60	mA
Forward surge current	$t_p \leq 10 \mu s$	I_{FSM}	3	A
Power dissipation		P_{diss}	70	mW
Junction temperature		T_j	125	°C
OUTPUT				
Collector base voltage		V_{CBO}	70	V
Collector emitter voltage		V_{CEO}	70	V
Emitter collector voltage		V_{ECO}	7	V
Collector current		I_C	50	mA
Collector peak current	$t_p/T = 0.5, t_p \leq 10 ms$	I_{CM}	100	mA
Power dissipation		P_{diss}	70	mW
Junction temperature		T_j	125	°C
COUPLER				
AC isolation test voltage (RMS)		V_{ISO}	5000	V_{RMS}
Total power dissipation		P_{tot}	200	mW
Ambient temperature range		T_{amb}	- 55 to + 110	°C
Storage temperature range		T_{stg}	- 55 to + 125	°C
Soldering temperature ⁽²⁾	2 mm from case, $t \leq 10 s$	T_{sld}	260	°C

Notes

(1) $T_{amb} = 25 \text{ }^\circ\text{C}$, unless otherwise specified.

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this document. Exposure to absolute maximum ratings for extended periods of the time can adversely affect reliability.

(2) Refer to wave profile for soldering conditions for through hole devices.

ELECTRICAL CHARACTERISTICS ⁽¹⁾							
PARAMETER	TEST CONDITION	PART	SYMBOL	MIN.	TYP.	MAX.	UNIT
INPUT							
Forward voltage	$I_F = 50 \text{ mA}$		V_F		1.25	1.6	V
Reverse current	$V_R = 6 \text{ V}$		I_R			10	μA
Junction capacitance	$V_R = 0 \text{ V}, f = 1 \text{ MHz}$		C_j		50		pF
OUTPUT							
Collector base voltage	$I_C = 100 \mu\text{A}$		V_{CBO}	70			V
Collector emitter voltage	$I_C = 1 \text{ mA}$		V_{CEO}	70			V
Emitter collector voltage	$I_E = 100 \mu\text{A}$		V_{ECO}	7			V
Collector emitter leakage current	$V_{CE} = 20 \text{ V}, I_F = 0 \text{ A}$		I_{CEO}			150	nA
COUPLER							
Collector emitter saturation voltage	$I_F = 10 \text{ mA}, I_C = 1 \text{ mA}$		V_{CEsat}			0.3	V
Cut-off frequency	$V_{CE} = 5 \text{ V}, I_F = 10 \text{ mA}, R_L = 100 \Omega$		f_c		110		kHz
Coupling capacitance	$f = 1 \text{ MHz}$		C_k		0.6		pF

Note

(1) $T_{amb} = 25 \text{ }^\circ\text{C}$, unless otherwise specified.

Minimum and maximum values were tested requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information only and are not part of the testing requirements.

CURRENT TRANSFER RATIO

PARAMETER	TEST CONDITION	PART	SYMBOL	MIN.	TYP.	MAX.	UNIT
I_C/I_F	$V_{CE} = 5\text{ V}, I_F = 1\text{ mA}$	CNY75GA	CTR	15			%
		CNY75GB	CTR	30			%
		CNY75GC	CTR	60			%
	$V_{CE} = 5\text{ V}, I_F = 10\text{ mA}$	CNY75GA	CTR	63		125	%
		CNY75GB	CTR	100		200	%
		CNY75GC	CTR	160		320	%

SWITCHING CHARACTERISTICS

PARAMETER	TEST CONDITION	PART	SYMBOL	MIN.	TYP.	MAX.	UNIT
Current time	$V_{CC} = 5\text{ V}, R_L = 100\ \Omega$	CNY75GA	I_F		10		mA
		CNY75GB	I_F		10		mA
		CNY75GC	I_F		10		mA
Delay time	$V_{CC} = 5\text{ V}, R_L = 100\ \Omega$	CNY75GA	t_d		2		μs
		CNY75GB	t_d		2.5		μs
		CNY75GC	t_d		2.8		μs
Rise time	$V_{CC} = 5\text{ V}, R_L = 100\ \Omega$	CNY75GA	t_r		2.5		μs
		CNY75GB	t_r		3		μs
		CNY75GC	t_r		4.2		μs
Fall time	$V_{CC} = 5\text{ V}, R_L = 100\ \Omega$	CNY75GA	t_f		2.7		μs
		CNY75GB	t_f		3.7		μs
		CNY75GC	t_f		4.7		μs
Storage time	$V_{CC} = 5\text{ V}, R_L = 100\ \Omega$	CNY75GA	t_s		0.3		μs
		CNY75GB	t_s		0.3		μs
		CNY75GC	t_s		0.3		μs
Turn-on time	$V_{CC} = 5\text{ V}, R_L = 100\ \Omega$	CNY75GA	t_{on}		4.5		μs
		CNY75GB	t_{on}		5.5		μs
		CNY75GC	t_{on}		7		μs
Turn-off time	$V_{CC} = 5\text{ V}, R_L = 100\ \Omega$	CNY75GA	t_{off}		3		μs
		CNY75GB	t_{off}		4		μs
		CNY75GC	t_{off}		5		μs
Turn-on time	$V_{CC} = 5\text{ V}, R_L = 1\text{ k}\Omega$	CNY75GA	t_{on}		10		μs
		CNY75GB	t_{on}		16.5		μs
		CNY75GC	t_{on}		11		μs
Turn-off time	$V_{CC} = 5\text{ V}, R_L = 1\text{ k}\Omega$	CNY75GA	t_{off}		25		μs
		CNY75GB	t_{off}		20		μs
		CNY75GC	t_{off}		37.5		μs

MAXIMUM SAFETY RATINGS ⁽¹⁾						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
INPUT						
Forward current		I _F			130	mA
OUTPUT						
Power dissipation		P _{diss}			265	mW
COUPLER						
Rated impulse voltage		V _{IOTM}			6	kV
Safety temperature		T _{si}			150	°C

Note

⁽¹⁾ According DIN EN 60747-5-5. This optocoupler is suitable for safe electrical isolation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

INSULATION RATED PARAMETERS						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Partial discharge test voltage - routine test	100 %, $t_{\text{test}} = 1 \text{ s}$	V_{pd}	1.6			kV
Partial discharge test voltage - lot test (sample test)	$t_{\text{Tr}} = 60 \text{ s}$, $t_{\text{test}} = 10 \text{ s}$, (see figure 1)	V_{IOTM}	6			kV
		V_{pd}	1.3			kV
Insulation resistance	$V_{\text{IO}} = 500 \text{ V}$	R_{IO}	10^{12}			Ω
	$V_{\text{IO}} = 500 \text{ V}$, $T_{\text{amb}} \leq 100 \text{ }^{\circ}\text{C}$	R_{IO}	10^{11}			Ω
	$V_{\text{IO}} = 500 \text{ V}$, $T_{\text{amb}} \leq 150 \text{ }^{\circ}\text{C}$ (construction test only)	R_{IO}	10^9			Ω

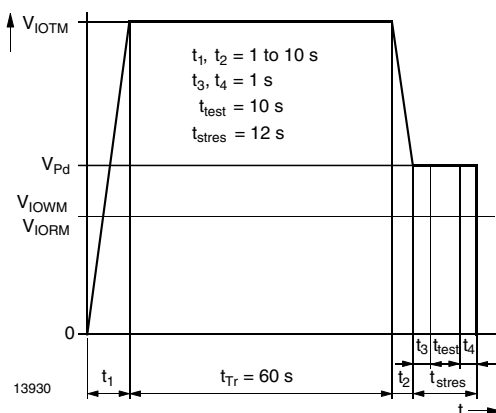


Fig. 1 - Test Pulse Diagram for Sample Test according to DIN EN 60747-5-5 (VDE 0884)/DIN EN 60747-; IEC60747

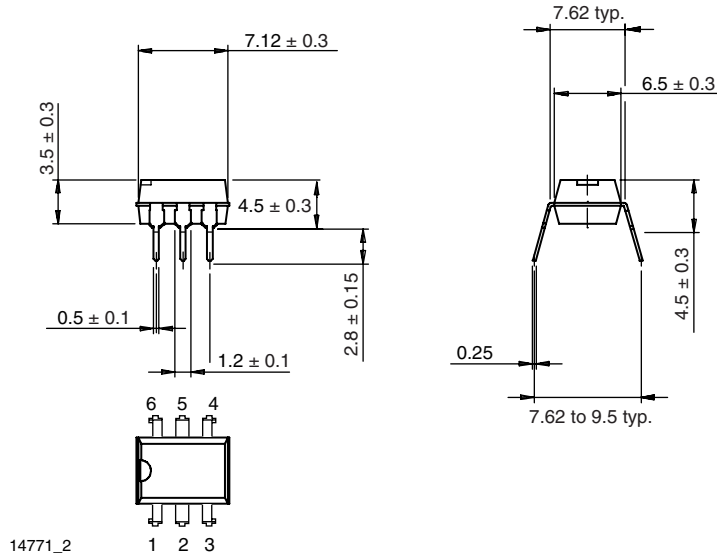
CNY75A, CNY75B, CNY75C, CNY75GA, CNY75GB, CNY75GC



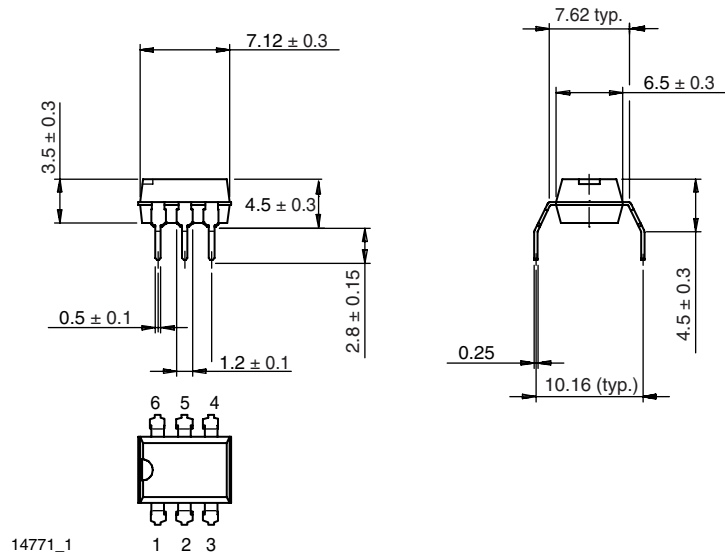
Vishay Semiconductors Optocoupler, Phototransistor Output,
with Base Connection

PACKAGE DIMENSIONS in millimeters

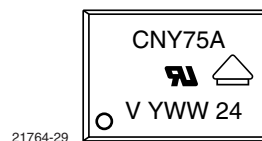
DIP-6



DIP-6, 400 mil



PACKAGE MARKING



Footprints

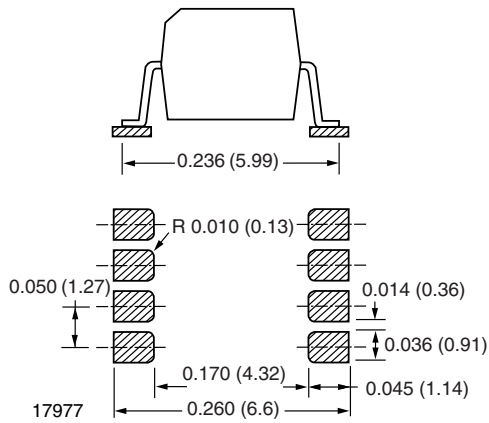


Fig. 1 - SO8A and DSO8A SMD

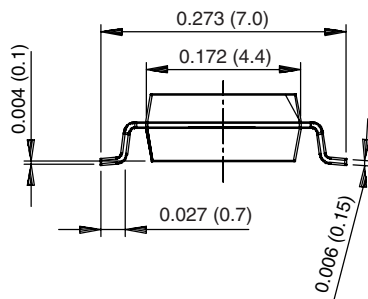


Fig. 2 - SOP-4, Miniflat

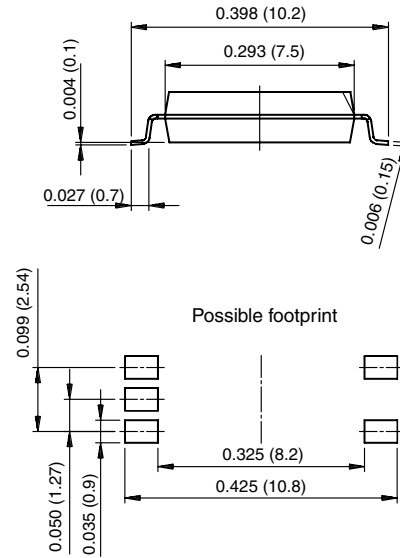


Fig. 3 - SOP-6, 5 Pin Wide Body

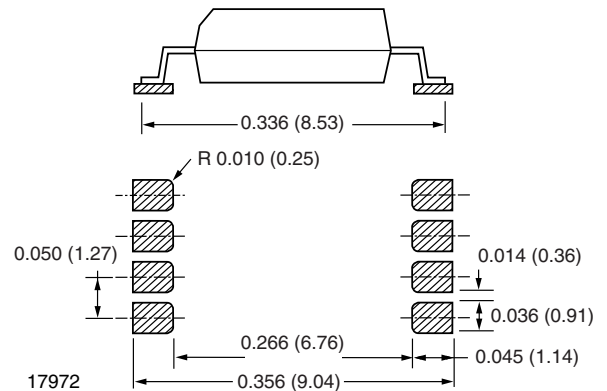


Fig. 4 - 8 Pin PCMCIA

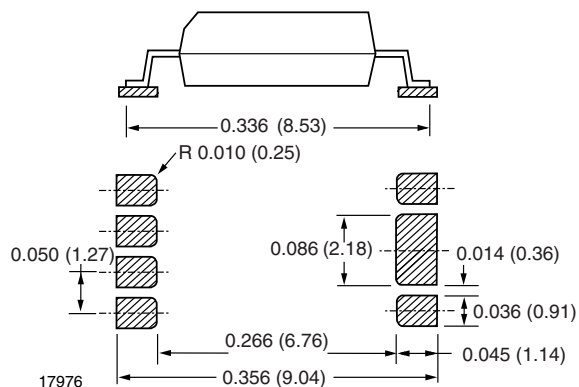


Fig. 5 - 8 Pin PCMCIA, Heat Sink

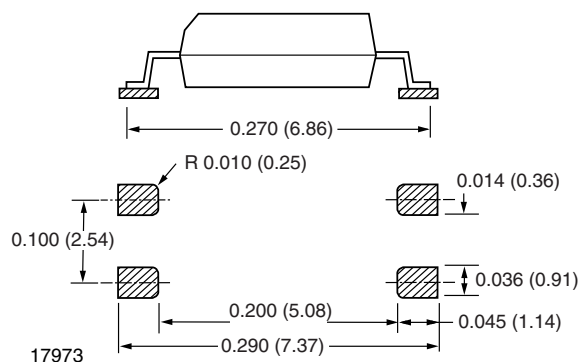


Fig. 8 - 4 Pin Mini-Flat

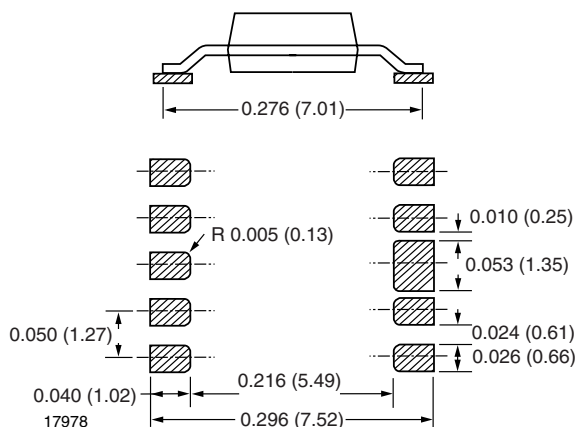


Fig. 6 - Mini Coupler

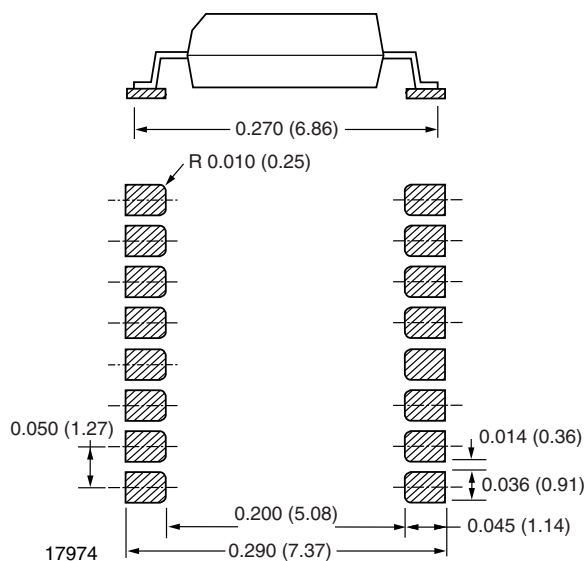


Fig. 7 - SOP-16

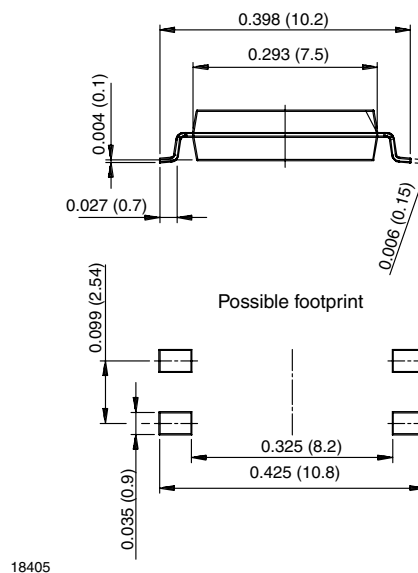


Fig. 9 - SOP-6, 4 Pin Wide Body

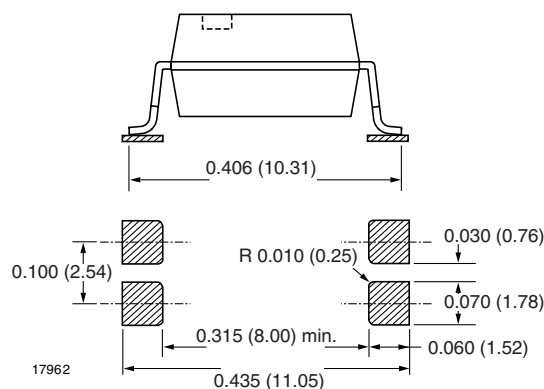


Fig. 10 - 4 Pin SMD Option 7

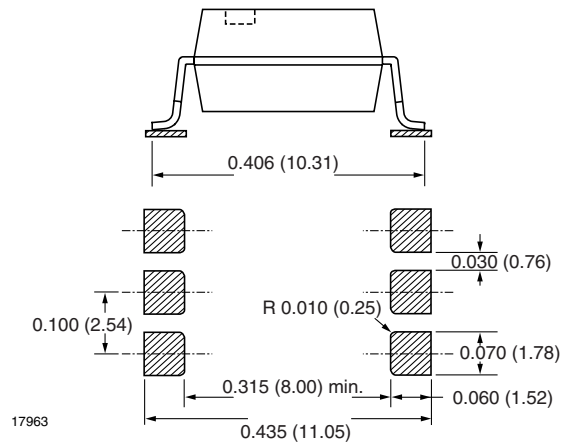


Fig. 11 - 6 Pin SMD Option 7

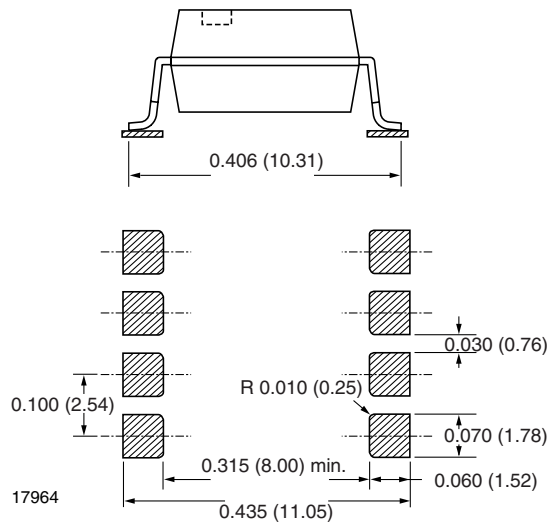


Fig. 12 - 8 Pin SMD Option 7

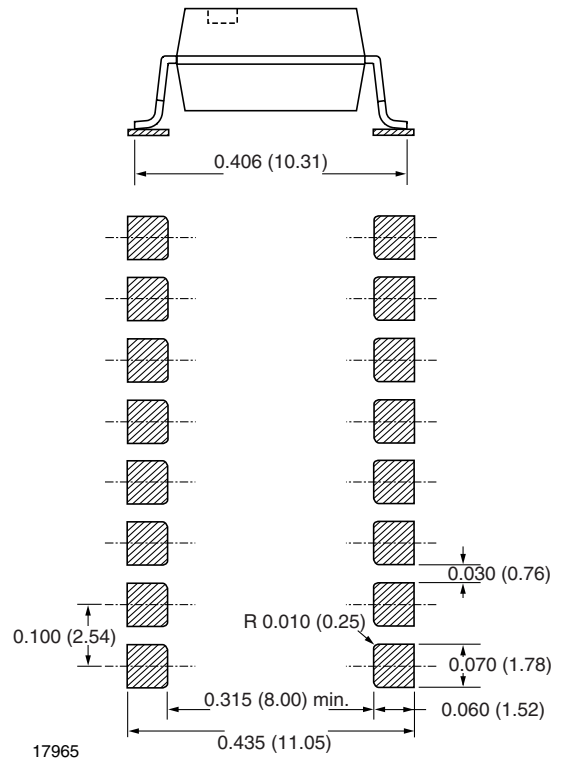


Fig. 13 - 16 Pin SMD Option 7

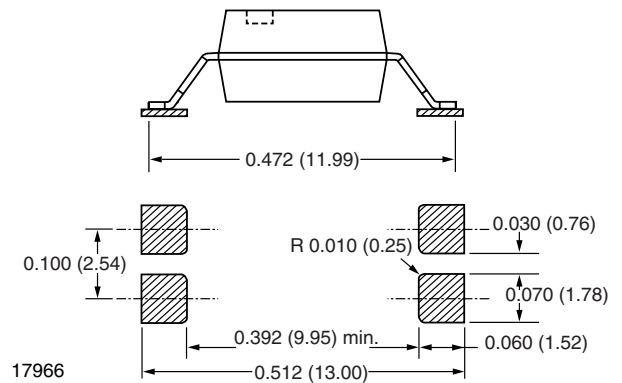


Fig. 14 - 4 Pin SMD Option 8

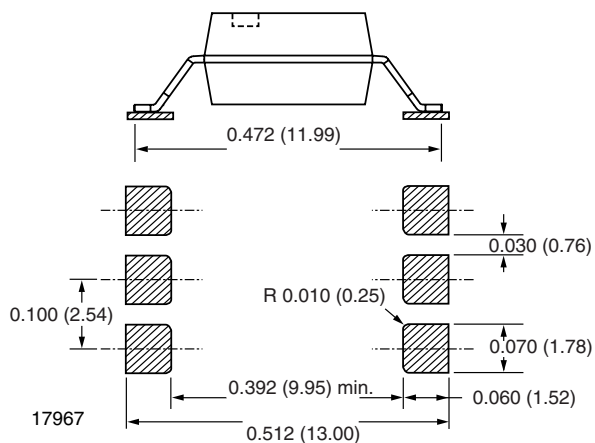


Fig. 15 - 6 Pin SMD Option 8

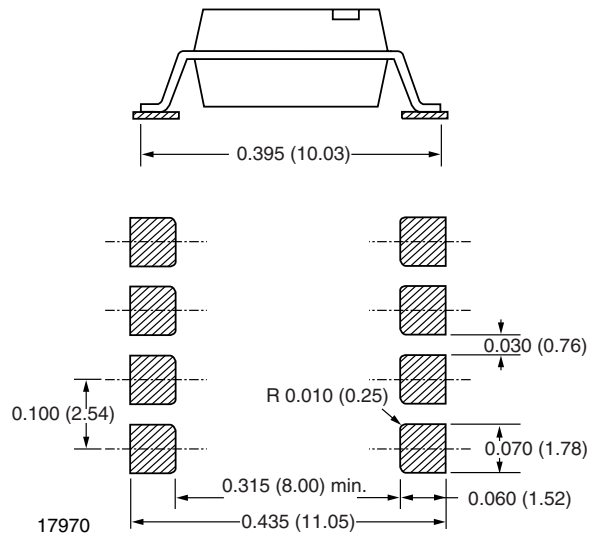


Fig. 18 - 8 Pin SMD Option 9

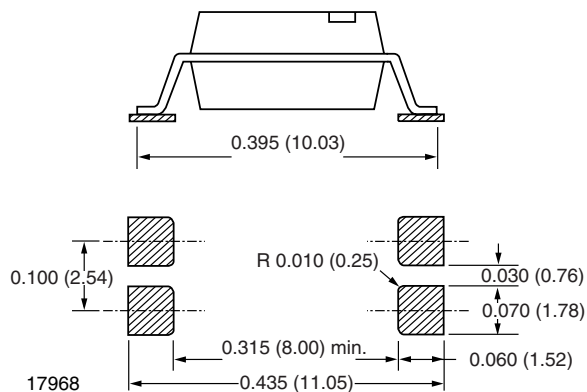


Fig. 16 - 4 Pin SMD Option 9

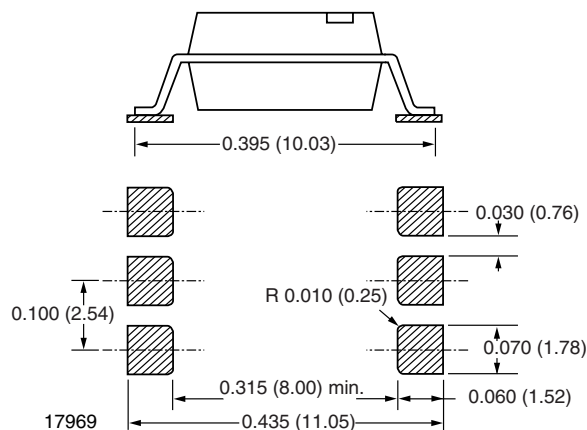


Fig. 17 - 6 Pin SMD Option 9

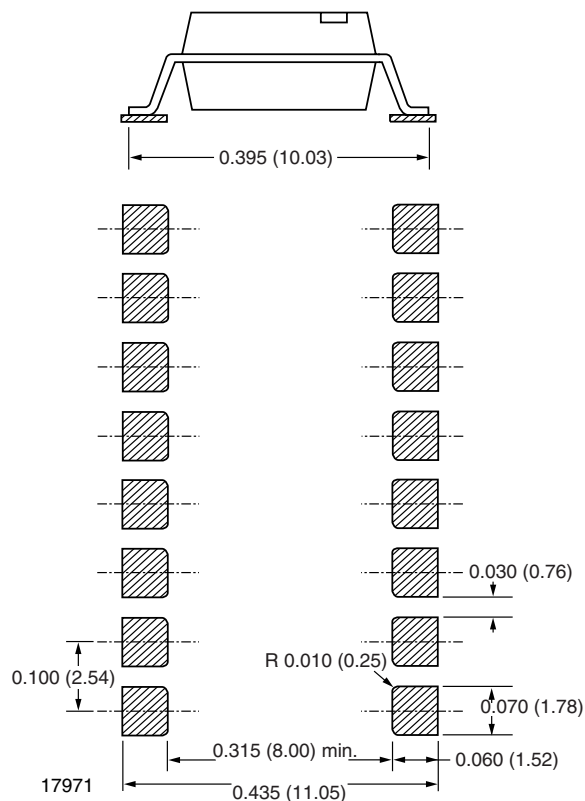
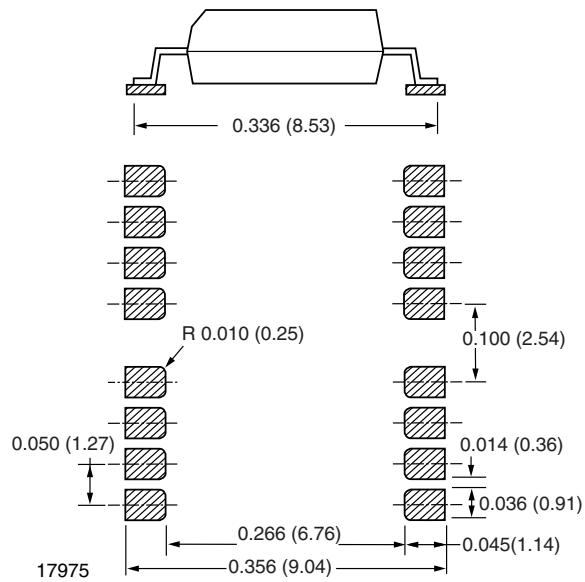


Fig. 19 - 16 Pin SMD Option 9





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