

FDMC5614P

P-Channel PowerTrench® MOSFET

60V, 5.7A, 100mΩ



General Description

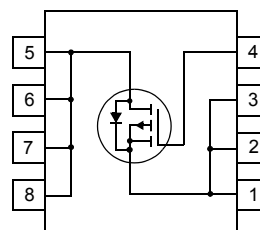
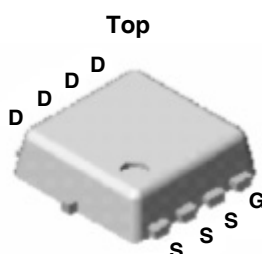
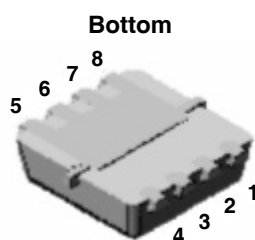
This P-Channel MOSFET is a rugged gate version of Fairchild Semiconductor's advanced Power Trench process. It has been optimized for power management applications requiring a wide range of gate drive voltage ratings (4.5V-20V).

Applications

- Power management
- Load switch
- battery protection

Features

- Max $r_{DS(on)}$ = 100 mΩ @ $V_{GS} = -10\text{ V}$, $I_D = -5.7\text{ A}$
- Max $r_{DS(on)}$ = 135 mΩ @ $V_{GS} = -4.5\text{ V}$, $I_D = -4.4\text{ A}$
- Low gate charge
- Fast switching speed
- High performance trench technology for extremely low $r_{DS(on)}$
- High power and current handling capability
- RoHS Compliant



MicroFET 3x3

Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	-60	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current -Continuous (Note 1a) -Pulsed	-5.7	A
		-23	
P_D	Power Dissipation (Steady State) (Note 1a) (Note 1b)	6.0	W
		1.2	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	52	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	108	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	5	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
5614P	FDMC5614P	7inch	12mm	3000 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

B_{VDSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = -250\mu A$	-60			V
$\frac{\Delta B_{VDSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\mu A$, referenced to 25°C		-54		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -48V, V_{GS} = 0V$			-1	μA
I_{GSS}	Gate-Body Leakage,	$V_{GS} = \pm 20V, V_{DS} = 0V$			± 100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1	-1.95	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\mu A$, referenced to 25°C		4.7		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10V, I_D = -5.7A$		84	100	m Ω
		$V_{GS} = -4.5V, I_D = -4.4A$		108	135	
		$V_{GS} = -10V, I_D = -5.7A$ $T_J = 125^\circ\text{C}$		140	168	
g_{FS}	Forward Transconductance	$V_{DS} = -15V, I_D = -5.7A$		11		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -30V, V_{GS} = 0V,$ $f = 1.0\text{MHz}$		792	1055	pF
C_{oss}	Output Capacitance			137	185	pF
C_{rss}	Reverse Transfer Capacitance			57	90	pF

Switching Characteristics (Note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -30V, I_D = -1A$ $V_{GS} = -10V, R_{GEN} = 6\Omega$		10.3	21	ns
t_r	Turn-On Rise Time			11.3	23	ns
$t_{d(off)}$	Turn-Off Delay Time			32.2	65	ns
t_f	Turn-Off Fall Time			11.0	22	ns
Q_g	Total Gate Charge	$V_{DS} = -30V, I_D = -5.7A,$ $V_{GS} = -10V$		15.3	20	nC
Q_{gs}	Gate-Source Charge			1.6	2.1	nC
Q_{gd}	Gate-Drain Charge			2.7	3.5	nC

Drain-Source Diode Characteristics (Note 2)

V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0V, I_S = -3.2A$		-0.82	-1.2	V
t_{rr}	Diode Reverse Recovery Time	$I_F = -3.2A, di/dt = 100A/\mu s$			36	ns
Q_{rr}	Diode Reverse Recovery Charge				29	nC

Notes:

1: $R_{\theta JA}$ is determined with the device mounted on a 1 in² oz. copper pad on a 1.5x1.5 in board of FR-4 material. $R_{\theta JC}$ are guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a. 52°C/W when mounted on a 1 in² pad of 2 oz, 24°C/W when power time = 10sec.



b. 108°C/W when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

Typical Characteristics

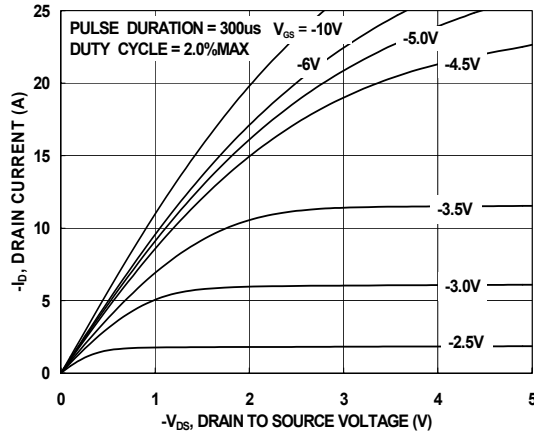


Figure 1. On Region Characteristics

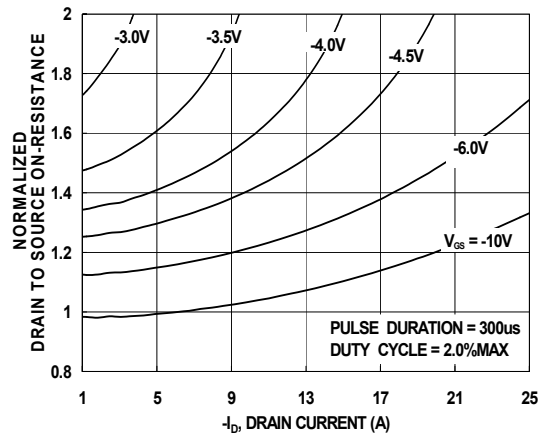


Figure 2. On Resistance vs Drain Current and Gate Voltage

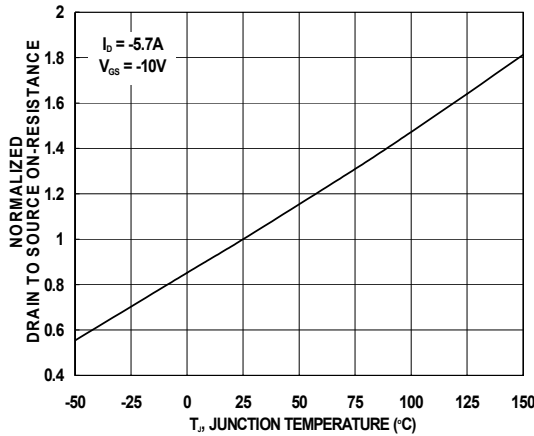


Figure 3. Normalized On Resistance vs Junction Temperature

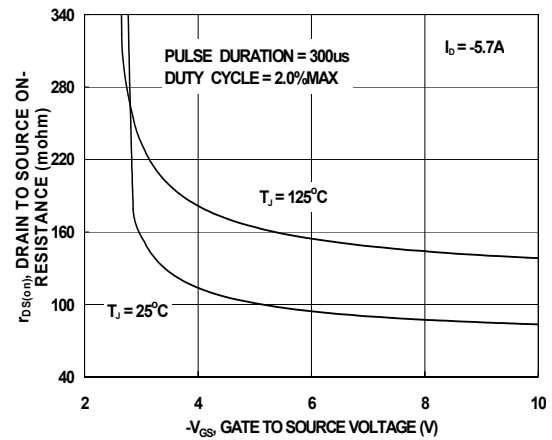


Figure 4. On-Resistance vs Gate to Source Voltage

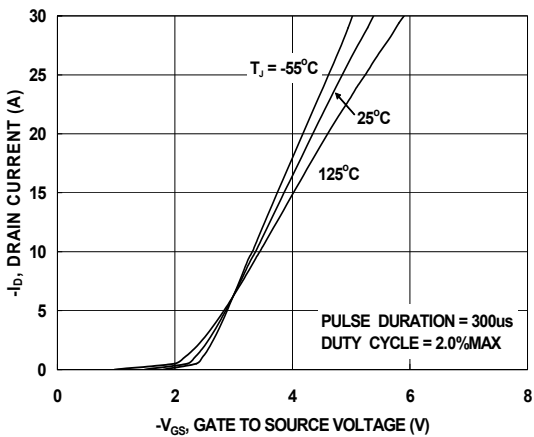


Figure 5. Transfer Characteristics

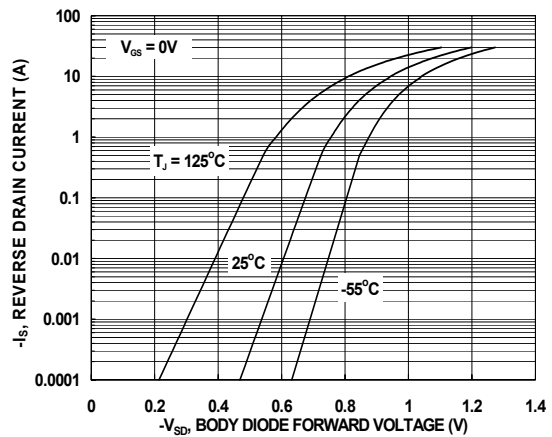


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics

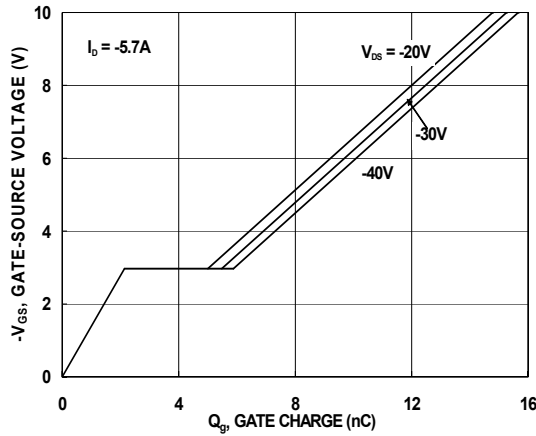


Figure 7. Gate Charge Characteristics

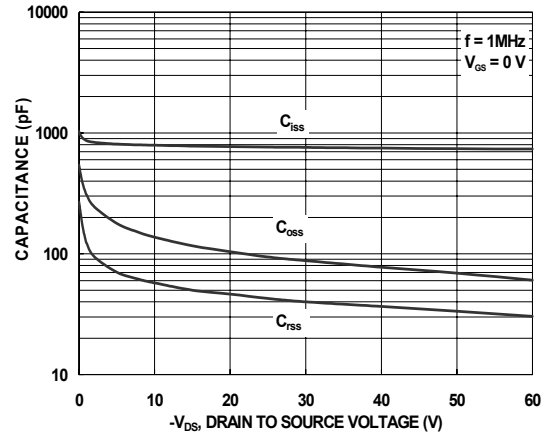


Figure 8. Capacitance vs Drain to Source Voltage

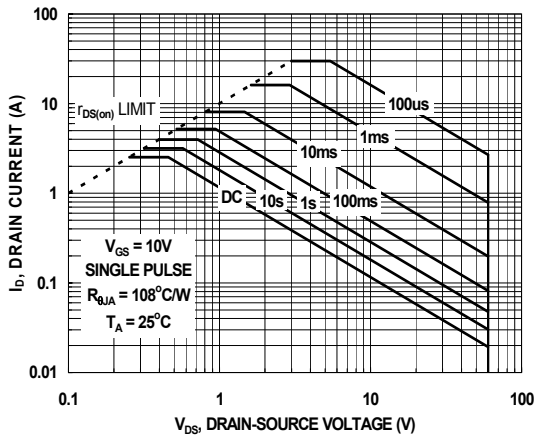


Figure 9. Forward Bias Safe Operation Area

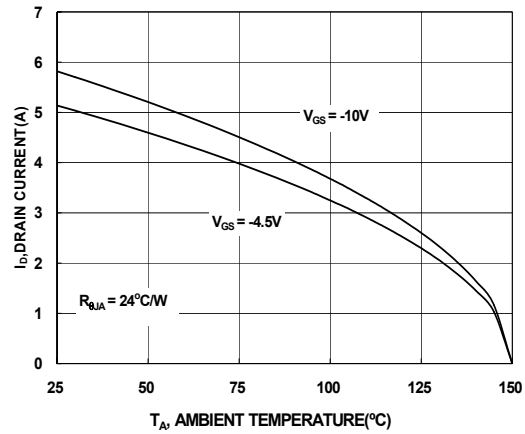


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

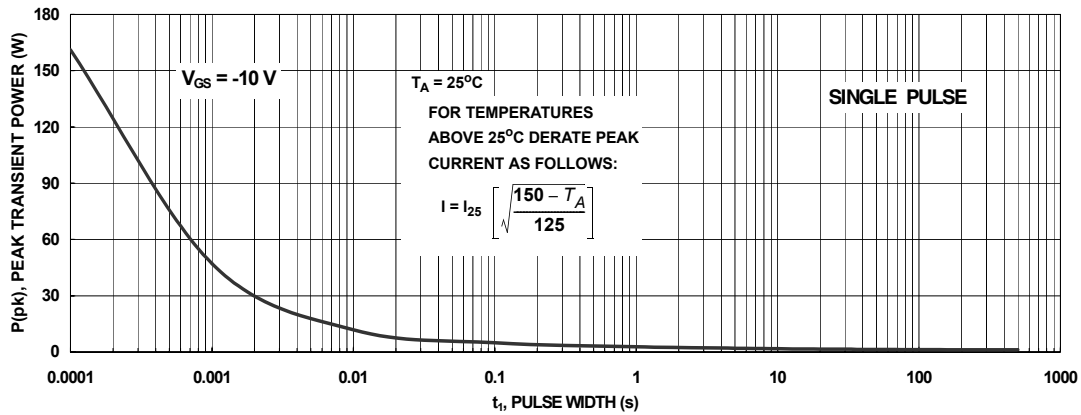


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics

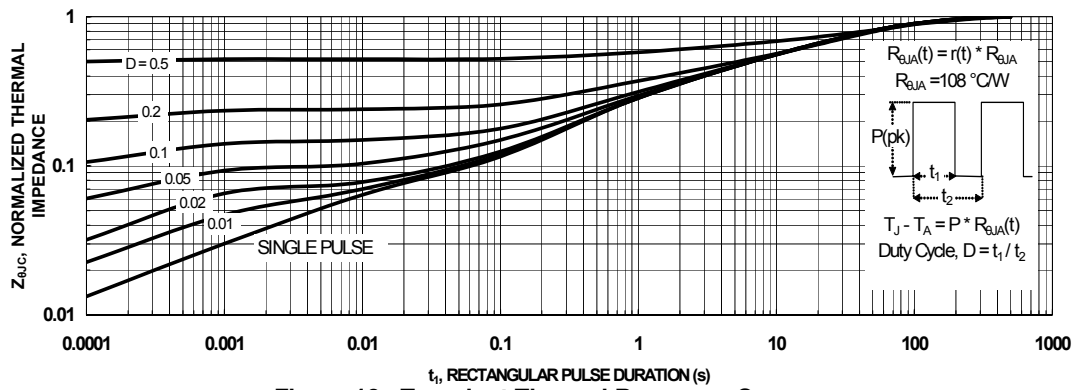
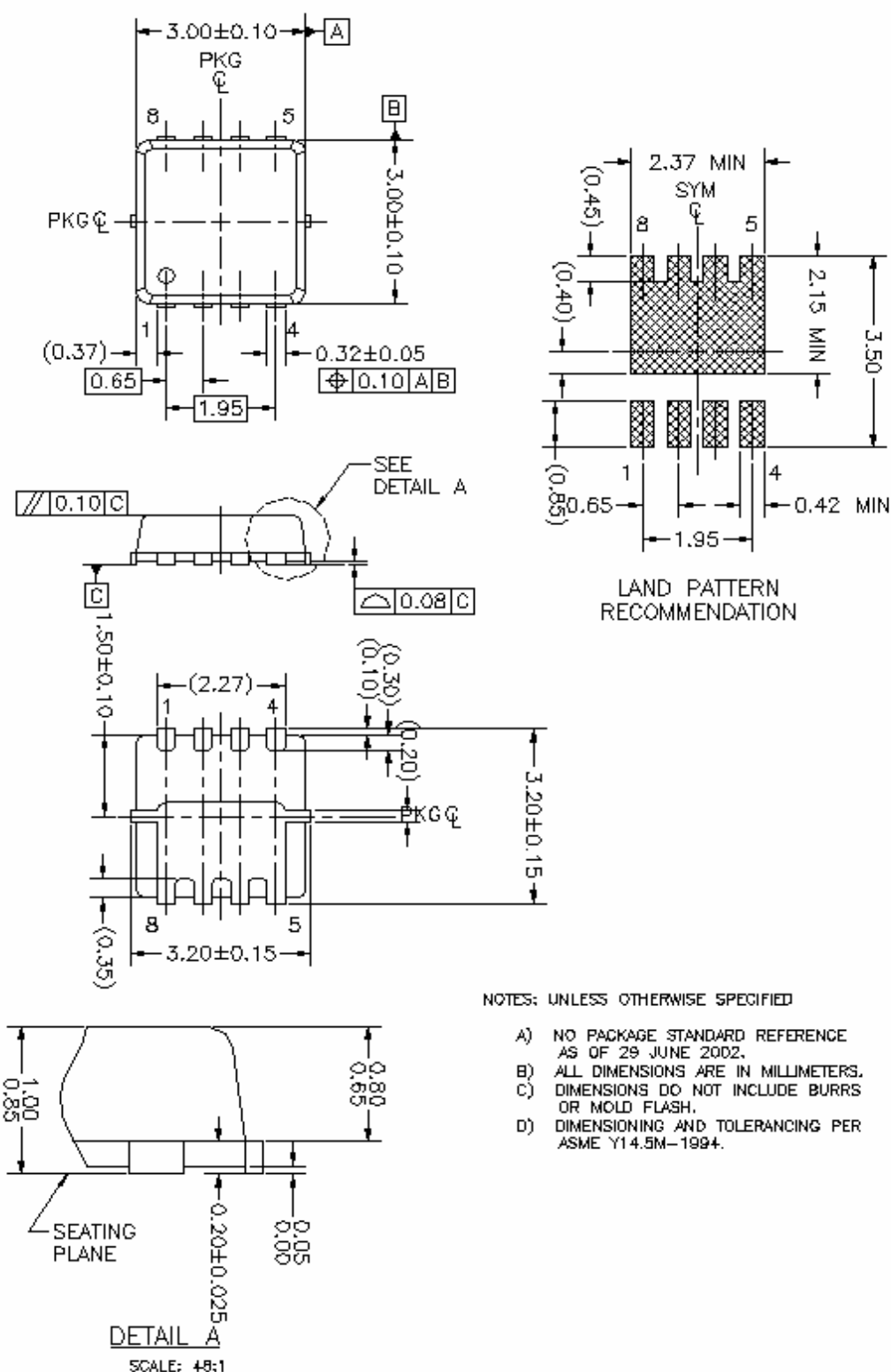


Figure 12. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

Dimensional Outline and Pad Layout



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