

BLF8G10LS-270V; BLF8G10LS-270GV

Power LDMOS transistor

Rev. 1 — 3 December 2012

Product data sheet

1. Product profile

1.1 General description

270 W LDMOS power transistor with improved video bandwidth for base station applications at frequencies from 790 MHz to 960 MHz.

Table 1. Typical performance

Typical RF performance at $T_{case} = 25\text{ }^{\circ}\text{C}$ in a common source class-AB production test circuit, tested on straight lead device.

Test signal	f (MHz)	V _{DS} (V)	P _{L(AV)} (W)	G _p (dB)	η_D (%)	ACPR _{5M} (dBc)
2-carrier W-CDMA	869 to 894	28	67	19.5	31	-37 ^[1]

[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 8.4 dB at 0.01 % probability on CCDF; carrier spacing 10 MHz.

1.2 Features and benefits

- Excellent ruggedness
- High efficiency
- Low R_{th} providing excellent thermal stability
- Designed for broadband operation (790 MHz to 960 MHz)
- Lower output capacitance for improved performance in Doherty applications
- Decoupling leads to enable improved video bandwidth (55 MHz typical)
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Design optimized for gull-wing and straight lead versions
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

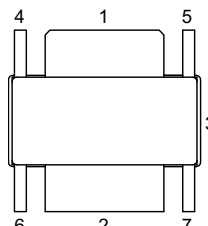
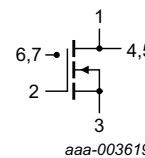
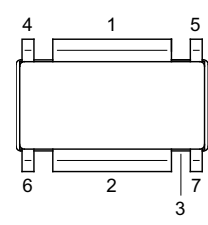
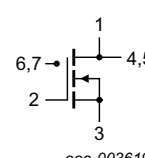
1.3 Applications

- RF power amplifiers for W-CDMA base stations and multi carrier applications in the 790 MHz to 960 MHz frequency range



2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF8G10LS-270V (SOT1244B)			
1	drain		 aaa-003619
2	gate		
3	source		
4	decoupling lead		
5	decoupling lead		
6	n.c.		
7	n.c.		
BLF8G10LS-270GV (SOT1244C)			
1	drain		 aaa-003619
2	gate		
3	source		
4	decoupling lead		
5	decoupling lead		
6	n.c.		
7	n.c.		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF8G10LS-270V	-	earless flanged ceramic package; 6 leads	SOT1244B
BLF8G10LS-270GV	-	earless flanged ceramic package; 6 leads	SOT1244C

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+13	V
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	225	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 80\text{ }^{\circ}\text{C}$; $P_L = 67\text{ W}$	0.257	K/W

6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ }^{\circ}\text{C}$; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$; $I_D = 4.5\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$; $I_D = 450\text{ mA}$	1.5	1.8	2.3	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}$; $V_{DS} = 28\text{ V}$	-	-	4.2	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $V_{DS} = 10\text{ V}$	-	82	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}$; $V_{DS} = 0\text{ V}$	-	-	420	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}$; $I_D = 450\text{ mA}$	-	3.92	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $I_D = 15.75\text{ A}$	-	0.04	-	Ω

Table 7. RF characteristics

Test signal: 2-carrier W-CDMA; PAR = 8.4 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1-64 DPCH; $f_1 = 871.5\text{ MHz}$; $f_2 = 881.5\text{ MHz}$; $f_3 = 881.5\text{ MHz}$; $f_4 = 891.5\text{ MHz}$; $f_5 = 881.5\text{ MHz}$; $f_6 = 891.5\text{ MHz}$; RF performance at $V_{DS} = 28\text{ V}$; $I_{Dq} = 2000\text{ mA}$; $T_{case} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified; in a class-AB production test circuit, tested on straight lead device.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)} = 67\text{ W}$	17.3	19.5	-	dB
RL_{in}	input return loss	$P_{L(AV)} = 67\text{ W}$	-	-16	-12	dB
η_D	drain efficiency	$P_{L(AV)} = 67\text{ W}$	26	31	-	%
$ACPR_{5M}$	adjacent channel power ratio (5 MHz)	$P_{L(AV)} = 67\text{ W}$	-	-37	-33	dBc

7. Test information

7.1 Ruggedness in class-AB operation

The BLF8G10LS-270V and BLF8G10LS-270GV are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: $V_{DS} = 28\text{ V}$; $I_{Dq} = 2000\text{ mA}$; $P_L = 270\text{ W}$; $f = 820\text{ MHz}$; $f = 869\text{ MHz}$; $f = 920\text{ MHz}$; $f = 960\text{ MHz}$ and a load mismatch corresponding to VSWR = 5 : 1 through all phases under the following conditions: $V_{DS} = 28\text{ V}$; $I_{Dq} = 2000\text{ mA}$; $P_L = 270\text{ W}$; $f = 790\text{ MHz}$.

7.2 Impedance information

Table 8. Typical impedance

$I_{DQ} = 2700 \text{ mA}$; main transistor $V_{DS} = 28 \text{ V}$.

f (MHz)	Z_S [1] (Ω)	Z_L [1] (Ω)
790	$1.4 - j1.84$	$1.22 - j2.07$
820	$1.58 - j1.96$	$1.29 - j1.95$
869	$1.84 - j2.70$	$1.12 - j1.83$
881	$1.78 - j2.94$	$1.12 - j1.84$
894	$1.90 - j3.08$	$1.12 - j1.84$
920	$2.06 - j2.50$	$1.04 - j1.13$
940	$2.10 - j2.90$	$1.04 - j1.13$
960	$2.56 - j2.65$	$1.00 - j1.22$

[1] Z_S and Z_L defined in [Figure 1](#).

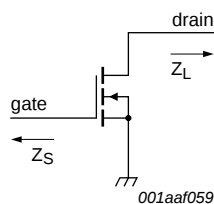


Fig 1. Definition of transistor impedance

7.3 VBW in class-AB operation

The BLF8G10LS-270V and BLF8G10LS-270GV show 55 MHz (typical) video bandwidth in class-AB test circuit in 800 MHz band at $V_{DS} = 28 \text{ V}$ and $I_{DQ} = 2 \text{ A}$.

7.4 Test circuit

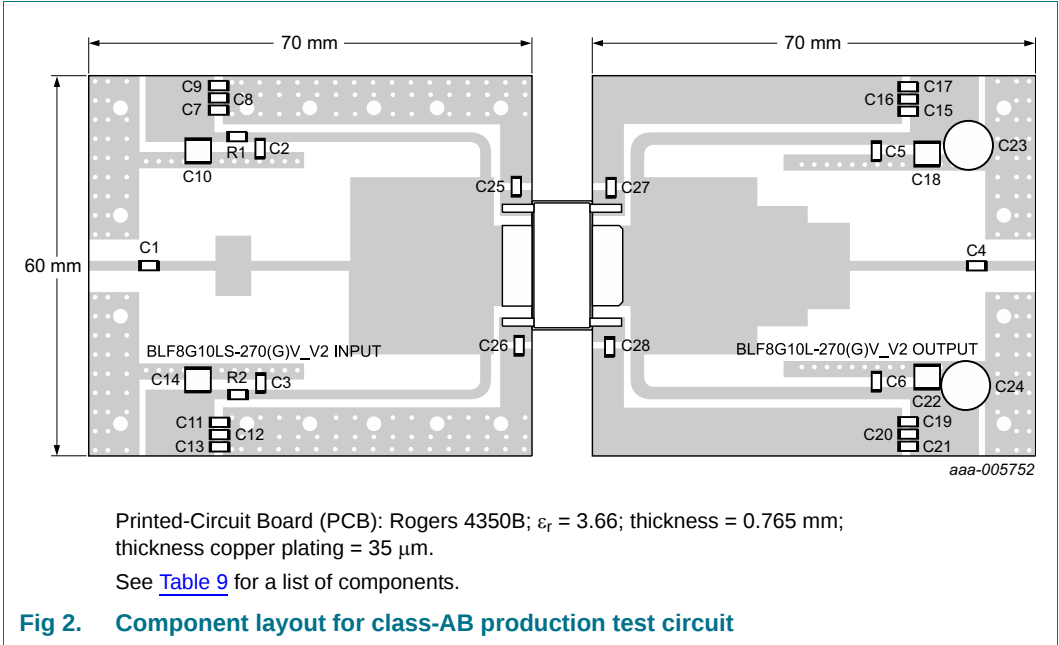


Table 9. List of components

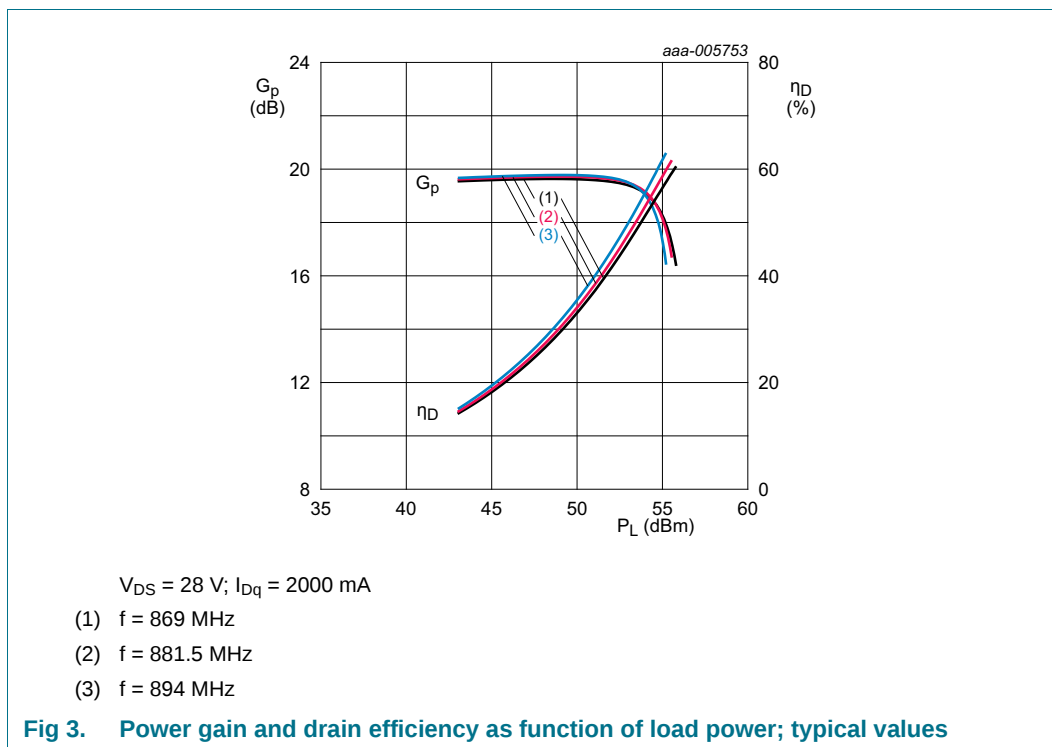
For test circuit see [Figure 2](#).

Component	Description	Value	Remarks
C1, C4	multilayer ceramic chip capacitor	47 pF	[1] ATC100B
C2, C3, C5, C6	multilayer ceramic chip capacitor	45 pF	[1] ATC100B
C7, C11, C15, C19	multilayer ceramic chip capacitor	0.01 μF	[2] Murata
C8, C12, C16, C20	multilayer ceramic chip capacitor	0.1 μF	[2] Murata
C9, C13, C17, C21	multilayer ceramic chip capacitor	1 μF	[2] Murata
C10, C14, C18, C22	multilayer ceramic chip capacitor	4.7 μF	[2] Murata
C23, C24	electrolytic capacitor	470 μF , 63 V	
C25, C26, C27, C28	multilayer ceramic chip capacitor	10 μF	[2] Murata
R1, R2	chip resistor	9.1 Ω	[3] Vishay Dale 0805

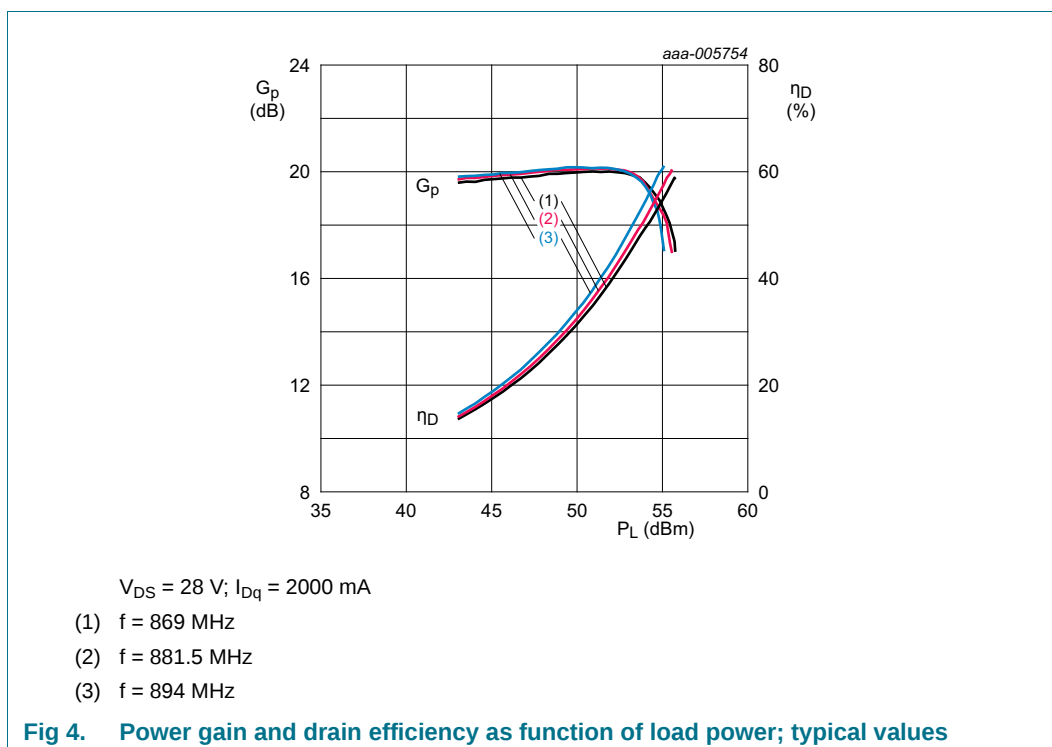
- [1] American Technical Ceramics type 100B or capacitor of same quality.
- [2] Murata or capacitor of same quality.
- [3] Vishay Dale resistor of same quality.

7.5 Graphical data

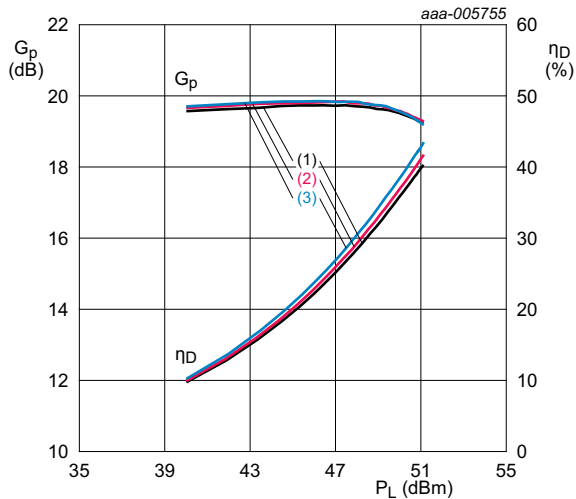
7.5.1 Straight lead sample CW



7.5.2 Straight lead sample CW pulsed



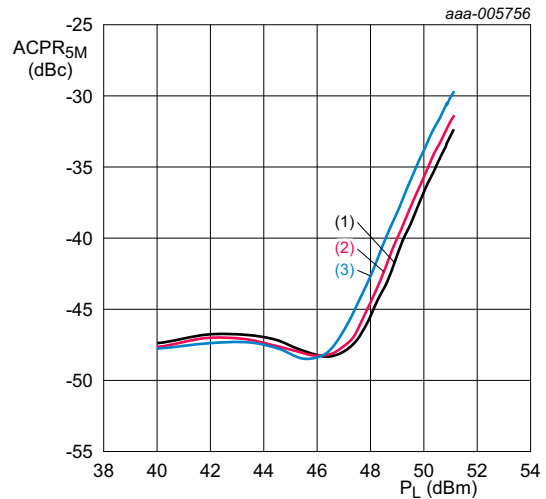
7.5.3 Straight lead sample 1-carrier W-CDMA



$V_{DS} = 28\text{ V}$; $I_{DQ} = 2000\text{ mA}$

- (1) $f = 869\text{ MHz}$
- (2) $f = 881.5\text{ MHz}$
- (3) $f = 894\text{ MHz}$

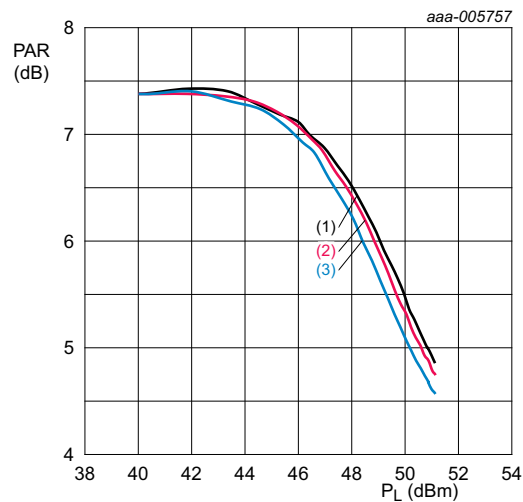
Fig 5. Power gain and drain efficiency as function of load power; typical values



$V_{DS} = 28\text{ V}$; $I_{DQ} = 2000\text{ mA}$

- (1) $f = 869\text{ MHz}$
- (2) $f = 881.5\text{ MHz}$
- (3) $f = 894\text{ MHz}$

Fig 6. Adjacent channel power ratio (5 MHz) as a function of load power; typical values

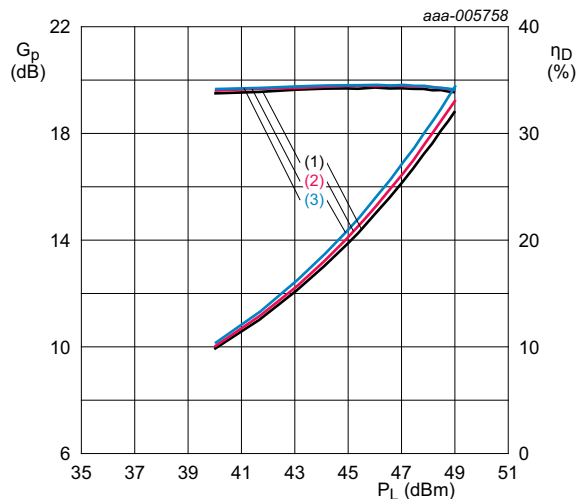


$V_{DS} = 28\text{ V}$; $I_{DQ} = 2000\text{ mA}$

- (1) $f = 869\text{ MHz}$
- (2) $f = 881.5\text{ MHz}$
- (3) $f = 894\text{ MHz}$

Fig 7. Peak-to-average ratio as a function of load power; typical values

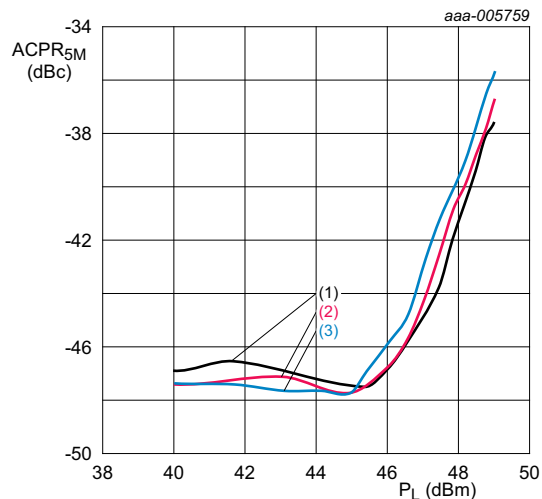
7.5.4 Straight lead sample 2-carrier W-CDMA



$V_{DS} = 28 \text{ V}$; $I_{DQ} = 2000 \text{ mA}$

- (1) $f = 869 \text{ MHz}$
- (2) $f = 881.5 \text{ MHz}$
- (3) $f = 894 \text{ MHz}$

Fig 8. Power gain and drain efficiency as function of load power; typical values

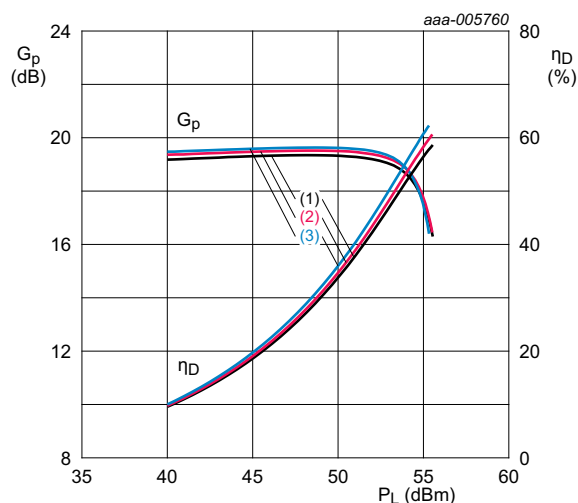


$V_{DS} = 28 \text{ V}$; $I_{DQ} = 2000 \text{ mA}$

- (1) $f = 869 \text{ MHz}$
- (2) $f = 881.5 \text{ MHz}$
- (3) $f = 894 \text{ MHz}$

Fig 9. Adjacent channel power ratio (5 MHz) as a function of load power; typical values

7.5.5 Gull-wing sample CW

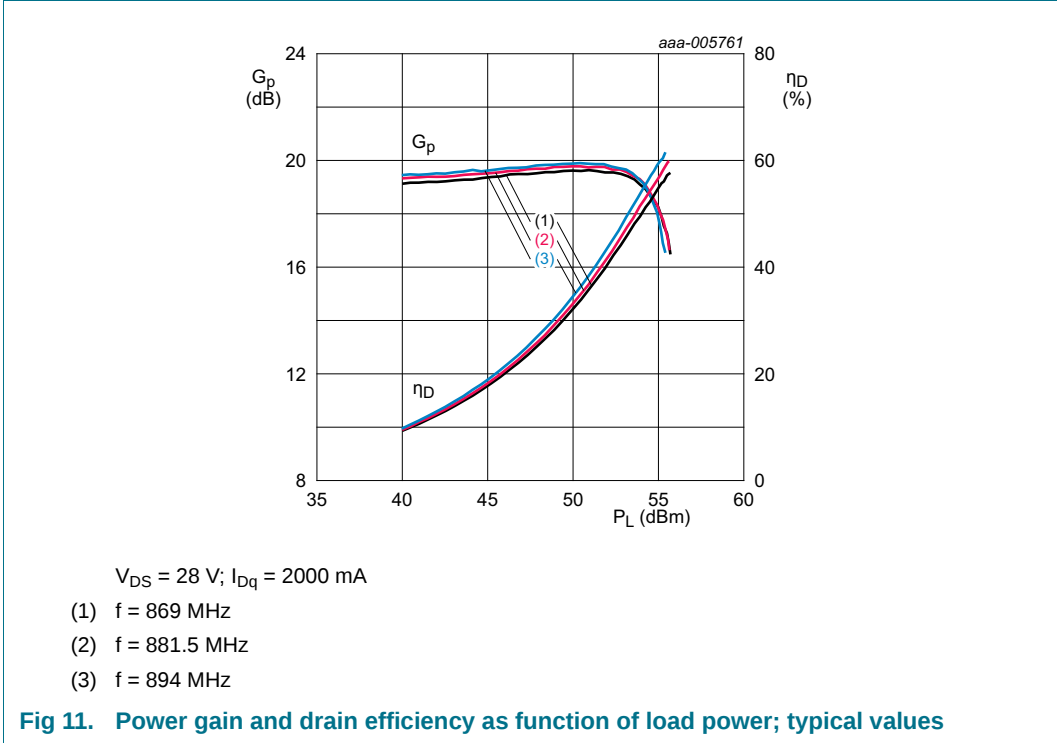


$V_{DS} = 28 \text{ V}$; $I_{DQ} = 2000 \text{ mA}$

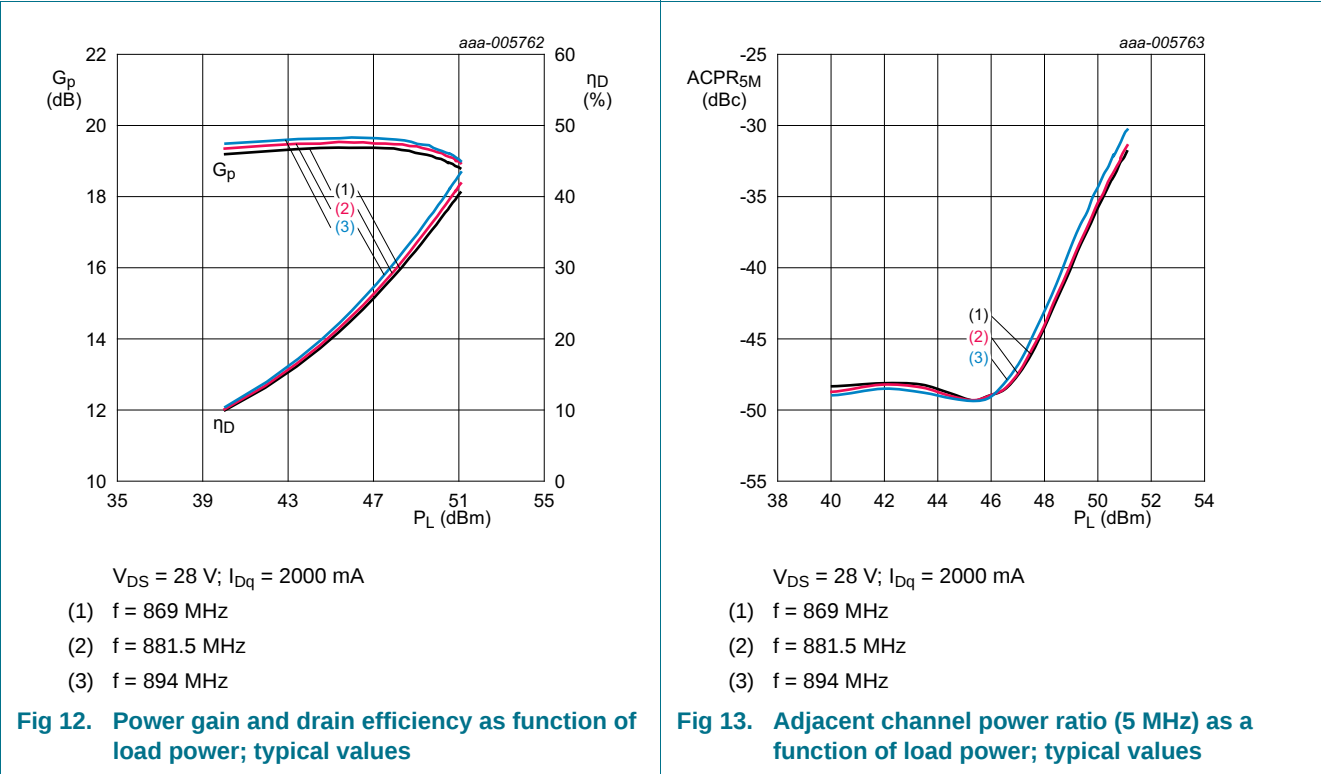
- (1) $f = 869 \text{ MHz}$
- (2) $f = 881.5 \text{ MHz}$
- (3) $f = 894 \text{ MHz}$

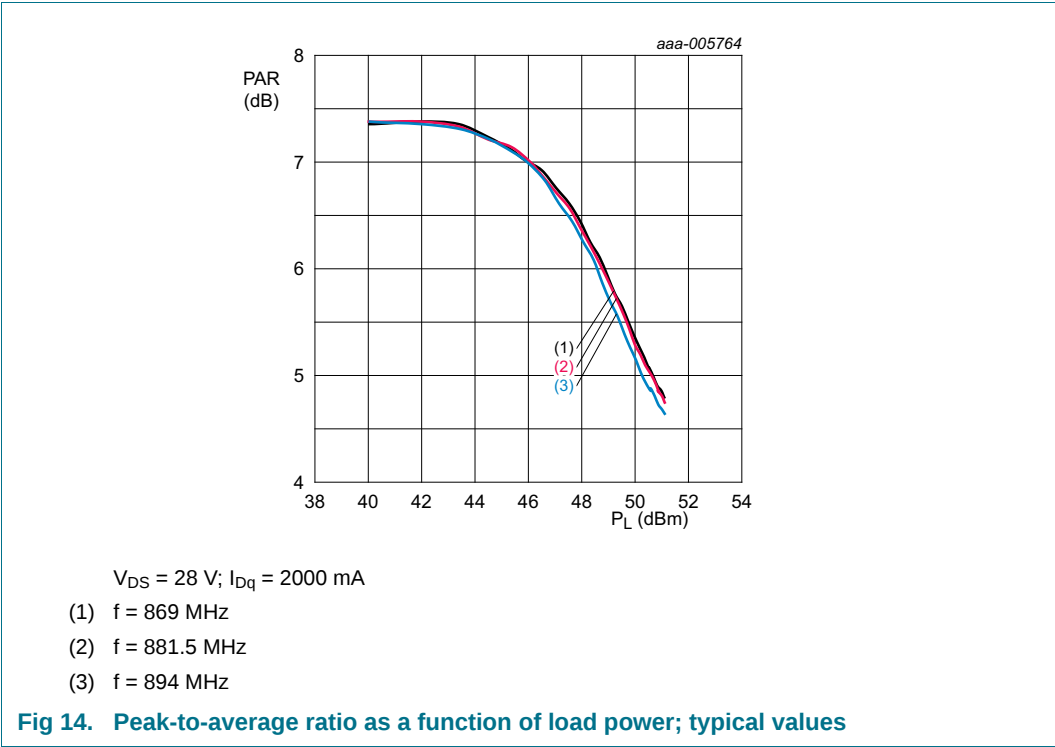
Fig 10. Power gain and drain efficiency as function of load power; typical values

7.5.6 Gull-wing sample CW pulsed

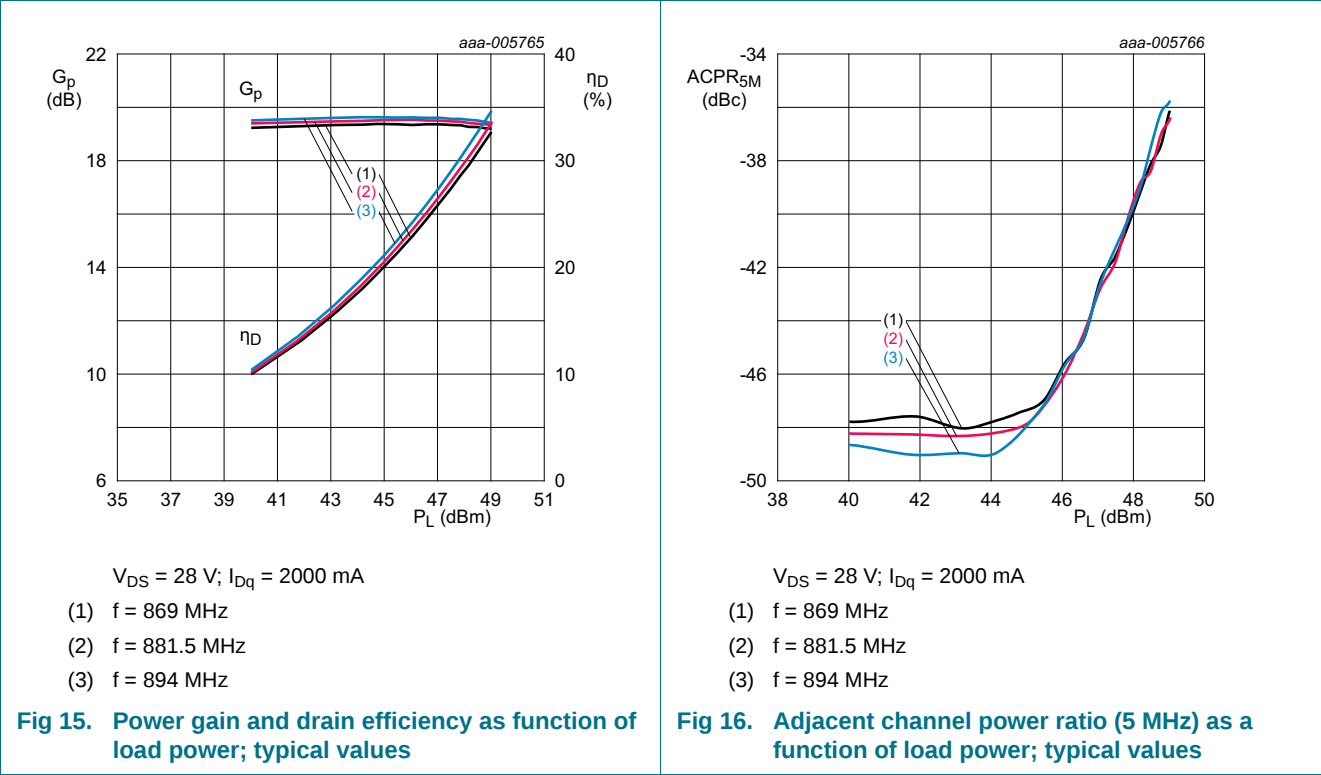


7.5.7 Gull-wing sample 1-carrier W-CDMA

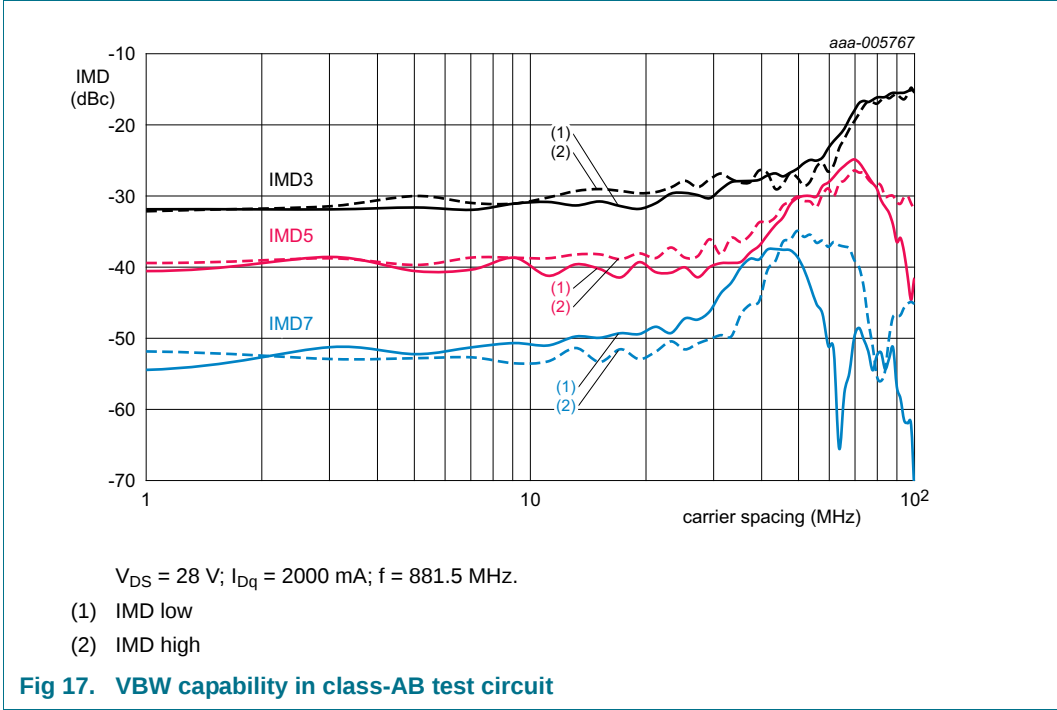




7.5.8 Gull-wing sample 2-carrier W-CDMA



7.5.9 2-Tone VBW



8. Package outline

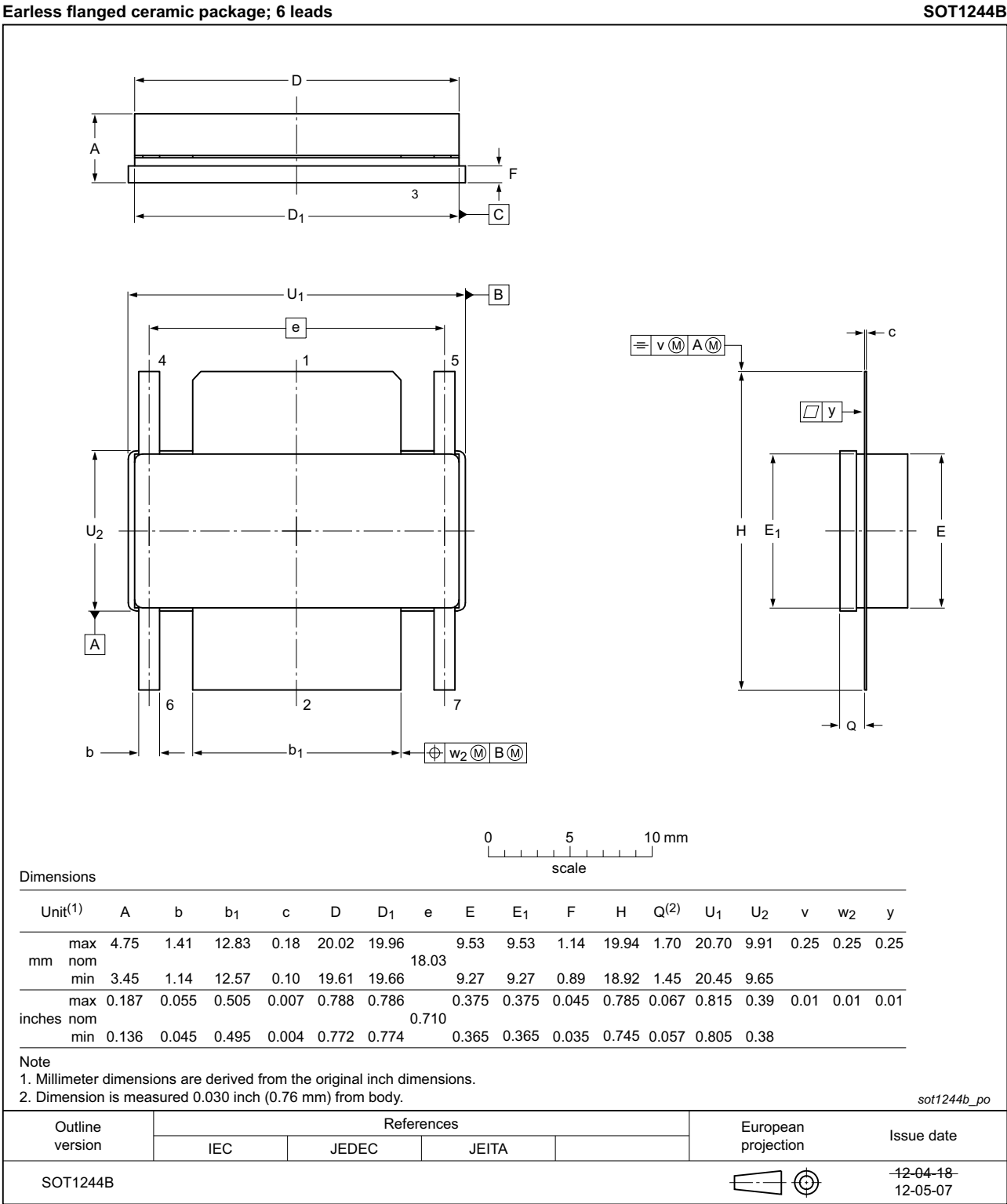


Fig 18. Package outline SOT1244B

Earless flanged ceramic package; 6 leads

SOT1244C

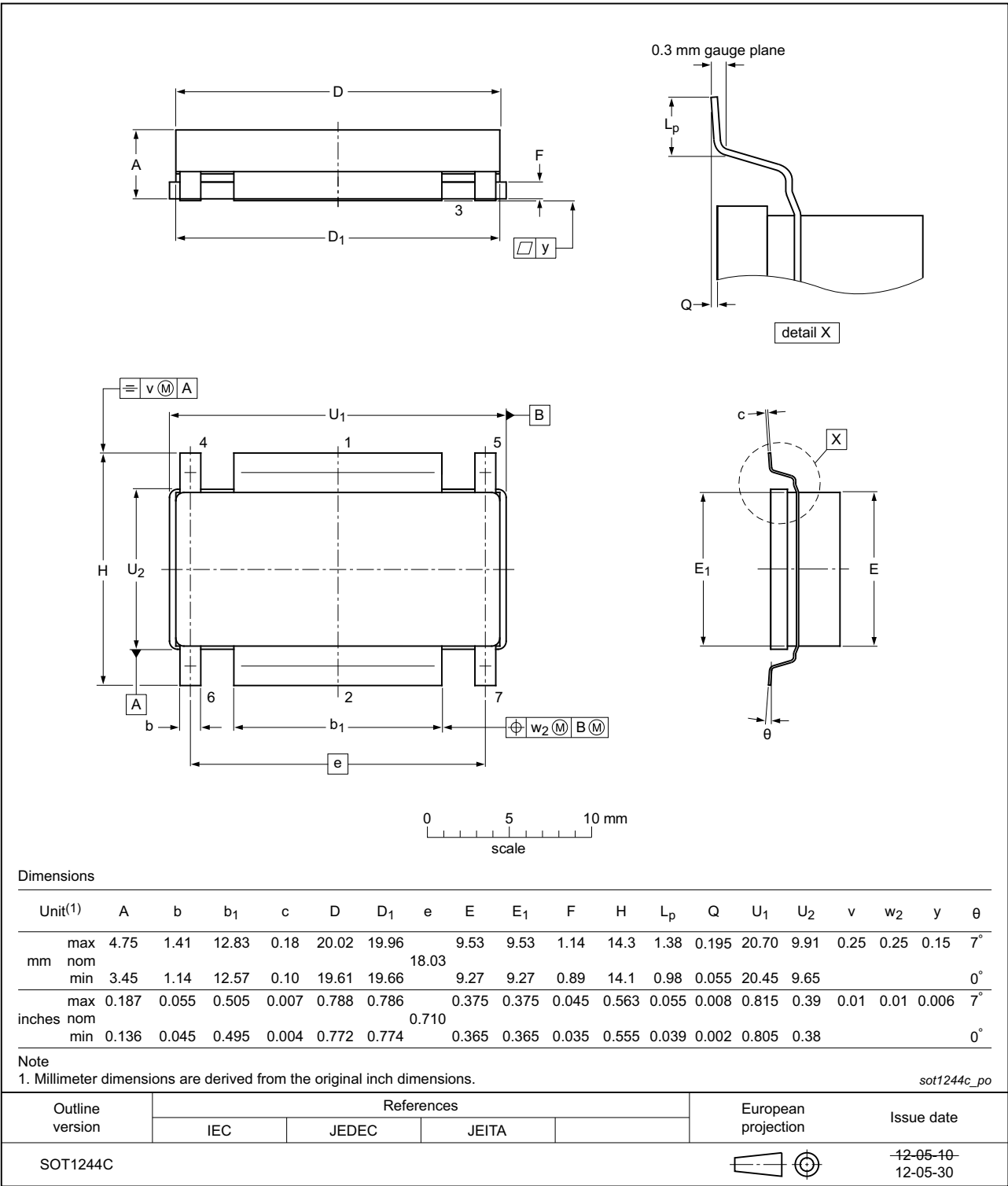


Fig 19. Package outline SOT1244C

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical Channel
ESD	ElectroStatic Discharge
IMD	InterModulation Distortion
LDMOS	Laterally Diffused Metal Oxide Semiconductor
PAR	Peak-to-Average Ratio
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF8G10LS-270V_8G10LS-270GV v.1	20121203	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

12.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

12.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

12.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

13. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

14. Contents

1	Product profile	1
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	1
2	Pinning information	2
3	Ordering information	2
4	Limiting values	2
5	Thermal characteristics	3
6	Characteristics	3
7	Test information	3
7.1	Ruggedness in class-AB operation	3
7.2	Impedance information	4
7.3	VBW in class-AB operation	4
7.4	Test circuit	5
7.5	Graphical data	6
7.5.1	Straight lead sample CW	6
7.5.2	Straight lead sample CW pulsed	6
7.5.3	Straight lead sample 1-carrier W-CDMA	7
7.5.4	Straight lead sample 2-carrier W-CDMA	8
7.5.5	Gull-wing sample CW	8
7.5.6	Gull-wing sample CW pulsed	9
7.5.7	Gull-wing sample 1-carrier W-CDMA	9
7.5.8	Gull-wing sample 2-carrier W-CDMA	10
7.5.9	2-Tone VBW	11
8	Package outline	12
9	Handling information	14
10	Abbreviations	14
11	Revision history	14
12	Legal information	15
12.1	Data sheet status	15
12.2	Definitions	15
12.3	Disclaimers	15
12.4	Trademarks	16
13	Contact information	16
14	Contents	17

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2012.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 3 December 2012

Document identifier: BLF8G10LS-270V_8G10LS-270GV