



128K x 16-Bit 3.3-V Asynchronous Magnetoresistive RAM

MR1A16A



44-TSOP
Case 924A-02

Introduction

The MR1A16A is a 2,097,152-bit magnetoresistive random access memory (MRAM) device organized as 131,072 words of 16 bits. The MR1A16A is equipped with chip enable (\overline{E}), write enable (\overline{W}), and output enable (\overline{G}) pins, allowing for significant system design flexibility without bus contention. Because the MR1A16A has separate byte-enable controls (\overline{LB} and \overline{UB}), individual bytes can be written and read.

MRAM is a nonvolatile memory technology that protects data in the event of power loss and does not require periodic refreshing. The MR1A16A is the ideal memory solution for applications that must permanently store and retrieve critical data quickly.

The MR1A16A is available in a 400-mil, 44-lead plastic small-outline TSOP type-II package with an industry-standard center power and ground SRAM pinout.

The MR1A16A is available in Commercial (0°C to 70°C), Industrial (-40°C to 85°C) and Extended (-40°C to 105°C) ambient temperature ranges.

Features

- Single 3.3-V power supply
- Commercial temperature range (0°C to 70°C), Industrial temperature range (-40°C to 85°C) and Extended temperature range (-40°C to 105°C)
- Symmetrical high-speed read and write with fast access time (35 ns)
- Flexible data bus control — 8 bit or 16 bit access
- Equal address and chip-enable access times
- Automatic data protection with low-voltage inhibit circuitry to prevent writes on power loss
- All inputs and outputs are transistor-transistor logic (TTL) compatible
- Fully static operation
- Full nonvolatile operation with 20 years minimum data retention

Device Pin Assignment

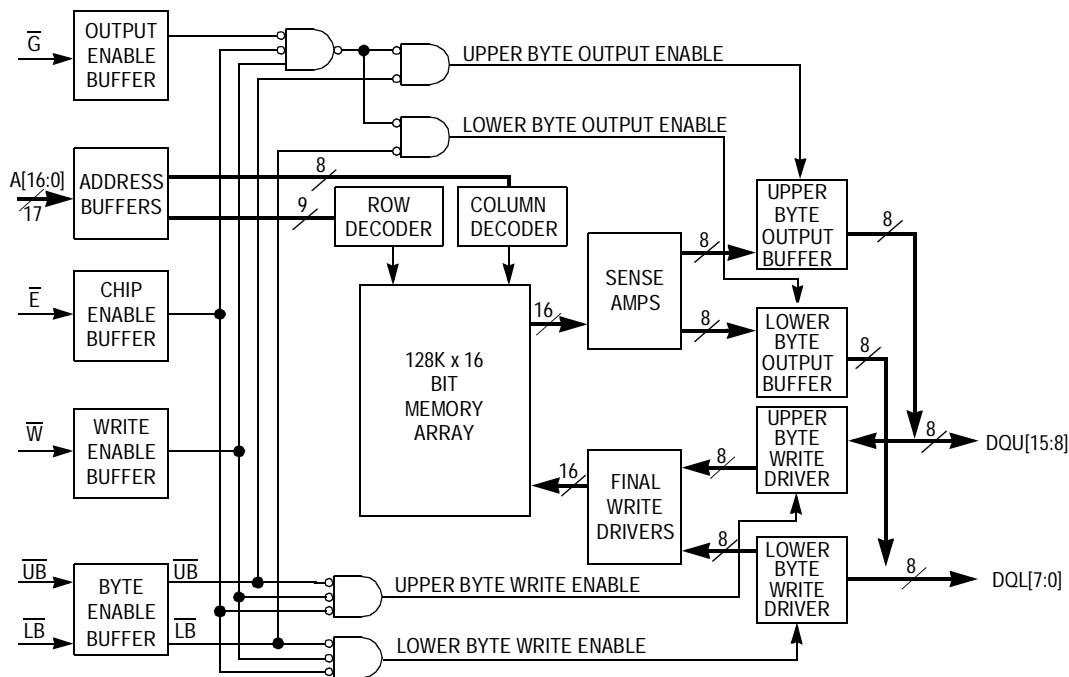


Figure 1. Block Diagram

Device Pin Assignment

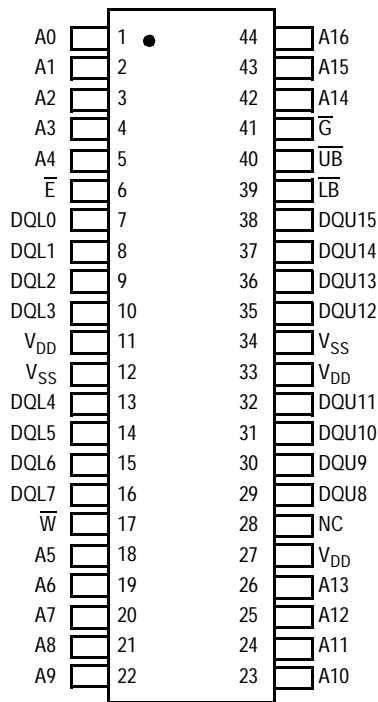


Table 1. Pin Functions

Signal Name	Function
A	Address input
\overline{E}	Chip enable
\overline{W}	Write enable
\overline{G}	Output enable
\overline{UB}	Upper byte select
\overline{LB}	Lower byte select
DQL	Data I/O, lower byte
DQU	Data I/O, upper byte
V_{DD}	Power supply
V_{SS}	Ground
NC	Do not connect this pin

Figure 2. MR1A16A in 44-Pin TSOP Type II Package

Table 2. Operating Modes

\overline{E}^1	\overline{G}^1	\overline{W}^1	\overline{LB}^1	\overline{UB}^1	Mode	V_{DD} Current	DQL[7:0] ²	DQU[15:8] ²
H	X	X	X	X	Not selected	I_{SB1}, I_{SB2}	Hi-Z	Hi-Z
L	H	H	X	X	Output disabled	I_{DDR}	Hi-Z	Hi-Z
L	X	X	H	H	Output disabled	I_{DDR}	Hi-Z	Hi-Z
L	L	H	L	H	Lower byte read	I_{DDR}	D_{Out}	Hi-Z
L	L	H	H	L	Upper byte read	I_{DDR}	Hi-Z	D_{Out}
L	L	H	L	L	Word read	I_{DDR}	D_{Out}	D_{Out}
L	X	L	L	H	Lower byte write	I_{DDW}	D_{In}	Hi-Z
L	X	L	H	L	Upper byte write	I_{DDW}	Hi-Z	D_{In}
L	X	L	L	L	Word write	I_{DDW}	D_{In}	D_{In}

NOTES:

¹ H = high, L = low, X = don't care² Hi-Z = high impedance

Electrical Specifications

Absolute Maximum Ratings

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the maximum field intensity specified in the maximum ratings.

Table 3. Absolute Maximum Ratings¹

Parameter	Symbol	Value	Unit
Supply voltage ²	V_{DD}	-0.5 to 4.0	V
Voltage on any pin ²	V_{In}	-0.5 to $V_{DD} + 0.5$	V
Output current per pin	I_{Out}	± 20	mA
Package power dissipation ³	P_D	0.600	W
Temperature under bias MR1A16AYS35 (Commercial) MR1A16ACYS35 (Industrial) MR1A16AVYS35 (Extended)	T_{Bias}	-10 to 85 -45 to 95 -45 to 110	°C
Storage temperature	T_{stg}	-55 to 150	°C
Lead temperature during solder (3 minute max)	T_{Lead}	260	°C
Maximum magnetic field during write MR1A16AYS35 (Commercial) MR1A16ACYS35 (Industrial) MR1A16AVYS35 (Extended)	H_{max_write}	15 25 25	Oe
Maximum magnetic field during read or standby	H_{max_read}	100	Oe

NOTES:

- ¹ Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.
- ² All voltages are referenced to V_{SS} .
- ³ Power dissipation capability depends on package characteristics and use environment.

Table 4. Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{DD}	3.0 ¹	3.3	3.6	V
Write inhibit voltage	V_{WI}	2.5	2.7	3.0 ¹	V
Input high voltage	V_{IH}	2.2	—	$V_{DD} + 0.3$ ²	V
Input low voltage	V_{IL}	-0.5 ³	—	0.8	V
Operating temperature MR1A16AYS35 (Commercial) MR1A16ACYS35 (Industrial) MR1A16AVYS35 (Extended)	T_A	0 -40 -40		70 85 105	°C

NOTES:

- ¹ After power up or if V_{DD} falls below V_{WI} , a waiting period of 2 ms must be observed, and \bar{E} and \bar{W} must remain high for 2 ms. Memory is designed to prevent writing for all input pin conditions if V_{DD} falls below minimum V_{WI} .
- ² $V_{IH} (max) = V_{DD} + 0.3 V_{dc}$; $V_{IH} (max) = V_{DD} + 2.0 V_{ac}$ (pulse width ≤ 10 ns) for $I \leq 20.0$ mA.
- ³ $V_{IL} (min) = -0.5 V_{dc}$; $V_{IL} (min) = -2.0 V_{ac}$ (pulse width ≤ 10 ns) for $I \leq 20.0$ mA.

Direct Current (dc)

Table 5. dc Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Input leakage current	$I_{lkg(I)}$	—	—	± 1	μA
Output leakage current	$I_{lkg(O)}$	—	—	± 1	μA
Output low voltage ($I_{OL} = +4 \text{ mA}$) ($I_{OL} = +100 \mu A$)	V_{OL}	—	—	0.4 $V_{SS} + 0.2$	V
Output high voltage ($I_{OH} = -4 \text{ mA}$) ($I_{OH} = -100 \text{ mA}$)	V_{OH}	2.4 $V_{DD} - 0.2$	—	—	V

Table 6. Power Supply Characteristics

Parameter	Symbol	Typ	Max	Unit
ac active supply current — read modes ¹ ($I_{Out} = 0 \text{ mA}$, $V_{DD} = \text{max}$)	I_{DDR}	55	80	mA
ac active supply current — write modes ¹ ($V_{DD} = \text{max}$) MR1A16AYS35 (Commercial) MR1A16ACYS35 (Industrial) MR1A16AVYS35 (Extended)	I_{DDW}	105 105 105	155 165 165	mA
ac standby current ($V_{DD} = \text{max}$, $\bar{E} = V_{IH}$) (no other restrictions on other inputs)	I_{SB1}	18	28	mA
CMOS standby current ($\bar{E} \geq V_{DD} - 0.2 \text{ V}$ and $V_{In} \leq V_{SS} + 0.2 \text{ V}$ or $\geq V_{DD} - 0.2 \text{ V}$) ($V_{DD} = \text{max}$, $f = 0 \text{ MHz}$)	I_{SB2}	9	12	mA

NOTES:

¹ All active current measurements are measured with one address transition per cycle.Table 7. Capacitance¹

Parameter	Symbol	Typ	Max	Unit
Address input capacitance	C_{In}	—	6	pF
Control input capacitance	C_{In}	—	6	pF
Input/output capacitance	$C_{I/O}$	—	8	pF

NOTES:

¹ $f = 1.0 \text{ MHz}$, $dV = 3.0 \text{ V}$, $T_A = 25^\circ\text{C}$, periodically sampled rather than 100% tested.

Table 8. ac Measurement Conditions

Parameter	Value
Logic input timing measurement reference level	1.5 V
Logic output timing measurement reference level	1.5 V
Logic input pulse levels	0 or 3.0 V
Input rise/fall time	2 ns
Output load for low and high impedance parameters	See Figure 3A
Output load for all other timing parameters	See Figure 3B

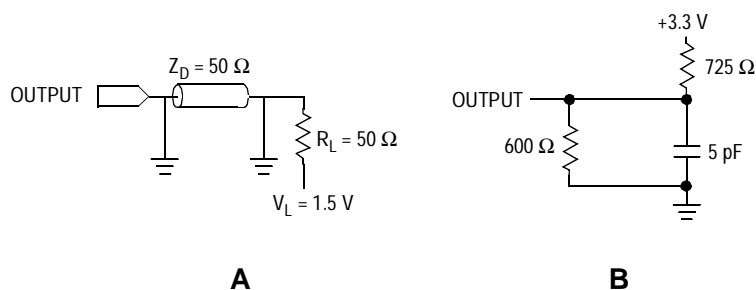


Figure 3. Output Load for ac Test

This page is intentionally blank.

Timing Specifications

Read Mode

Table 9. Read Cycle Timing^{1, 2}

Parameter	Symbol	Min	Max	Unit
Read cycle time	t_{AVAV}	35	—	ns
Address access time	t_{AVQV}	—	35	ns
Enable access time ³	t_{ELQV}	—	35	ns
Output enable access time	t_{GLQV}	—	15	ns
Byte enable access time	t_{BLQV}	—	15	ns
Output hold from address change	t_{AXQX}	3	—	ns
Enable low to output active ^{4, 5}	t_{ELQX}	3	—	ns
Output enable low to output active ^{4, 5}	t_{GLQX}	0	—	ns
Byte enable low to output active ^{4, 5}	t_{BLQX}	0	—	ns
Enable high to output Hi-Z ^{4, 5}	t_{EHQZ}	0	15	ns
Output enable high to output Hi-Z ^{4, 5}	t_{GHQZ}	0	10	ns
Byte high to output Hi-Z ^{4, 5}	t_{BHQZ}	0	10	ns

NOTES:

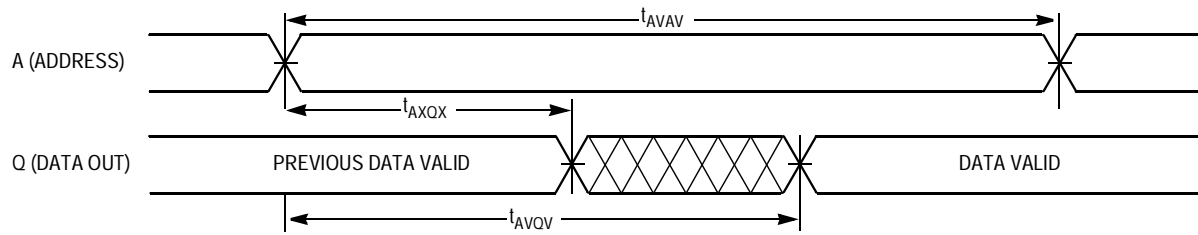
¹ \overline{W} is high for read cycle.

² Due to product sensitivities to noise, power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read and write cycles.

³ Addresses valid before or at the same time \overline{E} goes low.

⁴ This parameter is sampled and not 100% tested.

⁵ Transition is measured ± 200 mV from steady-state voltage.



NOTES:

Device is continuously selected ($\overline{E} \leq V_{IL}$, $\overline{G} \leq V_{IL}$).

Figure 4. Read Cycle 1

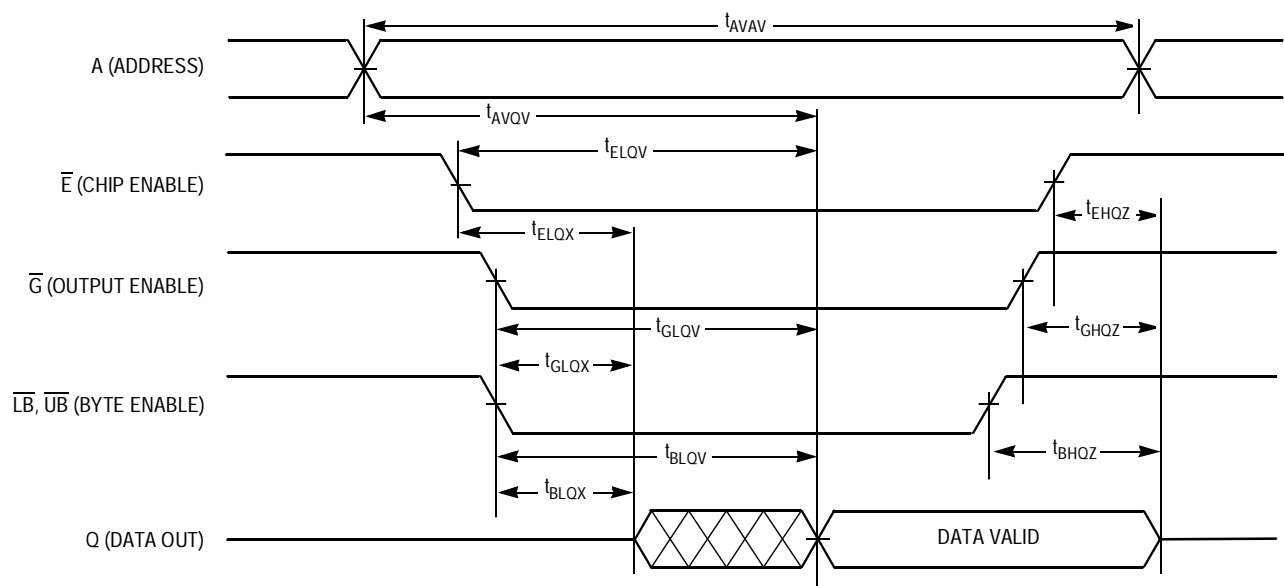


Figure 5. Read Cycle 2

Write Mode

Table 10. Write Cycle Timing 1 (\overline{W} Controlled)^{1, 2, 3, 4, 5}

Parameter	Symbol	Min	Max	Unit
Write cycle time ⁶	t_{AVAV}	35	—	ns
Address set-up time	t_{AVWL}	0	—	ns
Address valid to end of write (\overline{G} high)	t_{AVWH}	18	—	ns
Address valid to end of write (\overline{G} low)	t_{AVWH}	20	—	ns
Write pulse width (\overline{G} high)	t_{WLWH} t_{WLEH}	15	—	ns
Write pulse width (\overline{G} low)	t_{WLWH} t_{WLEH}	15	—	ns
Data valid to end of write	t_{DVWH}	10	—	ns
Data hold time	t_{WHDx}	0	—	ns
Write low to data Hi-Z ^{7, 8, 9}	t_{WLQZ}	0	12	ns
Write high to output active ^{7, 8, 9}	t_{WHQX}	3	—	ns
Write recovery time	t_{WHAX}	12	—	ns

NOTES:

- ¹ A write occurs during the overlap of \overline{E} low and \overline{W} low.
- ² Due to product sensitivities to noise, power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles.
- ³ If \overline{G} goes low at the same time or after \overline{W} goes low, the output will remain in a high-impedance state.
- ⁴ After \overline{W} , \overline{E} , or $\overline{UB/LB}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns.
- ⁵ The minimum time between \overline{E} being asserted low in one cycle to \overline{E} being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
- ⁶ All write cycle timings are referenced from the last valid address to the first transition address.
- ⁷ This parameter is sampled and not 100% tested.
- ⁸ Transition is measured ± 200 mV from steady-state voltage.
- ⁹ At any given voltage or temperature, $t_{WLQZ} \text{ max} < t_{WHQX} \text{ min}$.

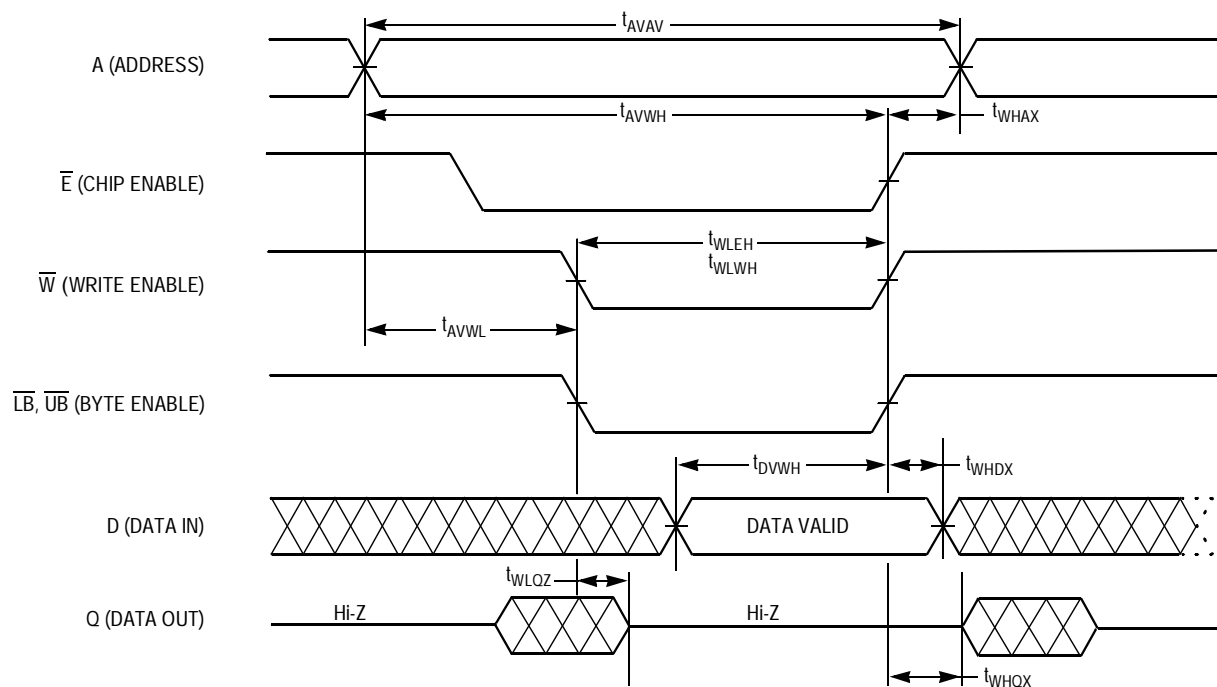


Figure 6. Write Cycle 1 (\overline{W} Controlled)

Table 11. Write Cycle Timing 2 (\overline{E} Controlled)^{1, 2, 3, 4, 5}

Parameter	Symbol	Min	Max	Unit
Write cycle time ⁶	t_{AVAV}	35	—	ns
Address set-up time	t_{AVEL}	0	—	ns
Address valid to end of write (\overline{G} high)	t_{AVEH}	18	—	ns
Address valid to end of write (\overline{G} low)	t_{AVEH}	20	—	ns
Enable to end of write (\overline{G} high)	t_{ELEH} t_{ELWH}	15	—	ns
Enable to end of write (\overline{G} low) ^{7, 8}	t_{ELEH} t_{ELWH}	15	—	ns
Data valid to end of write	t_{DVEH}	10	—	ns
Data hold time	t_{EHDX}	0	—	ns
Write recovery time	t_{EHAX}	12	—	ns

NOTES:

- ¹ A write occurs during the overlap of \overline{E} low and \overline{W} low.
- ² Due to product sensitivities to noise, power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles.
- ³ If \overline{G} goes low at the same time or after \overline{W} goes low, the output will remain in a high-impedance state.
- ⁴ After \overline{W} , \overline{E} , or $\overline{UB/LB}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns.
- ⁵ The minimum time between \overline{E} being asserted low in one cycle to \overline{E} being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
- ⁶ All write cycle timings are referenced from the last valid address to the first transition address.
- ⁷ If \overline{E} goes low at the same time or after \overline{W} goes low, the output will remain in a high-impedance state.
- ⁸ If \overline{E} goes high at the same time or before \overline{W} goes high, the output will remain in a high-impedance state.

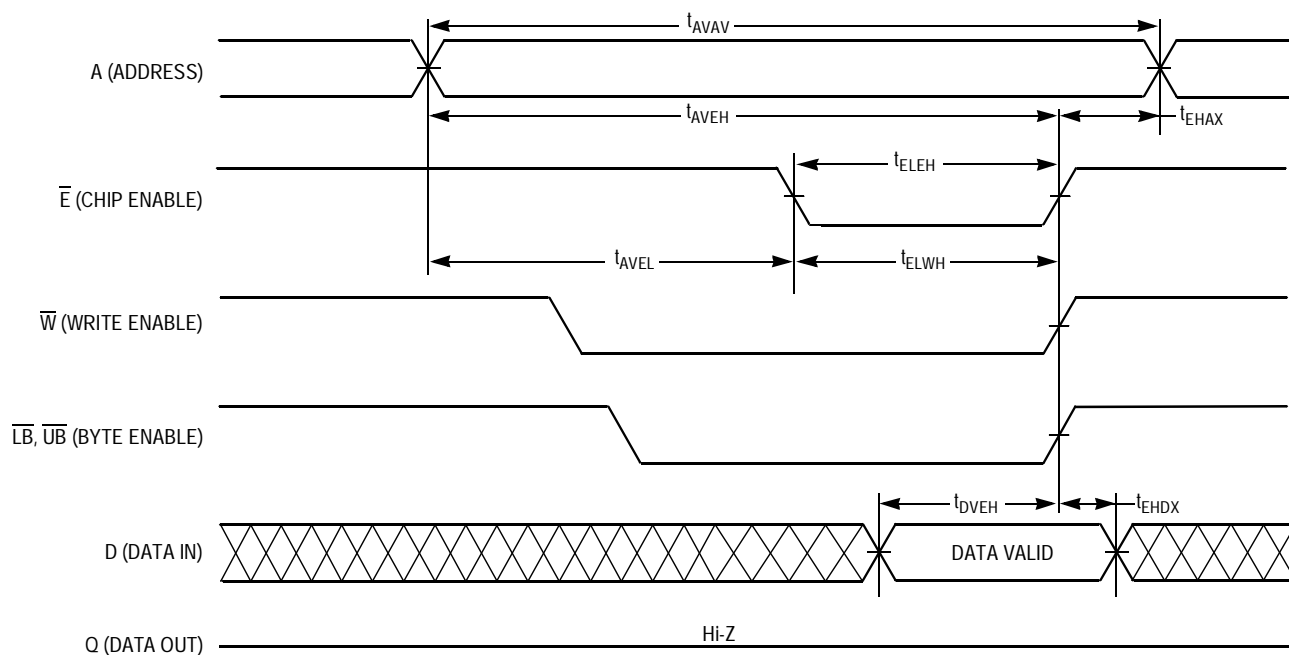


Figure 7. Write Cycle 2 (\overline{E} Controlled)

Table 12. Write Cycle Timing 3 ($\overline{\text{LB}}/\overline{\text{UB}}$ Controlled)^{1, 2, 3, 4, 5, 6}

Parameter	Symbol	Min	Max	Unit
Write cycle time ⁷	t_{AVAV}	35	—	ns
Address set-up time	t_{AVBL}	0	—	ns
Address valid to end of write ($\overline{\text{G}}$ high)	t_{AVBH}	18	—	ns
Address valid to end of write ($\overline{\text{G}}$ low)	t_{AVBH}	20	—	ns
Byte pulse width ($\overline{\text{G}}$ high)	t_{BLEH} t_{BLWH}	15	—	ns
Byte pulse width ($\overline{\text{G}}$ low)	t_{BLEH} t_{BLWH}	15	—	ns
Data valid to end of write	t_{DVBH}	10	—	ns
Data hold time	t_{BHDX}	0	—	ns
Write recovery time	t_{BHAX}	12	—	ns

NOTES:

- ¹ A write occurs during the overlap of $\overline{\text{E}}$ low and $\overline{\text{W}}$ low.
- ² Due to product sensitivities to noise, power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles.
- ³ If $\overline{\text{G}}$ goes low at the same time or after $\overline{\text{W}}$ goes low, the output will remain in a high-impedance state.
- ⁴ After $\overline{\text{W}}$, $\overline{\text{E}}$, or $\overline{\text{UB}}/\overline{\text{LB}}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns.
- ⁵ If both byte control signals are asserted, the two signals must have no more than 2 ns skew between them.
- ⁶ The minimum time between $\overline{\text{E}}$ being asserted low in one cycle to $\overline{\text{E}}$ being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
- ⁷ All write cycle timings are referenced from the last valid address to the first transition address.

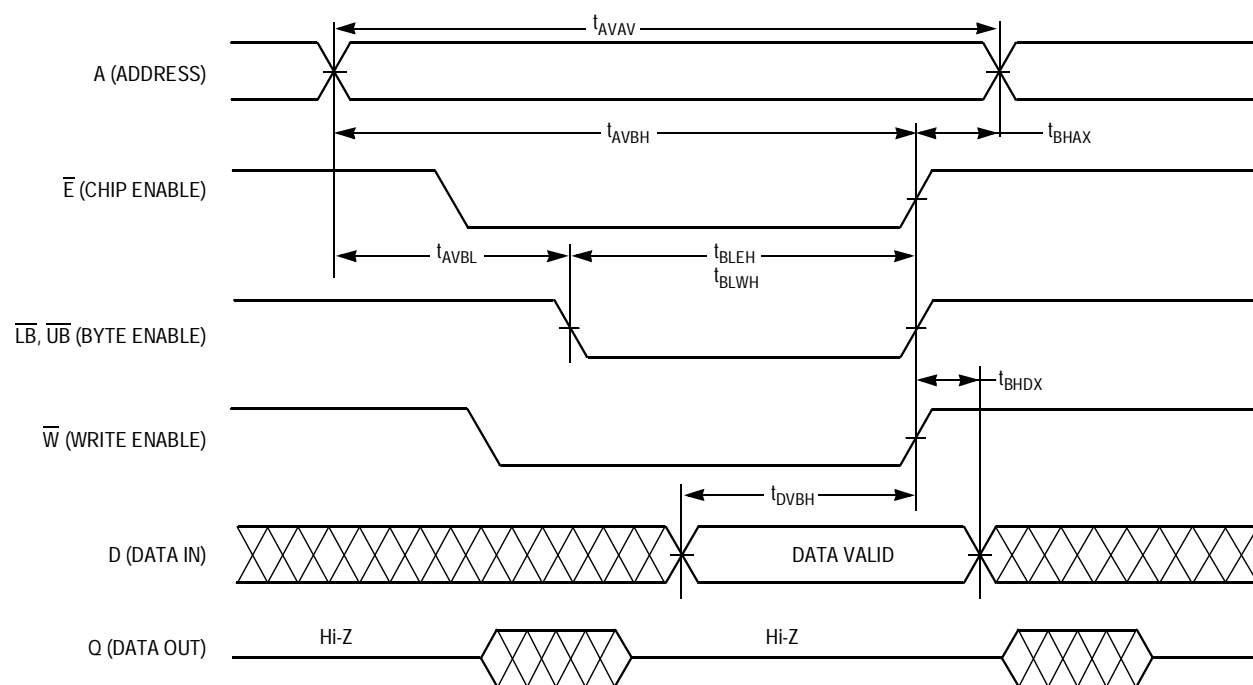


Figure 8. Write Cycle 3 ($\overline{LB}/\overline{UB}$ Controlled)

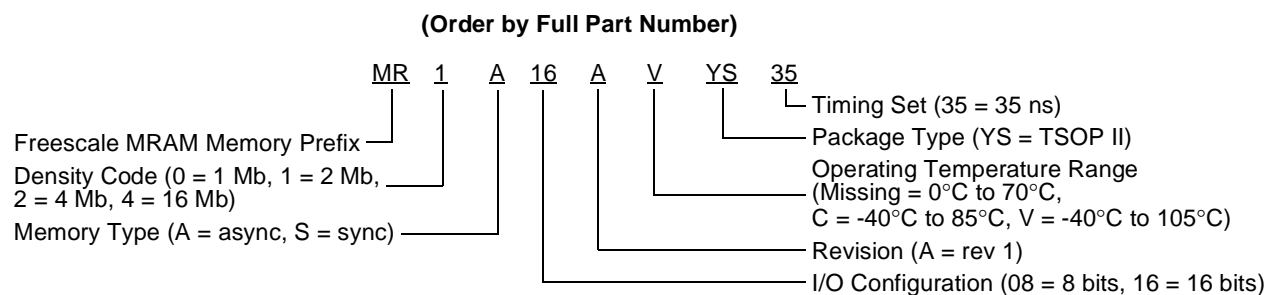
Ordering Information

This product is available in Commercial, Industrial, and Extended temperature versions.

Freescale's semiconductor products can be classified into the following tiers: "Commercial", "Industrial" and "Extended." A product should only be used in applications appropriate to its tier as shown below. For questions, please contact a Freescale sales representative.

- **Commercial** — Typically 5 year applications - personal computers, PDA's, portable telecom products, consumer electronics, etc.
- **Industrial, Extended** — Typically 10 year applications - installed telecom equipment, workstations, servers, etc. These products can also be used in Commercial applications.

Part Numbering System



Package Information

Table 13. Package Information

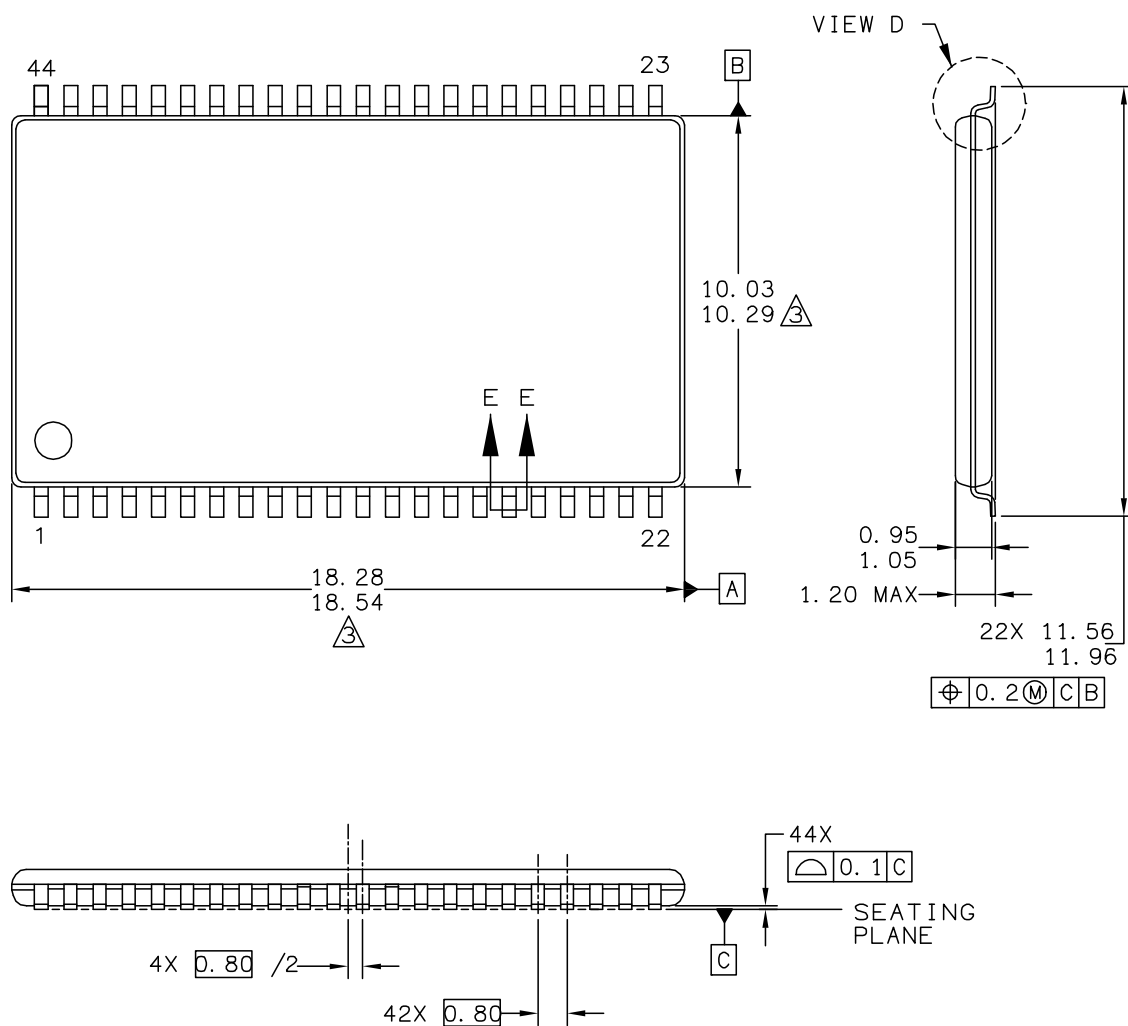
Device	Pin Count	Package Type	Designator	Case No.	Document No.	RoHS Compliant
MR1A16A	44	TSOP Type II	YS	924A-02	98ASS23673W	True

Revision History**Revision History**

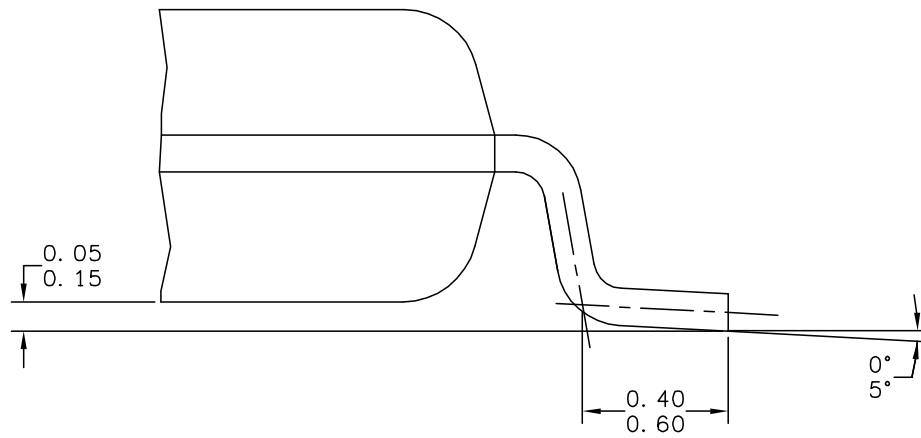
Rev	Date	Description of Change
1	10 Aug 2007	Initial public release version.
2	21 Sep 2007	Table 6: Applied values to TBD's in IDD specifications.
3	12 Nov 2007	Table 2: Changed IDDA to IDDR or IDDW.

Mechanical Drawing

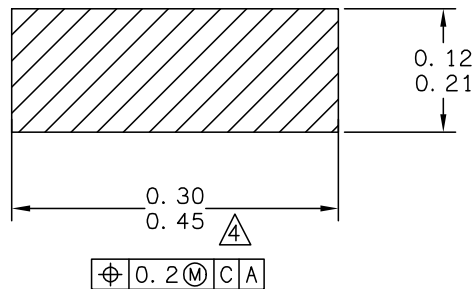
The following pages detail the package available to MR1A16A.



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 44 LEAD TSOP, TYPE II, .400 WIDE	DOCUMENT NO: 98ASS23673W		REV: C
	CASE NUMBER: 924A-02		17 MAY 2005
	STANDARD: NON-JEDEC		



VIEW D
ROTATED 90° CW



SECTION E-E
40 PLACES

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 44 LEAD TSOP, TYPE II, .400 WIDE	DOCUMENT NO: 98ASS23673W		REV: C
	CASE NUMBER: 924A-02		17 MAY 2005
	STANDARD: NON-JEDEC		

NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M – 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION.
ALLOWABLE MOLD PROTRUSION IS 0.15 PER SIDE.
4. DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSIONS.
DAM BAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH
TO EXCEED 0.58.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 44 LEAD TSOP, TYPE II, .400 WIDE	DOCUMENT NO: 98ASS23673W		REV: C
	CASE NUMBER: 924A-02		17 MAY 2005
	STANDARD: NON-JEDEC		

How to Reach Us:

USA/Europe/Locations not listed:

Freescale Semiconductor Literature Distribution
P.O. Box 5405, Denver, Colorado 80217
1-800-521-6274 or 480-768-2130

Japan:

Freescale Semiconductor Japan Ltd.
SPS, Technical Information Center
3-20-1, Minami-Azabu
Minato-ku
Tokyo 106-8573, Japan
81-3-3440-3569

Asia/Pacific:

Freescale Semiconductor H.K. Ltd.
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T. Hong Kong
852-26668334

Learn More:

For more information about Freescale
Semiconductor products, please visit
<http://www.freescale.com>

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.
© Freescale Semiconductor, Inc. 2007.