73M1866B/73M1966B
MicroDAA™ with PCM Highway

Simplifying System Integration™

DATA SHEET

DS_1x66B_001 **April 2010**

DESCRIPTION

The 73M1866B and 73M1966B use the Teridian patented Data Access Arrangement function (MicroDAA®) designed exclusively for Foreign-Exchange-Office (FXO) in Voice-over-IP (VoIP) applications. These devices provide much of the circuitry required to connect PCM formatted voice channels to a PSTN via a two-wire twisted pair interface. The package options provide the necessary functional programmability and protection required for easy worldwide homologation.

The family of devices consists of the 73M1866B and the 73M1966B. The 73M1866B MicroDAA is the world's first single-package silicon Data Access Arrangement (DAA). Suitable applications for the 73M1866B and 73M1966B devices include VoIP equipment that must provide connectivity to the PSTN for purposes of guaranteeing emergency service calling, redundancy for supplementary connectivity for voice, and maintenance services.

The 73M1966B device set consists of the 73M1906B Host-Side Device that provides digital data, control interfaces and power to the 73M1916 Line-Side Device.

These devices are based on an innovative and patented technology, which sets new standards in reliability and cost. A small pulse transformer forms a digital isolation barrier, transferring both power and data to the PSTN line-side components. This method results in reliable operation in the presence of EMI and a tolerance to line voltage variations by providing power to the Line-Side Device across the barrier. The devices also support the ability to provide up to an additional +6 dB of analog gain to the line-side transmit and +3 dB in the receive signal paths. The device supports transmit and receive digital gain ranging from –18 dB to +7.375 dB by increments of 0.125 dB.

The digital side provides a PCM highway interface with automatic clock rate detection. With an 8-kHz sampling rate, the devices include an ITU-T G.711 compliant codec with selectable µ-law and A-law companding modes. The devices also provide a 16-bit linear mode, which is suitable for interfacing with wide band codecs, as well as 16 kHz sampling rate. Device control is performed over an SPI interface. The SPI supports daisy chain operation.

Through its PCM interface, the 73M1966B can be connected to other PCM enabled devices such as POTS codecs, ISDN codecs, E1/T1 framers, etc.

Additional DAA functions supported by the 73M1x66B devices include a call progress monitor, Caller ID Type I and II, ring detection, pulse dialing, billing tone detection and polarity reversal detection.

APPLICATIONS

- Computer Telephony
- VOIP Equipment
- PBX Systems
- Internet Appliances
- Voicemail Systems
- POTS Termination Equipment

FEATURES

- PCM highway data interface supporting both slave and master modes
- PCM highway interface supporting both E-1 and T-1
- SPI control interface, with daisy chain support for up to 16 devices
- Designed to meet global DAA compliance FCC, ETSI ES 203 021-2, JATE and other PTT standards.
- 8 kHz and 16 kHz sample rates
- 16-bit linear mode
- TX and RX gains adjustable in 0.125 dB increments
- µ-Law, A-law *ITU-T Recommendation G.711* compliant compander operation
- Automatic clock rate detection
- Low power modes
- Polarity Reversal detection
- GPIO for user-configurable I/O ports
- Call Progress Monitor
- Isolation up to 6 kV
- THD -80 dB
- 5 V tolerant I/O on selected pins
- 3.0 V – 3.6 V operating voltage
- Industrial temperature range (-40 °C to +85 °C)
- 5x5 mm 32-pin QFN or 20-pin TSSOP packages
- RoHS compliant (6/6) lead-free package

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1 Introduction

The 73M1966B is a two-device chip set that provides embedded FXO functionality by connecting a PCM interface to a voice-band PSTN. The device set supports *ITU-T Recommendation G.711* µ-law and A-law companding, and also a 16-bit linear mode. High-voltage isolation is provided by the physical separation of the Host-Side (73M19106) and Line-Side (73M1916) Devices. The Host-Side and the Line-Side Devices communicate with each other using a single pulse transformer. A few low-cost components complete the DAA interface to the network. The pulse transformer transmits encoded digital data rather than analog signals as with other transformer designs. Data is transmitted and received without the usual degradation from common mode noise and magnetic coupling typical of other capacitive and voice-band transformer techniques. The data stream passed between the Host-Side and Line-Side Devices includes the media stream data, control, status, and clocking information.

This data sheet describes both the 73M1966B and 73M1866B, which will be collectively referred to as the 73M1x66B in this document.

A unique capability of the 73M1x66B Host Side device (73M1906B) is its ability to provide power to the 73M1x66B Line Side device (73M1916) via the pulse transformer.

The 73M1906B exchanges control and status information with the host using the SPI interface, while the PCM encoded media streams connect with other PCM-enabled devices using the PCM highway bus interface.

Figure 1 shows a reference block diagram of the 73M1x66B connected by a pulse transformer and example external line interface circuitry shown for clarification.

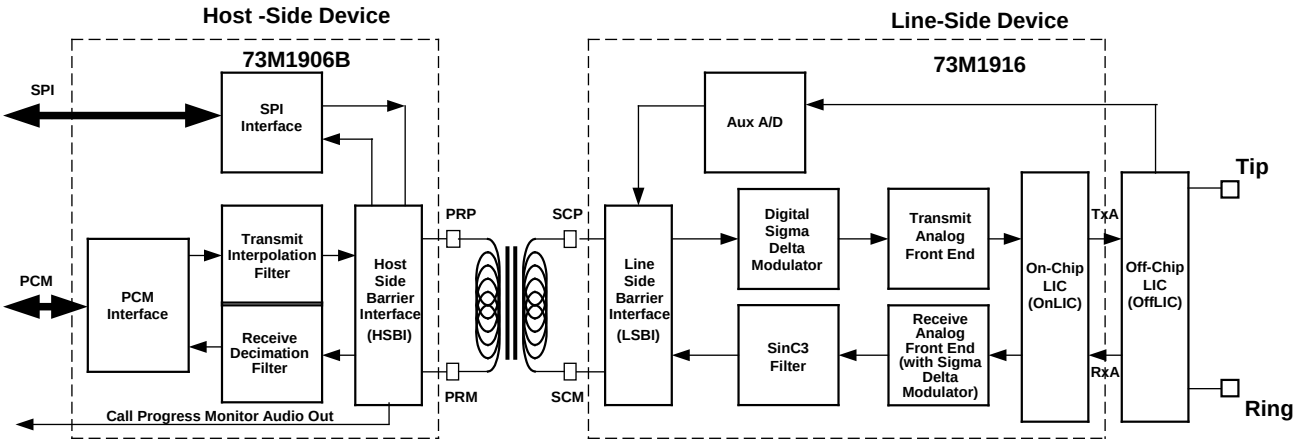


Figure 1: Simple 73M1x66B Reference Block Diagram

The Host-Side Device (73M1906B) consists of:

1. PCM Interface Block (PCM)
2. SPI Interface Block (SPI)
3. Transmit Interpolation Filter
4. Receive Decimation Filter
5. Host-Side Barrier Interface Circuit (HSBI)

The Line-Side Device (73M1916) consists of:

1. Digital Sigma Delta Modulator
2. Transmit Analog Front End
3. Receive Analog Front End including Sigma Delta Modulator
4. $Sinc^3$ Filter (Sinc3)
5. On-chip Line Interface Circuit
6. Line-Side Barrier Interface Circuit (LSBI)

Received data from a host connected to the PCM bus is interpolated from the sampling frequency of 8 kHz or 16 kHz (for PCM encoded streams) to twice the sampling frequency. The control information is multiplexed with the audio stream signals and transmitted across the isolation barrier to the Line-Side Device. In the Line-Side Device, the two streams are separated and the audio signal is converted to analog for transmission to the line.

An audio stream received at the analog line input pins is converted to a serialized data stream and, along with status information such as line condition from the Auxiliary Analog to Digital Converter, is transmitted over the isolation barrier using the pulse transformer. The data is extracted with status information being transmitted on the SPI. The audio stream is sent to a host using the PCM bus.

The 73M1x66B is an enhanced version of the 73M1966 that includes the additional functionality of finer resolution of transmit and receive gain, receiver DC offset subtraction and support for T-1 PCLK frequencies.

2 Pinout

The 73M1906B and the 73M1916 are supplied as 20-pin TSSOP packages and as 32-pin QFN packages.

2.1 73M1906B 20-Pin TSSOP Pinout

Figure 2 shows the 73M1906B 20-pin TSSOP pinout.

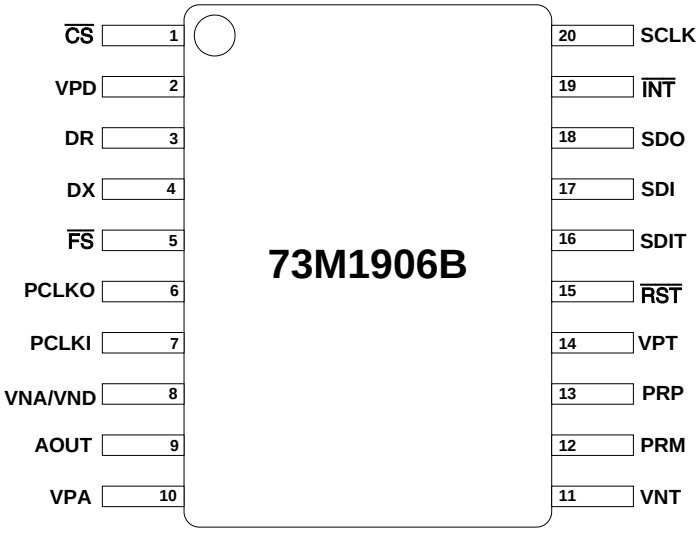


Figure 2: 73M1906B 20-Pin TSSOP Pinout

Table 1 describes the pin functions for the device. Decoupling capacitors on the power supplies should be included for each pair of supply pins.

Table 1: 73M1906B 20-Pin TSSOP Pin Definitions

Pin Number	Pin Name	Type	Description
1	$\overline{CS}$	I	SPI chip select (active low)
2	VPD	PWRI	Positive digital supply
3	DR	I	PCM transmit data sent to the D to A
4	DX	O	PCM received data from the A to D
5	$\overline{FS}$	I/O	PCM frame synchronization
6	PCLKO	O	PCM clock output
7	PCLKI	I	PCM clock in
8	VNA/VND	GND	Negative analog/digital ground
9	AOUT	O	Audio output – must be buffered for speaker
10	VPA	PWRI	Positive analog supply
11	VNT	GND	Negative transformer supply
12	PRM	I/O	Transformer primary minus
13	PRP	I/O	Transformer primary plus
14	VPT	PWRI	Positive transformer supply
15	$\overline{RST}$	I	Hardware reset (active low)
16	SDIT	O	SPI data out for daisy chain mode
17	SDI	I	SPI data in
18	SDO	O	SPI data out
19	$\overline{INT}$	O	Interrupt / ring detect (active low – open drain)
20	SCLK	I	SPI clock

2.2 73M1916 20-Pin TSSOP Pinout

Figure 3 shows the 73M1916 20-pin TSSOP pinout.

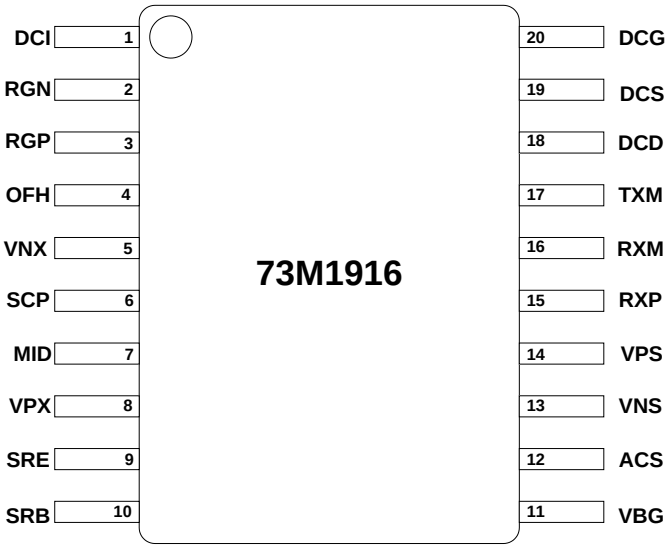


Figure 3: 73M1916 20-Pin TSSOP Pinout

Table 2 describes the pin functions for the device. Decoupling capacitors on the power supplies should be included for each pair of supply pins.

Table 2: 73M1916 20-Pin TSSOP Pin Definitions

Pin Number	Pin Name	Type	Description
1	DCI	I	DC loop input
2	RGN	I	Ring detect negative voltage input
3	RGP	I	Ring detect positive voltage input
4	OFH	O	Off-hook control
5	VNX	GND	Negative supply voltage (line side of the barrier)
6	SCP	I/O	Positive side of the secondary pulse transformer winding
7	MID	I/O	Charge pump midpoint
8	VPX	PWR	Supply from the barrier
9	SRE	I	Voltage regulator sense
10	SRB	O	Voltage regulator drive
11	VBG	O	VBG bypass, connect to 0.1 µF capacitor to VNS
12	ACS	I	AC current sense
13	VNS	GND	Analog negative supply voltage
14	VPS	PWRO	Analog positive supply voltage (output)
15	RXP	I	Receive plus – signal input
16	RXM	I	Receive minus – signal input
17	TXM	O	Transmit minus – transhybrid cancellation output
18	DCD	O	DC loop output
19	DCS	I	DC loop current sense
20	DCG	O	DC loop control

2.3 73M1906B 32-Pin QFN Pinout

Figure 4 shows the 73M1906B 32-pin QFN pinout.

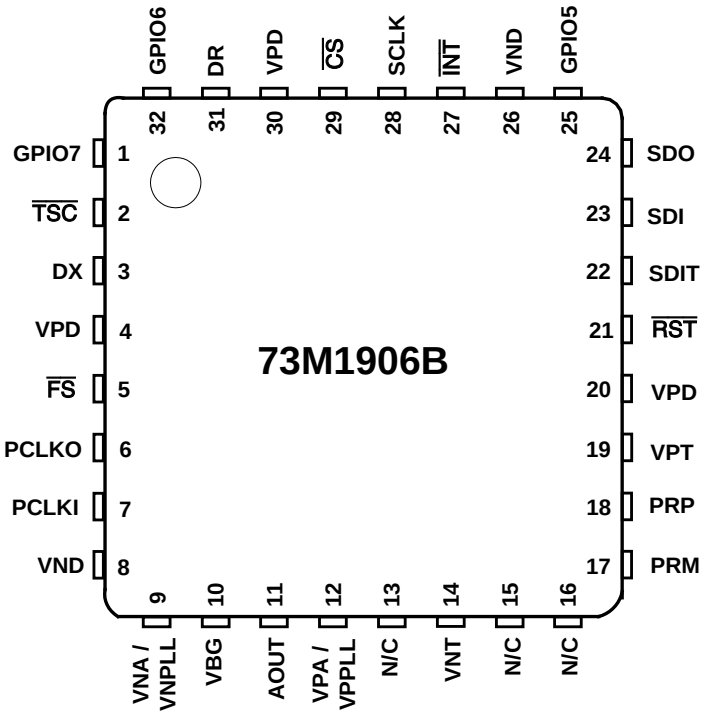


Figure 4: 73M1906B 32-Pin QFN Pinout

Table 3 describes the pin functions for the device. Decoupling capacitors on the power supplies should be included for each pair of supply pins.

Table 3: 73M1906B 32-Pin QFN Pin Definitions

Pin Number	Pin Name	Type	Description
1	GPIO7	I/O	Configurable input/output pin
2	$\overline{TSC}$	O	PCM time slot control (active low)
3	DX	O	PCM received data from the A to D
4	VPD	PWR	Positive digital supply
5	$\overline{FS}$	I/O	PCM frame synchronization
6	PCLKO	O	PCM clock output
7	PCLKI	I	PCM clock in
8	VND	GND	Negative digital ground
9	VNA/VNPLL	GND	Negative analog/PLL ground
10	VBG	O	Band gap voltage reference monitor
11	AOUT	O	Audio output – must be buffered for speaker
12	VPA/VPPLL	PWR	Positive analog/PLL supply
13	N/C	–	No connect
14	VNT	GND	Negative transformer supply
15	N/C	–	No connect
16	N/C	–	No connect

Pin Number	Pin Name	Type	Description
17	PRM	I/O	Transformer primary minus
18	PRP	I/O	Transformer primary plus
19	VPT	PWR	Positive transformer supply
20	VPD	PWR	Positive digital supply
21	$\overline{\text{RST}}$	I	Hardware reset (active low)
22	SDIT	O	SPI data out for daisy-chain mode
23	SDI	I	SPI data in
24	SDO	O	SPI data out
25	GPIO5	I/O	Configurable input/output pin
26	VND	GND	Negative digital ground
27	$\overline{\text{INT}}$	O	Interrupt / ring detect (active low – open drain)
28	SCLK	I	SPI clock
29	$\overline{\text{CS}}$	I	SPI chip select (active low)
30	VPD	PWR	Positive digital supply
31	DR	I	PCM transmit data sent to the D to A
32	GPIO6	I/O	Configurable input/output pin

2.4 73M1916 32-Pin QFN Pinout

Figure 5 shows the 73M1916 32-pin QFN pinout.

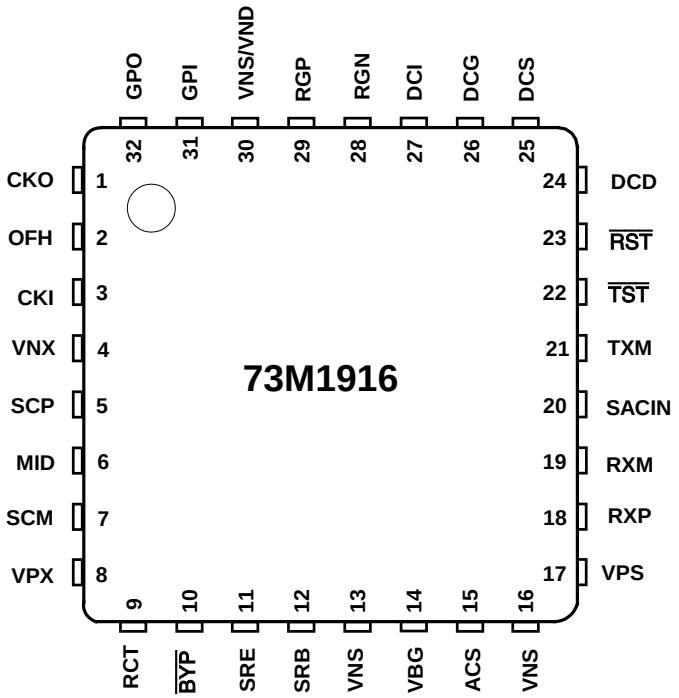


Figure 5: 73M1916 32-Pin QFN Pinout

Table 4 describes the pin functions for the device. Decoupling capacitors on the power supplies should be included for each pair of supply pins.

Table 4: 73M1916 32-Pin QFN Pin Definitions

Pin Number	Pin Name	Type	Description
1	CKO	O	Test point for recovered clock
2	OFH	O	Off-hook control
3	CKI	I	Test input for clock
4	VNX	GND	Negative supply voltage
5	SCP	I/O	Positive side of the secondary pulse transformer winding
6	MID	I/O	Charge pump midpoint
7	SCM	I/O	Negative side of the secondary pulse transformer winding
8	VPX	PWR	Supply from the barrier
9	RCT	I	External rectification – disables internal rectifier when low, leave open
10	$\overline{\text{BYP}}$	I	Test pin, leave open
11	SRE	I	Voltage regulator sense
12	SRB	O	Voltage regulator drive
13	VNS	GND	Digital negative supply voltage
14	VBG	O	VBG bypass, connect to 0.1µF capacitor to VNS
15	ACS	I	AC current sense

Pin Number	Pin Name	Type	Description
16	VNS	GND	Analog negative supply voltage
17	VPS	PWRO	Analog positive supply voltage (output)
18	RXP	I	Receive plus – signal input
19	RXM	I	Receive minus – signal input
20	SACIN	I	Caller ID mode AC impedance connection
21	TXM	O	Transmit Minus – transhybrid cancellation output
22	$\overline{\text{TST}}$	I	Factory test mode, leave open
23	$\overline{\text{RST}}$	I	Resets the control registers to default – weakly pulled high
24	DCD	O	DC loop output
25	DCS	I	DC loop current sense
26	DCG	O	DC loop control
27	DCI	I	DC loop input
28	RGN	I	Ring detect negative voltage input
29	RGP	I	Ring detect positive voltage input
30	VNS	GND	Negative supply voltage (line side of the barrier)
31	GPI	I	General purpose input (test pin)
32	GPO	O	General purpose output (test pin)

2.5 73M1866B Pinout

Figure 6 shows the 73M1866B 42-pin pinout.

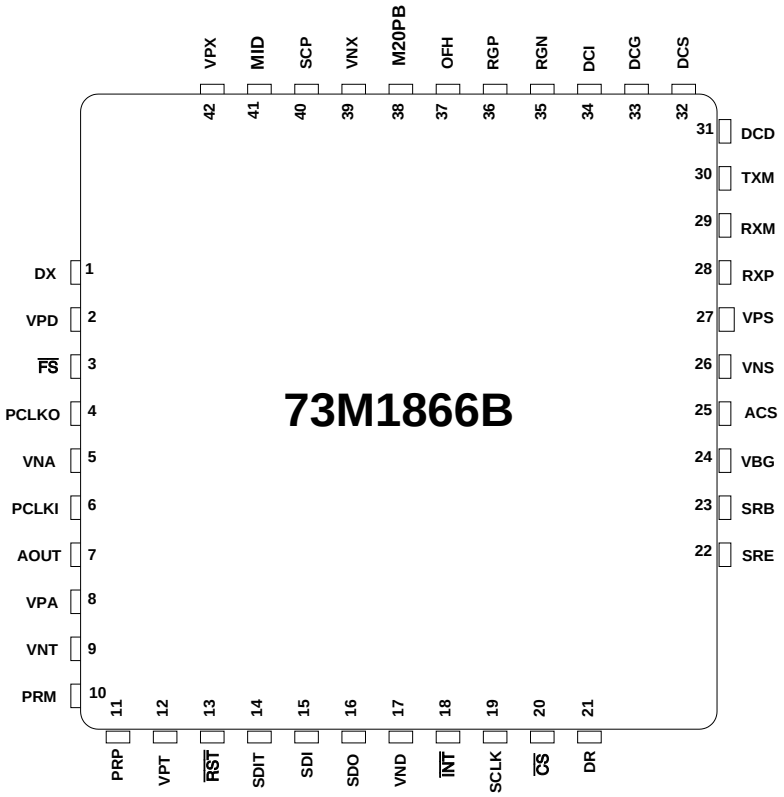


Figure 6: 73M1866B 42-Pin Pinout

Table 5 describes the pin functions for the device. Decoupling capacitors on the power supplies should be included for each pair of supply pins.

Table 5: 73M1866B Pin Definitions

Pin Number	Pin Name	Type	Description
1	DX	O	PCM received data from the A to D
2	VPD	PWR	Positive digital supply
3	$\overline{FS}$	I/O	PCM frame synchronization
4	PCLKO	O	PCM clock output
5	VNA	GND	Negative analog ground
6	PCLKI	I	PCM clock in
7	AOUT	O	Audio output – must be buffered for speaker
8	VPA	PWR	Positive analog supply
9	VNT	GND	Negative transformer supply
10	PRM	I/O	Transformer primary minus
11	PRP	I/O	Transformer primary plus
12	VPT	PWR	Positive transformer supply
13	$\overline{RST}$	I	Hardware reset (active low)
14	SDIT	O	SPI data out for daisy-chain mode
15	SDI	I	SPI data in
16	SDO	O	SPI data out

Pin Number	Pin Name	Type	Description
17	VND	GND	Negative digital ground
18	$\overline{INT}$	O	Interrupt / ring detect (active low – open drain)
19	SCLK	I	SPI clock
20	$\overline{CS}$	I	SPI chip select (active low)
21	DR	I	PCM transmit data sent to the D to A
22	SRE	I	Voltage regulator sense
23	SRB	O	Voltage regulator drive
24	VBG	O	VBG bypass, connect to 0.1µF capacitor to VNS
25	ACS	I	AC current sense
26	VNS	GND	Analog negative supply voltage
27	VPS	PWRO	Analog positive supply voltage (output)
28	RXP	I	Receive plus – signal input
29	RXM	I	Receive minus – signal input
30	TXM	O	Transmit Minus – transhybrid cancellation output
31	DCD	O	DC loop output
32	DCS	I	DC loop current sense
33	DCG	O	DC loop control
34	DCI	I	DC loop input
35	RGN	I	Ring detect negative voltage input
36	RGP	I	Ring detect positive voltage input
37	OFH	O	Off-hook control
38	M20PB	I	Test pin. Connect to VNX.
39	VNX	GND	Negative supply voltage
40	SCP	I/O	Positive side of the secondary pulse transformer winding
41	MID	I/O	Charge pump midpoint
42	VPX	PWR	Supply from the barrier

2.6 Requisite Use of Exposed Bottom Pad on 73M1866B and 73M1966B QFN Packages

The exposed bottom pad is not intended for thermal relief (heat dissipation) and should not be soldered to the PCB. Soldering of the exposed pad could also compromise electrical isolation/insulation requirements for proper voltage isolation. Avoid any PCB traces or through-hole vias on the PCB beneath the exposed pad area.

3 Electrical Characteristics and Specifications

3.1 Isolation Barrier Characteristics

Table 6 provides the characteristics of the 73M1x66B Isolation Barrier.

Table 6: Isolation Barrier Characteristics

Parameter	Rating
Barrier frequency	768 kHz
Data transfer rate across the barrier for the sampling rate of 8 kHz	1.536 Mbps

When 16 kHz sampling rate is selected, the frequency and data transfer rates are twice those shown above.

3.2 Electrical Specifications

This section provides the absolute maximum ratings, the recommended operating conditions and the DC characteristics.

3.2.1 Absolute Maximum Ratings

Table 7 lists the maximum operating conditions for the 73M1x66B. Permanent device damage may occur if absolute maximum ratings are exceeded. Exposure to the extremes of the absolute maximum rating for extended periods may affect device reliability.

Table 7: Absolute Maximum Device Ratings

Parameter	Min	Max	Unit
Supply voltage	-0.5	4.0	V
Pin input voltage (except OSCIN)	-0.5	6.0	V
Pin input voltage (OSCIN)	-0.5 to VDD	0.5	V

3.2.2 Recommended Operating Conditions

Function operation should be restricted to the recommended operating conditions specified in Table 8.

Table 8: Recommended Operating Conditions

Parameter	Min	Max	Unit
Supply voltage (VDD) with respect to VSS	3.0	3.6	V
Operating temperature	-40	85	°C

3.2.3 DC Characteristics

Table 9 lists the 73M1x66B DC characteristics.

Table 9: DC Characteristics

Parameter		Condition	Min	Nom	Max	Unit
Input low voltage	VIL	–	-0.5	–	0.2 ∗ VDD	V
Input high voltage	VIH1	–	0.7 VDD	–	5.5	V
Output low voltage	VOL	IOL=4 mA	–	–	0.45	V
Output low voltage FSB,SCLK,	VOL	IOL=1 mA	–	–	0.45	V
Output high voltage	VOH	IOH=-4 mA	VDD - 0.45	–		V
Output high voltage FSB, FSBD, SCLK	VOH	IOH=-1 mA	VDD - 0.45	–		V
Input low leakage current	IIL1	VSS < Vin < VIL1	10	–	40	µA
Input high leakage current	IIH1	VIH1 < Vin < 5.5	–	–	1	µA
IDD current at 3.0 V – 3.6 V			**Nominal at 3.3 V**			
Active digital current	$IDD1_{dig}$	–	–	1.0	1.5	mA
Active PLL current	$IDD1_{pll}$	–	–	1.0	1.5	mA
Active analog current	$IDD1_{ana}$	–	–	12	17	mA
IDD total current*	IDD1	–	–	15	20	mA
IDD total current*	IDD2	–	–	20	30	mA
IDD current PWDN=1	IDD3	–	–	1.0	5	µA
IDD current SLEEP=1 (Ext Ref Clk)	IDD4	–	–	0.5	1.0	mA
IDD current ENFEH=0 (Ext Ref Clk)	IDD6	–	–	1.0	1.5	mA

*Note: IDD1 is with the secondary of the barrier left open.
IDD2 is with the secondary of the barrier connected to 73M1916 fully powered.

3.3 Interface Timing Specification

There are three interfaces associated with the 73M1x66B: the SPI interface, the PCM highway interface and the line interface. This section provides the timing specification for the SPI interface and the PCM highway interface.

3.3.1 SPI Interface

Table 10 lists the characteristics for the SPI interface.

Table 10: SPI Interface Switching Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
SCLK cycle time[1]	t_{scy}	62.5	–	–	ns
SCLK rise time	t_{scr}	–	–	25	ns
SCLK fall time	t_{scf}	–	–	25	ns
$\overline{CS}$ setup time	t_{ics}	25	–	–	ns
$\overline{CS}$ hold time	t_{ich}	20	–	–	ns
SDI setup time	t_{ids}	25	–	–	ns
SDI hold time	t_{idh}	20	–	–	ns
SDO turn on delay	t_{odd}	–	–	20	ns
SDO turn off delay	t_{odo}	–	–	20	ns
SDO hold time	t_{odh}	–	–	20	ns
SDI to SDITHRU propagation delay	t_{idt}	–	6	–	ns

Note1: The minimal value of this parameter is for the case where only one 73M1906B is connected to the host. If the daisy chain mode is used, the minimum SCLK cycle time increases according to the number of slaves in the chain.

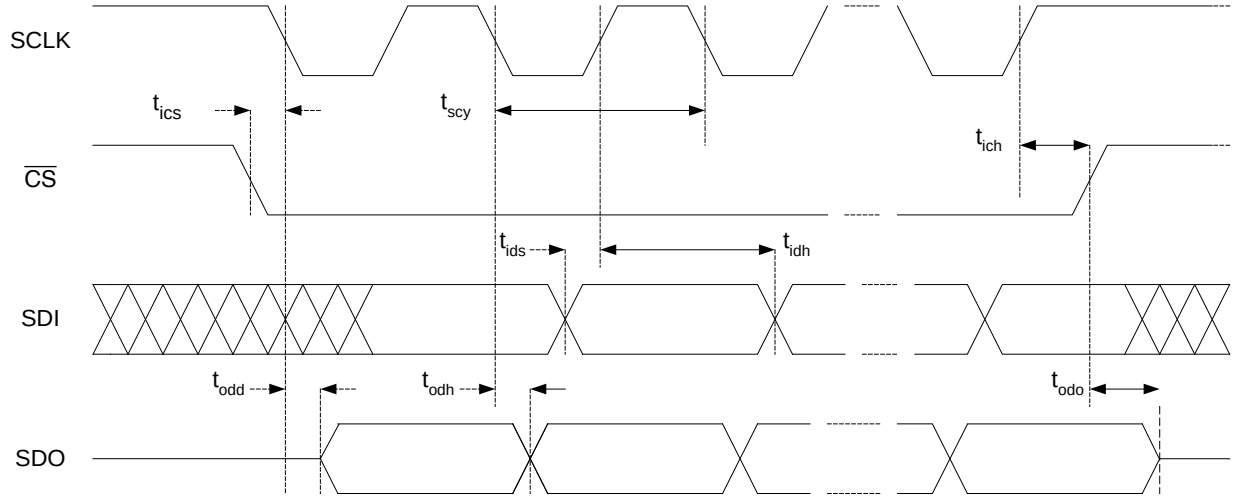


Figure 7: SPI Timing Diagram

3.3.2 PCM Highway Interface

Table 11: Switching Characteristics – PCM Interface (Slave Mode)

Parameter	Symbol	Min	Typ	Max	Unit
PCLK_IN cycle time	t_{pcy}	122	–	3906	ns
PCLK_IN rise time	t_{pcr}	–	–	25	ns
PCLK_IN fall time	t_{pcf}	–	–	25	ns
FS setup time	t_{ifs}	25	–	–	ns
FS hold time	t_{ifh}	20	–	–	ns
FS cycle time	t_{ifc}	–	125	–	µs
DR setup time	t_{ids}	25	–	–	ns
DR hold time	t_{idh}	20	–	–	ns
DX turn on delay	t_{odd}	–	–	20	ns
DX turn off delay	t_{odo}	–	–	20	ns
DX hold time	t_{odh}	–	–	20	ns

Table 12: Switching Characteristics – PCM Interface (Master Mode)

Parameter	Symbol	Min	Typ	Max	Unit
PCLK_OUT cycle time	t_{pcy}	–	488	–	ns
PCLK_OUT rise time	t_{pcr}	–	–	25	ns
PCLK_OUT fall time	t_{pcf}	–	–	25	ns
FS setup time	t_{ifs}	50	–	–	ns
FS hold time	t_{ifh}	50	–	–	ns
FS cycle time	t_{ifc}	–	125	–	µs
DR setup time	t_{ids}	25	–	–	ns
DR hold time	t_{idh}	20	–	–	ns
DX turn on delay	t_{odd}	–	–	20	ns
DX turn off delay	t_{odo}	–	–	20	ns
DX hold time	t_{odh}	–	–	20	ns

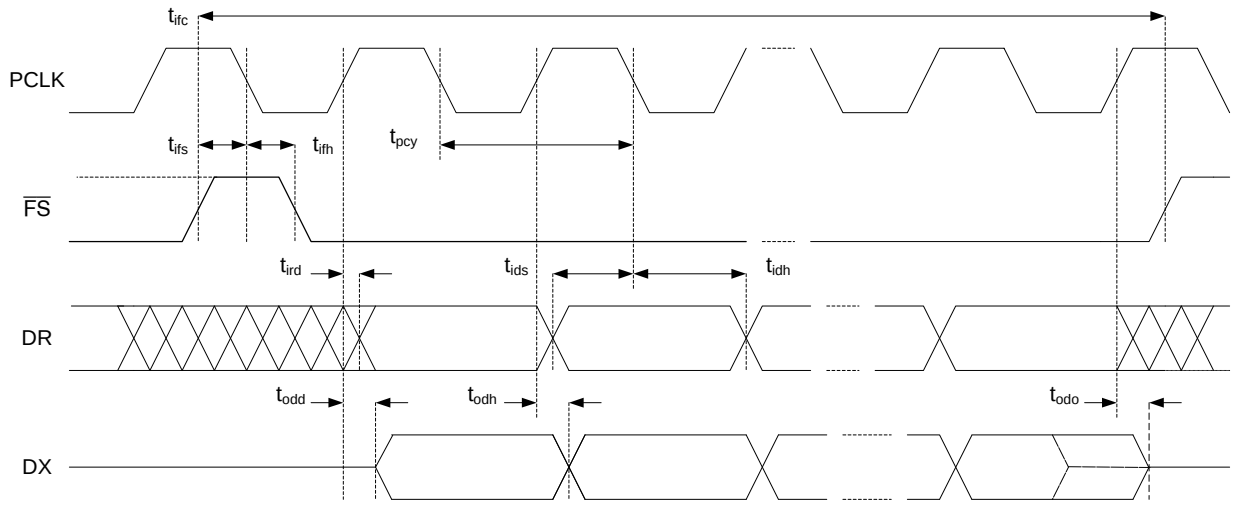


Figure 8: PCM Timing Diagram for Positive Edge Transmit Mode and Negative Edge Receive Mode

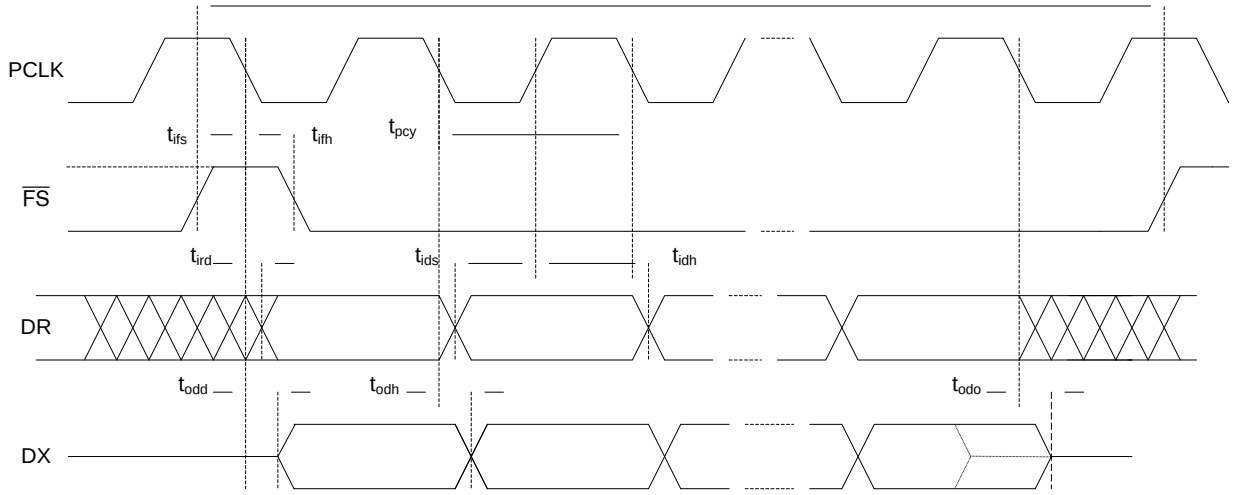


Figure 9: PCM Timing Diagram for Negative Edge Transmit Mode and Positive Edge Receive Mode

3.4 Analog Specifications

This section provides the electrical characterizations of the 73M1x66B analog circuitry.

3.4.1 DC Specifications

VBG is to be connected to an external bypass capacitor with a minimum value of 0.1 µF. This pin is not intended for any other external use.

Table 13: Reference Voltage Specifications

Parameter	Test Condition	Min	Nom	Max	Units
VBG	VDD=3.0 V – 3.6 V	0.9	1.19	1.4	V
VBG Noise	300 Hz – 3.3 kHz	–	-86	-80	dBm_{600}
VBG PSRR	300 Hz – 30 kHz	40	–	–	dB

3.4.2 Call Progress Monitor

The Call Progress Monitor monitors activities on the line. The audio output contains both transmit and receive data with a configurable level individually set by Register 10h.

Figure 10 shows the frequency response of the Call Progress Monitor Filter based upon the characteristics of the device plus the external circuitry as shown.

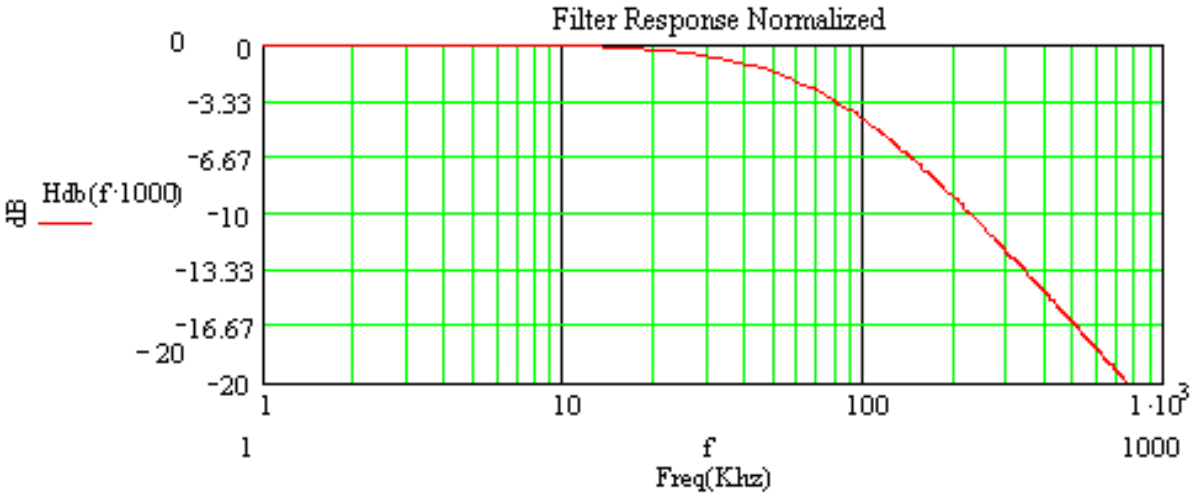


Figure 10: Frequency Response of the Call Progress Monitor Filter

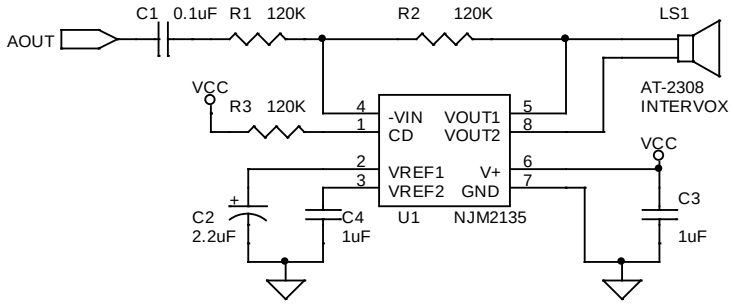


Figure 11: Demo Board Circuit Connecting AOUT to a Speaker

Table 14: Component Values for the Speaker Driver

Quantity	Reference	Part Description	Part
1	C1	Ceramic capacitor	0.1 µF
1	C2	Ceramic capacitor	2.2 µF (optional)
2	C3, C4	Ceramic capacitor	1 µF
1	LS1	Sound transducer	Speaker (Intervox)
3	R1, R2, R3	1/8 W resistor 0603	120 kΩ
1	U1	Audio amplifier	NJM2135 (New Japan Radio)

All measurements are at the AOUT pin with CMVSEL=0. Note that when CMVSEL=1, the peak signal at AOUT is increased to approximately 1.11 Vpk.

Table 15: Call Progress Monitor Specification

Parameter	Test Condition	Min	Nom	Max	Units
AOUT for transmit	1 kHz full swing code (ATX) CMRXG=11 (Mute) Observe AOUT pin	–	–	–	–
	CMTXG=00	–	0.98	–	Vpk
	CMTXG=01 relative to CMTXG=00	–	-6	–	dB
	CMTXG=10 relative to CMTXG=00	–	-12	–	dB
	CMTXG=11 (Mute)	–	Mute	–	dB
AOUT transmit THD	CMTXG=00	–	40	–	dB
AOUT for receive	1.0 Vpk, 1 kHz at the line or 0.5 Vpk at RXP/RXM with RXG=10 CMTXG=11 (Mute) Observe AOUT pin	–	–	–	–
	CMRXG=00	–	0.96	–	Vpk
	CMRXG=01 relative to CMRXG=00	–	-6	–	dB
	CMRXG=10 relative to CMRXG=00	–	-12	–	dB
	CMRXG=11 (Mute)	–	Mute	–	dB
AOUT receive THD	CMRXG=00	–	40	–	dB
AOUT output impedance		–	10	–	kΩ

3.5 73M1x66B Line-Side Electrical Specifications (73M1916)

Table 16 lists the absolute maximum ratings for the line side. Operation outside these rating limits may cause permanent damage to this device.

Table 16: Line-Side Absolute Maximum Ratings

Parameter	Min	Max	Unit
Pin input voltage from VPX to VNX	-0.5	6.0	V
Pin input voltage (all other pins) to VNS	-0.5	4.0	V

3.6 Reference and Regulation

Table 17 lists the VBG specifications. VBG should be connected to an external bypass capacitor with a minimum value of 0.1 µF. This pin is not intended for any other external use.

The following conditions apply: VPX=5 V; Barrier Powered Mode; Barrier Data Rate across the Barrier=1.5 Mbps; VBG connected to 0.1 µF external cap.

Table 17: VBG Specifications

Parameter	Test Condition	Min	Nom	Max	Units
VBG	See conditions above.	–	1.19	–	V
VBG noise	300 Hz – 3.3 kHz	–	-86*	-80	dBm_{600}
VBG PSRR	300 Hz – 30 kHz	40	–	–	dB
VPS	VPX=5.5 V	–	3.15	–	V
VPS PSRR	VPX=4.5 V to 5.5 V	–	40	–	dB

3.7 DC Transfer Characteristics

Table 18 lists the maximum DC transmit levels. All tests are driven at pin DCI and measured at pin DCS. DCEN=1. ILM=1.

Table 18: Maximum DC Transmit Levels

Parameter	Test Condition	Min	Nom	Max	Units
V_{DCON} (DC "On" Voltage)	DCIV=00	0.62	0.69	0.78	V
	DCIV=01	0.83	0.92	1.00	V
	DCIV=10	1.08	1.16	1.24	V
	DCIV=11	1.32	1.42	1.53	V
With ENAC=0	DCIV=XX	0.20	0.26	0.30	V
DC Gain	$V_{DCON}<V_{DCI}<0.4V+V_{DCON}$	-0.30	0 .0	+0.25	dB
I_{DCI} before ILIM	ILM=1 $V_{DCI}=0.28V+V_{DCON}$	–	–	10	µA
I_{DCI} after ILIM	ILM=1 $V_{DCI}=0.44V+V_{DCON}$	20	–	–	µA
Delta $V_{\underline{DCS}}$ Delta I_{DCI}	$8.2*45mA< V_{DCS} < 8.2*60mA$	–	0.85	–	mA/V
*Noise	At the line with 300 Ω(ac) (0.15 - 4.0 kHz)	–	-85	-80	dBm

3.8 Transmit Path

Table 19 list the transmit path characteristics. A pattern for a sinusoid of 1 kHz, full scale (code word of +/- 32,767) from the 73M1x66B is forced and ACS is measured with R10=174 Ω. Unless stated otherwise, test conditions are: ACZ=0000 (600 Ω termination), THEN=1, ATEN=1, DAA=01, TXBST=0, sample rate=8kHz.

Table 19: Transmit Path

Parameter	Test Condition	Min	Nom	Max	Units
Offset voltage 8 and 16 kHz sample rate	50% 1's density relative to 1.4 V common mode.	–	25	–	mV
Tx gain, relative to DAA[1:0]=01	DAA=00	2.5	+3	3.5	dB
	DAA=01	-0.5	0	0.5	dB
	DAA=10	-4.5	-4	-3.5	dB
	DAA=11	-8.5	-8	-7.5	dB
AC swing (1 kHz sinusoid) 8 and 16 kHz sample rate	DAA=01	–	0.317	–	Vpk
	DAA=00	–	0.447	–	Vpk
	TXBST=1, DAA=xx	–	0.634	–	Vpk
	ACZ=0001	–	0.211	–	Vpk
	ACZ=0010	–	0.211	–	Vpk
	ACZ=0011	–	0.200	–	Vpk
	ACZ=0100	–	0.254	–	Vpk
	ACZ=0101	–	0.220	–	Vpk
	ACZ=0110	–	0.171	–	Vpk
	ACZ=0111	–	0.194	–	Vpk
	ACZ=1000	–	0.222	–	Vpk
	ACZ=1001	–	0.205	–	Vpk
	ACZ=1010	–	0.223	–	Vpk
	ACZ=1011	–	0.313	–	Vpk
	ACZ=1100	–	0.208	–	Vpk
	ACZ=1101	–	0.211	–	Vpk
	ACZ=1110	–	0.285	–	Vpk
	ACZ=1111	–	0.235	–	Vpk
Idle noise	300 Hz – 4 kHz	–	-80	–	dBm
THD	300 Hz – 4 kHz	–	-80	–	dB
Intermod distortion 1.0 kHz and 1.2 kHz summed	300 Hz – 4 kHz	–	-85	–	dB
Passband ripple	150 Hz – 3.3 kHz	-0.125	–	+0.125	dB
	Gain relative to 1 kHz	–	–	–	dB
	0.5 kHz	–	0.17	–	dB
	1.0 kHz	–	0	–	dB
	2.0 kHz	–	0.193	–	dB
	3.3 kHz	–	-0.12	–	dB
Aliased image	Fs +/- 1 kHz, relative to 1 kHz	–	-75	–	dB

3.9 Receive Path

Table 20 lists the receive path characteristics. All test inputs are driven through an AC coupling network shown in Figure 29. The receive bit stream is measured at the DX pin. RXEN=1.

Table 20: Receive Path

Parameter	Test Condition	Min	Nom	Max	Units
Differential input resistance	RXP/RXM	–	1000	–	kΩ
Input level	Differential, RXP/RXM	–	1.1	1.16	Vpk
Input level	Common mode, RXP/RXM	–	1.37	–	V
Overall sigma-delta ADC modulation gain inclusive of 73M1906B processing	Normalized to VBG=1.19 V. RXG=00 Divide Vrxp/m by PCM Output	–	47.3	–	µV/bit
Offset voltage	R6=17.4 kΩ, R8=52.3 kΩ, R9=21 kΩ. See Figure 12.	–	0	+/- 30	mV
Rx gain (See Note 1.)	RXG=00	-0.5	0	0.5	dB
	RXG=01	2.5	3	3.5	dB
	RXG=10	5.5	6	6.5	dB
	RXG=11	8.5	9	9.5	dB
	RXBST=1, RXG=00	18.3	19.3	20.3	dB
Overall receive frequency response inclusive of 73M1906B processing	Relative to 1 kHz	–	–	–	–
	0.3 kHz – 3.3 kHz	-0.25	0	+0.25	dB
	Fs (8 kHz)	–	-75	–	dB
Idle noise	300 Hz – 4 kHz	–	-80	–	dBm
THD	RXG=00	–	-85	–	dB
	RXBST=1	–	-60	–	
Intermod Dist 1.0 kHz and 1.2 kHz summed	300 Hz – 4 kHz	–	-85	–	dB
Crosstalk	1 Vpk 1 kHz sine wave at TXP; FFT on Rx ADC samples, first four harmonics reflected to the line.	–	-90	–	dBm
CMRR	RXP=RXM 1 Vpk	40	–	–	dB
PSRR	-30 dBm signal at VPX in Barrier Powered Mode; 300 Hz – 30 kHz.	–	–	40*	dB
On-Hook AC Impedance	300 Hz – 4 kHz, without EMI caps.	–	2	–	MΩ

Note 1: RXG controls the amount of gain or attenuation of the receiver analog gain element as specified in Table 20. The overall receiver channel gain has 6 dB of attenuation and the net effect of the RXG bits on the receiver channel gain is defined in Table 36.

3.10 Transmit Hybrid Cancellation

Table 21 lists the transmit hybrid cancellation characteristics. Unless stated otherwise, test conditions are: ACZ[3:0]=0000 (600 Ω termination), THEN=1, ATEN=1, DAA[1:0]=01, TXBST=0. TXM is externally fed back into the 73M1916 to effect cancellation of transmit signal.

Table 21: Transmit Hybrid Cancellation Characteristics

Parameter	Test Condition	Min	Nom	Max	Units
Transmit hybrid cancellation	Measure in 73M1906B	–	20	–	dB
Offset voltage	50% 1's density	–	0	25	mV
AC swing	1 kHz sinusoid	1.00	1.05	1.10	Vpk
Idle noise	300 Hz – 4 kHz	–	-80	–	dBm

3.11 Receive Notch Filter

Table 22 lists the receive notch filter characteristics. All measurements taken with RLPNEN=1, TXEN=0, RXG=00, ATEN=1. RXP is driven with 1 Vpk signal.

Table 22: Receive Notch Filter

Parameter	Test Condition	Min	Nom	Max	Unit
Magnitude response	**RLPNH=0 (12 kHz Notch)**				
	300 Hz	–	0.0	–	dB
	1 kHz	–	+0.03	–	dB
	3 kHz	–	+0.04	–	dB
	12 kHz	-30	-50	–	dB
	Passband Ripple (0.3 kHz – 3.4 kHz)	–	+/- 0.15	–	dB
Delay		–	28.8	–	µs
	300 Hz	–	28.93	–	µs
	1 kHz	–	30.25	–	µs
	3 kHz	–	41.62	–	µs
	12 kHz	–	9.95	–	µs
Magnitude response	**RLPNH=1 (16 kHz Notch)**				
	300 Hz	–	0.0	–	dB
	1 kHz	–	+0.04	–	dB
	3 kHz	–	+0.11	–	dB
	16 kHz	-30	-50	–	dB
	Passband Ripple (0.3 kHz – 3.4 kHz)	–	+/- 0.15	–	dB
Delay		–	30.53	–	µs
	300 Hz	–	30.66	–	µs
	1 kHz	–	31.93	–	µs
	3 kHz	–	42.26	–	µs
	16 kHz	–	4.74	–	µs

3.12 Detectors

This section provides electrical characteristics for the following detectors:

- Over-Voltage.
- Over-Current.
- Under-Voltage.
- Over-Load.

3.12.1 Over-Voltage Detector

The values in Table 23 were measured between RGP and RGN.

Table 23: Over-voltage Detector

Parameter	Test Condition	Min	Nom	Max	Unit
Over voltage levels	OVDTH=0	0.52	0.6	0.68	V
	OVDTH=1	0.59	0.7	0.77	V

3.12.2 Over-Current Detector

The values in Table 24 were measured in Barrier Powered Mode.

Table 24: Over-current Detector

Parameter	Test Condition	Min	Nom	Max	Unit
Over current level	Measured at DCS.	0.90	1.025	1.20	V

3.12.3 Under-Voltage Detector

The values in Table 25 were measured in Barrier Powered Mode. In the recommended schematic (see Figure 12), disconnect Q5 collector and connect to an external power supply, VPE, through a 600 Ω resistor.

Table 25: Under-voltage Detector

Parameter	Test Condition	Min	Nom	Max	Unit
Under voltage detect	Measure VPE when UVD is detected as VPE is decreased.	–	7.5	–	V

3.12.4 Over-Load Detector

The values in Table 26 were measured in Barrier Powered Mode.

Table 26: Over-load Detector

Parameter	Test Condition	Min	Nom	Max	Unit
Over load level	Measured at DCI with 1 kHz.	0.6	0.75	0.9	Vpk

4 Applications Information

This section provides general usage information for the design and implementation of the 73M1x66B.

4.1 Example Schematic of the 73M1966B and 73M1866B

Figure 12 shows a typical application schematic for the implementation of the 73M1966B. Figure 13 shows a typical application schematic for the implementation of the 73M1866B. Note that minor changes may occur to the reference material from time to time and the reader is encouraged to contact Teridian for the latest information. For more information about schematic and layout design, see the *73M1866B/73M1966B Schematic and Layout Guidelines*.

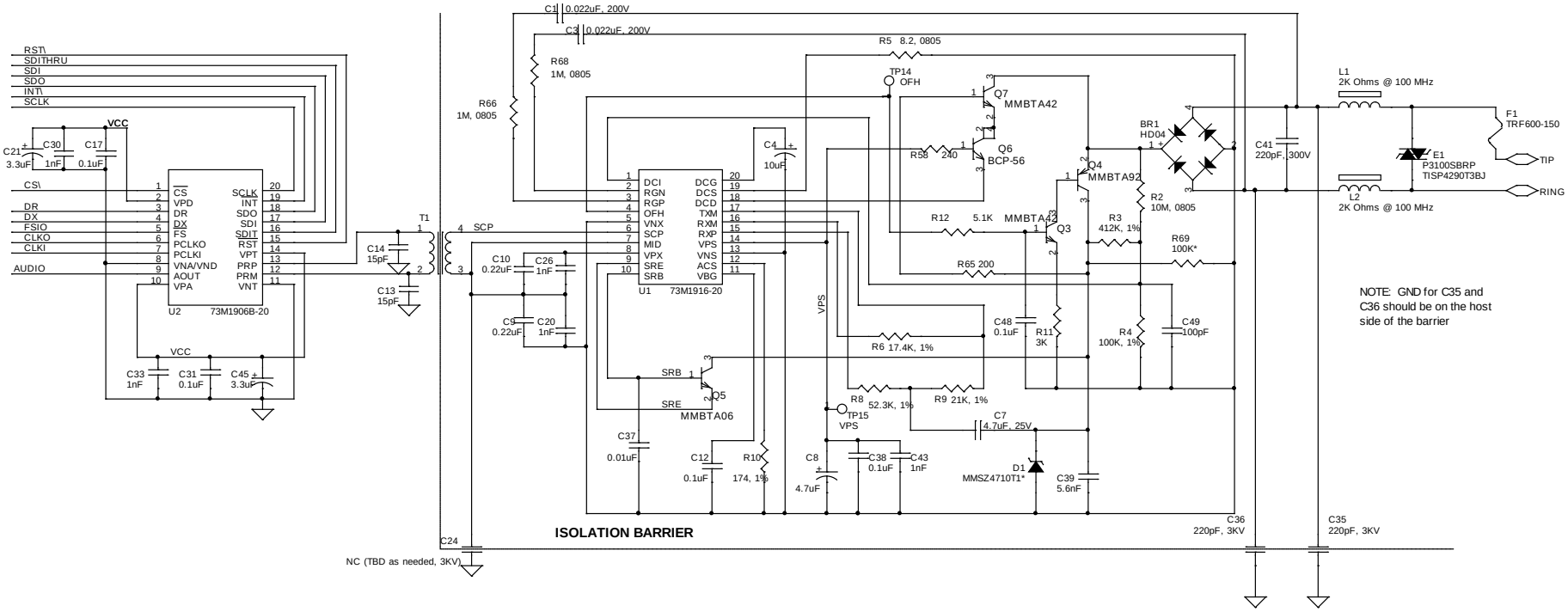


Figure 12: Recommended Circuit for the 73M1966B

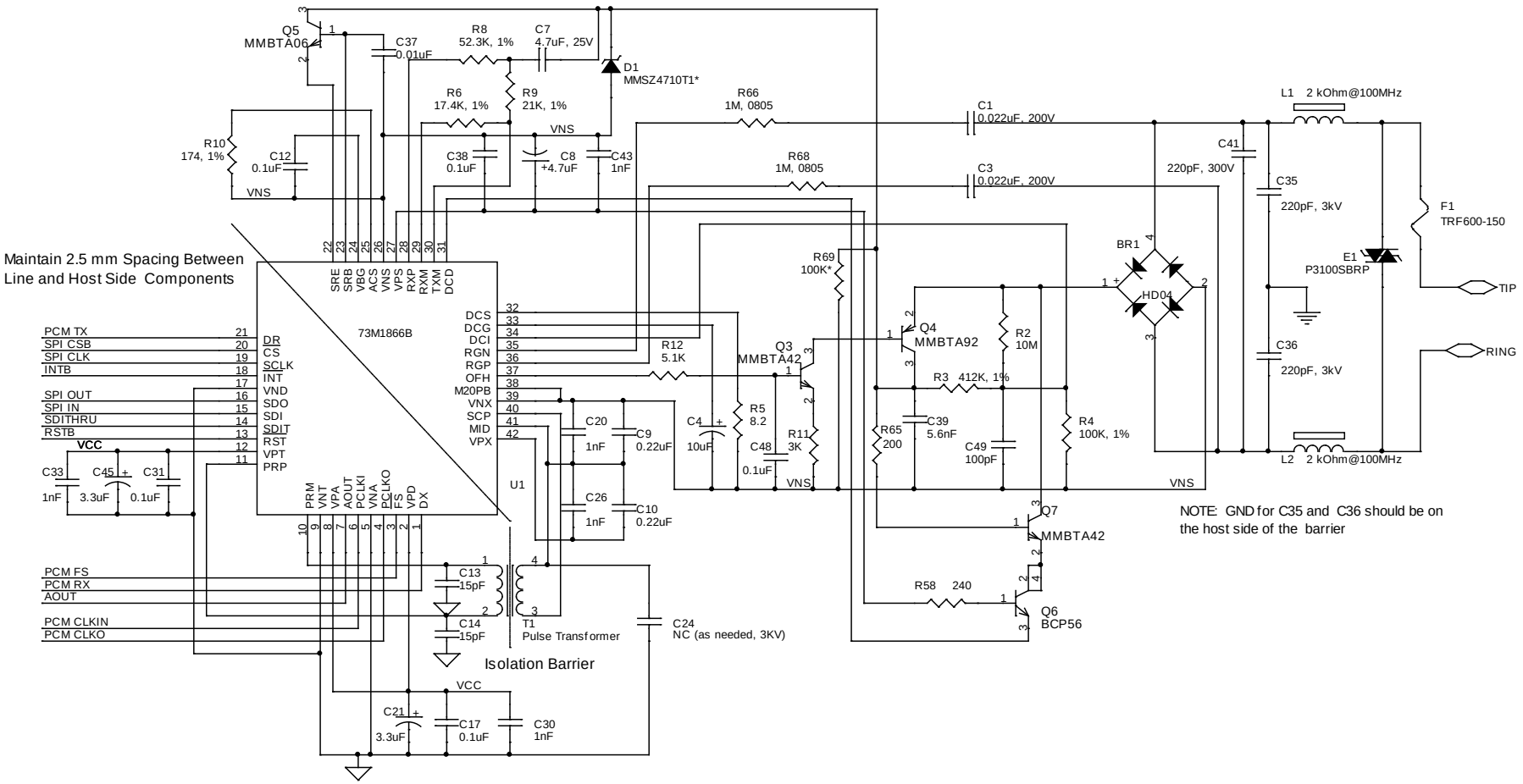


Figure 13: Recommended Circuit for the 73M1866B

4.2 Bill of Materials

Table 27 provides the 73M1x66 bill of materials for the reference schematics provided in Figure 12 and Figure 13.

Table 27: Reference Bill of Materials for 73M1x66B

Qty	Reference	Part Description	Source	Example MFR P/N
1	BR1	HD04 rectifier bridge, 0.8A, 400V	Diodes Inc.	HD04-T
2	C1, C3	0.022µF 200V, X7R, 1206	Panasonic	ECJ-3FB2D223K
1	C4	10µF 6.3V, tantalum, 0805	AVX, Panasonic	TCP0J106M8RA
1	C7	4.7µF 25V, X5R, 0805	AVX, Panasonic	08053D475KAT2A
1	C8	4.7uF 6.3V, tantalum, 0805	Rohm	TCP0J475M8R
2	C9, C10	0.22µF 16V, X7R, ceramic, 0603	Panasonic	C0603C224K8RACTU
4	C12,C17,C31, C38, C48	0.1µF 16V, X7R, ceramic, 0603	Panasonic, Kemet	C0603C104K8RACTU
2	C13, C14	15pF 50V, ceramic, 0603	Panasonic	ECJ-1VC1H150J
5	C20, C26, C30, C33, C43	1nF 10V, X7R, ceramic, 0603	Panasonic	C0603C102K8RACTU
2	C21, C45	3.3µF 6.3V, tantalum, 0805	Rohm	TCP0J335M8R
1	C37	0.01µF 50V, X7R, ceramic, 0603	AVX, Panasonic	06035C103KAT2A
1	C39	5.6nF 50V, X7R, ±10% ceramic, 0603	Panasonic	ECJ-1VB1H562K
1	C49	100pF 50V, ceramic, 0603	Taiyo Yuden	UMK107CH101JZ-T
1	D1	25V, 500mW Zener diode	ON Semi	MMSZ4710T1,
1	Q5	MMBTA06, NPN 80 V transistor SOT23	Diodes, Fairchild, Central, On Semi	MMBTA06LT1G
1	Q4	MMBTA92, PNP 300 V transistor SOT23	Diodes, Fairchild, Central, On Semi	MMBTA92LT1G
2	Q3, Q7	MMBTA42, NPN 300 V transistor SOT23	Diodes, Fairchild, Central, On Semi	MMBTA42LT1G
1	Q6	NPN 80 V transistor SOT223	Fairchild, On Semi	BCP56
1	R2	10M, 5%, 1/8W resistor 0805	Yageo	RC0805JR-0710ML
1	R3	412K, 1%, 1/10W resistor 0603	Yageo	RC0603FR-07412KL
1	R4	100K, 1%, 1/10W resistor 0603	Yageo	RC0603FR-07100KL
1	R5	8.2, 5%, 1/8W resistor 0805	Yageo	RC0805JR-078R2L
1	R6	17.4K, 1%, 1/10W resistor 0603	Yageo	RC0603FR-0717K4L
1	R8	52.3K, 1%, 1/10W resistor 0603	Yageo	RC0603FR-0752K3L
1	R9	21K, 1%, 1/10W resistor 0603	Yageo	RC0603FR-0721KL
1	R10	174, 1%, 1/10W resistor 0603	Yageo	RC0603FR-07174RL
1	R11	3K, 5%, 1/10W resistor 0603	Yageo	RC0603JR-073K0L
1	R12	5.1 K, 5%, 1/10W resistor 0603	Yageo	RC0603JR-075K1L
1	R58	240, 5%, 1/10W resistor 0603	Yageo	RC0603JR-07240RL
1	R65	200, 5%, 1/10W resistor 0603	Yageo	RC0603JR-07200RL
2	R66, R68	1 M, 5%, 1/8W resistor 0805	Yageo	RC0603JR-071ML
1	R69*	100K typ. 5%, 1/10W resistor 0603	Yageo	RC0603JR-07100KL
1	T1	Pulse transformer	See Table 29.	

* Optional – see the *73M1866B/1966B Schematics and Layout Guidelines* for details.

4.3 Over-Voltage and EMI Protection

Over-voltage protection is required to meet worst-case conditions for target countries. UL1950, EN60950, IEC 60950, ITU-T K.20/K.21 and GR-1089-CORE specifications define the protection requirements for many countries. A single design can be implemented to meet all these requirements.

Figure 14 shows a recommended protection circuit topology. Fuse (F1) should be rated appropriately for the country of operation, and the bidirectional thyristor (E1) should have a minimum break-over of 220 V, a maximum break-over of 275 V and be able to survive a 100 A fast transient. In addition to over-voltage and current protection, the 73M1x66B should make provisions to prevent EMI emissions and EMC susceptibility. Figure 14 also illustrates how L1, L2, C35, C36 and C41can provide this suppression. The ferrite beads, L1 and L2, should be capable of passing 150 mA and have an impedance of 2K Ω at 100 MHz. C35, C36 and C41 should be between 47pF and 220nF, and rated for a breakdown voltage greater than the highest isolation voltage or line voltage that is required for country compatibility. C35 and C36 should be returned to an earth ground. EMI suppression is highly dependent on the physical design of the overall circuit and not all the suppression components may be needed in every design and application.

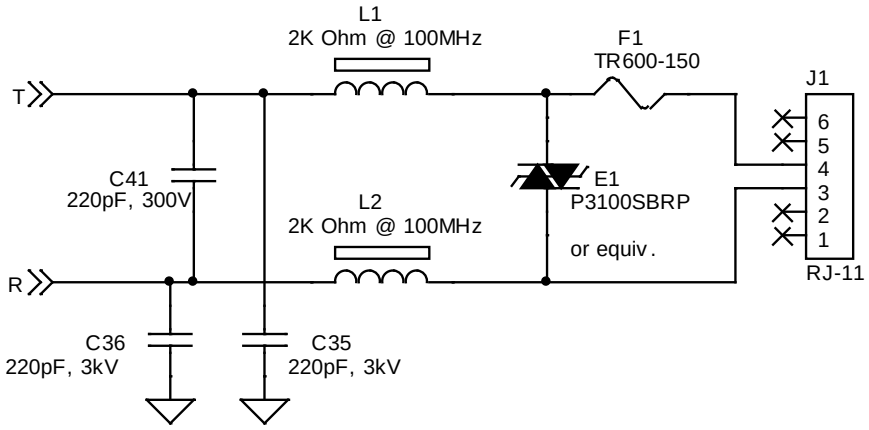


Figure 14: Suggested Over-Voltage Protection and EMI Suppression Circuit

Table 28: Reference Bill of Materials for Figure 14

Reference	Part Description	Source	Example MFR P/N
E1	Bidirectional Thyristor	Diodes Inc., Bourns	TB3100H-13-H, TISP4290T3BJR-S
F1	PPTC Fuse	Tyco, Bourns	MF-R015/600 or equiv.
L1,L2	2 KΩ @ 100 MHz, 150 mA min, 0805	Steward, TDK	MPZ2012S601A
C35, C36	220 pF, 3000 V	TDK	C4532COG3F221K
C41	220 pF, 300 V	Vishay	VJ1206Y221KXEAT5Z

4.4 Isolation Barrier Pulse Transformer

The isolation element used by the 73M1x66B is a standard digital pulse transformer. Several vendors supply compatible transformers with up to 6000 V ratings. Since the transformer is the only component crossing the isolation barrier other than EMI capacitors that may be required, it solely determines the isolation between the PSTN and the FXO's digital interface. This method of isolation is significantly superior to other isolation techniques with major advantages in high common mode voltage operation, lower radiated noise (EMI) and improved operation in noisy environments. Table 29 lists some pulse transformers compatible with the 73M1x66B. The table also includes low-voltage transformers that offer low-cost alternatives if such voltages are sufficient.

Table 29: Compatible Pulse Transformer Sources

Company	Number
Sumida	ESMIT 4180 ESMIT 4181
Wurth Electronics Midcom Inc.	750110001
UMEC	TG-UTB01543S
Datatronics	PT79280
AAsupreme	P950003

Table 30 lists some of the typical pulse transformer specifications used by the 73M1x66B. Contact the manufacturer directly for product information.

Table 30: Pulse Transformer Electrical Characteristics

Parameter	Test Condition	Min	Nom	Max	Tolerance	Unit
Inductance	100 kHz, 10 mVAC, 1-2, Ls.	54	60	200	–	µH
Interwinding Capacitance	–	–	–	6	–	pF
Turn Ratio	–	–	1:1	–	±2 %	N/A
DC Resistance	Primary	–	–	0.25	–	Ω
	Secondary	–	–	0.25	–	Ω
Dielectric Breakdown Voltage	1 sec	2000	3750	–	–	Vrms
ET Constant	–	–	1.2	–	–	Vµs
Surge Test	1.2 x 50 µs	2800	6000		–	V
Operating Temperature	–	-40	–	85	–	°C

5 SPI Interface

The host accesses the 73M1x66B using an SPI interface to write to control registers and read status registers. The host is the master of the transaction. Four pins orchestrate the communication between the host and the SPI, and a fifth pin is dedicated to support the daisy-chain mode. The signals are as follows:

- SDI Serial data input driven by the host.
- SDO Serial data output driven by the 73M1x66B.
- SCLK Clock input driven by the host.
- $\overline{CS}$ Chip select input driven by the host.
- SDIT Serial data output for daisy-chain mode.

The SPI implemented by the 73M1x66B has the following key features:

- Support for 8-bit and 16-bit mode operations.
- Support for daisy-chain operations.
- Support for both continuously active SCLK or SCLK active during transfers only.
- Support for broadcast mode.

Transactions between the host and the 73M1x66B require three bytes. All bytes are transmitted most significant byte first. The first is the control byte, the second the address byte and the third is the data byte. The control byte is structured as follows:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BRCT	R/W	X	X	CID[0]	CID[1]	CID[2]	CID[3]

The value of CID[0:3] determines which 73M1x66B in the daisy chain should execute the read or write operation requested by the host. Up to 16 devices in the daisy chain can be supported. The daisy chain organization is shown in Figure 15. The control byte is submitted to the first 73M1x66B in the daisy chain. If the value of CID[0:3] is different from zero, the SPI of that device decreases the value of CID[0:3] by one and passes the new value through SDIT to the next 73M1x66B in the chain. This process continues until CID[0:3] is zero, thus stopping at the device designated to execute the operation. The value of CID will be the position in the daisy chain for the device being addressed minus one.

If the host is controlling only one 73M1x66B, CID[0:3] must be set to 0.

The BRCT bit overrides the chip addressing driven by CID[0:3]. The host asserts BRCT for all write operations that must be executed by all 73M1x66B devices in the chain. At that time, whatever comes in SDI comes out through SDIT. BRCT does not affect read operations.

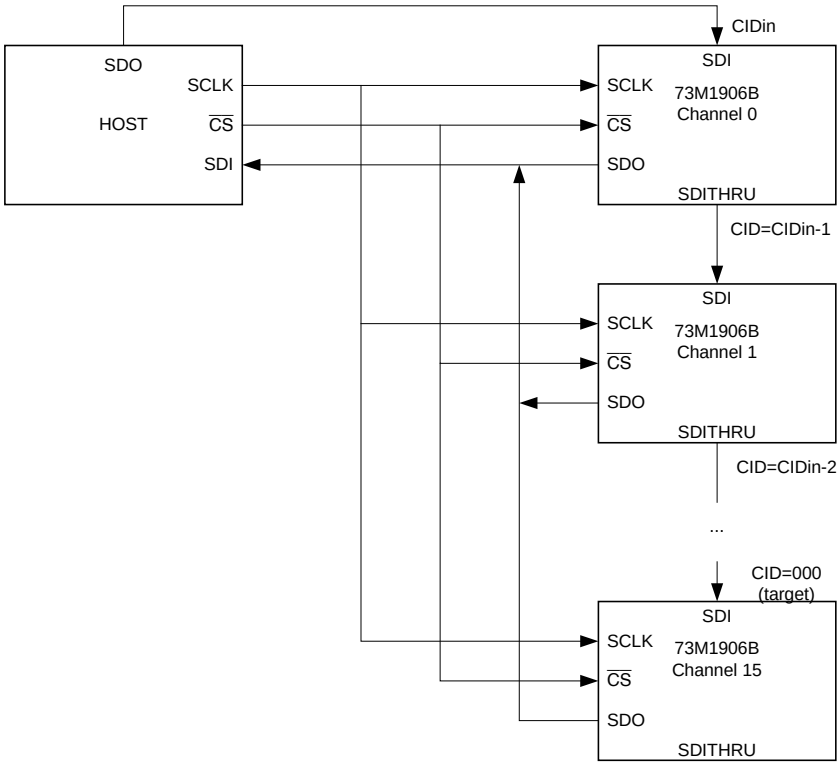


Figure 15: Daisy-Chain Configuration

The R/W bit determines whether the host requests a read (1) or a write (0) operation.

The second byte of the SPI transaction is the address byte. The address byte simply contains the 8-bit value for the register targeted by the operation. For the 73M1x66B, only six bits of the address are relevant for the register space, and the two most-significant bits of the address byte are always set to 0.

The third byte of the SPI transaction is the data byte. It contains the data to write to the addressed 73M1x66B registers or the data read from the addressed 73M1x66B register.

In the 8-bit mode, the three bytes are exchanged over three frames, as directed by $\overline{CS}$. Figure 16 and Figure 17 show a write and read transaction between the 73M1x66B and the host in 8-bit mode.

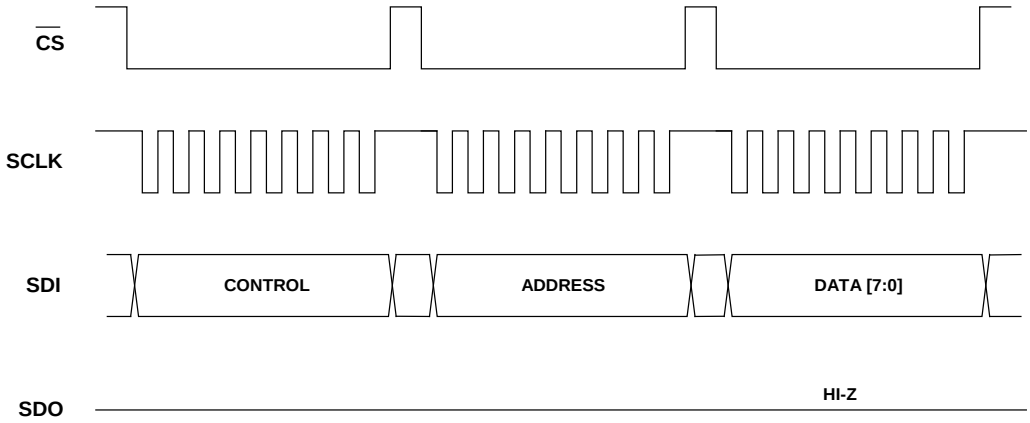


Figure 16: SPI Write Operation – 8-bit Mode

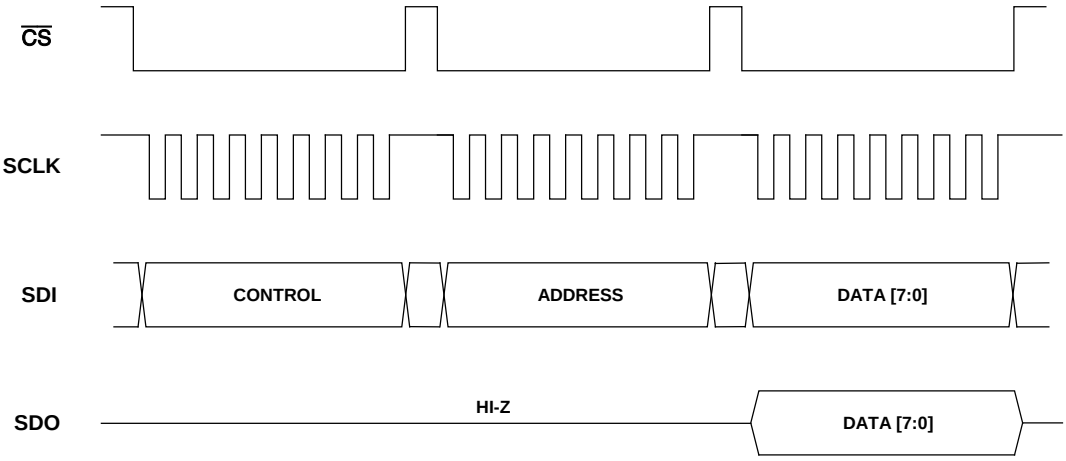


Figure 17: SPI Read Transaction – 8-bit Mode

In 16-bit mode, the first frame of 16 bits contains both the control and address bytes, and the second frame contains the data bytes. Note that the second part of the second frame is irrelevant. Figure 18 and Figure 19 show the write and read transactions in 16-bit mode.

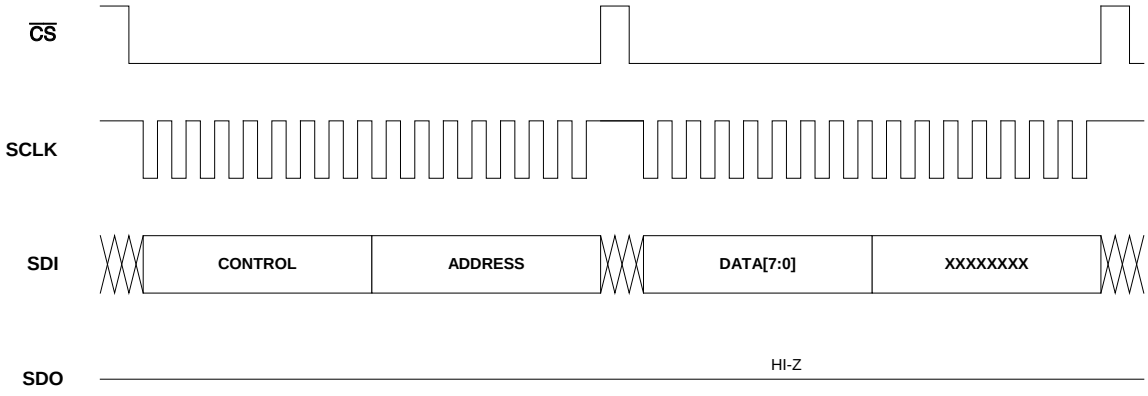


Figure 18: SPI Write Transaction – 16-bit Mode

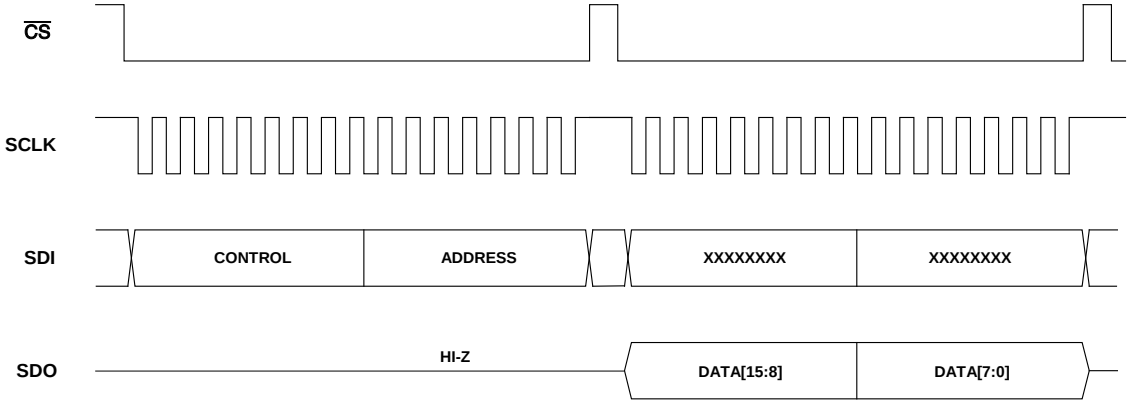


Figure 19: SPI Read Transaction – 16-bit Mode

The transaction diagrams show the case where SCLK is only active during the transaction frames. The same transaction remains valid even if SCLK runs continuously, regardless of frame boundaries. The SPI state machine resets when the host sends a frame containing a number of SCLK periods different from a multiple of eight:

- In 8-bit mode, if either the control or the address frames do not correspond to a multiple of eight SCLK cycles, the SPI state machine resets and the transaction is aborted. If the data frame is shorter than eight SCLK cycles, the state machine resets and the transaction is aborted. If the data frame is longer than eight SCLK cycles, while not being a multiple of eight cycles, the write/read transaction is performed and the state machine resets.
- In 16-bit mode, if the control/address frame does not contain a multiple of eight SCLK cycles, the SPI state machine resets and the transaction is aborted. If the data frame is shorter than eight SCLK cycles, the state machine resets and the transaction is aborted. If the data frame is longer than eight SCLK cycles, while not being a multiple of eight cycles, the write/read transaction is performed and the state machine resets. This scheme can be used to reset the SPI if one looses track of frames.

6 Control and Status Registers

Table 31 shows the 73M1x66B register map of addressable registers. The shaded cells indicate read-only bits and cannot be modified. Reserved bits should be left in their default state. Accessing unspecified registers should be avoided. Each register and bit is described in detail in the following sections.

For registers 0x12 through 0x1F, which are located in the Line-Side Device, there is a minimum time between consecutive write transactions of 300 μs when using an 8 kHz sample rate.

Table 31: Control and Status Register Map

Address (hex)	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
02	10h	TMEN	Reserved	Reserved	Reserved	Reserved	ENLPW	Reserved	Reserved
03	E0h	GPIO7	GPIO6	GPIO5	PCLKDT	RGMON	DET	SYNL	RGDT
04	E4h	DIR7	DIR6	DIR5	Reserved	REVHSD3	REVHSD2	REVHSD1	REVHSD0
05	1Bh	ENGPIO7	ENGPIO6	ENGPIO5	ENPCLKDT	ENAPOL	ENDET	ENSYNL	ENRGDT
06	00h	POL7	POL6	POL5	Reserved	Reserved	Reserved	Reserved	Reserved
07	00h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	DTST1	DTST0
08	00h	TXDG -12	TXDG -6	TXDG +3.5	TXDG +2	TXDG +1	TXDG +0.5	TXDG +0.25	TXDG +0.125
09	00h	RXDG -12	RXDG -6	RXDG +3.5	RXDG +2	RXDG +1	RXDG +0.5	RXDG +0.25	RXDG +0.125
0D	40h	LOKDET	SLHS	Reserved	Reserved	RSTLSBI	Reserved	Reserved	Reserved
0E	00h	FRCVCO	Reserved	Reserved	Reserved	Reserved	Reserved	RGTH1	RGTH0
0F	80h	ENFEH	PWDN	SLEEP	Reserved	Reserved	Reserved	Reserved	Reserved
10	00h	Reserved	Reserved	Reserved	CMVSEL	CMTXG1	CMTXG0	CMRXG1	CMRXG0
12	00h	OFH	ENDC	ENAC	ENSHL	$\overline{\text{ENLVD}}$	ENFEL	ENDT	ENNOM
13	00h	DCIV1	DCIV0	ILM	Reserved	PLDM	OVDTH	IDISPD	SEL16K
14	00h	TXBST	DAA1	DAA0	Reserved	RXBST	RLPNH	RXG1	RXG0
15	00h	ENOLD	DISNTR	Reserved	CIDM	THEN	ENUVD	ENOVD	ENOID
16	00h	TXEN	RXEN	RLPNEN	ATEN	ACZ3	ACZ2	ACZ1	ACZ0
17	00h	Reserved	Reserved	RXOCEN	Reserved	Reserved	Reserved	Reserved	Reserved
18	01h	TEST3	TEST2	TEST1	TEST0	Reserved	Reserved	Reserved	Reserved
19	00h	POLL	MATCH	Reserved	Reserved	INDX3	INDX2	INDX1	INDX0
1A	00h	RNG7	RNG6	RNG5	RNG4	RNG3	RNG2	RNG1	RNG0
1B	00h	LV7	LV6	LV5	LV4	LV3	LV2	LV1	Reserved
1C	00h	LC6	LC5	LC4	LC3	LC2	LC1	LC0	Reserved
1D	00h	REVLSD3	REVLSD2	REVLSD1	REVLSD0	Reserved	Reserved	Reserved	Reserved
1E	00h	ILMON	UVDET	OVDET	OIDET	OLDET	SLLS	Reserved	Reserved
1F	00h	POLVAL7	POLVAL6	POLVAL5	POLVAL4	POLVAL3	POLVAL2	POLVAL1	POLVAL0
20	00h	TPOL	TTS6	TTS5	TTS4	TTS3	TTS2	TTS1	TTS0
21	00h	RPOL	RTS6	RTS5	RTS4	RTS3	RTS2	RTS1	RTS0
22	00h	SR	ADJ	RCS2	RCS1	RCS0	TCS2	TCS1	TCS0
23	00h	PCMEN	MASTER	PCODE3	PCODE2	PCODE1	PCODE0	LIN	LAW
24	00h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LB
25	00h	RXOM7	RXOM6	RXOM5	RXOM4	RXOM3	RXOM2	RXOM1	RXOM0

Throughout this document, type W is read/write, type WO is write only and type R is read only. Registers and bits are defined as 0x16[3:0], where 0x16 is the register address and the numbers in square brackets specify the address bits. The bit order is [msb – lsb] for a field. For example, [3:0] means bits 3 through 0 of a particular field.

Table 32: Alphabetical Bit Map

Bit Name	Register	Page	Default	Type	Category
ACZ	0x16[3:0]	68	0000	W	DAA Control Function
ADJ	0x22[6]	52	0	W	PCM Control Function
ATEN	0x16[4]	69	0	W	DAA Control Function
CIDM	0x15[4]	75	0	W	DAA Control Function
CMRXG1/0	0x10[1:0]	44	00	W	Call Progress Monitor
CMTXG1/0	0x10[3:2]	44	00	W	Call Progress Monitor
CMVSEL	0x10[4]	44	0	W	Call Progress Monitor
DAA1/0	0x14[6:5]	52	00	WO	PCM Control Function
DCIV1/0	0x13[7:6]	69	00	WO	DAA Control Function
DET	0x03[2]	76	0	R	Line Sensing Control
DIR5	0x04[5]	43	1	W	GPIO Control
DIR6	0x04[6]	43	1	W	GPIO Control
DIR7	0x04[7]	43	1	W	GPIO Control
DISNTR	0x15[6]	61	0	WO	Barrier Control Function
DTST1/0	0x07[1:0]	79	00	W	Loopback Control
ENAC	0x12[5]	69	0	WO	DAA Control Function
ENAPOL	0x05[3]	61	1	W	Barrier Control Function
ENDC	0x12[6]	69	0	WO	DAA Control Function
ENDET	0x05[2]	76	0	W	Line Sensing Control
ENDT	0x12[1]	76	0	WO	Line Sensing Control
ENFEH	0x0F[7]	42	1	W	Power Management
ENFEL	0x12[2]	70	0	WO	Current Limiting Detection Control and Status
ENGPIO7	0x05[7]	43	0	W	GPIO Control
ENGPIO6	0x05[6]	43	0	W	GPIO Control
ENGPIO5	0x05[5]	43	0	W	GPIO Control
$\overline{\text{ENLPW}}$	0x02[2]	61	0	W	Barrier Control Function
$\overline{\text{ENLVD}}$	0x12[3]	70	0	WO	Current Limiting Detection Control and Status
ENNOM	0x12[0]	70	0	WO	DAA Control Function
ENOID	0x15[0]	77	0	WO	Over-Current Detection Control and Status
ENOLD	0x15[7]	77	0	WO	Over-Load Detection Control and Status
ENOVD	0x15[1]	77	0	WO	Over-Voltage Detection Control and Status
ENPCLKDT	0x05[4]	52	1	W	PCM Control Function
ENRGDT	0x05[0]	75	1	W	Ring Detection Function
ENSHL	0x12[4]	70	0	WO	Current Limiting Detection Control and Status
ENSYNL	0x05[1]	61	1	W	Barrier Control Function
ENUVD	0x15[2]	76	0	WO	Under-Voltage Detection Control and Status
FRCVCO	0x0E[7]	42	0	W	Device Clock Management
GPIO5	0x03[5]	43	1	W	GPIO Control
GPIO6	0x03[6]	43	1	W	GPIO Control
GPIO7	0x03[7]	43	1	W	GPIO Control
IDISPD	0x13[1]	69	0	WO	DAA Control Function
ILM	0x13[5]	70	0	WO	Current Limiting Detection Control and Status
ILMON	0x1E[7]	70	0	R	Current Limiting Detection Control and Status
INDX	0x19[3:0]	40	0	W	Line-Side Device Register Polling
LAW	0x23[0]	52	0	W	PCM Control Function
LB	0x24[0]	79	0	W	Loopback Control Function
LC	0x1C[7:1]	76	0	R	Auxiliary A/D Converter Status
LIN	0x23[1]	52	0	R/W	PCM Control Function
LOKDET	0x0D[7]	42	0	R	Device Clock Management

Bit Name	Register	Page	Default	Type	Category
LV	0x1B[7:1]	76	0	R	Auxiliary A/D Converter Status
MASTER	0x23[6]	52	0	W	PCM Control Function
MATCH	0x19[6]	41	0	R	Line-Side Device Register Polling
OFH	0x12[7]	70	0	WO	DAA Control Function
OIDET	0x1E[4]	77	0	R	Over-Current Detection Control and Status
OLDET	0x1E[3]	77	0	R	Over-Load Detection Control and Status
OVDET	0x1E[5]	77	0	R	Over-Voltage Detection Control and Status
OVDTH	0x13[2]	77	0	WO	Over-Voltage Detection Control and Status
PCLKDT	0x03[4]	52	0	R	PCM Control Function
PCMEN	0x23[7]	52	0	W	PCM Control Function
PCODE	0x23[5:2]	53	0	W	PCM Control Function
PLDM	0x13[3]	70	0	WO	DAA Control Function
POL7	0x06[7]	43	0	W	GPIO Control Function
POL6	0x06[6]	43	0	W	GPIO Control Function
POL5	0x06[5]	43	0	W	GPIO Control Function
POLL	0x19[7]	40	0	W	Line-Side Device Register Polling
POLVAL	0x1F[7:0]	40	0	R	Line-Side Device Register Polling
PWDN	0x0F[6]	42	0	W	Power Management
RCS	0x22[5:3]	53	0	W	PCM Control Function
REVHSD	0x04[3:0]	41	0100	R	Device Revision
REVLSD	0x1D[7:4]	41	0	R	Device Revision
RGDT	0x03[0]	78	0	R	Ring Detection Function
RGMON	0x03[3]	78	0	R	Ring Detection Function
RGTH1/0	0x0E[1:0]	75	0	W	Ring Detection Function
RLPNEN	0x16[5]	71	0	W	DAA Control Function
RLPNH	0x14[2]	71	0	W	DAA Control Function
RNG	0x1A[7:0]	76	0	R	Auxiliary A/D Converter Status
RPOL	0x21[7]	53	0	W	PCM Control Function
RSTLSBI	0x0D[3]	62	0	W	Barrier Control Function
RTS	0x21[6:0]	53	0000000	W	PCM Control Function
RXBST	0x14[3]	75	0	WO	PCM Control Function
RXDG	0x09[7:0]	54	00000000	WO	PCM Control Function
RXEN	0x16[6]	54	0	WO	PCM Control Function
RXG0	0x14[0]	54	0	WO	PCM Control Function
RXG1	0x14[1]	54	0	WO	PCM Control Function
RXOCEN	0x17[5]	54	0	W	PCM Control Function
RXOM	0x25[7:0]	54	0	W	PCM Control Function
SLEEP	0x0F[5]	42	0	W	Power Management
SLHS	0x0D[6]	62	1	R	Barrier Control Function
SLLS	0x1E[2]	62	0	R	Barrier Control Function
SR	0x22[7]	55	0	W	PCM Control Function
SYNL	0x03[1]	62	0	R	Barrier Control Function
TCS	0x22[2:0]	55	0	W	PCM Control Function
THEN	0x15[3]	71	0	W	DAA Control Function
TMEN	0x02[7]	79	0	W	Loopback Control Function
TPOL	0x20[7]	55	0	W	PCM Control Function
TEST	0x18[7:4]	79	0	W	Loopback Control Function
TTS	0x20[6:0]	55	0000000	W	PCM Control Function
TXBST	0x14[7]	55	0	WO	PCM Control Function
TXDG	0x08[7:0]	56	00000000	WO	PCM Control Function
TXEN	0x16[7]	56	0	WO	PCM Control Function
UVDET	0x1E[6]	76	0	R	Under-Voltage Detection Control and Status

While all registers may be read or written to via an SPI operation without error, some registers react differently to read and write operations, as follows:

- Read/Write (W) registers change in response to an SPI write transaction and report their correct current value for a read SPI transaction.
- Read Only (R) registers do not change in response to an SPI write transaction but report their correct current value for a read SPI transaction.
- Write Only (WO) registers are shadow registers to corresponding registers on the Line-Side Device (0x12-0x18) that are written to during the barrier communications, and so are written to indirectly. The true contents of these Line-Side registers cannot be read directly from the shadow registers representing them, but these Line-Side registers can be read using the polling register described in 6.1. Certain events, such as lightning or voltage surges, could corrupt the contents of the Line-Side registers, so to verify their contents, the polling registers (0x19 and 0x1F) must be used.

6.1 Line-Side Device Register Polling

The Register Map as read from a 73M1x66B Host-Side Device consists of two groups. The first is the Host-Side Device registers (0x00 through 0x10 and 0x20 through 0x24) and the second is a copy of the Line-Side Device registers (0x12 through 0x1F).

As an extra degree of integrity, the 73M1x66B supports the ability to manually monitor the registers of its Line-Side Device. This is achieved by using the Manual Poll Function. The Line-Side registers that can be polled are 0x12 through 0x18 (index values 0x0-0x6 respectively).

The method is to write the offset address of the Line-Side Device register to be read into the INDX field. The value of this is the offset index from 0x12; that is, Register 0x12 is 0x0, 0x13 is 0x1, etc. The next step is to set the POLL bit, which causes the device to read the requested register from the Line-Side Device. The value of the requested Line-Side Device register is written by the Line-Side Device into POLVAL (0x1F). This value is compared with that of the Host-Side copy and, if they are the same, the MATCH bit is set to 1.

The values presented at MATCH and POLVAL are valid approximately 600 µs after a poll request, and are valid only after the POLL bit has been reset by the Host-Side Device.

Function Mnemonic	Register Location	Type	Description
INDX	0x19[3:0]	W	Index Address of the register to be manually polled with the results placed in POLVAL. This address should be cleared after the poll. Default = 0.
MATCH	0x19[6]	R	Polling Match 0 = No match. (Default) 1 = This read-only bit indicates that there is match with the corresponding polled register in the Host-Side Device. The result of the polling function can be read only after the POLL bit is reset to zero by the 73M1x66B.
POLL	0x19[7]	W	Polling Enable 0 = Polling disabled. (Default) 1 = Manually polls the control register in the Line-Side Device whose address is given by INDX. The Poll bit remains high until the MATCH result is available at which time it will be reset to 0 and the MATCH bit status can be read.
POLVAL	0x1F[7:0]	R	Polling Value When 73M1x66B is polled, the content of the Line-Side Device Register given by the offset address in INDX is placed in this register. Default = 0. This register can be read after the POLL bit has been reset to zero, indicating the result is ready.

7 Hardware Control Functions

This section describes the 73M1x66B capabilities with respect to its configuration and hardware pin control. These include features such as Device Revision, Interrupt Management, Power Management, Clock Control, General Purpose Input/Output (GPIO) and control of the Call Progress Monitor.

7.1 Device Revision

The 73M1x66B provides the device revision number for the Host-Side Device and the Line-Side Device.

For the 73M1x66B:

- Revision for the Host-Side Device is: 0100.
- Revision for the Line-Side Device is: 1101.

Function Mnemonic	Register Location	Type	Description
REVHSD	0x04[3:0]	R	Host-Side Device Revision These read only status bits indicate the revision of the 73M1x66B Host-Side Device (73M1906B).
REVLSD	0x1D[7:4]	R	Line-Side Device Revision These read-only status bits provide the Device ID for the 73M1x66B Line-Side Device (73M1916). When barrier is synchronized, REV has the value of 1101. When barrier is not synchronized, the value of the field is 0000.

7.2 Interrupt Control

The 73M1x66B supports a single interrupt that can be asserted under several configurable conditions. These include status of GPIOs, PCLKDT, RGMON, DET, SYNL and RGDT.

All interrupt sources that are enabled are ORed together to create the $\overline{INT}$ output signal. GPIO ports that are configured to be output will not generate interrupts.

When the $\overline{INT}$ pin goes active (low), the host should read the interrupt source Register 0x03, which is then automatically cleared after the read operation. An interrupt during wake-on-ring should be interpreted as the detection of a valid ring signal.

Address 0x03

Reset State E0h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GPIO7	GPIO6	GPIO5	PCLKDT	RGMON	DET	SYNL	RGDT

7.3 Power Management

The 73M1x66B supports three modes of power control for the device.

Normal mode	The 73M1x66B operates normally.
ENFEH = 0	In this mode the Host Side of the Barrier interface is disabled and the line side device is disabled. The Host side continues to operate normally.
Sleep mode	The device PLL is turned off and PCLK is propagated on the clock tree. The PCM DX and $\overline{TSC}$ outputs are tri-stated. Control and status registers of the Host side maintain their content.
Power Down	The device is shut down altogether. The registers remain accessible through the SPI. Control and status registers of the Host side maintain their content. To restart the PCM operations, the PCODE register must be set for the appropriate PCLK frequency value.

In all reduced power modes of operation the SPI interface remains active.

Function Mnemonic	Register Location	Type	Description
ENFEH	0x0F[7]	W	Enable Front End Host 1 = Enable Front End of the 73M1906B Host-Side Device. (Default) 0 = Disable Front End of the 73M1906B Host-Side Device.
PWDN	0x0F[6]	W	Power Down Mode 0 = Disable Power Down Mode. (Default) 1 = Enable Power Down Mode.
SLEEP	0x0F[5]	W	Sleep Mode 0 = Disable Sleep Mode. (Default) 1 = Enable Sleep Mode.

7.4 Device Clock Management

Function Mnemonic	Register Location	Type	Description
FRCVCO	0x0E[7]	W	Force VCO 0 = The system clock is the same as PCLK. (Default) 1 = The system clock is derived from locked PLL. This is set to 0 upon reset, Sleep or Power Down mode enabled.
LOKDET	0x0D[7]	R	Phase Locked Loop Lock Detect 0 = PLL is not locked. (Default) 1 = PLL is locked to PCLK.

7.5 GPIO Registers

Three user-defined I/O pins are provided in the 32-pin QFN package of the 73M1966B only. The pins are GPIO7, GPIO6 and GPIO5.

GPIO pins are not available on the 20-pin package of the 73M1966B.
GPIO pins are not available on the 42-pin package of the 73M1866B.

Each pin can be configured independently as either an input or an output by writing to the corresponding I/O Direction (DIR) register.

At power on and after a reset, the GPIO pins are initialized to a high impedance state to avoid unwanted current contention and consumption. The input structures are protected from floating inputs, and no output levels are driven by any of the GPIO pins.

The mapping of GPIO pins is designed to correspond to the bit location in their control and status registers.

The 73M1x66B supports the ability to generate an interrupt on the $\overline{INT}$ pin. The source can be configured to generate on a rising or a trailing edge. Only GPIO ports that are configured as inputs can be used to generate interrupts.

Function Mnemonic	Register Location	Type	Description
DIR	0x04[7:5]	W	GPIO Input/Output Select These control bits are used to designate the GPIO pins as either inputs or outputs. 0 = GPIO pin is defined as an output. 1 = GPIO pin is defined as an input. (Default)
GPIOn	0x03[7:5]	W	GPIO State These bits reflect the status of the GPIO7, GPIO6 and GPIO5 pins. If the DIR bit is reset, reading this field returns the logical value of the appropriate GPIOn pin as an input. If the DIR bit is set, the pins output the logical value as written.
ENGPIOn	0x05[7:5]	W	GPIO Enable Each of the GPIO enable bits in this register enables the corresponding GPIO bit as an edge-triggered interrupt source. If a GPIO bit is set to one, an edge (which edge depends on the value in the GIP register) of the corresponding GPIO pin will cause the $\overline{INT}$ pin to go active low, and the edge detectors will be rearmed when the GPIO data register is read.
POLn	0x06[7:5]	W	GPIO Interrupt Edge Selection Defines the interrupt source as being either on a rising or a falling edge of the corresponding GPIO pin. 0 = A rising edge will trigger an interrupt from the corresponding pin. (Default) 1 = A falling edge will trigger an interrupt from the corresponding pin.

7.6 Call Progress Monitor

For the purpose of monitoring activities on the line, a Call Progress Monitor is provided in the 73M1x66B. This audio output contains both transmit and receive data with configurable levels.

Function Mnemonic	Register Location	Type	Description
CMRXG	0x10[1:0]	W	Receive Path Gain Setting 00 – 0 dB (for full swing, AOUT=1.08 Vpk) (Default) 01 – -6 dB 10 – -12 dB 11 – MUTE
CMTXG	0x10[3:2]	W	Transmit Path Gain Setting 00 – 0 dB (for full swing, AOUT=1.08 Vpk) (Default) 01 – -6 dB 10 – -12 dB 11 – MUTE
CMVSEL	0x10[4]	W	Call Progress Monitor Voltage Reference Select Quiescent DC voltage select at AOUT. 0 = 1.5 Vdc. (Default) 1 = VCC/2 Vdc.

7.7 16 kHz Operation of Call Progress Monitor

After switching from 8 kHz sampling rate to 16 kHz sampling rate, the SLEEP bit must be enabled then disabled if the Call Progress Monitor function is used. After cycling the SLEEP bit, the Line-Side Device registers (Registers 0x12 to 0x18) must be reconfigured.

7.8 Device Reset

For a correct reset of the 73M1x66B, the $\overline{RST}$ signal must be asserted for a minimum period of 1 ms. PCLK must be active for a minimum of 8 clock cycles before the $\overline{RST}$ signal can be de-asserted. The PLL locks to the PCLK after 20 PCM frames as defined by the occurrence of the Frame Sync Signal (FS). This gives a minimum period of 3.5 ms from the assertion of $\overline{RST}$ until the PLL is locked and normal operations may occur, including access to all device registers and the transmission and reception of PCM data samples. If PCLK changes frequency, then the PLL will lose lock so a stable clock must be used during this reset period. If a PCLK frequency change is required after the reset, the user should implement the procedure described for PCODE (Register 0x23 bits 2 to 5).

8 PCM Highway Interface and Signal Processing

The PCM highway is the method by which the 73M1x66B exchanges PCM data with the host or other PCM-enabled devices. The PCM data can be in either 8-bit compressed mode or in 16-bit linear mode. Compression of the received signals from the PSTN line interface is selectable A-law or µ-law, as specified by *ITU-T Recommendation G.711*. The 73M1x66B is configurable with respect to tuning the clock and time slot relationships. See Section 8.1 for details.

The PCM interface provided by the 73M1x66B consists of the following signals:

- PCLK The frequency at which bits are driven on the PCM highway. (Goes to the PCLKI pin.)
- $\overline{FS}$ PCM frame synchronization pulse.
- DX PCM data transmitted to the PCM highway.
- DR PCM data received from the PCM highway.

The basic timing relationship of PCM highway interface signals is shown in Figure 20.

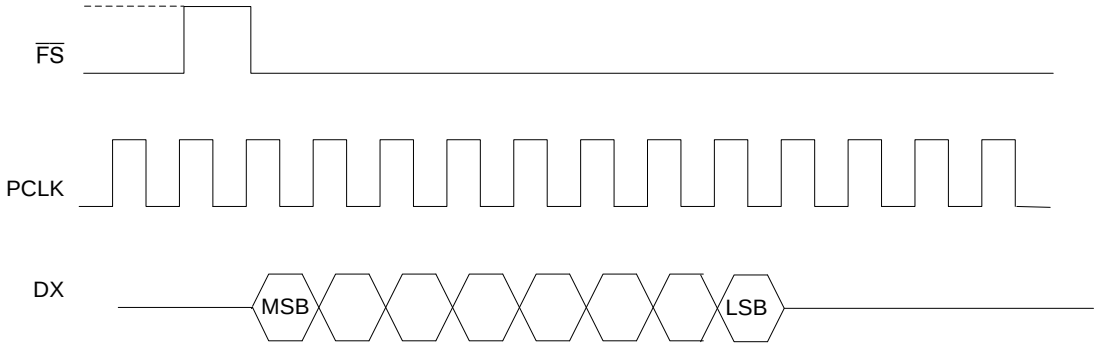


Figure 20: 8-bit Transmission Example

8.1 PCM Highway Interface Timing

Signal $\overline{FS}$ defines the frame boundaries by being asserted at a rate of 8 kHz. The duration of $\overline{FS}$ is defined by the setup and hold times around the falling edge of PCLK and can be extended to multiple PCLK cycles. The timing relationship between $\overline{FS}$ and PCLK is determined by the rising edge of $\overline{FS}$ and the first falling edge of PCLK that follows the $\overline{FS}$ rising edge. PCLK and $\overline{FS}$ are common to all devices connected to the PCM highway. The ratio of PCLK frequency to $\overline{FS}$ frequency determines the number of bit slots available during a frame, i.e., the number of bits per frame. The number of bit slots divided by 8 is the number of 8-bit time slots available during the frame.

$$\frac{\text{PCLK Frequency}}{\overline{FS}\text{ Frequency (8 kHz)}} = \text{Bits per Frame} \qquad \frac{\text{Bits per Frame}}{\text{8-bits per Time Slot}} = \text{Number of Time Slots per Frame}$$

Refined granularity to the time slot can be achieved by programming the clock slot offset. The clock slot defines an offset in terms of the number of bits from the start of the time slot. The combination of the transmit and receive time slot and clock slot registers determines the bit slot at which the 73M1x66B begins transmitting or receiving a data sample. Adjustments of a half clock period can be made using these controls in conjunction with TPOL and RPOL.

The 73M1x66B supports a 16-bit linear transmission and receive mode. The transmission and reception of the data samples consumes two adjacent 8-bit time slots each on the PCM highway. The 16-bit data sample is transmitted most significant bit first starting at the bit slot defined by the TTS and TCS controls. The transmission lasts for 16 consecutive bit slots, as illustrated in Figure 21.

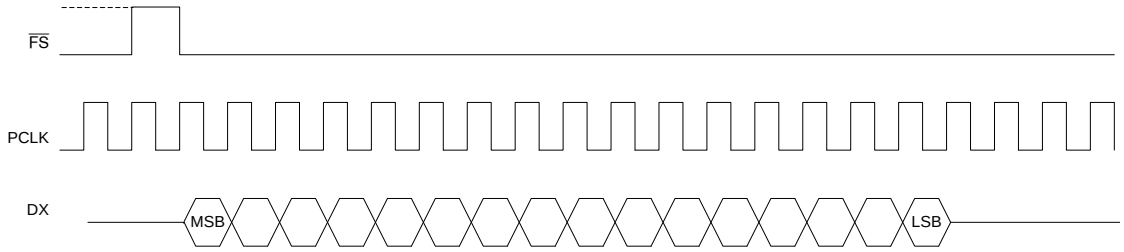


Figure 21: 16-bit Transmission Example

Similarly, the 16-bit data sample is received most significant bit first, beginning at the bit slot defined by the RTS and RCS control registers. The reception lasts for 16 consecutive bit slots.

SR selects between 8 kHz and 16 kHz sampling rates. However, $\overline{FS}$ remains constant at 8 kHz. Therefore, in 16 kHz sampling mode, two data samples are transmitted to (or received from) the PCM highway starting at the bit slot dictated by the time and clock slot registers. In 16 kHz mode, either two or four adjacent 8-bit time slots are used for two compressed 8-bit data samples or two linear 16-bit data samples, respectively. The 16 kHz mode is enabled by setting SR=1 followed by SEL16K=1.

When switching to 16 kHz sampling rate and if the Call Progress Monitor function is being used, the Line-Side Device needs to be reconfigured. See Section 7.7.

PCM highway interfaces are designed such that a device can transmit and receive to other devices on the PCM highway. For example, Codec A will use a time slot assignment for its transmit to the PCM highway and Codec B will assign its receiver to the same time slot. The time slot assignment is such that if Codec A wants to transmit its data sample to Codec B, then Codec A transmit time/clock slot value is identical to the Codec B receive time/clock slot value.

The 73M1x66B uses the DX signal pin to transmit to the PCM highway and the DR signal pin to receive from the PCM highway. Figure 22 illustrates a typical example.

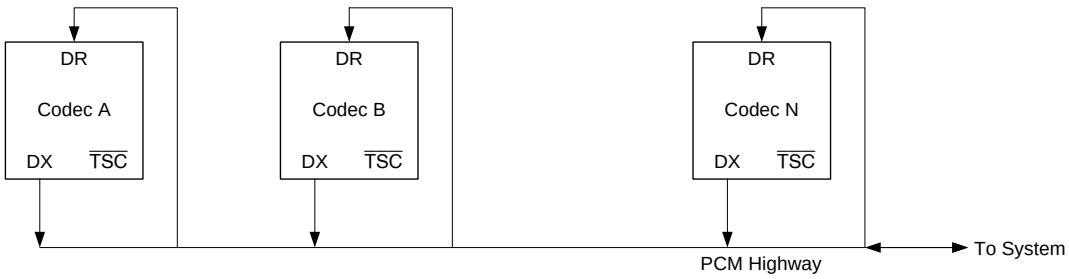


Figure 22: Example of PCM Highway Interconnect

Larger systems may use buffers to interconnect multiple segments of the PCM highway (across line cards for instance). In the 73M1x66B, Control $\overline{TSC}$ is used to control the tri-state mode of the transmit side of the PCM highway as shown in Figure 23. $\overline{TSC}$ is asserted (active low) for the duration of the time slot during which the 73M1x66B is transmitting to the PCM highway.

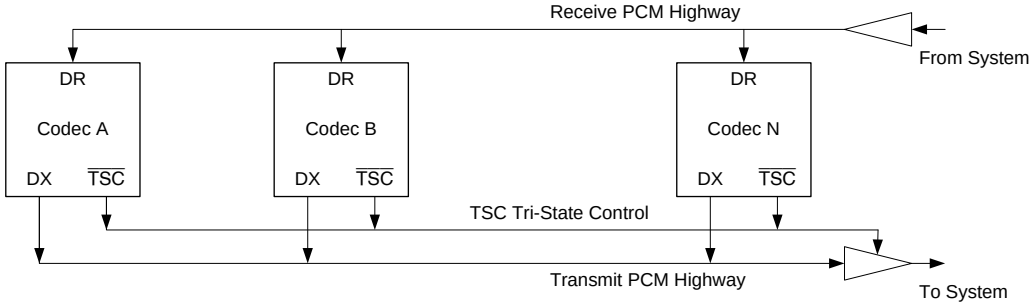


Figure 23: Example of PCM Highway Interconnect for Typical Large Systems

8.2 PCM Clock Frequencies

The 73M1x66B supports the following PCLK input frequencies:

- 256 kHz
- 512 kHz
- 768 kHz
- 1.024 MHz
- 1.536 MHz
- 1.544 MHz
- 2.048 MHz
- 3.088 MHz
- 4.096 MHz
- 6.176 MHz
- 8.192 MHz

The 73M1x66B automatically detects the frequency of PCLK and adjusts its internal PLL parameters accordingly. At startup, the first eight frames are discarded. The next eight frames are used to count the number of PCLK cycles during each frame. If the count differs among these eight frames or if the count is a non-supported value, then a PCLKDT interrupt is asserted.

If PCLK is set at a frequency different from the above list, the PLL will be set for a PCLK of 2.048 MHz. Since there will be a discrepancy between the frequency of PCLK and the frequency considered for PLL settings, a PCLKDT interrupt may occur if required. It takes about 20 PCM frames before PLL is locked, which is shown through the assertion of the FRCVCO status bit. PCLK must be running for several cycles when reset is de-asserted. After that point, SPI transactions can start.

8.3 Master Mode

The default mode of operation for the PCM highway in the 73M1x66B is the slave mode i.e., $\overline{FS}$ and PCLK are inputs to the device. The 73M1x66B offers a master mode by which a 4.096 MHz clock is applied to the PCLKI pin. The master clock is divided by two to generate a 2.048 MHz clock that is connected to the PCM highway via the PCLKO pin. Similarly, $\overline{FS}$ of one 2.048 MHz period long is generated and driven to the PCM highway.

The master mode is set by setting the MASTER bit.

8.4 A-law / µ-law Compander

The 73M1x66B may be programmed for compressed A-law mode, compressed µ-law mode, or linear mode. Compression schemes are used to minimize the bandwidth required for exchanging data samples on the PCM highway. For instance, when PCLK is 8.192 MHz there are 128 8-bit time slots available. The density of the overall system is halved when working in linear mode, which requires 16-bit time slots.

The 73M1x66B fully complies with the A-law and µ-law companding specifications defined in the *ITU-T Recommendation G.711*.

8.5 Transmit and Receive Levels

8.5.1 A-Law

According to the *ITU-T Recommendation G.711*, A-law assumes +4096 (in sign plus 12 bit) to represent 3.14 dBm. That is, a sinusoid having a peak value of +4095 to correspond to +3.14 dBm or 1.1119 Vrms or 1.5725 Vpk or 3.145 Vpp.

Figure 24 shows the mapping implied in the *ITU-T Recommendation G.711*. Therefore, one least significant bit in 16-bit code is equivalent to:

$$LSB = \frac{1.5725V}{2^{15} - 8} = 48.0\mu V / bit$$

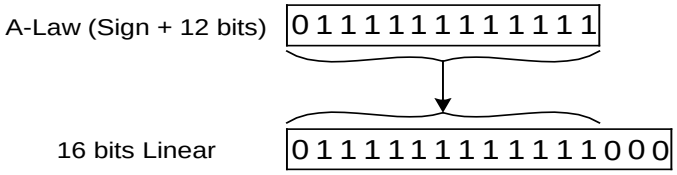


Figure 24: Mapping of A-law Code to 16-bit Code

For A-law, 0 dBm=774.6 mVrms=1.095 Vp (sinusoid) implies a peak code of 22,821=5925h.

8.5.2 µ-Law

Similarly, µ-Law assumes +8159 (in sign plus 13 bit) to represent 3.17 dBm. That is, a sinusoid having a peak value of +8159 to correspond to +3.17 dBm or 1.1157 Vrms or 1.578 Vpk or 3.156 Vpp.

Figure 25 shows the mapping implied in the *ITU-T Recommendation G.711*. Therefore, one least significant bit in 16-bit code is equivalent to:

$$LSB = \frac{1.578V}{32636} = 48.35\mu V / bit$$

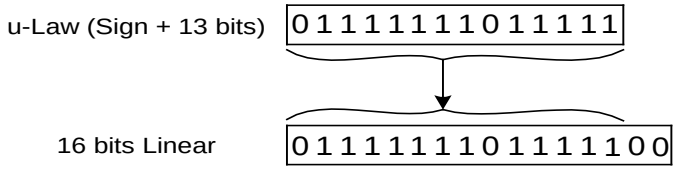


Figure 25: Mapping of µ-law Code to 16-bit Code

For µ-law, 0 dBm=774.6 mVrms=1.095 Vp (sinusoid) implies a peak code of 22,647=5876h.

8.5.3 Transmit and Receive Level Control

The 73M1x66B provides digital and analog control over the gains of transmit and receive signal. The overall transmit gain adjustment is +13.4 dB to –26 dB and the range of the receiver gain is +10.4 dB to –24 dB. Both gain adjustments are in steps of 0.125 dB. Optimal performance on how the overall gain is to be achieved requires the appropriate management of the gain elements in the signal paths.

8.6 Transmit Path Signal Processing

8.6.1 General Description

In the transmit path, data is first sent by the host DSP through a serial interface to the 73M1x66B then interpolated by an interpolation filter, serialized and transmitted across barrier interface to the Line-Side Device, which is floating relative to the Host-Side Device earth ground. The data received on the Line-Side Device is then de-serialized and digitally sigma-delta modulated to a one-bit data stream of 1.536 Mbps for a sample frequency of 8 kHz or 3.072 Mbps for a sample frequency of 16 kHz. The signal is further filtered first by a switched capacitor filter and then a continuous time anti-aliasing circuit.

- The 0.2 dB pass-band ripple frequency is from dc to 3.422 kHz for an 8 kHz sample rate or 6.844 kHz for a 16 kHz sample rate.
- The 3 dB bandwidth is 3.65 kHz for an 8 kHz sample rate or 7.299 kHz for a 16 kHz sample rate.

8.6.2 Total Transmit Path Response

Figure 26 and Figure 27 show the transmit path frequency response. The response shape is the same, but the frequencies double for a 16 kHz sample rate.

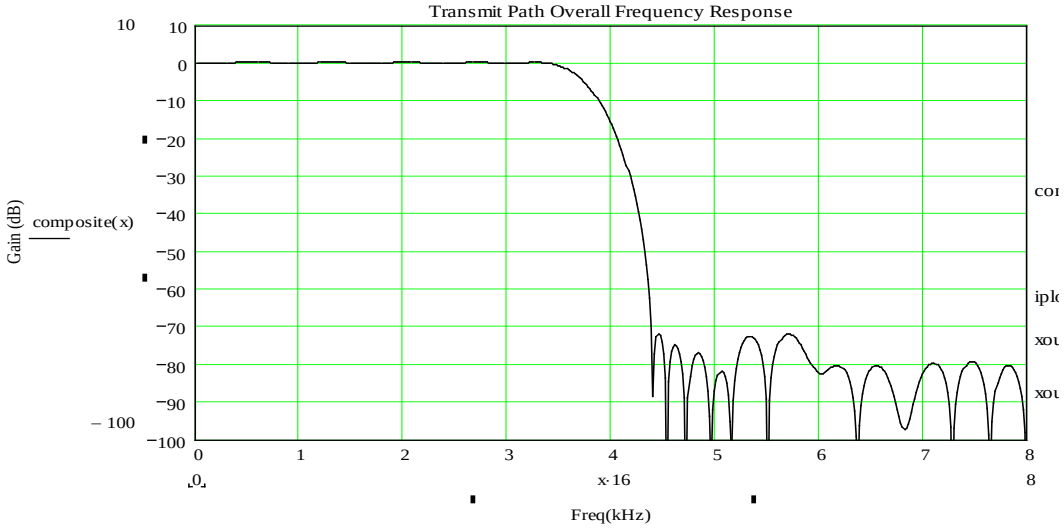


Figure 26: Transmit Path Overall Frequency Response to Fs of 8 kHz

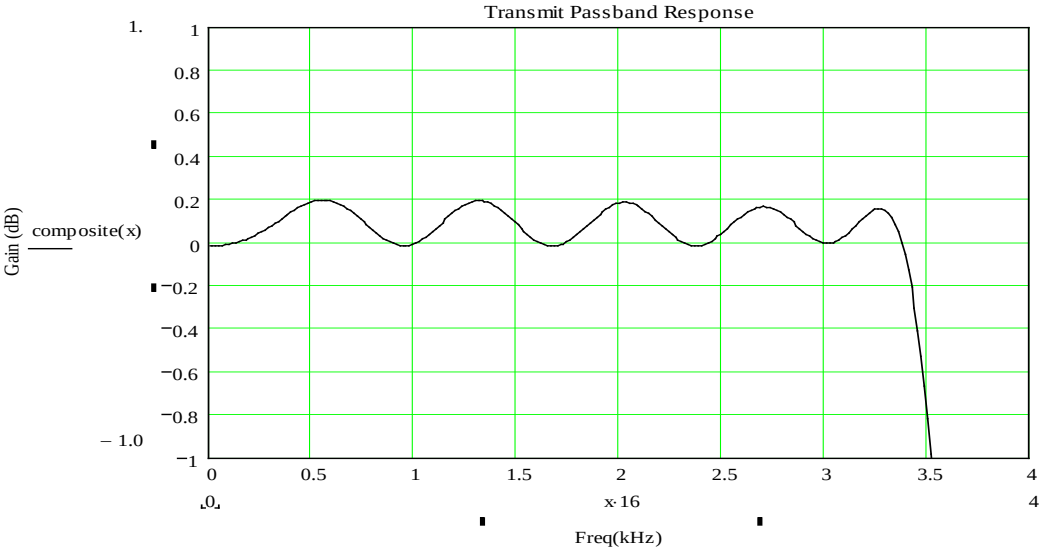


Figure 27: Transmit Path Passband Response for an 8 kHz Sample Rate

8.6.3 73M1x66B Transmit Spectrum

Figure 28 shows the transmit spectrum observed on the line from dc to 32 kHz for a sample frequency (Fs) of 8 kHz. The transmit signal is band-limited (by default) to Fs/2=4 kHz and is flat (with 0.2 dB ripple) to 3.65 kHz and is marked as Txdb(x) in the figure. All frequencies double for a 16 kHz sample rate

Also shown, and marked as signaldb(x), is the baseband signal from 1 kHz to 2 kHz for an 8 kHz sample rate (2 kHz to 4 for a 16 kHz sample rate). The aliases of signaldb(x) are shown as aliasdb(x) and are attenuated significantly with better than 80 dB attenuation at 8 kHz, better than 60 dB at 16 kHz, better than 100 dB at 24 kHz, etc for an 8 kHz sample rate and the frequencies double for a 16 kHz sample rate.

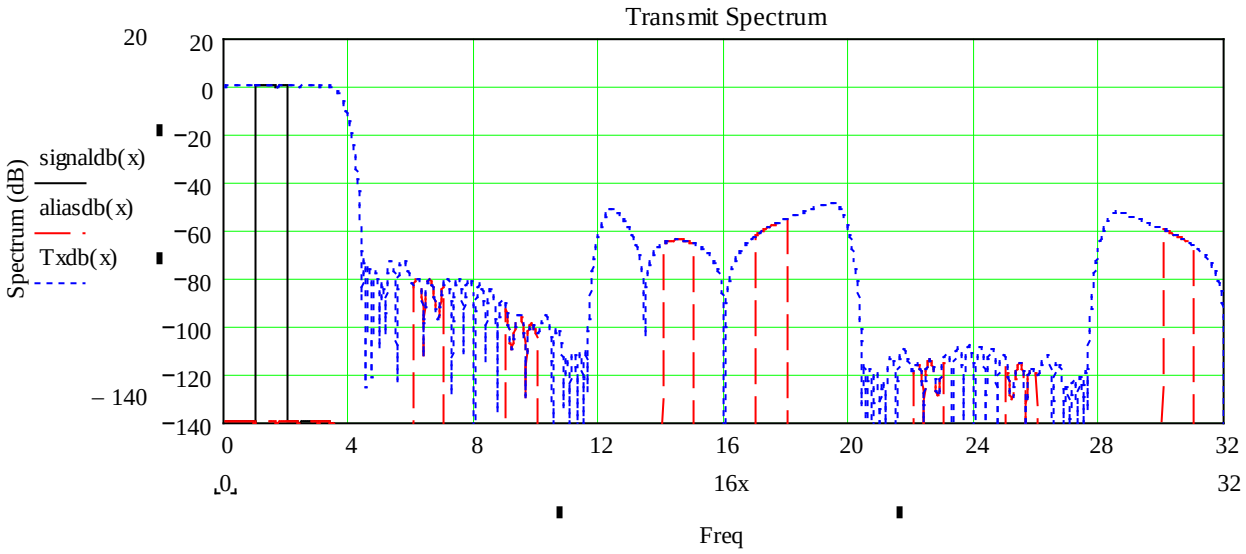


Figure 28: Transmit Spectrum to 32 kHz for an 8 kHz Sample Rate

8.7 Receive Path Signal Processing

8.7.1 General Description

In the receive path, the signal from the telephone line is input to the anti-aliasing filter and passed through a selectable low pass (notch) filter, which can be used to attenuate in-band Billing Tones. The analog signal is digitized by a sigma-delta analog to digital converter. The resulting high frequency one-bit data stream is decimated and sent to the Host-Side Device via the barrier. Another decimation FIR filter in the Host-Side Device filters the received data and sends it to the host DSP for processing.

The response of the receive path, in conjunction with the decimation filter in the Host-Side Device, provides a flat pass-band response to 3.342 kHz at an 8 kHz sample rate or 6.744 kHz with a 16 kHz sample rate with 0.2 dB ripple. The 3 dB bandwidth is 3.58 kHz at 8kHz sample rate or 7.226 kHz at a 16 kHz sample rate. . The one-bit data stream is 1.536 Mbps for an 8 kHz sample rate or 3.072 Mbps with a 16 kHz sample rate.

8.7.2 Total Receive Path Response

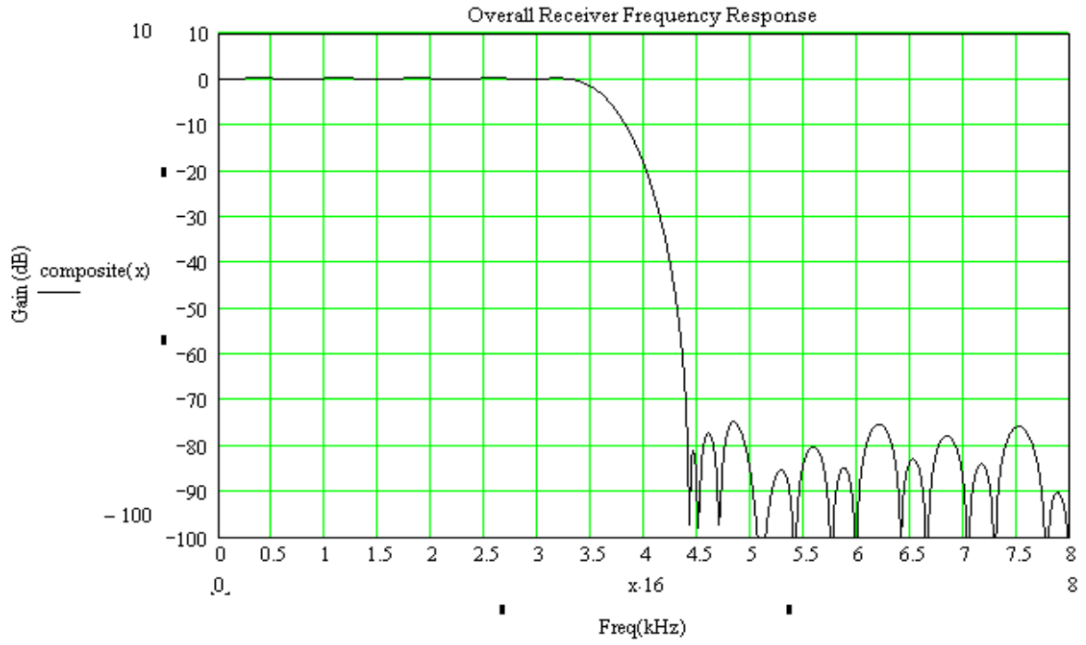


Figure 29: Overall Frequency Response of the Receive Path

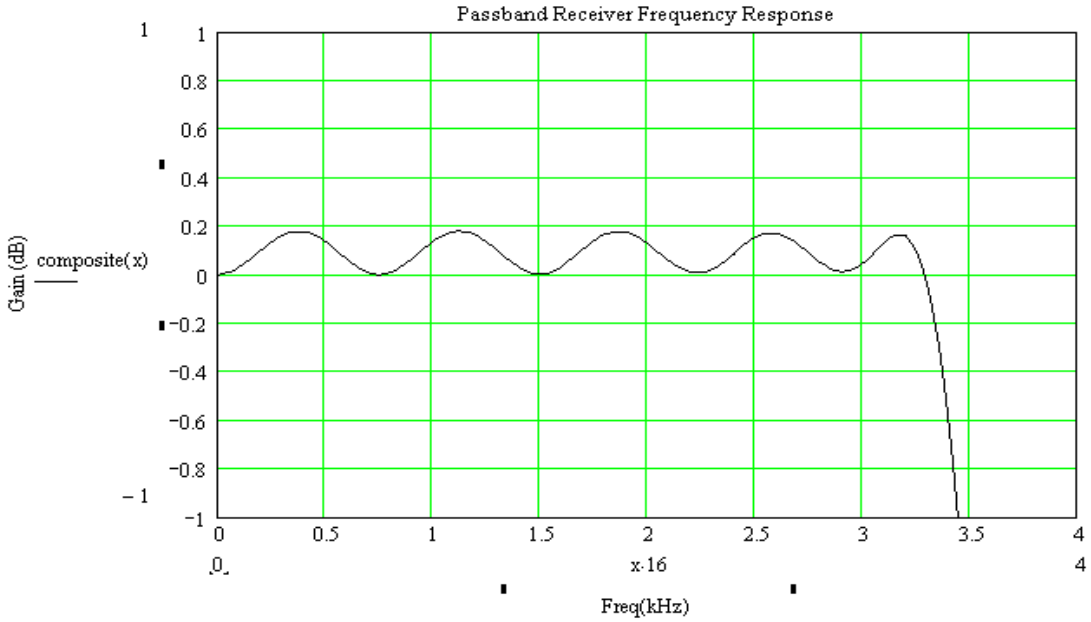


Figure 30: Pass-band Response of the Overall Receive Path

8.7.3 Receiver DC Offset Subtraction

The 73M1x66B provides a method to improve audio quality by reducing unwanted DC offset from the receiver signal path in A-law or µ-law compression modes. This method requires that a signal path calibration be performed. This calibration is benign to the performance of the device and is only required after an initialization or device reset sequence. Receiver DC offset calibration can only be executed when the device is on-hook and not in linear mode, otherwise the process will disturb signal quality. See the *73M1866B/73M1966B Implementer's Guide* for the steps to enable the calibration of receive DC offset.

8.8 PCM Control Functions

Table 33: PCM Control Functions

Function Mnemonic	Register Location	Type	Description
ADJ	0x22[6]	W	Adjacent Time Slot Driver Control Allows LSB of the PCM frame (DX) to be tri-stated during the second half of the clock cycle. This feature allows adjacent time slots to be used by different devices without risking a contention at the time slot boundary. 0 = Drives DX during the entire bit time. (Default) 1 = Drives DX only during the first half of bit time.
DAA	0x14[6:5]	W	DAA Transmit Gain Used in conjunction with TXBST to manage transmit level. See Section 8.8.1.
ENPCLKDT	0x05[4]	W	Enable PCLK Error Detection Interrupt 0 = Disables this function. 1 = Enables the detection of an interrupt resulting from an incoherency in the PCLK count during the second set of eight frames received after power up. (Default)
LAW	0x23[0]	W	Law Compression Mode Selects the PCM compression mode. 0 = Selects the A-law compression mode. (Default) 1 = Selects the µ-law compression mode.
LIN	0x23[1]	W	Linear Mode Enable 0 = The compression modes of either A-law or µ-law are enabled. (Default.) See the LAW bit. 1 = 16-bit linear mode.
MASTER	0x23[6]	W	Master/Slave Mode The 73M1x66B is in Slave Mode by default. See Section 8.3 for details of master and slave operation. 0 = Enables Slave Mode. (Default) 1 = Enables Master Mode.
PCLKDT	0x03[4]	R	PCLK Detect Error PCLKDT is an interrupt resulting from the detection of two possible events: 1. The number of PCLK periods per frame is not consistent among the second set of eight frames after power up. 2. The number of PCLK periods per frame does not equate to any of the acceptable PCLK frequencies. This is a maskable interrupt. It is enabled by the ENPCLKDT bit. See Section 7.2.
PCMEN	0x23[7]	W	PCM Transmit Enable Controls DX and $\overline{TSC}$. This bit must be set on completion of all configuration changes to enable transmission on to the PCM highway. When powered up, the 73M1x66B PCM outputs are tri-stated. The host must set PCMEN after setting the time/clock slot control bits to avoid contention on the PCM highway.

<table>
<tr><th>Function Mnemonic</th><th>Register Location</th><th>Type</th><th>Description</th></tr>
<tr><td>PCODE</td><td>0x23[5:2]</td><td>W</td><td>PCM Clock Code
The default state of PCODE out of reset is 0000. In PCM Slave Mode at reset, the device will attempt to automatically detect the correct frequency of PCLK. If the PCLK frequency is different from those listed in the table below or an incorrect PCODE value is written, the PLL will not lock (LOCKDET 0x0D[7] == 0). To modify the value of PCODE, first write a value of 0000 and then write the required PCODE value. Toggling of the MASTER bit 0x23[6] (0 →1 → 0) with a PCODE of 0000 will also restart the automatic PCLK frequency detection function.

<table>
<tr><th>PCLK Frequency</th><th>PCODE [3:0]</th></tr>
<tr><td>256 kHz</td><td>0001</td></tr>
<tr><td>512 kHz</td><td>0010</td></tr>
<tr><td>768 kHz</td><td>0011</td></tr>
<tr><td>1.024 MHz</td><td>0100</td></tr>
<tr><td>1.536 MHz</td><td>0101</td></tr>
<tr><td>1.544 MHz</td><td>0110</td></tr>
<tr><td>2.048 MHz</td><td>0111</td></tr>
<tr><td>3.088 MHz</td><td>1000</td></tr>
<tr><td>4.096 MHz</td><td>1001</td></tr>
<tr><td>6.176 MHz</td><td>1010</td></tr>
<tr><td>8.192 MHz</td><td>1011</td></tr>
</table>
</td></tr>
<tr><td>RCS</td><td>0x22[5:3]</td><td>W</td><td>Receive Clock Slot
These bits control the starting clock of the receive channel. The clock slot value allows the adding of an offset of up to 7 (111) bits to the time slot value. A value of 000 is zero offset.</td></tr>
<tr><td>RPOL</td><td>0x21[7]</td><td>W</td><td>Receive Polarity
0 = The receive PCM data is to be sampled on the falling edge of PCLK. (Default)
1 = The receive PCM data is to be sampled on the rising edge of PCLK.</td></tr>
<tr><td>RTS</td><td>0x21[6:0]</td><td>W</td><td>Receive Time Slot
Selects the time slot number on the PCM highway for the receiver. The maximum number of 8-bit time slots is 128 (with a PCLK frequency of 8.192 MHz). A value of 0000000 is time slot zero and 1111111 is time slot 128. The default is 0000000.</td></tr>
</table>

<table>
<tr><th>Function Mnemonic</th><th>Register Location</th><th>Type</th><th>Description</th></tr>
<tr><td>RXDG</td><td>0x09[7:0]</td><td>WO</td><td>Receiver Digital Gain
These bits controls the value of the digital gain section of the 73M1x66B receive path. Each bit indicates either a gain or attenuation value. The net value of the gain setting is the linear sum of each attributed value. Reading the RXDG register returns all zeros, regardless of what was written to them.

<table>
<tr><th>RXDG –12dB</th><th>RXDG –6dB</th><th>RXDG +3.5dB</th><th>RXDG +2dB</th><th>RXDG +1dB</th><th>RXDG +0.5dB</th><th>RXDG +0.25dB</th><th>RXDG +0.125dB</th><th>Gain/Attenuate</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0dB (default)</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>-12 dB</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>-6 dB</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>+3.5 dB</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>+2 dB</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>+1 dB</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>+0.5 dB</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>+0.25 dB</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>+0.125 dB</td></tr>
</table>

Examples:
10000000 -12dB
00100000 +3.5dB
00010011 +2 + 0.25 + 0.125 =2.375dB
01001000 -6 + 1 = -5dB</td></tr>
<tr><td>RXEN</td><td>0x16[6]</td><td>W</td><td>Receive Path Enable
1 = Enable Receive Path.
0 = Disable Receive Path. (Default)</td></tr>
<tr><td>RXG</td><td>0x14[1:0]</td><td>W</td><td>Receive Gain
Sets the receive path gain/attenuation. See Table 36.</td></tr>
<tr><td>RXOCEN</td><td>0x17[5]</td><td>W</td><td>Rx DC Offset Calibrate Enable
When RXOCEN is set to 1 and OFH, ENDC and ENNOM are reset to 0, the receiver dc offset calibration process is enabled. RXOCEN must be reset to 0 before OFH, ENDC and ENNOM are set to 1 in order for the calibration to operate correctly. RXOCEN should not be used in linear mode.

Default value is 0.</td></tr>
<tr><td>RXOM</td><td>0x25[7:0]</td><td>W</td><td>RX Offset Measurement
Stores the result of the receive offset measurement.
See Section 8.8.3.</td></tr>
</table>

Function Mnemonic	Register Location	Type	Description
SEL16K	0x13[0]	W	Sample Rate Mode Configuration Select Configures the 16 kHz mode of operation. See also SR. 0 = 8 kHz sampling rate. (Default) 1 = 16 kHz sampling rate. The 16 kHz mode is enabled by setting SR=1 followed by SEL16K=1.
SR	0x22[7]	W	Sampling Rate Mode Enables the 16 kHz mode of operation. See also SEL16K. 0 = 8 kHz sampling rate. (Default) 1 = 16 kHz sampling rate. The 16 kHz mode is enabled by setting SR=1 followed by SEL16K=1.
TCS	0x22[2:0]	W	Transmit Clock Slot Controls the starting clock of the transmit channel. The clock slot value allows the adding of an offset of up to 7 (111) bits to the time slot value. A value of 000 is zero offset.
TPOL	0x20[7]	W	Transmit Polarity 0 = The transmit PCM data is to be transmitted based on the falling edge of PCLK. (Default) 1 = The transmit PCM data is to be transmitted based on the rising edge of PCLK.
TTS	0x20[6:0]	W	Transmit Time Slot Selects the time slot number on the PCM highway for the transmitter. The maximum number of 8-bit time slots is 128 (with a PCLK frequency of 8.192 MHz). A value of 0000000 is time slot zero and 1111111 is time slot 128. The default is 0000000.
TXBST	0x14[7]	WO	Transmit Boost Used in conjunction with DAA to manage transmit level. See Section 8.8.1.

<table>
<tr><th>Function Mnemonic</th><th>Register Location</th><th>Type</th><th>Description</th></tr>
<tr><td>TXDG</td><td>0x08[7:0]</td><td>WO</td><td>Transmitter Digital Gain
These bits control the value of the digital gain section of the 73M1x66B transmit path. Each bit indicates either a gain or attenuation value. The net value of the gain setting is the linear sum of each attributed value. Reading the TXDG register returns all zeros, regardless of what was written to them.

<table>
<tr><th>TXDG –12dB</th><th>TXDG –6dB</th><th>TXDG +3.5dB</th><th>TXDG +2dB</th><th>TXDG +1dB</th><th>TXDG +0.5dB</th><th>TXDG +0.25dB</th><th>TXDG +0.125dB</th><th>Gain/Attenuate</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0 dB (default)</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>-12 dB</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>-6 dB</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>+3.5 dB</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>+2 dB</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>+1 dB</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>+0.5 dB</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>+0.25 dB</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>+0.125 dB</td></tr>
</table>

Examples:
10000000 -12dB
00100000 +3.5dB
00010011 +2 + 0.25 + 0.125 =2.375dB
01001000 -6 + 1 = -5dB</td></tr>
<tr><td>TXEN</td><td>0x16[7]</td><td>WO</td><td>Transmit Path Enable
1 = Enable Transmit Path.
0 = Disable Transmit Path. (Default)</td></tr>
</table>

8.8.1 Transmit and Receive Level Control

Refer to Section 8.5 for information about 73M1x66B levels.

8.8.1.1 Transmit Gain Scaling

The first gain stage in the transmit signal path is the digital gain whose value is controlled by writing to Register 0x08 (TXDG). The second gain stages are the analog gains that are controlled by Register 0x14[7] (TXBST) and Register 0x14[6:5] (DAA). As a general rule to prevent clipping of the analog gain stages, it is important to choose a value of the digital gain such that the transmit data after multiplied by TXDG does not exceed +1.25 dBm. So for correct use of the gain controls the appropriate mix of digital and analog settings must be used. Generally speaking, for best S/N performance, it is advisable to make the digital words, after digital gain scaling, as large as possible without going over the +1.25 dBm limit.

Example:

If +2 dBm transmit level is desired for the case where the maximum input is 0 dBm:

Set analog gain to +3 dB (i.e. TXBST and DAA = 0) add attenuation of –1 dB by setting TXDG to 01101100 (-6 + 3.5 + 1 + 0.5 = -1); therefore, +3 - 1 = +2. Note in this case any digital gain could cause clipping at high input levels in the analog circuitry.

Table 34 lists transmit level analog gain adjustment settings based upon the values of TXBST and DAA.

Table 34: Transmit Gain Control

TXBST 0x14[7]	DAA1 0x14[6]	DAA0 0x14[5]	Gain, Nom. (dB)
0	0	0	+3.0
0	0	1	0.0
0	1	0	-4.0
0	1	1	-8.0
1	0	0	+6.0
1	0	1	+6.0
1	1	0	+2.0
1	1	1	-2.0

Table 35 shows a recommended gain settings for various transmit levels. With 0 dBm of Tx Data and default setting of DAA1:0 = 01, Txbst=0, TXDG=00h, the transmit level is slightly off at –0.25 dBm. TXDG=00000010 is required to achieve 0 dBm transmit level. For Tx level > 6 dBm, Tx Data is assumed less than 0 dBm such that the product of Tx Data and TXDG is less than 1.25 dBm.

Table 35: Recommended Gain Setting

TX Level	Analog Gain				Digital Gain		Ana+Dig
dBm	TxBst	DAA1	DAA0	dB	TXDG	dB	dB
-26	0	1	1	-8	1100_0010	-17.75	-25.75
-25	0	1	1	-8	1100_1010	-16.75	-24.75
-24	0	1	1	-8	1101_0010	-15.75	-23.75
-23	0	1	1	-8	1101_1010	-14.75	-22.75
-22	0	1	1	-8	1110_0110	-13.75	-21.75
-21	0	1	1	-8	1110_1110	-12.75	-20.75
-20	0	1	1	-8	1000_0010	-11.75	-19.75
-19	0	1	1	-8	1000_1010	-10.75	-18.75
-18	0	1	1	-8	1001_0010	-9.75	-17.75

TX Level	Analog Gain				Digital Gain		Ana+Dig
dBm	TxBst	DAA1	DAA0	dB	TXDG	dB	dB
-17	0	1	1	-8	1001_1010	-8.75	-16.75
-16	0	1	1	-8	1010_0110	-7.75	-15.75
-15	0	1	1	-8	1010_1110	-6.75	-14.75
-14	0	1	1	-8	0100_0010	-5.75	-13.75
-13	0	1	1	-8	0100_1010	-4.75	-12.75
-12	0	1	1	-8	0101_0010	-3.75	-11.75
-11	0	1	1	-8	0101_1010	-2.75	-10.75
-10	0	1	1	-8	0110_0110	-1.75	-9.75
-9	0	1	1	-8	0110_1110	-0.75	-8.75
-8	0	1	1	-8	0000_0010	0.25	-7.75
-7	0	1	1	-8	0000_1010	1.25	-6.75
-6	0	1	0	-4	0110_0110	-1.75	-5.75
-5	0	1	0	-4	0110_1110	-0.75	-4.75
-4	0	1	0	-4	0000_0010	0.25	-3.75
-3	0	1	0	-4	0000_1010	1.25	-2.75
-2	1	1	1	-2	0000_0010	0.25	-1.75
-1	0	0	1	0	0110_1110	-0.75	-0.75
0	0	0	1	0	0000_0010	0.25	0.25
1	0	0	1	0	0000_1010	1.25	1.25
2	1	1	0	2	0000_0010	0.25	2.25
3	0	0	0	3	0000_0010	0.25	3.25
4	0	0	0	3	0000_1010	1.25	4.25
5	1	0	0	6	0110_1110	-0.75	5.25
6	1	0	0	6	0000_0010	0.25	6.25
Note (1)	1	0	0	6	0000_1010	1.25	7.25
Note (1)	1	0	0	6	0001_0010	2.25	8.25
Note (1)	1	0	0	6	0001_1010	3.25	9.25
Note (1)	1	0	0	6	0010_0110	4.25	10.25
Note (1)	1	0	0	6	0010_1110	5.25	11.25
Note (1)	1	0	0	6	0011_0110	6.25	12.25

Note 1. Tx Data is assumed small enough that the combination of Tx Data and TXDG is less than 1.25 dBm.

8.8.1.2 Receive Gain Scaling

On the receive side, a 0 dBm receive signal on the line results in ~0 dBm at the PCM interface.

Means is provided to adjust receive signal path gain by use of a digital gain stage. This gain value is controlled by Register 0x09[7:0] (RXDG). The gain values are explained in Table 33.

The two RXG bits (Register 0x14[1:0]) control the value of the receiver analog gain. The RXG bits must be set to 10 to enable 0 dB gain in the receive path.

For the best S/N performance it is recommended to use a gain value up front in the analog domain. The digital control should be used to fine-tune the receiver signal path gain.

When the received line signal exceeds a voltage level greater than specified by *ITU-T Recommendation G.711*, the receive gain must be reduced to prevent saturation and clipping within the receive signal processing path.

Table 36 lists the value of Receive Gain for each value of RXG.

Table 36: Receive Gain Control

RXG1 0x14[1]	RXG0 0x14[0]	Gain Nom (dB)
0	0	-6.0
0	1	-3.0
1	0	0.0
1	1	+3.0

The precise values of the digital gain settings are:

Bit	7	6	5	4	3	2	1	0
Gain	0.25	0.5	1.5	1.25	1.125	1.0625	1.03125	1.015625
Gain / Attenuation	-12.04dB	-6.02dB	3.52dB	1.94dB	1.02dB	0.53dB	0.27dB	0.13dB

8.8.1.3 Maximum Levels

The 73M1x66B is capable of providing gain attenuation in both the digital and analog domain. It is important to note that for optimum performance the transmitter output and receiver input should not exceed more than +7.25 dBm. Signal levels that are greater than this will cause distortion and reduced performance.

This implies that the maximum input signal capable by the transmitter, if adjusted for unity gain, is the +7.25 dBm, e.g. digital gain of -6.0 dB (ensures analog input is less than +1.25 dBm) and analog gain of +6 dB gives +7.25 dBm.

8.8.2 Time Slot Assignment Example

Figure 31 shows an example of the timing of transmit and receive time slots with changes in the time slot, clock slot and edge controls. Refer to Section 8.8, PCM Control Functions.

To program the first transmit time slot after $\overline{FS}$, TTC=31, TCS=7 and TPOL=1:

- The first receive time slot after $\overline{FS}$ would be RTS=31, RCS=7 and RPOL=0.
- Adjustments of ½ clock period can be made using these registers.

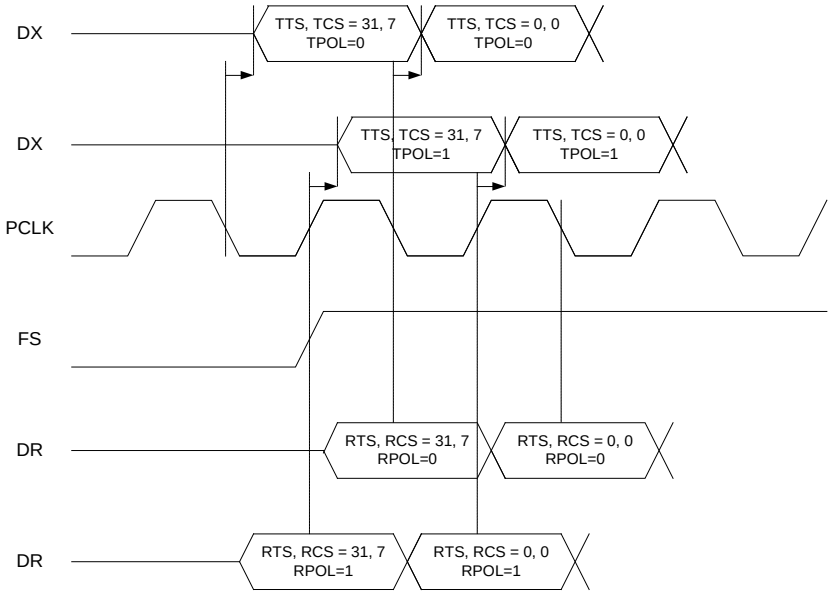


Figure 31: Timing Relationships with Various TTS, TCS, TPOL, and RTS, RCS, RPOL Settings

9 Barrier Information

9.1 Isolation Barrier

The 73M1x66B uses the Teridian MicroDAA proprietary isolation method based upon low-cost pulse transformer coupling. This technique provides several advantages over other methods, including:

- Lower BOM cost.
- Reduced component count.
- Lower radiated noise (EMI).
- Improved operation in noisy environments.

The MicroDAA has additional and enhanced functionality such as the support of powering the Line-Side DAA circuit from the Host-Side Device. This allows operation on leased lines circuits and on low current conditions commonly encountered in long loops. The MicroDAA can also operate entirely from line power when sufficient loop current is available.

Since the transformer is the only component crossing the isolation barrier, it solely determines the isolation between the PSTN and the FXO's digital interface. Several vendors can supply compatible transformers with ratings up to 6000 V.

Communication of PCM data, control data and status data is performed in the digital domain and is bidirectional at a rate of 1.536 Mbps.

9.2 Barrier Powered Options

The 73M1x66B has the ability to be used either in a Line Powered Mode or one where the Line-Side Device can be powered across the barrier from the Host-Side Device. The power-on default for the 73M1x66B is Barrier Powered Mode.

9.2.1 Barrier Powered Operation

In this default mode of operation, the 73M1x66B Host-Side Device drives the pulse transformer in such a way that power pulses are time division multiplexed into the transmit bit stream (half the time) that is rectified by circuitry in the Line-Side Device and uses this energy to power itself.

9.2.2 Line Powered Operation

If there is sufficient current available from the PSTN line, the 73M1x66B can be programmed to use line power instead of power from across the barrier.

9.3 Synchronization of the Barrier

Since the communication across the barrier is digital, synchronization of data across the barrier is of absolute importance. To that end, the devices implement special procedures to ensure reliability across the barrier.

When loss of synchronization is detected, the SLHS bit is set to 1 and likewise SYNL is also set to 1 and initiates an interrupt to the host. Once the SYNL bit is asserted a new barrier synchronization sequence will automatically begin.

Once read, the SLHS bit is reset, but will be set again if the synchronization loss continues.

Upon power up, the following sequence should be used to ensure barrier synchronization:

1. The 73M1906B starts in Barrier Powered Mode and transmits a preamble to aid the PLL locking of the Line-Side Device.
2. When PLL Lock detect is achieved the Line-Side Device transmits status data to the Host-Side Device.
3. When the Line-Side status Data is detected by the Host-Side Device, the barrier is considered to be in synchronization by the Host-Side Device.
4. If the auto-poll mode is enabled, the Device ID is transmitted, which is followed by transmit data.
5. Upon detection of the Device ID, the Line-Side Device considers the barrier to be in synchronization in host-to-line side direction.
6. The Line-Side Device starts sending Receive Data.
7. If the Auto-Poll bit is enabled, the Host-Side Device will have polled the Device ID of the Line-Side Device. If the barrier is synchronized, then Register 1Dh, bits 7-4, will be 1101. If not synchronized, then 0000.

9.4 Auto-Poll

Once the Barrier Interface acquires synchronization, the Barrier Interface state machine automatically sends a polling command to Line-Side Device requesting it to return its Device ID. This is provided in REV. Upon power up or loss of barrier synchronization, the contents of REV is cleared. After the auto-poll sequence, the host should read REV. A non-zero value indicates that synchronization is established.

The auto-poll mechanism is disabled by resetting the ENAPOL control bit.

9.5 Barrier Control Functions

Table 37: Barrier Control Functions

Function Mnemonic	Register Location	Type	Description
DISNTR	0x15[6]	WO	Disable No-Transition Timer If enabled, the No-Transition Timer is a safety feature. If the barrier fails, i.e. no transition is detected for 400 µs, the Line-Side Device resets itself and goes on hook to prevent line holding in a failure condition. 0 = Enables No-Transition Timer of 400 µs. (Default) 1 = Disables No-Transition Timer.
ENAPOL	0x05[3]	W	Enable Automatic Polling 0 = Disables automatic polling. 1 = Initiates automatic polling of the 73M1x66B Device ID upon the establishment of the barrier SYN. (Default) If SYN is lost, the Device ID will be reset to 0000.
ENLPW	0x02[2]	W	Enable Line Power 0 = Barrier Powered Mode is selected. (Default) 1 = Line Powered Mode is selected. ✓ Bit $\overline{\text{ENLVD}}$ must have the value of 0 before switching from Line Powered Mode to Barrier Powered Mode. Otherwise level detection is disabled and the transition to Barrier Powered Mode will not occur.
ENSYNL	0x05[1]	W	Enable Synch Loss Detection Interrupt 0 = Disables Synch Loss Detection Interrupt. 1 = Enables Synch Loss Detection Interrupt. (Default) When the 73M1x66B detects a loss of synchronization in Host-Side Barrier Interface, SYNL 0x03[1] will be set and reset when read.

Function Mnemonic	Register Location	Type	Description
RSTLSBI	0x0D[3]	W	Reset Line-Side Barrier Interface To reset the Line-Side Barrier Interface, set this bit to 1. 1 = Resets the Line-Side Barrier Interface. The chip sets this bit back to 0 after it has completed resetting the Line-Side Barrier Interface.
SLHS	0x0D[6]	R	Synchronization Lost Host Side This bit indicates the status of the Barrier Interface as seen from the Host-Side. 0 = Host-Side Barrier Interface is synchronized. 1 = Host-Side Barrier Interface lost synchronization. Once read, the SLHS bit is reset, but will be set again if the synchronization loss continues.
SLLS	0x1E[2]	R	Synchronization Loss Line Side 0 = TXRDY will continuously be generated following Synchronization Loss so as to allow SLLS information to be transferred across the barrier. This causes an automatic transfer of 1Eh. (Default) 1 = Synchronization is lost in the Line-Side Device due to Header.
SYNL	0x03[1]	R	Barrier Synchronization Loss 0 = Indicates synchronization of data across the barrier. 1 = Indicates a loss of synchronization of data across the barrier. This status bit is reset when read. This is a maskable interrupt. It is enabled by the ENSYNL bit.

9.6 Line-Side Device Operating Modes

The architecture of the 73M1x66B is unique in that the isolation barrier device, an inexpensive pulse transformer, is used to provide power and also bidirectional data between the Host-Side Device and the Line-Side Device. When the 73M1x66B is on hook, all the power for the Line-Side Device is provided over the barrier interface. After the Line-Side Device goes off hook, the telco line supplies approximately 8 mA to the Line-Side Device while the host provides the remainder across the barrier. It is also possible to power the Line-Side Device entirely from the line provided there is at least 17 mA of loop current available. Setting the ENLPW bit enables this mode and turns off the power supplied across the barrier. There is a penalty in using this mode in that the noise and dynamic range are about 6 dB worse than with the Barrier Powered Mode. It is therefore recommended that the Line Powered Mode be reserved for applications where the absolute minimum power from the host side is a priority and the reduction in performance can be tolerated.

Figure 32 shows the AC and DC circuits of the Line-Side Device.

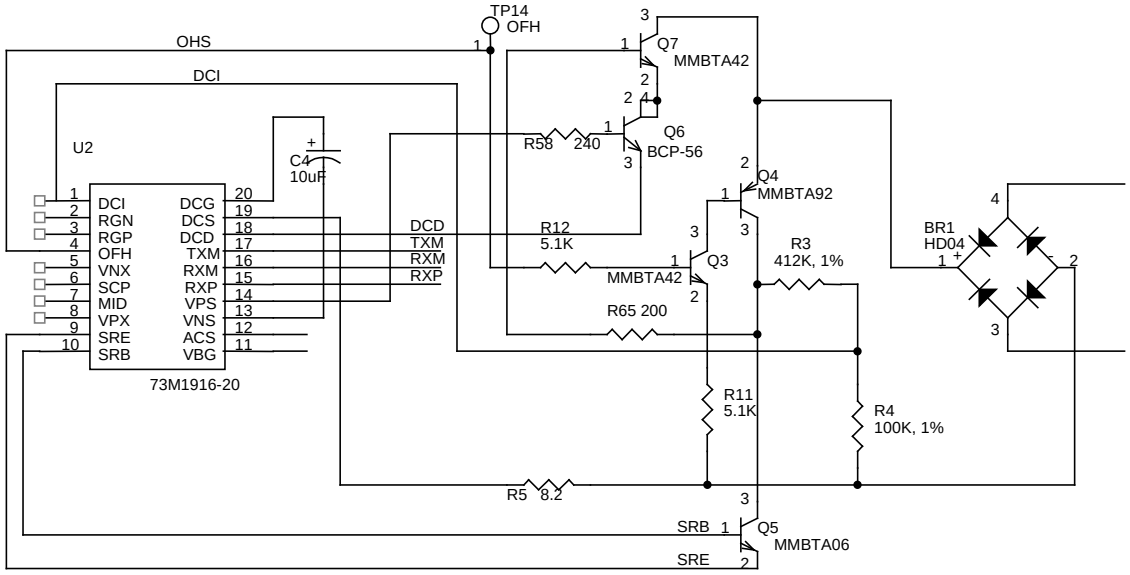


Figure 32: Line-Side Device AC and DC Circuits

The DCIV bits control the voltage versus current characteristics of the 73M1x66B by monitoring the voltage at the line divided down by the ratios of (R3+R4)/R4 (5:1) measured at the DCI pin. This voltage does not include the voltage across the Q4 and the bridge. When both the ENAC and ENDC bits are set (the hold mode), the DCIV characteristics follow approximately a 50 Ω load line offset by a factor determined by the DCIV bits. If ENDC=1 and ENAC=0, the 73M1x66B will go into the "Seize state mode" and the DC voltage load characteristic will be reduced to meet the Australian seize voltage requirements regardless of the setting of the DCIV bits.

9.7 Fail-Safe Operation of Line-Side Device

The 73M1x66B provides additional protection against improper operation during error and harmful external events. These include power or communication failure with the Line-Side Device and the detection of abnormal voltages and currents on the line. The basis of this protection is to ensure that under these conditions the device is in the On-Hook state and the isolation is provided.

The following events will cause the 73M1x66 Line-Side Device to go to the On-Hook state if it is Off-Hook:

1. A Power-On Reset occurs while Off-Hook.
2. The non-transition timer function (see DISNTR) is triggered by the absence of any signal transitions for more than 400 µs on the barrier interface, indicating a problem with communications.
3. The power supply to the Line-Side Device is below normal operating levels.

10 Configurable Direct Access Arrangement (DAA)

The 73M1x66B Line-Side Device integrates most of the circuitry to implement a PSTN line interface or DAA that is capable of being globally compliant with a single bill of materials.

The 73M1x66B supports the following DAA functions:

- Pulse dialing
- On and Off Hook switch control
- Loop current (DC-IV) regulation
- Line impedance matching
- Ring detection
- Tip and Ring voltage polarity reversal detection
- Billing tone rejection
- Trans-hybrid cancellation

The device is able to support Barrier Powered Mode in which the PSTN loop current may be as low as 8 mA.

10.1 Pulse Dialing

The 73M1x66B supports Pulse Dialing. See Section 10.6 for the descriptions of applicable control and status bits.

10.2 DC Termination

DC Termination or Loop Current (DC-IV) regulation is managed by the 73M1x66B Line-Side Device by configuring the appropriate registers. No additional components are necessary.

The 73M1x66B provides a DC transconductance circuit that regulates the tip to ring voltage depending on the DC current supplied by the line. There are four settings that can be used to set the voltage to current ratio.

Figure 33 shows the DC-IV characteristics of the 73M1x66B with special regions of interest.

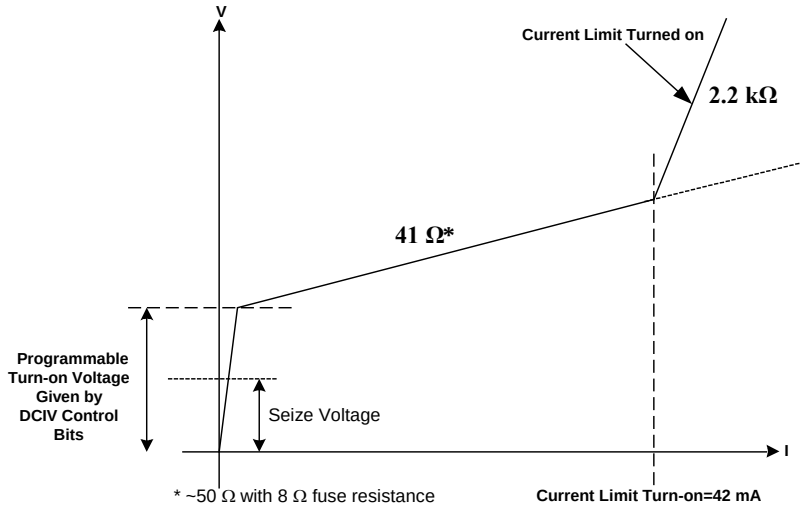


Figure 33: DC-IV Characteristics

The 73M1x66B can:

- Shift the characteristics by setting the turn-on voltage.
- Enable a current limit of 42 mA.

The 73M1x66B meets a wide range of different countries' requirements under software control. See Section 10.7.

There are two operating states for the DC-IV circuits: Hold and Seize.

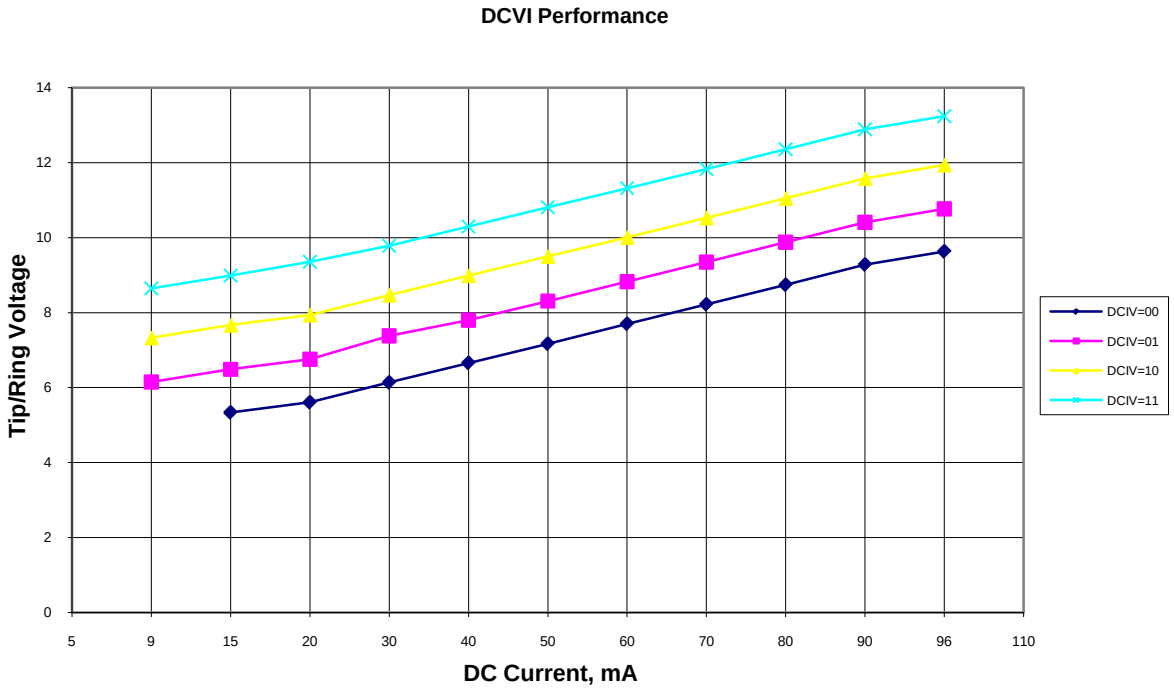


Figure 34: Tip-Ring Voltage versus Current Using Different DCIV Settings

The Hold state is the nominal operational point for the DC-IV circuits. The response shown in Figure 34 is for the Hold state (both DC and AC transconductance circuits are enabled). The slope of the DC-IV characteristics is approximately 50 Ω when the series resistance of a typical PPTC resettable fuse is taken into account.

The Seize state is a condition that is used by some central offices to determine an off-hook condition. In this state an additional load is added to the nominal operational DC-IV characteristics used during the Hold state

In the Seize state (only the DC transconductance circuit is enabled), the turn-on voltage is reduced on the line independent of the DCIV control bits. See Figure 35 and the description of the DCIV bits in Section 10.6.

An example of the use of the Seize state is for Australia, which requires this state for the first 300 ms immediately after going off hook.

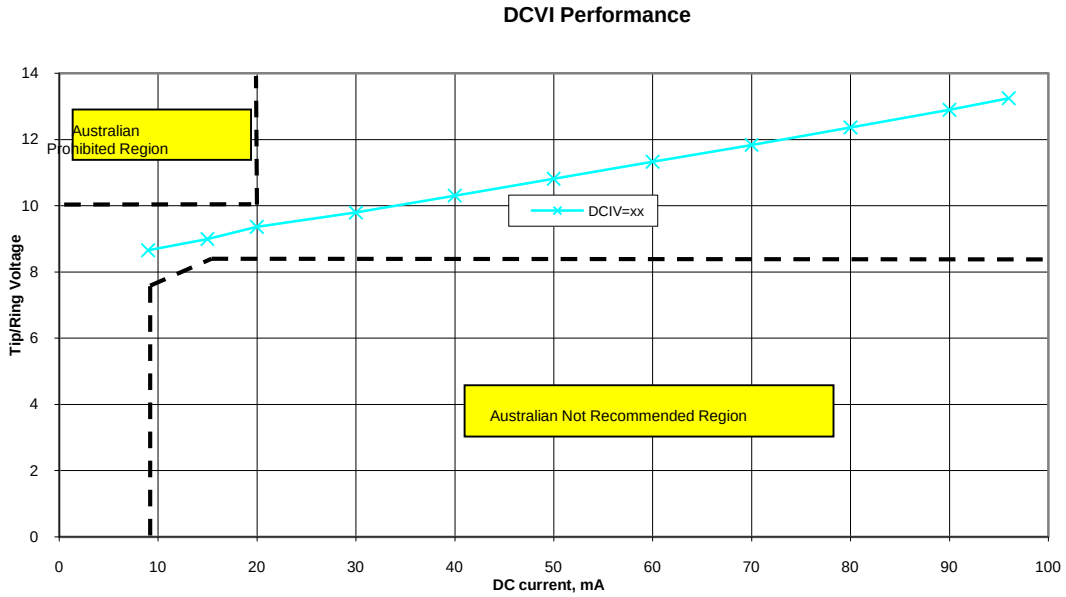


Figure 35: Voltage versus Current in the Seize Mode is the Same for All DCIV Settings

To facilitate the quick capture of the loop, the bandwidth of the DC loop is high upon power up. On the completion of DC loop capture, it should be lowered to avoid the interaction of DC and AC loops. See the description of the ENNOM bit in Section 10.6.

10.2.1 Current Limit Detection

If the DAA Current Limiting feature is enabled and the device detects an I-limit condition, a status bit is set to report this event.

10.3 AC Termination

The 73M1x66B supports 16 impedance configurations. This set of AC impedances has been selected to provide global coverage without the need for changing external components.

The AC Termination function is controlled by an enable and a disable control bit and by writing the appropriate network configuration code to the device. The AC Terminations provided include ones suitable for ETSI ES 203 021-2, Australia, FCC and China, among others. See Section 10.7 on how to select a configuration.

When using the 900 Ω termination, an additional gain of 1.75 dB should be added to the transmitter path.

Upon selection of a particular AC impedance configuration, the 73M1x66B monitors the line and controls the AC current back to the line, such that the desired impedance looking into the RXP pins is realized. The 73M1x66B provides an AC transconductance circuit that is used to modulate the AC signal onto the line as well as to regulate the current and provide the AC load in the AC signal path.

Figure 36 shows the magnitude response of the impedance matching filter for the case of ES 203 021-2.

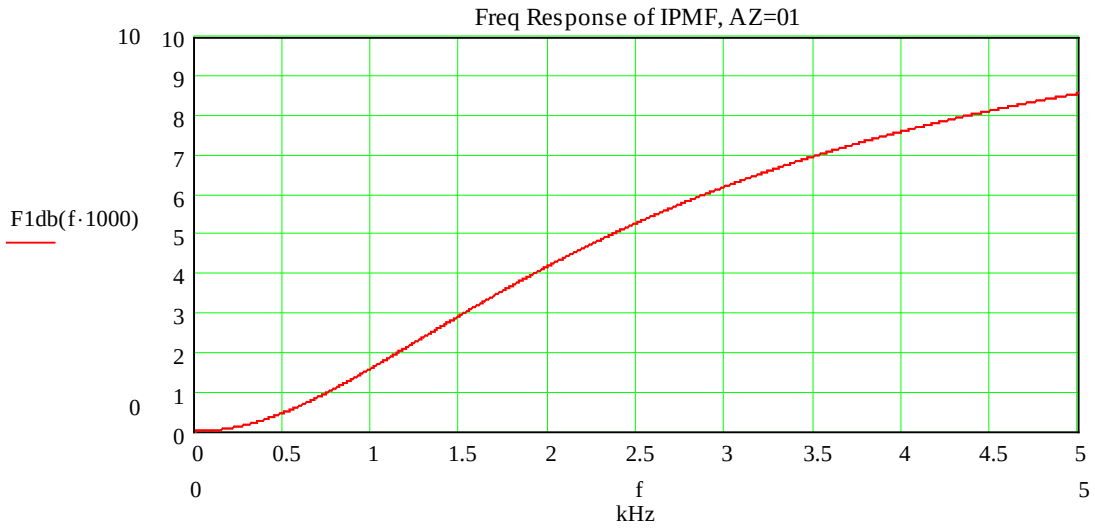


Figure 36: Magnitude Response of Impedance Matching Filter, ACZ (3:0)=0010 (ES 203 021-2)

10.4 Billing Tone Rejection

Some countries use a large amplitude out-of-band tone to measure call duration and to allow remote central offices to determine the duration of a call for billing purposes. To avoid saturation and distortion of the input caused by these tones, it is important to be able to reject them. These frequencies are typically 12 kHz or 16 kHz.

The 73M1x66B has an integrated notch filter that attenuates either of these tones. By enabling this filter and selecting the position of the notch frequency, such tones will be attenuated.

Figure 37 shows the magnitude response of the filter with a notch at either 12 kHz (F1) or 16 kHz (F2).

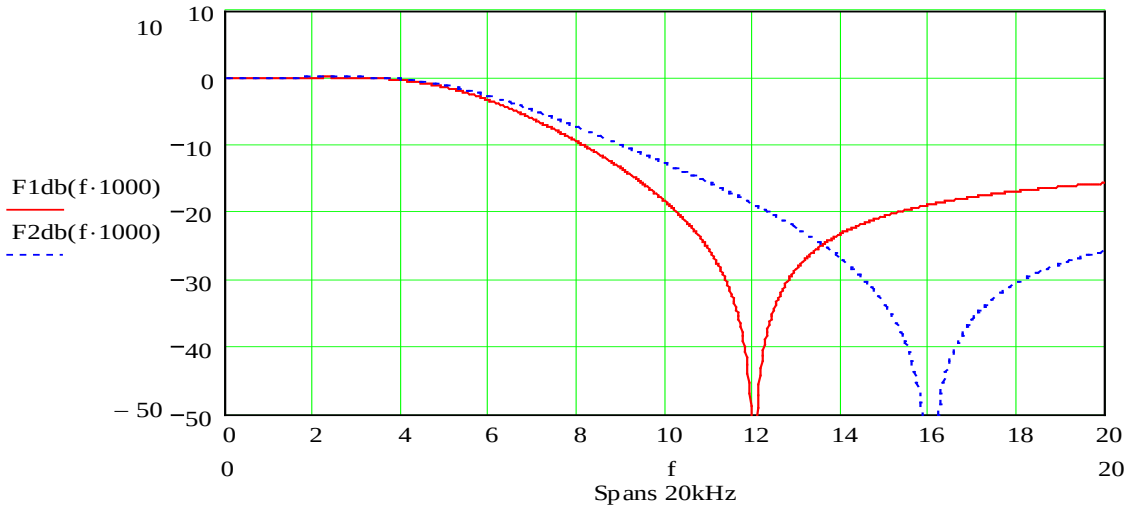


Figure 37: Magnitude Response of Billing Tone Notch Filter

In addition to the notch filter, the 73M1x66B can indicate the presence of an overload condition when a line's AC voltage exceeds 3.5 Vpk.

10.5 Trans-Hybrid Cancellation

In order to improve performance, the Trans-hybrid Cancellation option allows a replica of the transmit signal to be created within the 73M1x66B and fed back to the RXM pin via an external circuit at the line interface. With a well matched AC impedance the amount of cancellation achieved is >26 dB. This function can be enabled or disabled.

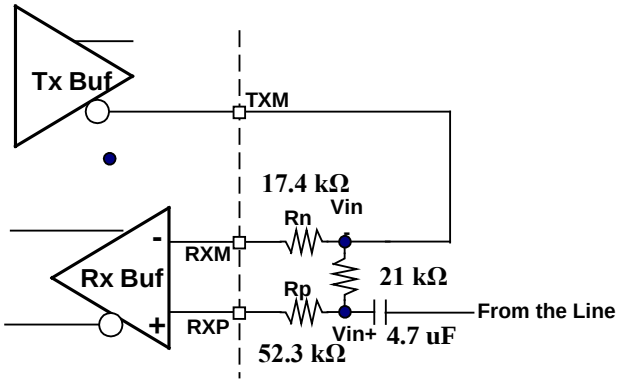


Figure 38: Trans-hybrid Cancellation

10.6 Direct Access Arrangement Control Functions

These Transmit Control Registers contain control information to set up the line side of the 73M1x66B. Included are DC-IV characteristics, off-hook control, etc.

Table 38: DAA Control Functions

Function Mnemonic	Register Location	Type	Description
ACZ	0x16[3:0]	W	Active Termination Loop Controls the selection of the active termination loops per the table shown below. ATEN must be set to 1 for selection to be enabled.

ACZ Field	Active Termination Loop Setting
0000	600 Ω
0001	900 Ω
0010	270 Ω + 750 Ω || 150 nF and 275 Ω + 780 Ω || 150 nF (ETSI ES 203 021-2)
0011	220 Ω + 820 Ω || 120 nF and 220 Ω + 820 Ω || 115 nF (Australia)
0100	370 Ω + 620 Ω || 310 nF
0101	320 Ω + 1050 Ω || 230 nF
0110	370 Ω + 820 Ω || 110 nF
0111	275 Ω + 780 Ω || 115 nF
1000	120 Ω + 820 Ω || 110 nF
1001	350 Ω + 1000 Ω || 210 nF
1010	200 Ω + 680 Ω || 100 nF (China)
1011	600 Ω + 2.16 µF
1100	900 Ω + 1 µF
1101	900 Ω + 2.16 µF
1110	220 Ω + 400 Ω || 70 nF (China)
1111	270 Ω + 600 Ω || 150 nF (Global Impedance)

<table>
<tr><th>Function Mnemonic</th><th>Register Location</th><th>Type</th><th>Description</th></tr>
<tr><td>ATEN</td><td>0x16[4]</td><td>W</td><td>Active Termination Loop Enable
Enables or disables Active Termination Loop.
0 = Disable. (Default)
1 = Enable Active Termination Loop.
Note: normal operation requires this bit to be set to always enable a termination circuit.</td></tr>
<tr><td>DCIV</td><td>0x13[7:6]</td><td>W</td><td>DC Current Voltage Characteristic Control
Hold state with ENDC and ENAC=1, at 20 mA DC loop current measured at DCI. The Tip/Ring voltage assumes that there is a 5:1 attenuation of off-hook voltage at the DCI input pin.

<table>
<tr><th>DCIV1</th><th>DCIV0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>DC Loop On Voltage of 0.73 V (5.60 V at Tip/Ring assuming a 5:1 step down of off-hook voltage)</td></tr>
<tr><td>0</td><td>1</td><td>DC Loop On Voltage of 0.977 V (6.75 V at Tip/Ring assuming a 5:1 step down of off-hook voltage)</td></tr>
<tr><td>1</td><td>0</td><td>DC Loop On Voltage of 1.232 V (7.65 V at Tip/Ring assuming a 5:1 step down of off-hook voltage)</td></tr>
<tr><td>1</td><td>1</td><td>DC Loop On Voltage of 1.488 V (9.35 V at Tip/Ring assuming a 5:1 step down of off-hook voltage)</td></tr>
</table>

*Seize state with ENDC=1 and ENAC=0, 20 mA loop current.
DCIV =xxProvides a DC Loop “On” Voltage of 0.281V (3.9 V at Tip/Ring assuming 5:1 step down of off-hook voltage)</td></tr>
<tr><td>ENAC</td><td>0x12[5]</td><td>WO</td><td>Enable AC Transconductance Circuit
0 = Shut Down AC Transconductance Circuit. Aux A/D input = Ring Detect Buffer (RGP/RGN) / Line Voltage (DCI). Seize state for going off hook. (Default)
1 = Enable AC Transconductance Circuit. Aux A/D input = Line Current (DCS) / Line Voltage (DCI).</td></tr>
<tr><td>ENDC</td><td>0x12[6]</td><td>WO</td><td>Enable DC Transconductance Circuit
0 = Shut down Transconductance Circuit. (Default)
1 = Enable Transconductance Circuit.</td></tr>
<tr><td>ENFEL</td><td>0x12[2]</td><td>WO</td><td>Enable Front End Line-Side Circuit
0 = Power down Front End Line-Side circuits. (Default)
1 = Enable Front End blocks excluding DCGM, ACGM, shunt regulator.</td></tr>
</table>

Function Mnemonic	Register Location	Type	Description
$\overline{\text{ENLVD}}$	0x12[3]	WO	LeV Detection (OVDET, UVDET, OIDET monitors) 0 = Enable LeV detection. (Default) 1 = Disable LeV detection (used in line-powered mode to save power). This bit will be 0 when Line Powered Mode is detected (ENLPW is set in Register 0x02[2]) and set to 1 when an interrupt occurs within the 73M1916. This bit must be reset prior to switching back to Barrier Powered Mode.
ENNOM	0x12[0]	WO	Enable Nominal Operation 0 = Speeds up the on and off hook transitions time by increasing the DC loop bandwidth of the DC transconductance circuit in the 73M1x66B. This should be used for pulse dialing, going on and off hook, etc. In addition, ENNOM=0 prevents the reset of all bits in Register 0x12. (Default) 1 = Enter Nominal Operation. Reduces the loop bandwidth of the DC transconductance circuit. Allows reset of Register 0x12 caused by bits UVDET, OVDET or OIDET.
ENSHL	0x12[4]	WO	Enable Shunt Loading 0 = Disable shunt loading. (Default) 1 = Enable shunt loading of the line. Not used for most applications.
IDISPD	0x13[1]	WO	Discharge and Pulse Dialing Controls the DC discharge current and how fast the loop turns off. Affects pulse dialing waveform. Controls the amount of discharge current during hook switch transitions. 0 = Minimum current. (Default) 1 = Maximum current. It is recommended to set IDISPD to 1 prior to hook switching operations.
ILM	0x13[5]	WO	Current Limit Enable This control enables or disables loop current limit. 0 = No current limit. (Default) 1 = 42 mA current limit enabled.
ILMON	0x1E[7]	R	Current Limit Mode On This status bit is effective only when the ILM bit is set to 1. 0 = Loop current is lower than 42 mA. 1 = Loop current is higher than 42 mA and the current limiting mode is active.
OFH	0x12[7]	WO	Off-Hook Enable This bit controls the state of the Hook signal. 0 = On-Hook. (Default) 1 = Off-Hook.
PLDM	0x13[3]	WO	Pulse Dialing Mode Enable Alleviates the strict timing requirements for the Host having to control ENDC and OFH during pulse dialing. With PLDM = 1, the Host only has to toggle OFH to perform pulse dialing. 0 = Pulse Dialing Mode is disabled. (Default) 1 = Pulse Dialing Mode is enabled.
RLPNEN	0x16[5]	W	Receive Low Pass Notch Enable 0 = Billing Tone Receive Low Pass Notch (RLPN) filter bypassed. (Default) 1 = RLPN Filter Enabled. See RLPNH for notch frequency selection.

Function Mnemonic	Register Location	Type	Description
RLPNH	0x14[2]	W	Receive Low Pass Notch 0 = Selects Receive Low Pass Notch (RLPN) at 12 kHz. (Default) 1 = Selects RLPN at 16 kHz. See RLPNEN (Register 0x16[5]) to enable the filter.
THEN	0x15[3]	W	Enable Transhybrid Circuit The rejection of the transmit signal from the receive signal path. 0 = Transhybrid Circuit disabled. (Default) 1 = Transhybrid Circuit enabled. This bit should always be set for optimal performance.

10.7 International Register Settings Table for DC and AC Terminations

Table 39 lists the recommended ACZ and DCIV register settings for various countries. Other parameters can also be set in addition to the AC and DC termination. These settings along with the reference schematic (see Figure 12) can realize a single design for global usage without country-specific modifications. For more information on worldwide approvals, refer to the *73M1x66 Worldwide Design Guide Application Note*.

Table 39: Recommended Register Settings for International Compatibility

Country	ACZ(3:0)	DCIV(1:0)	Country	ACZ(3:0)	DCIV(1:0)	Country	ACZ(3:0)	DCIV(1:0)
Argentina	0000	10	Hungary[1]	0010	10	Pakistan	0000	10
Australia	0011	11	Iceland[2]	0010	10	Peru	0000	10
Austria[1]	0010	10	India	0000	10	Philippines	0000	10
Bahrain	0000	10	Indonesia	0000	10	Poland[1]	0010	10
Belgium[1]	0010	10	Ireland[1]	0010	10	Portugal[1]	0010	10
Bolivia	0000	10	Israel	0000	10	Romania[1]	0010	10
Brazil	0000	10	Italy[1]	0010	10	Russia	0000	10
Bulgaria[1]	0010	10	Japan	0000	00	Saudi Arabia	0000	10
Canada	0000	10	Jordan	0000	10	Singapore	0000	10
Chile	0000	10	Kazakhstan	0000	10	Slovakia[1]	0010	10
China[3]	1110	10	Kuwait	0000	10	Slovenia[1]	0010	10
Columbia	0000	10	Latvia[1]	0010	10	South Africa[3]	0011	10
Croatia	0010	10	Lebanon	0000	10	South Korea	0000	10
Cyprus[1]	0010	10	Leichtenstein[2]	0010	10	Spain[1]	0010	10
Czech Rep[1]	0010	10	Lithuania[1]	0010	10	Sweden[1]	0010	10
Denmark[1]	0010	10	Luxembourg[1]	0010	10	Switzerland[2]	0010	10
Ecuador	0000	10	Macao	0000	10	Syria	0000	10
Egypt	0000	10	Malaysia	0000	10	Taiwan	0000	10
El Salvador	0000	10	Malta[1]	0010	10	ES 203 021-2	0010	10
Estonia[1]	0010	10	Mexico	0000	10	Thailand	0000	10
Finland[1]	0010	10	Morocco	0000	10	Turkey	0000	10
France[1]	0010	10	Netherlands[1]	0010	10	UAE	0000	10
Germany[1]	0010	10	New Zealand[3]	0100	10	UK[1]	0010	10
Greece[1]	0010	10	Nigeria	0000	10	Ukraine	0000	00
Guam	0000	10	Norway[2]	0010	10	USA	0000	10
Hong Kong	0000	10	Oman	0000	10	Yemen	0000	10

[1] These countries are members of the European Union, where there are no longer any regulatory requirements for AC impedance. The suggested setting complies with ETSI ES 203 021-2. Other settings can be used if desired.

[2] These countries are members of the European Free Trade Association, and their regulations generally follow the European Union model. The suggested setting complies with ETSI ES 203 021-2.

[3] These countries can use the suggested complex setting for voice or data products

11 Line Sensing and Status

The 73M1x66 supports the means to implement several line status functions such as ring detection, Line In Use detection, parallel pickup detection, and line voltage polarity reversals. To support these functions, 73M1x66 is able to measure the line voltage and current characteristics. In conjunction with these measurements, procedures can be implemented in the host to fully support these capabilities in an application.

11.1 Auxiliary A/D Converter

An 8-bit auxiliary A/D converter integrated in the 73M1x66B provides line monitoring and sensing capabilities. The A/D converter input signals are connected to the RGP and RGN pins of the device. It is possible to use this A/D converter to sample signals unrelated to PSTN DAA functions. However, in this application, it is necessary to isolate the input signal with optical or other means since the 73M1x66B is connected directly to the PSTN. Under normal conditions, RGP and RGN are AC coupled to the line through high voltage (250 V) capacitors.

Through the use of this auxiliary A/D converter, the following line status sensing features are supported by the 73M1x66B:

- Ring detection.
- PSTN line already in use detection.
- Off-hook detection that a parallel phone has been picked-up – parallel pick-up detection (PPU).
- On-hook detection of DC loop voltage polarity reversals.
- On-hook detection of Type II Caller ID.

11.2 Ring Detection

Ring Detection is provided through circuitry connected to the device pins RGP and RGN. Any large voltage transition (ringing or line reversal) will be a source for the “Wake up” signal to the 73M1x66B. Upon reception of a wake-up signal, the 73M1x66B passes the detected signal to the host where it is to be qualified for frequency and cadence (on and off timing of the ring tone bursts) as a valid ring signal.

11.3 Line In Use Detection (LIU)

If the 73M1x66B is preparing to go off-hook and dial, it is required to be aware whether the phone line is already in use by another device. If the 73M1x66B determines that the phone line is presently in use, it can avoid going off-hook and interrupting the call in progress. The timing of the FXO’s off-hook transition can be delayed until the FXO determines that the phone line is available. LIU sensing is done at pin DCIN with the Aux A/D.

11.4 Parallel Pick Up (PPU)

Parallel Pick Up is a means for the 73M1x66B to determine and notify a host in the case when the DAA is off-hook and a second or parallel-connected device during the course of a connection is also made to go off-hook.

11.5 Polarity Reversal Detection

A third type of line sensing requirement is associated with Caller ID protocols found in Japan and some European countries. In these countries, the Caller ID signals are sent prior to the start of normal ringing. A polarity reversal is used to indicate to the FXO that transmission of Caller ID information is about to begin. The detection of a polarity reversal takes place while the FXO is in the on-hook state.

11.6 Off-hook Detection of Caller ID Type II

It is also possible to receive Caller ID signals while the telephone is in use, referred to as Type II CID. This requires the 73M1916 to constantly monitor the line for signals, such as special in-band or CAS tones, while the FXO is in the off-hook state. This is done through the normal receive path.

11.7 Voltage and Current Detection

The 73M1x66B is capable of detecting the following circumstances:

- Under voltage on the line.
- Over voltage on the line.
- Over current.

These 73M1x66B built-in mechanisms provide protection to both the device itself and the external line circuitry.
If enabled, Over Voltage and Over Current detection will cause the 73M1x66B to go on-hook without the intervention of the host.
If configured in Line Powered Mode, the detection of an under-voltage condition causes the 73M1x66B to switch automatically to Barrier Powered Operation (see Section 9.2.1). This is done without the intervention of the host.

For each of the detection functions there are enable control bits and detection status bits. For each function there is a master detection function enable bit that must be set in order for the functions to work.

11.8 Under Voltage Detection (UVD)

Under Voltage Detection is an important feature of 73M1x66B. It determines if the phone line is not capable of supplying the current that the 73M1x66B requires from the line for proper operation. If this function is enabled and if the line is not capable of providing this current, the UVD condition will be asserted and can become a source of interrupt from the 73M1x66B to its connected host.

11.9 Over Voltage Detection (OVD)

If enabled, Over Voltage Detection is indicated if the device senses that the line voltage exceeds a defined threshold. The device allows the selection of choice of either 60 Vpk or 70 Vpk (depending upon the attenuation ratio, typically this is 100:1).

If enabled, the 73M1x66B will automatically go on-hook if over voltage is detected.

11.10 AC Signal Overload Detection

This is the same feature as used for the detection of billing tones (see Section 10.4). In this most generic sense, this detector provides an indicator that the AC signal on the line exceeds a value of 3.5 Vpk.

11.11 Over Current Detection (OID)

When the line current exceeds the safe operating range of the 73M1x66B or the external transistors, the device indicates this condition. If enabled, the 73M1x66B will automatically go on-hook if an over current event is detected.

11.12 Line Sensing Control Functions

These registers contain control information to set up and use the 73M1x66B line sensing functions.

Table 40: Line Sensing Control Functions

<table>
<tr><th>Function Mnemonic</th><th>Register Location</th><th>Type</th><th>Description</th></tr>
<tr><td>CIDM</td><td>0x15[4]</td><td>W</td><td>Caller ID Mode
0 = Disable Caller ID Mode. (Default)
1 = Enables Caller ID Mode by coupling the signal from the RGN/RGP pins to the PCM DX pins in the appropriate PCM codec format. A 20 dB gain boost is included in the signal path. The RXBST bit should also be set to allow the total nominal gain of 40 dB in the Caller ID path. The normal signal path is disconnected.</td></tr>
<tr><td>RXBST</td><td>0x14[3]</td><td>WO</td><td>Received Boost
If set to 1, Receive signal is increased by 20 dB. Default is 0. This is used to amplify signals that are passed through the auxiliary A/D when On-Hook.</td></tr>
<tr><td colspan="4">Ring Detection Status Bits</td></tr>
<tr><td>ENRGDT</td><td>0x05[0]</td><td>W</td><td>Enable Ring Detection Interrupt
This control bit enables the ring detection interrupt.
0 = Ring Detection Interrupt Disabled.
1 = Ring Detection Interrupt Enabled. (Default)
When 73M1922 detects an incoming ring signal, this bit will be set, if enabled, and reset when read.</td></tr>
<tr><td>RGDT</td><td>0x03[0]</td><td>R</td><td>Ring or Line Reversal Detection
Voltage greater than the Ring Detect Threshold was detected at RGP/RGN. This value is latched upon the event and cleared on read. The threshold is determined by RGTH. This is a maskable interrupt. It is enabled by the ENRGDT bit.
0 = No Latched Ring or Line Reversal Detection event. (Default)
1 = A Latched Ring or Line Reversal Detection event.</td></tr>
<tr><td>RGMON</td><td>0x03[3]</td><td>R</td><td>Ringing Monitor
Bit 3 monitors the activity of Ringing for further cadence check by the host:
0 = Silent
1 = Ringing
This bit is not latched. This status bit is reset when read.</td></tr>
<tr><td>RGTH</td><td>0x0E[1:0]</td><td>W</td><td>Ring Detect Threshold
Controls the Ring Detect Threshold assuming a 100:1 reduction of Ring Voltage into the RGP/RGN pins.
<table>
<tr><th>RGTH1</th><th>RGTH0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>Ring Detect disabled. For ring detection to occur, these bits must be programmed to a non-zero state.</td></tr>
<tr><td>0</td><td>1</td><td>0.15 Vpk equivalent to ±15 Vpk at Auxiliary A/D input.</td></tr>
<tr><td>1</td><td>0</td><td>0.30 Vpk equivalent to ±30 Vpk at Auxiliary A/D input.</td></tr>
<tr><td>1</td><td>1</td><td>0.45 Vpk equivalent to ±45 Vpk at Auxiliary A/D input.</td></tr>
</table></td></tr>
</table>

Function Mnemonic	Register Location	Type	Description
Auxiliary A/D Converter Status Bits			
LC	0x1C[7:1]	R	Loop Current In DC Path Result of Auxiliary A/D measuring the Loop Current (7-bit resolution, least significant bits only). Note: LC0=1 lsb=1.31/128=~10.23 mV=1.25 mA; magnitude only. The value of the resistor between the rectifier bridge and the DCS pin is assumed to be 8.2 Ω. Example: 0000011 → 30.7 mV/RE=3.74 mA; 0010000 → 20 mA Note: The AC path also has ~7 mA of loop current that should be added to get the total loop current provided by the line.
LV	0x1B[7:1]	R	Line Voltage On and Off Hook Contains the seven most significant bits of an 8-bit A/D representation of the voltage of the input of pin DCI. The voltage at the DCI pin is equal to the decimal value of LV bits [7:1] x 11 mV. For example, if the value of 0100000x is read from LV bits [7:1], this has a decimal value of 64, therefore DCI voltage equals 64 x 11 = 704 mV. Note that the voltage at the DCI pin is the voltage divided by 5 (off hook) or 100 (on hook). When offhook the diode bridge, switch saturation voltage, etc. should also be added to calculate the voltage at tip and ring.
RNG	0x1A[7:0]	R	Result of Auxiliary A/D measuring the attenuated ring voltage. Note: 1 lsb=1.31/128=~10.23 mV; 1's compliment. Example: 00100000 → 327 mV or Ring Voltage=32.7 V
Line Sensing Control			
DET	0x03[2]	R	Detection of Voltage or Current Fault 0 = None of the three conditions is detected. 1 = Indicates the detection of one of three conditions: Under Voltage, Over Voltage and Over Current. This status bit is reset when read. This is a maskable interrupt. It is enabled by the ENDET bit.
ENDET	0x05[2]	W	Enables Line Sensing Interrupt On Host-Side Device This bit controls whether an interrupt is generated based upon the detection of Under Voltage, Over Voltage and Over Current. 0 = Disable detector interrupt (Default) 1 = Enable detector interrupt.
ENDT	0x12[1]	WO	Enable Detectors On Line-Side Device 0 = UVD, OVD and OID conditions are ignored. (Default) 1 = Enables UVD, OVD and OID in the Line-Side Device and allows them to be used in the Host-Side Device.
Under-Voltage Detection Control and Status			
ENUVD	0x15[2]	WO	Enable Under Voltage Detector On Line-Side Device 0 = Under Voltage Detector not enabled. 1 = Under Voltage Detector enabled. When enabled, the ENNOM bit is temporarily set to the wide bandwidth mode if an under-voltage condition detected to allow fast reacquisition of the line.
UVDET	0x1E[6]	R	Under-Voltage Detector On Line-Side Device 0 = Under Voltage condition is not detected at VPS. 1 = Under Voltage condition is detected at VPS.

Function Mnemonic	Register Location	Type	Description
Over-Voltage Detection Control and Status			
ENOVD	0x15[1]	WO	Enable Over-Voltage Detector On Line-Side Device 0 = Over Voltage Detector not enabled. 1 = Over Voltage Detector enabled (not latched). Over voltage detector is enabled if ENOVD, ENFEL and ENNOM all equal 1.
OVDET	0x1E[5]	R	Over-Voltage Detector On Line-Side Device 0 = Over Voltage condition is not detected at RGP/RGN inputs. 1 = Over Voltage Condition is detected at RGP/RGN inputs.
OVDTH	0x13[2]	WO	Over-Voltage Threshold Setting 0 = Over Voltage Threshold is 0.6 Vpk at the chip or 60 Vp on the line. 1 = Over Voltage Threshold is 0.7 Vpk at the chip or 70 Vp on the line.
Over-Load Detection Control and Status			
ENOLD	0x15[7]	WO	Enable Over-Load Detector 0 = Over Load Detector is not enabled. 1 = Over Load Detector is enabled (not latched).
OLDET	0x1E[3]	R	Over-Load Detector 0 = Over-Load condition is not detected. 1 = Over-Load condition detected. Asserted when the line voltage exceeds 3.5 Vpk typically. OLDET is performed partially in analog domain and partially in digital domain. OLDET is asserted when the delta from aux A/D between two consecutive DCI samples is greater than 76.
Over-Current Detection Control and Status			
ENOID	0x15[0]	WO	Enable Over-Current Detector On Line-Side Device 0 = Over-Current Detector is not enabled. (Default) 1 = Over-Current Detector is enabled.
OIDET	0x1E[4]	R	Over-Current (I) Detector On Line-Side Device 0 = Over-Current (I) condition is not detected. 1 = Over-Current (I) condition is detected at the DCS pin when Loop Current is > 125 mA if ILM=0, or > 55 mA if ILM=1.

12 Loopback and Testing Modes

Figure 39 shows the six loop back modes available within the 73M1x66B.

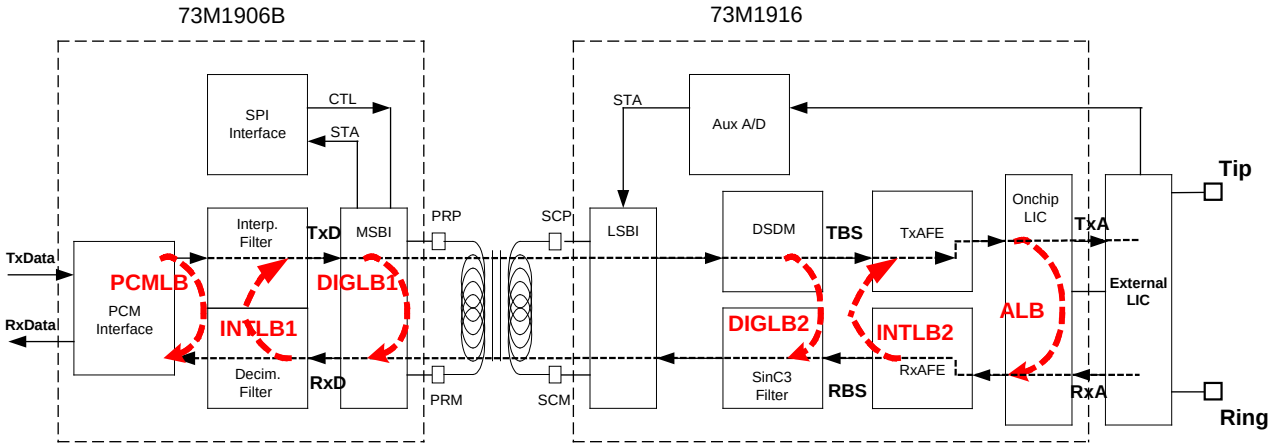


Figure 39: Loopback Modes Highlighted

Table 41 describes how the above control bits interact to provide each of the six loopback modes.

Table 41: Loopback Modes

TEST	TMEN	DTST	LB	Loopback Mode	Mnemonic
0000	0	00	0	Normal Mode. (Default)	No Loops
0000	0	00	1	Loopback between PCM Compander and FXO core.	PCMLB
0000	1	10	0	Digital Loopback Mode Interpolated TxData (TxD) is looped back to the Decimated RxData input (RxD).	DIGLB1
0000	1	11	0	Remote Analog Loopback Received RxD is looped back as TxD and transmitted back to the 73M1x66B Line-Side Device; RxD is D/A converted to yield the analog transmit signal (TxA).	INTLB1
0001	0	00	0	Digital Loopback Mode DR Transmit Bit Stream (TBS) is looped back to receive digital channel and received at DX (DIGLB2).	DIGLB2
0010	0	00	0	Remote Analog Loopback Receive analog signal is converted to Received Bit Stream (RBS) and is looped back to TBS and the analog transmit channel (INTLB2).	INTLB2
0011	0	00	0	Analog Loopback The transmit DR data is connected to the receiver at the analog interface and received at the DX pin (ALB).	ALB

12.1 Loopback Controls

Table 42 describes the registers used for loopback control.

Table 42: Loopback Controls

<table>
<tr><th>Function Mnemonic</th><th>Register Location</th><th>Type</th><th>Description</th></tr>
<tr><td>TMEN</td><td>0x02[7]</td><td>W</td><td>Test Mode Enable
Used to enable the activation of the test loops controlled by the DTST bits (DIGLB1 and INTLB1).
0 = Disables DTST loops.
1 = Enables DTST loops.

✓ TMEN has to be set to 1 before the setting of the DTST bits.</td></tr>
<tr><td>DTST</td><td>0x07[1:0]</td><td>W</td><td>Digital Test Mode Select
These control bits enable DIGLB1 and INTLB1.

✓ Prior to writing to these bits, TMEN must be set to 1.
<table>
<tr><th>DTST1</th><th>DTST0</th><th>Selected Test Mode</th></tr>
<tr><td>0</td><td>0</td><td>Normal (Default)</td></tr>
<tr><td>1</td><td>0</td><td>DIGLB1</td></tr>
<tr><td>1</td><td>1</td><td>INTLB1</td></tr>
</table></td></tr>
<tr><td>LB</td><td>0x24[0]</td><td>W</td><td>Loopback
0 = Disables PCM Loopback.
1 = Enables PCM Loopback within the Host-Side Device.</td></tr>
<tr><td>TEST</td><td>0x18[7:4]</td><td>W</td><td>This four-bit field is used to enable the loopback mode per the following table:
<table>
<tr><th>TEST</th><th>Loopback Mode</th></tr>
<tr><td>0000</td><td>Normal Mode. (Default)
Transmit and receive channels are independent.</td></tr>
<tr><td>0001</td><td>Digital Loopback Mode.
DR Transmit Bit Stream (TBS) is looped back to receive digital channel and received at DX (DIGLB2).</td></tr>
<tr><td>0010</td><td>Remote Analog Loopback.
Receive analog signal is converted to Received Bit Stream (RBS) and is looped back to TBS and the analog transmit channel (INTLB2).</td></tr>
<tr><td>0011</td><td>Analog Loopback.
The transmit DR data is connected to the receiver at the analog interface and received at the DX pin (ALB).</td></tr>
</table></td></tr>
</table>

13 Performance

This section provides an overview of typical performance characteristics measured using 73M1x66B production devices on a Teridian Reference Board. The measurements were made using a Wandel and Goltermann PCM-4 test unit. The tests conform to *ITU-T Recommendation G.712 (2001)*. For more information, see the *73M1966B Performance Characterization*.

13.1 Transmit

Figure 40 provides performance characteristics for transmit gain tracking.

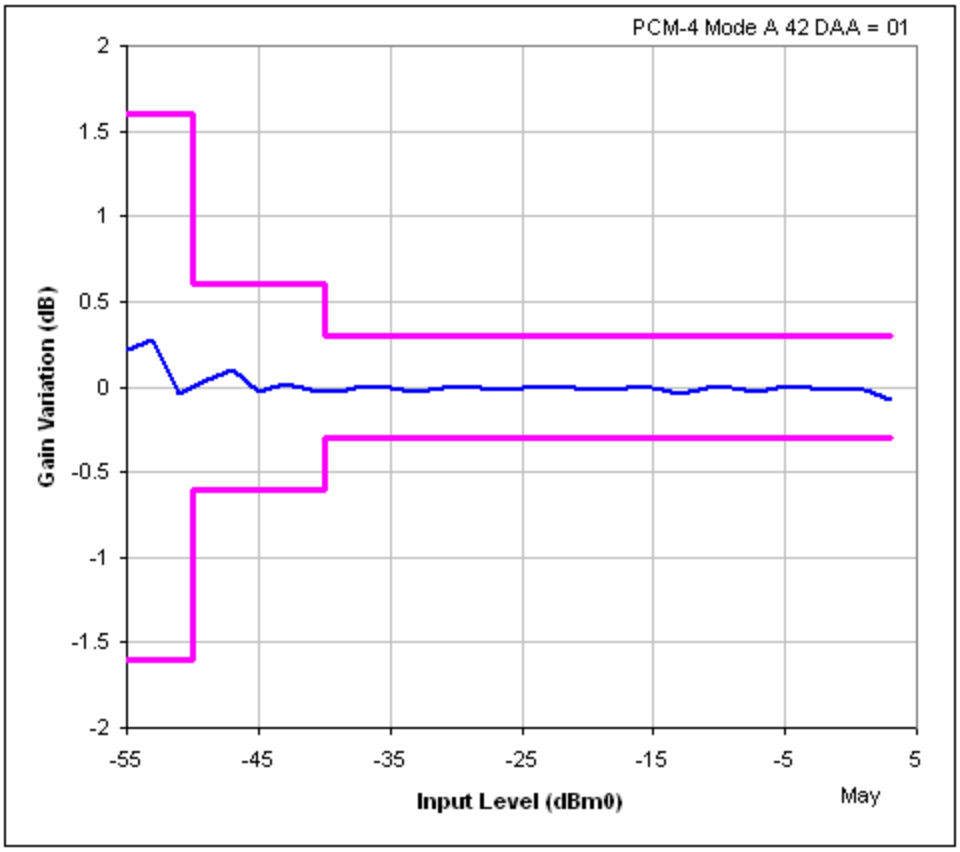


Figure 40: Variation of Transmit Gain Digital Input to Analog Output at the Line

Figure 41 provides performance characteristics for receive gain variation against frequency.

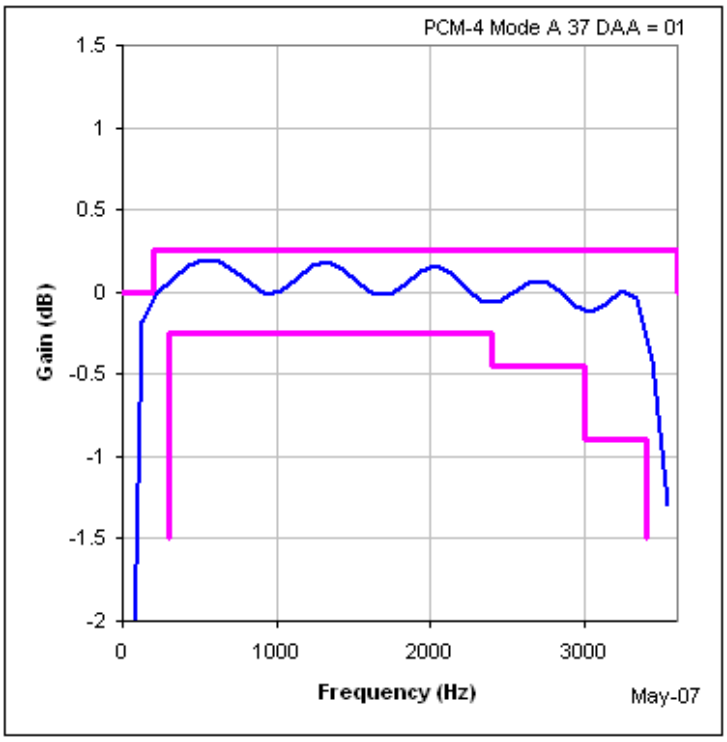


Figure 41: Gain versus Frequency for Digital Input to Analog Output at the Line

Figure 42 provides performance characteristics for distortion in the direction of the digital port to analog port.

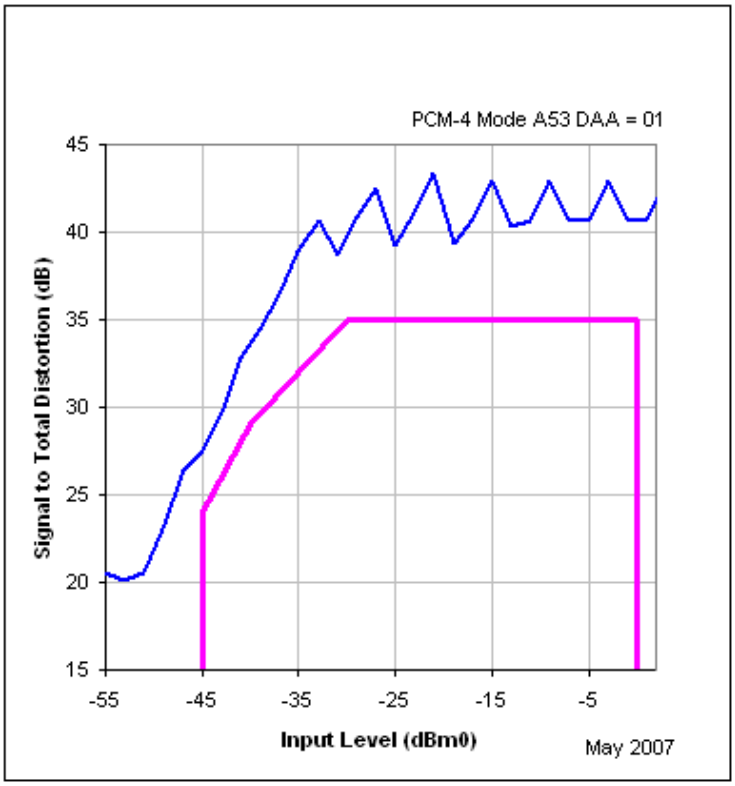


Figure 42: Signal to Total Distortion versus Input Level for Digital Input to Analog Output to the Line

13.2 Receive

Figure 43 provides performance characteristics for receive gain tracking.

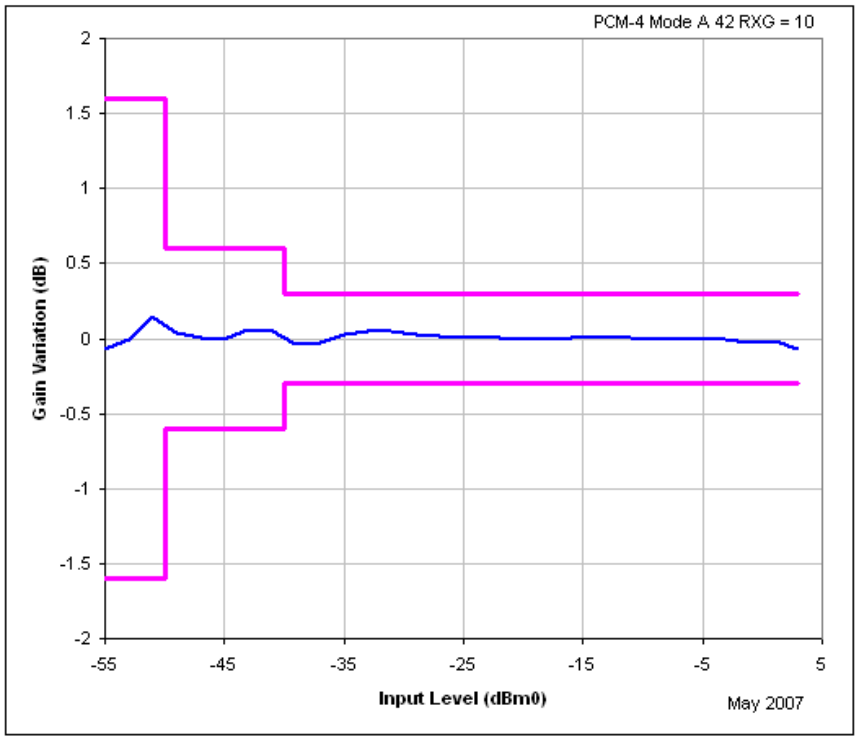


Figure 43: Variation of Receiver Analog Gain at the Line to the Digital DX Output

Figure 44 provides performance characteristics for gain variation against frequency.

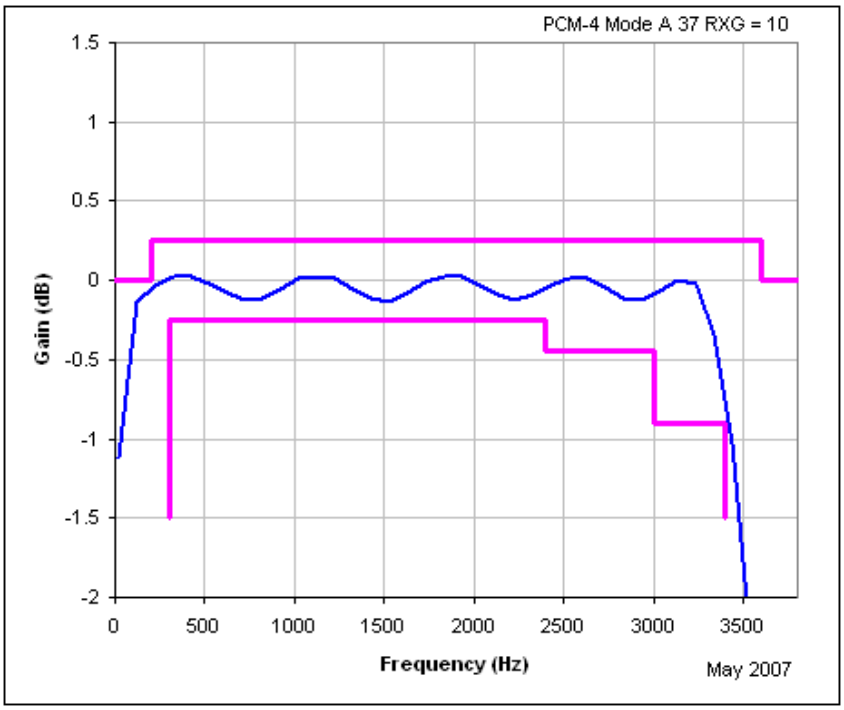


Figure 44: Gain versus Frequency for Analog Input at the Line to the Digital DX Output

Figure 45 provides performance characteristics for distortion in the direction of the analog port to digital port.

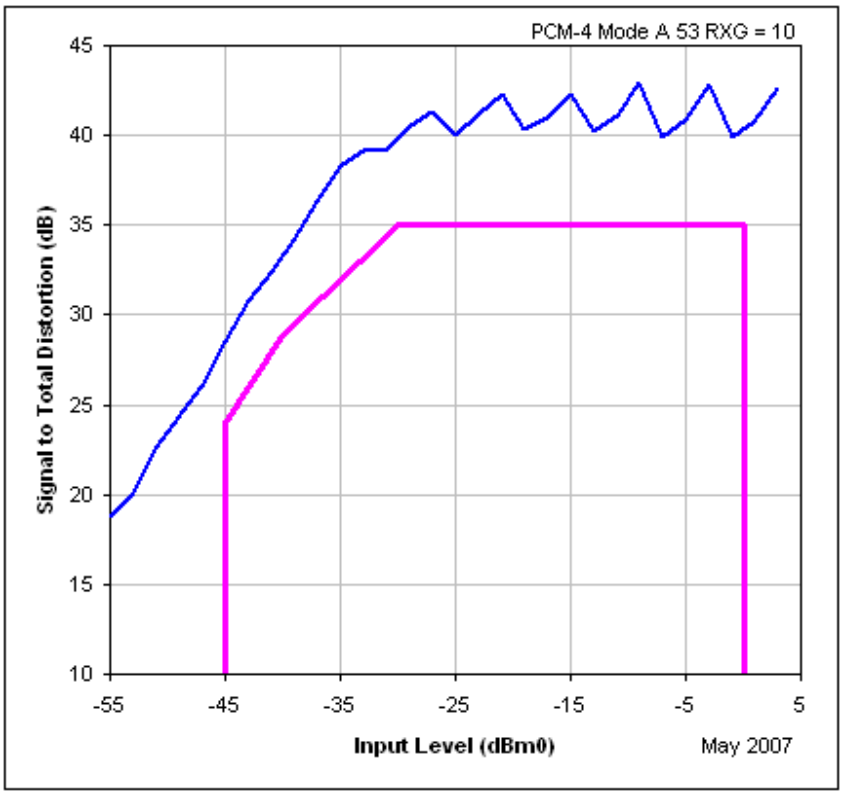


Figure 45: Signal to Total Distortion versus Input Level for Analog at the Line to the Digital DX Output

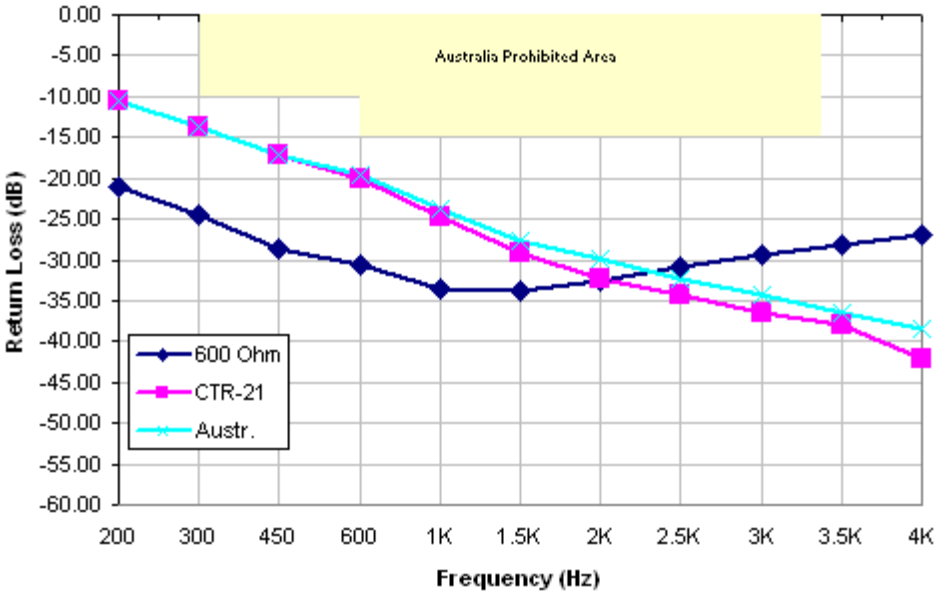
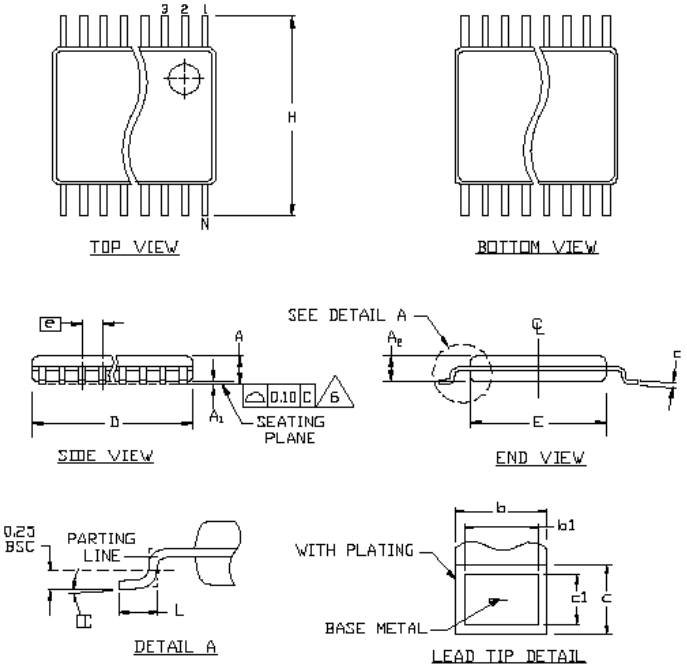


Figure 46: Return Loss, @ 80 mA

14 Package Layout



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_e	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

Figure 47: 20-Pin TSSOP Package Dimensions

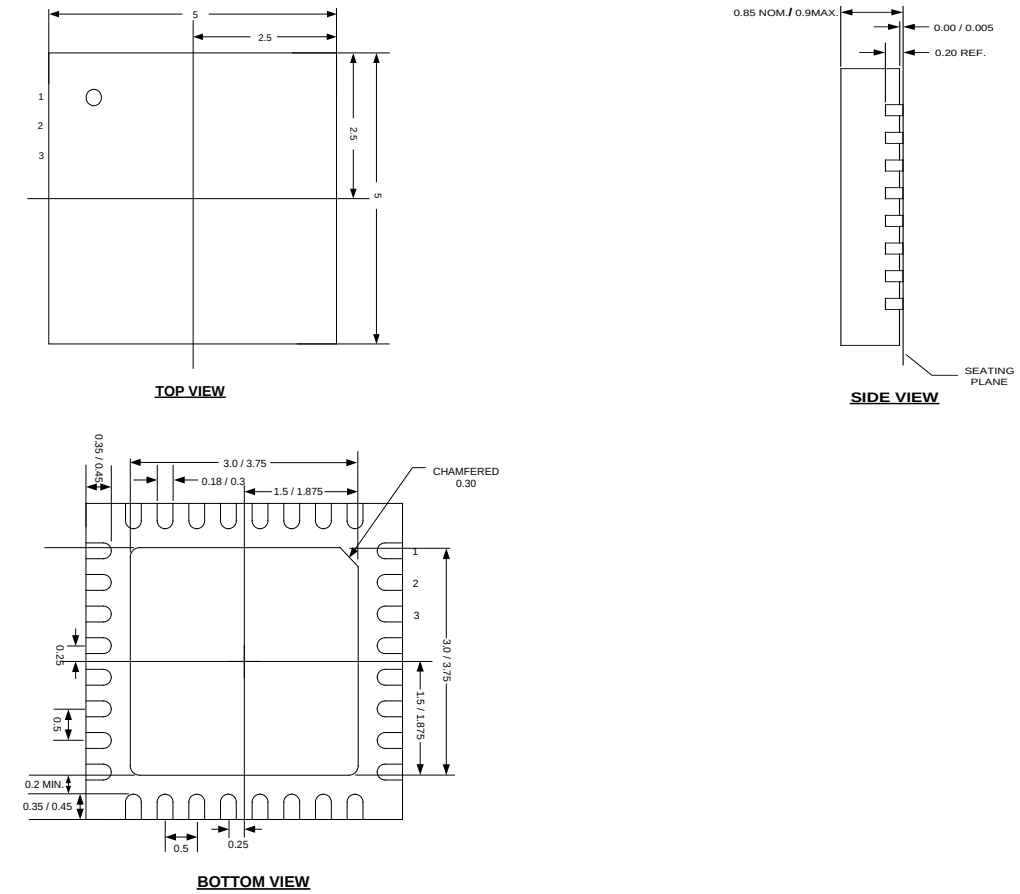
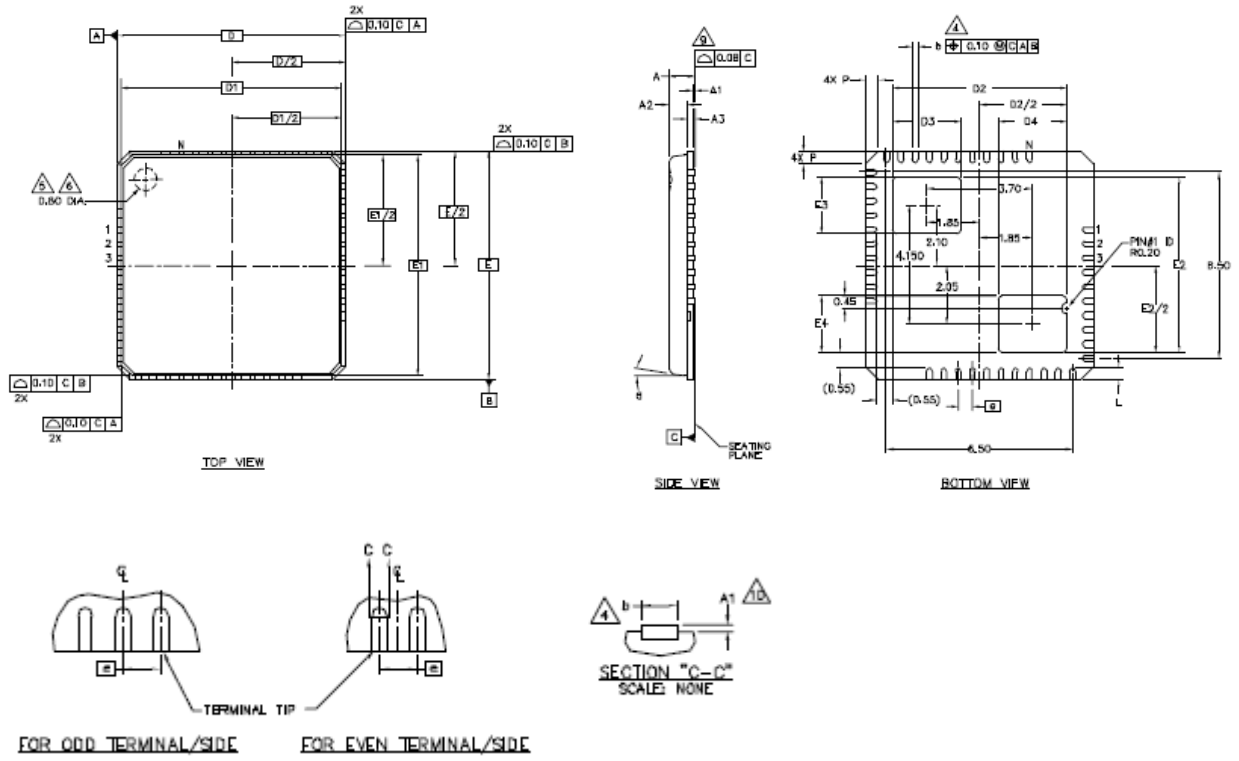


Figure 48: 32-Pin QFN Package Dimensions



NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.

4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.

7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.08mm.

9. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
10. APPLIED ONLY FOR TERMINALS.

SYMBOL	DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	—	0.85	0.90	
A1	0.00	0.01	0.05	9
A2	—	0.65	0.70	
A3		0.20 REF.		
e		0.50 BSC		
N		42		
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4
D		8.00 BSC		
D1		7.75 BSC		
E		8.00 BSC		
E1		7.75 BSC		
θ			12°	
P	0.24	0.42	0.60	

SYMBOLS	D2			E2			NOTE
	MIN	NOM	MAX	MIN	NOM	MAX	
EXPOSED PAD VARIATIONS	5.95	6.10	6.25	6.00	6.15	6.30	
SYMBOLS	D3			E3			NOTE
	MIN	NOM	MAX	MIN	NOM	MAX	
EXPOSED PAD VARIATIONS	2.25	2.40	2.55	1.85	2.00	2.15	
SYMBOLS	D4			E4			NOTE
	MIN	NOM	MAX	MIN	NOM	MAX	
EXPOSED PAD VARIATIONS	2.25	2.40	2.55	1.85	2.00	2.15	

Figure 49: 42-Pin QFN Package Dimensions

15 Ordering Information

Table 43 lists the order numbers and packaging marks used to identify 73M1x66B products.

Table 43: Order Numbers and Packaging Marks

Part Description	Order Number	Packaging Mark	Host/Line
73M1966B 32-Pin QFN, Lead free	73M1966B-IM/F	73M1916A-M 73M1906B	Line-Side IC Host-Side IC
73M1966B 32-Pin QFN, Lead free, Tape and Reel	73M1966B-IMR/F	73M1916A-M 73M1906B	Line-Side IC Host-Side IC
73M1966B 20-Pin TSSOP, Lead free	73M1966B-IVT/F	73M1916AVT 73M1906BVT	Line-Side IC Host -Side IC
73M1966B 20-Pin TSSOP, Lead free, Tape and Reel	73M1966B-IVTR/F	73M1916AVT 73M1906BVT	Line-Side IC Host -Side IC
73M1866B 42-Pin QFN, Lead free	73M1866B-IM/F	73M1866B-IM	
73M1866B 42-Pin QFN, Lead free, Tape and Reel	73M1866B-IMR/F	73M1866B-IM	

16 Contact Information

For more information about Teridian Semiconductor products or to check the availability of the *73M1966B*, contact us at:

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FAX: (714) 508-8878
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For a complete list of worldwide sales offices, go to http://www.teridian.com.

Revision History

Revision	Date	Description
1.0	11/7/2007	First publication.
1.1	5/13/2008	
1.2	7/30/2008	
1.3	11/17/2008	
1.4	7/21/2009	
1.5	10/16/2009	
1.6	4/2/2010	Replaced Table 16 with a new table. Replaced the schematics in Figure 12 and Figure 13 with new schematics. Moved the steps to enable the calibration of receive DC offset from Section 8.8.3 to the *73M1866B/73M1966B Implementer's Guide*. Corrected the Types (R, W, WO) in Table 32. Rewrote the description of the ADJ bit. Added clarification to the description of the PLDM bit. Added clarification to the description of the RGDT bit.

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73M1966B-KEYCHN 73M1866B-IM/F 73M1866B-IMR/F 73M1866B-IFX 73M1906B-IM/F 73M1906B-IMR/F 73M1916-IM/F 73M1916-IMR/F 73M1906B-IVT/F 73M1906B-IVTR/F 73M1916-IVT/F 73M1916-IVTR/F 73M1966B-IVTR/F 73M1966B-IVT/F 73M1966B-IM/F 73M1966B-IMR/F