CY7B144
CY7B145

8K x 8/9 Dual-Port Static RAM with Sem, Int, Busy

Features

- **0.8-micron BiCMOS for high performance**
- **High-speed access**
  — 15 ns (commercial)
  — 25 ns (military)
- **Automatic power-down**
- **Fully asynchronous operation**
- **Master/Slave select pin allows bus width expansion to 16/18 bits or more**
- **Busy arbitration scheme provided**
- **Semaphores included to permit software handshaking between ports**
- **$\overline{INT}$ flag for port-to-port communication**
- **Available in 68-pin LCC/PLCC, 64-pin and 80-pin TQFP**
- **TTL compatible**
- **Pin compatible and functionally equivalent to IDT7005 and IDT7015**

Functional Description

The CY7B144 and CY7B145 are high-speed BiCMOS 8K x 8 and 8K x 9 dual-port static RAMs. Various arbitration schemes are included on the CY7B144/5 to handle situations when multiple processors access the same piece of data. Two ports are provided permitting independent, asynchronous access for reads and writes to any location in memory. The CY7B144/5 can be utilized as a standalone 64-Kbit dual-port static RAM or multiple devices can be combined in order to function as a 16/18-bit or wider master/slave dual-port static RAM. An $M/\overline{S}$ pin is provided for implementing 16/18-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: chip enable ($\overline{CE}$), read or write enable ($R/\overline{W}$), and output enable ($\overline{OE}$). Two flags, $\overline{BUSY}$ and $\overline{INT}$, are provided on each port. $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. The interrupt flag ($\overline{INT}$) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by a chip enable ($\overline{CE}$) pin or $\overline{SEM}$ pin.

The CY7B144 and CY7B145 are available in 68-pin LCCs, PLCCs, 64-pin (CY7B144) and 80-pin TQFP (CY7B145).

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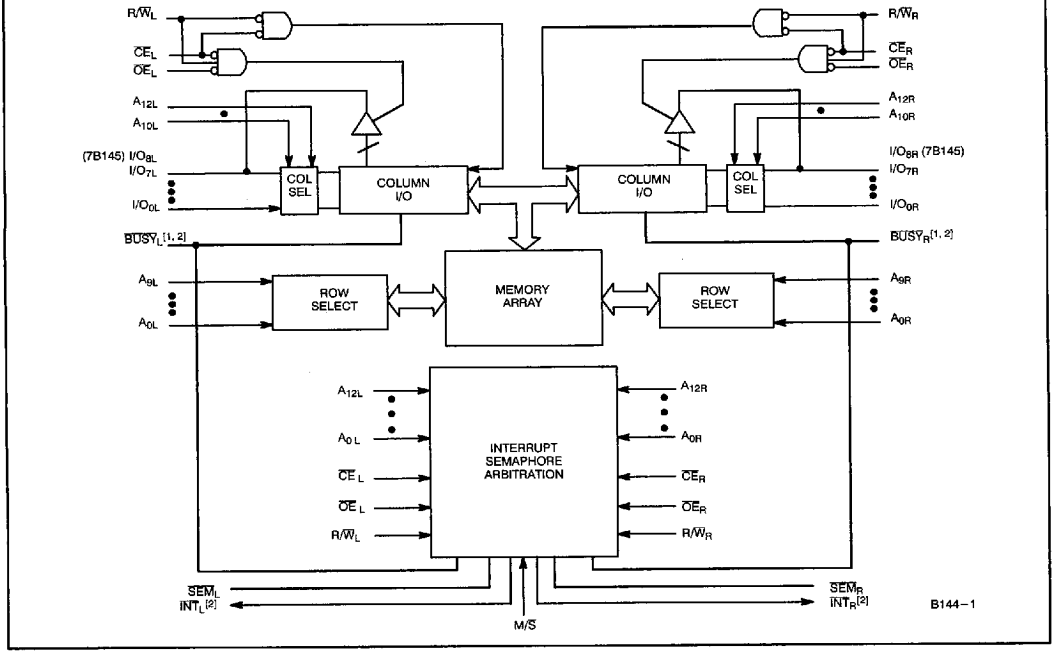
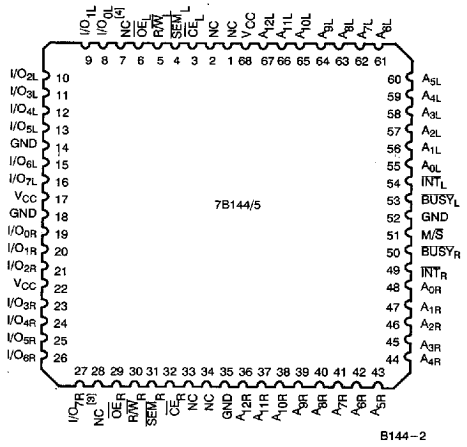
Logic Block Diagram



Notes:
1. $\overline{BUSY}$ is an output in master mode and an input in slave mode.
2. Master: push-pull output and requires no pull-up resistor.

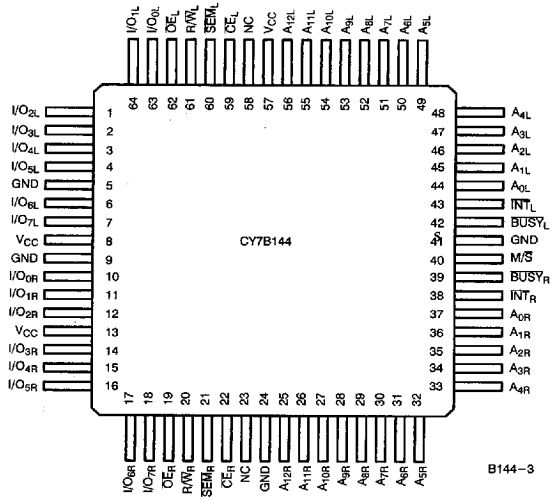
Pin Configurations

68-Pin LCC/PLCC
Top View



B144–2

64-Pin TQFP
Top View

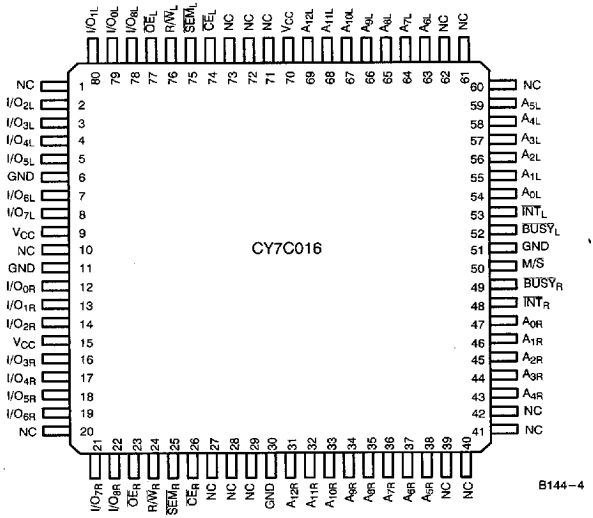


B144–3

Notes:
3. I/O_{8R} on the CY7B145.
4. I/O_{8L} on the CY7B145.

Pin Configurations (continued)

80-Pin TQFP
Top View



Pin Definitions

Left Port	Right Port	Description
$I/O_{0L-7L(8L)}$	$I/O_{0R-7R(8R)}$	Data bus Input/Output
A_{0L-12L}	A_{0R-12R}	Address Lines
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable. When asserted LOW, allows access to eight semaphores. The three least significant bits of the address lines will determine which semaphore to write or read. The I/O_0 pin is used when writing to a semaphore. Semaphores are requested by writing a 0 into the respective location.
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag. $\overline{INT}_L$ is set when right port writes location 1FFE and is cleared when left port reads location 1FFE. $\overline{INT}_R$ is set when left port writes location 1FFF and is cleared when right port reads location 1FFF.
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

Selection Guide

		7B144–15 7B145–15	7B144–25 7B145–25	7B144–35 7B145–35	7B144–55 7B145–55
Maximum Access Time (ns)		15	25	35	55
Maximum Operating Current (mA)	Commercial	260	220	210	210
	Military		280	250	
Maximum Standby Current for I_{SB1} (mA)	Commercial	110	95	90	90
	Military		100	95	

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage[5] ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military[6]	−55°C to +125°C	5V ± 10%

Notes:

5. Pulse width < 20 ns.

6. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[7]

Parameter	Description	Test Conditions		7B144–15 7B145–15 Min.	7B144–15 7B145–15 Max.	7B144–25 7B145–25 Min.	7B144–25 7B145–25 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	Outputs Disabled, GND ≤ V_O ≤ V_{CC}		−10	+10	−10	+10	μA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA Outputs Disabled	Com'l		260		220	mA
			Mil/Ind				280	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[8]	Com'l		110		95	mA
			Mil/Ind				100	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[8]	Com'l		165		145	mA
			Mil/Ind				180	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0[8]	Com'l		15		15	mA
			Mil/Ind				30	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs, f = f_{MAX}[8]	Com'l		160		140	mA
			Mil/Ind				160	

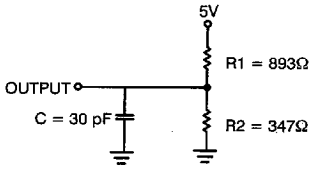
Parameter	Description	Test Conditions		7B144–35 7B145–35 Min.	7B144–35 7B145–35 Max.	7B144–55 7B145–55 Min.	7B144–55 7B145–55 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	Outputs Disabled, GND ≤ V_O ≤ V_{CC}		−10	+10	−10	+10	μA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA Outputs Disabled	Com'l		210		210	mA
			Mil/Ind		250		250	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[8]	Com'l		90		90	mA
			Mil/Ind		95		95	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[8]	Com'l		135		135	mA
			Mil/Ind		160		160	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0[8]	Com'l		15		15	mA
			Mil/Ind		30		30	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs, f = f_{MAX}[8]	Com'l		130		130	mA
			Mil/Ind		140		140	

Notes:
7. See the last page of this specification for Group A subgroup testing information.
8. f_{MAX} = 1/t_{RC} = All inputs cycling at f = 1/t_{RC} (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.

Capacitance[9]

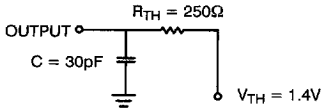
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25°C$, f = 1 MHz, $V_{CC} = 5.0V$	10	pF
C_{OUT}	Output Capacitance		15	pF

AC Test Loads and Waveforms



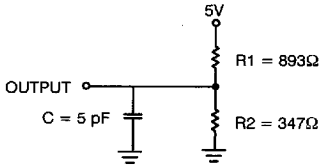
(a) Normal Load (Load 1)

B144–5



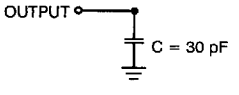
(b) Thévenin Equivalent (Load 1)

B144–6



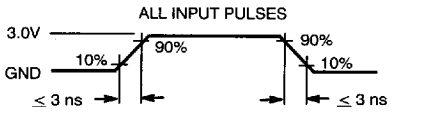
(c) Three-State Delay (Load 3)

B144–7



Load (Load 2)

B144–8



B144–9

Switching Characteristics Over the Operating Range[7, 10]

Parameter	Description	7B144–15 7B145–15 Min.	7B144–15 7B145–15 Max.	7B144–25 7B145–25 Min.	7B144–25 7B145–25 Max.	7B144–35 7B145–35 Min.	7B144–35 7B145–35 Max.	7B144–55 7B145–55 Min.	7B144–55 7B145–55 Max.	Unit
READ CYCLE										
t_{RC}	Read Cycle Time	15		25		35		55		ns
t_{AA}	Address to Data Valid		15		25		35		55	ns
t_{OHA}	Output Hold From Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		25		35		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		15		20		25	ns
t_{LZOE}[11, 12]	$\overline{OE}$ Low to Low Z	3		3		3		3		ns
t_{HZOE}[11, 12]	$\overline{OE}$ HIGH to High Z		10		15		20		25	ns
t_{LZCE}[11, 12]	$\overline{CE}$ LOW to Low Z	3		3		3		3		ns
t_{HZCE}[11, 12]	$\overline{CE}$ HIGH to High Z		10		15		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		25		35		55	ns

Notes:

9. Tested initially and after any design or process changes that may affect these parameters.
10. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
11. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
12. Test conditions used are Load 3.

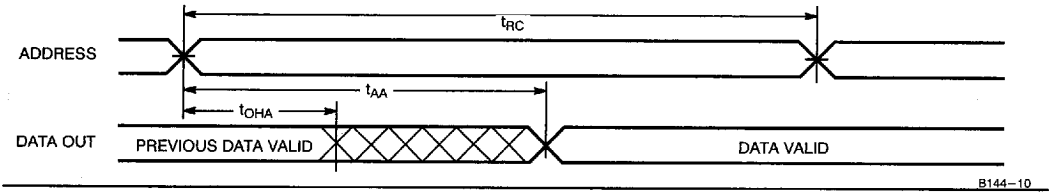
Switching Characteristics Over the Operating Range[7, 10] (continued)

Parameter	Description	7B144–15 7B145–15		7B144–25 7B145–25		7B144–35 7B145–35		7B144–55 7B145–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
t_{WC}	Write Cycle Time	15		25		35		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		20		30		45		ns
t_{AW}	Address Set-Up to Write End	12		20		30		45		ns
t_{HA}	Address Hold From Write End	2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	Write Pulse Width	12		20		25		40		ns
t_{SD}	Data Set-Up to Write End	10		15		15		25		ns
t_{HD}	Data Hold From Write End	0		0		0		0		ns
t_{HZWE}[12]	R/$\overline{W}$ LOW to High Z		10		15		20		25	ns
t_{LZWE}[12]	R/$\overline{W}$ HIGH to Low Z	3		3		3		3		ns
t_{WDD}[13]	Write Pulse to Data Delay		30		50		60		70	ns
t_{DDD}[13]	Write Data Valid to Read Data Valid		25		30		35		40	ns
BUSY TIMING[14]										
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		15		20		20		30	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch		15		20		20		30	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		15		20		20		30	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH		15		20		20		30	ns
t_{PS}	Port Set-Up for Priority	5		5		5		5		ns
t_{WB}	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0		0		0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	13		20		30		30		ns
t_{BDD}	$\overline{BUSY}$ HIGH to Data Valid		15		25		35		55	ns
INTERRUPT TIMING[14]										
t_{INS}	$\overline{INT}$ Set Time		15		25		25		35	ns
t_{INR}	$\overline{INT}$ Reset Time		15		25		25		35	ns
SEMAPHORE TIMING										
t_{SOP}	$\overline{SEM}$ Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10		10		15		20		ns
t_{SWRD}	SEM Flag Write to Read Time	5		5		5		5		ns
t_{SPS}	SEM Flag Contention Window	5		5		5		5		ns

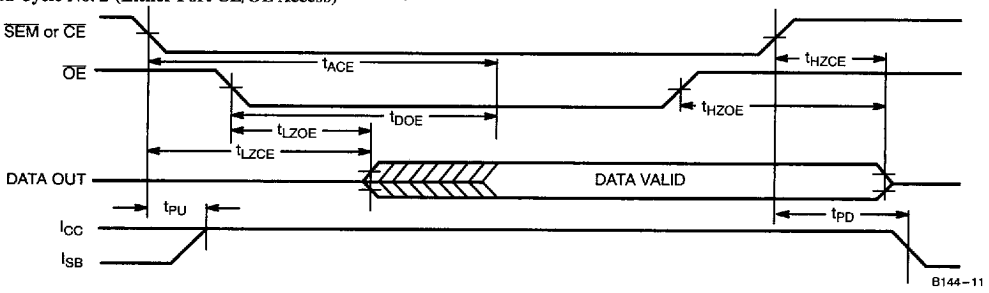
Notes:
13. For information on part-to-part delay through RAM cells from writing port to reading port, refer to Read Timing with Port-to-Port Delay waveform.
14. Test conditions used are Load 2.

Switching Waveforms

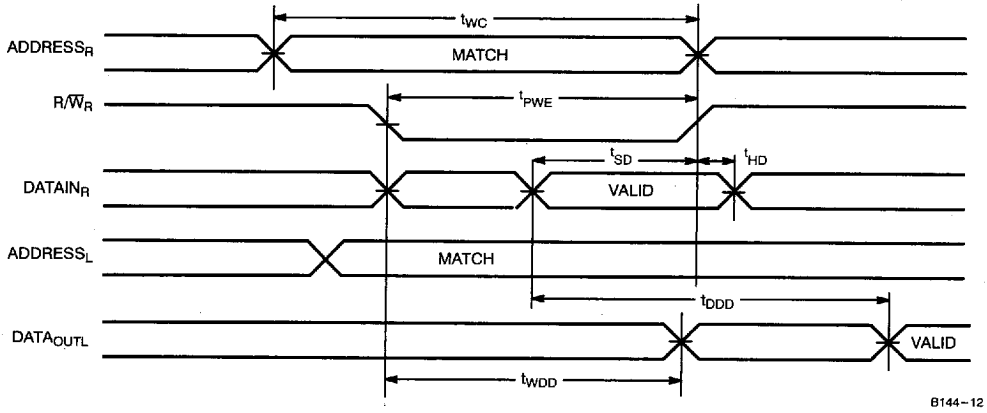
Read Cycle No. 1 (Either Port Address Access)[15, 16]



Read Cycle No. 2 (Either Port $\overline{CE}/\overline{OE}$ Access)[15, 17, 18]



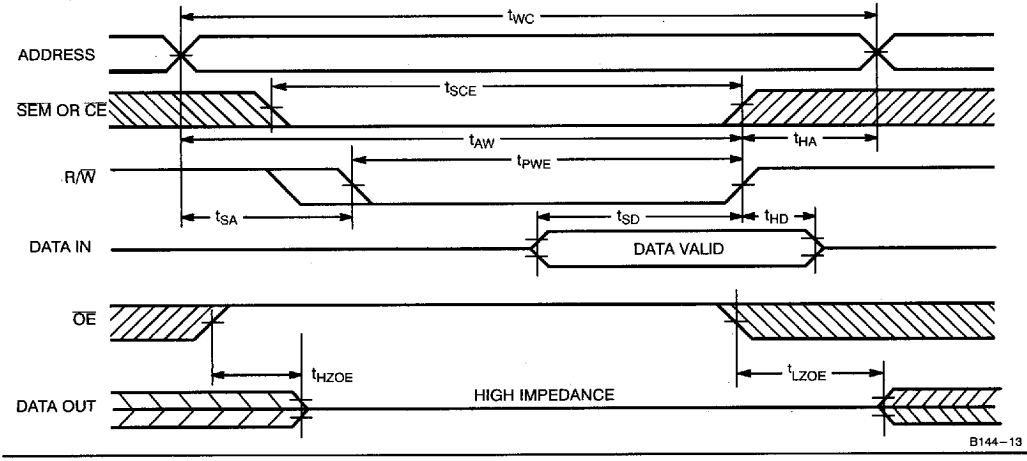
Read Timing with Port-to-Port Delay ($M/\overline{S}$ = L)[19, 20]



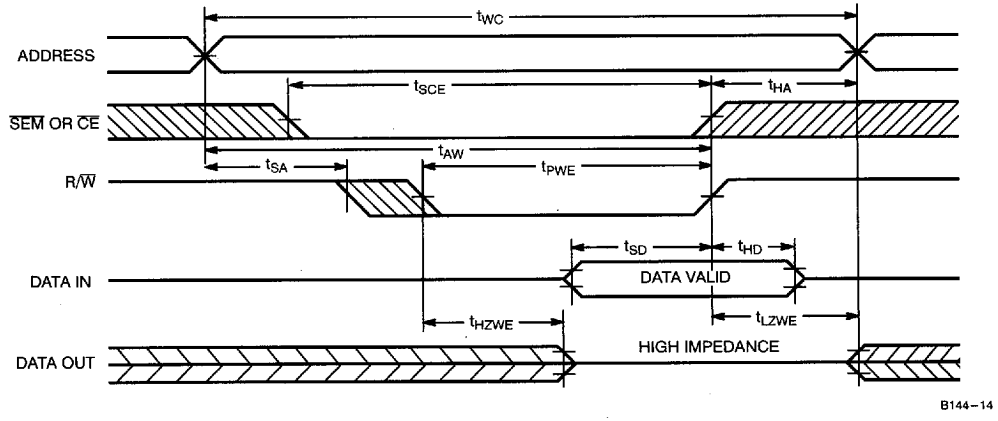
Notes:
15. $R/\overline{W}$ is HIGH for read cycle.
16. Device is continuously selected $\overline{CE}$ = LOW and $\overline{OE}$ = LOW. This waveform cannot be used for semaphore reads.
17. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
18. $\overline{CE}_L$ = L, $\overline{SEM}$ = H when accessing RAM. $\overline{CE}$ = H, $\overline{SEM}$ = L when accessing semaphores.
19. $\overline{BUSY}$ = HIGH for the writing port.
20. $\overline{CE}_L = \overline{CE}_R$ = LOW.

Switching Waveforms (continued)

Write Cycle No. 1: $\overline{OE}$ Three-State Data I/Os (Either Port)[21, 22, 23]



Write Cycle No. 2: R/$\overline{W}$ Three-State Data I/Os (Either Port)[21, 23, 24]

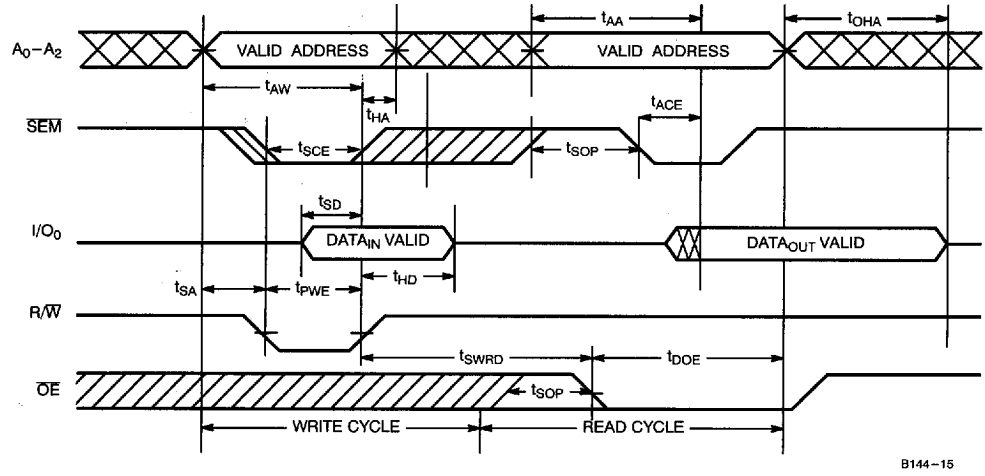


Notes:

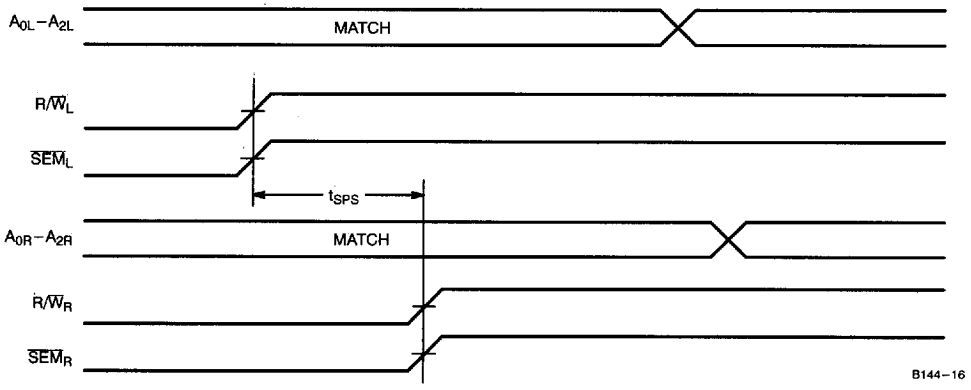
21. The internal write time of the memory is defined by the overlap of $\overline{CE}$ or $\overline{SEM}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write, and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
22. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during a R/$\overline{W}$ controlled write cycle (as in this example), this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
23. R/$\overline{W}$ must be HIGH during all address transitions.
24. Data I/O pins enter high impedance when $\overline{OE}$ is held LOW during write.

Switching Waveforms (continued)

Semaphore Read After Write Timing, Either Side[25]



Semaphore Contention[26, 27, 28]

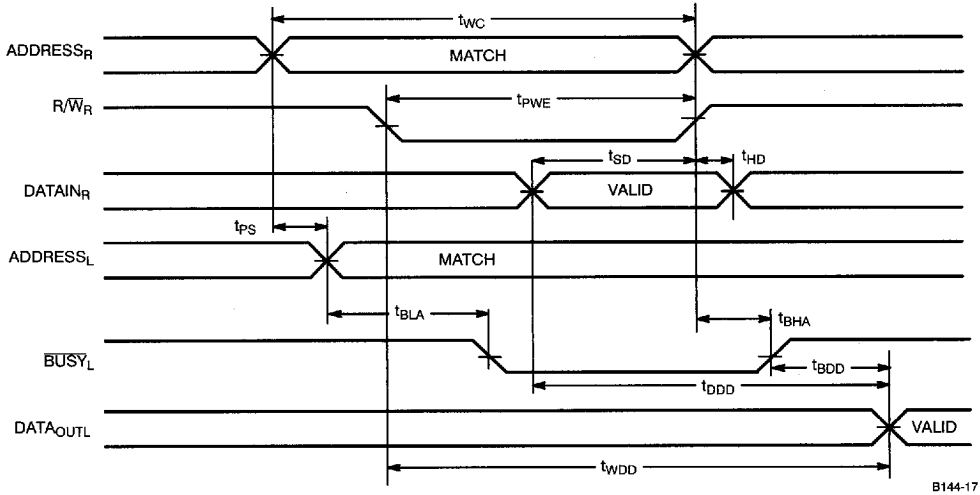


Notes:

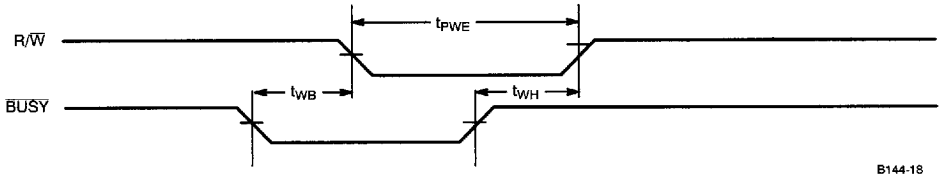
25. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).
26. $I/O_{0R} = I/O_{0L}$ = LOW (request semaphore); $\overline{CE}_R = \overline{CE}_L$ = HIGH
27. Semaphores are reset (available to both ports) at cycle start.
28. If t_{SPS} is violated, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Switching Waveforms (continued)

Read with $\overline{BUSY}$ (M/$\overline{S}$=HIGH)[20]



Write Timing with Busy Input (M/$\overline{S}$=LOW)



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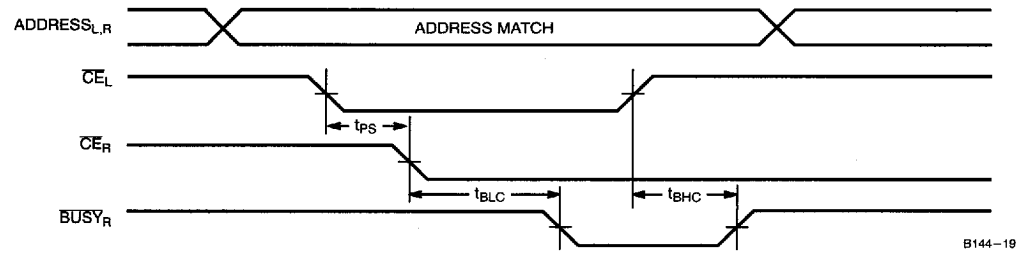
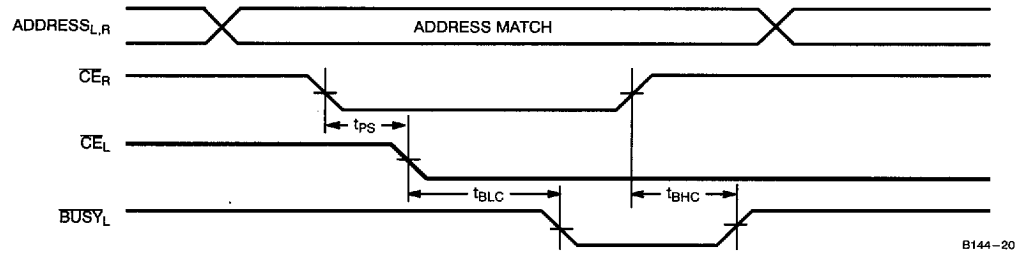
Switching Waveforms (continued)

Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)[29]

$\overline{CE}_L$ Valid First:

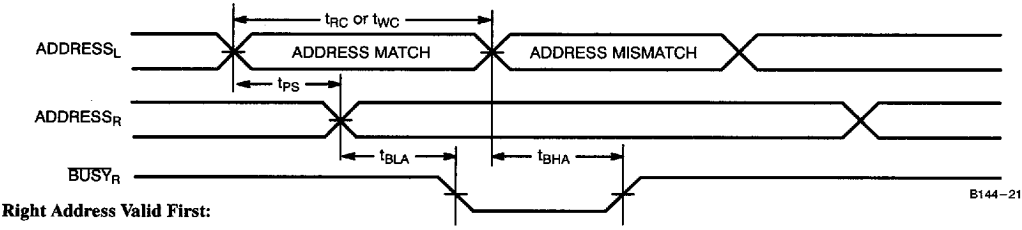


$\overline{CE}_R$ Valid First:

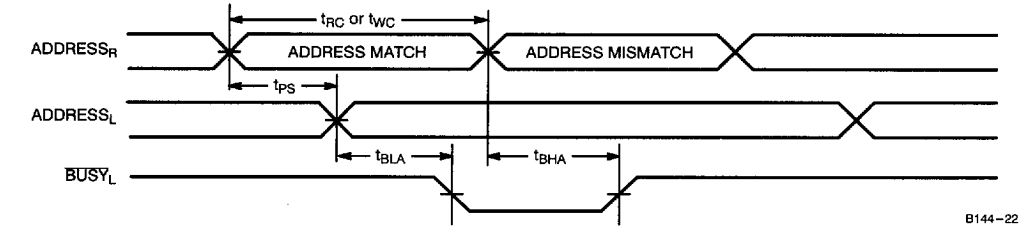


Busy Timing Diagram No. 2 (Address Arbitration)[29]

Left Address Valid First:



Right Address Valid First:



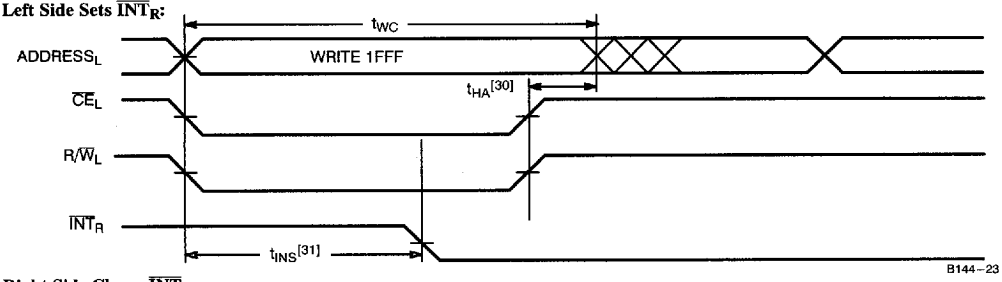
Note:

29. If t_{PS} is violated, the busy signal will be asserted on one side or the other, but there is no guarantee on which side $\overline{BUSY}$ will be asserted
30. t_{HA} depends on which enable pin ($\overline{CE}_L$ or R/$\overline{W}_L$) is deasserted first.
31. t_{INS} or t_{INR} depends on which enable pin ($\overline{CE}_L$ or R/$\overline{W}_L$) is asserted last.

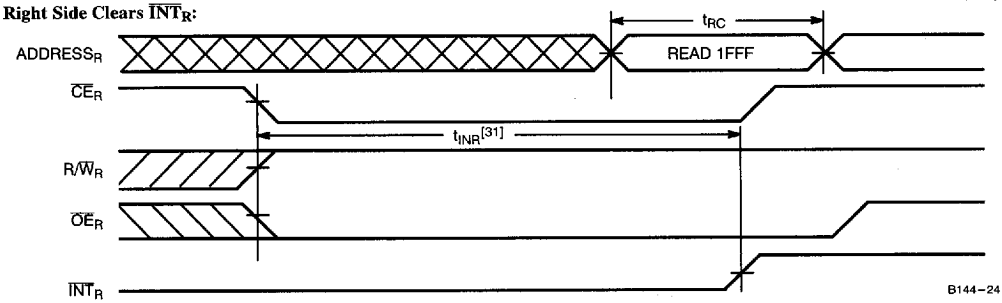
Switching Waveforms (continued)

Interrupt Timing Diagrams

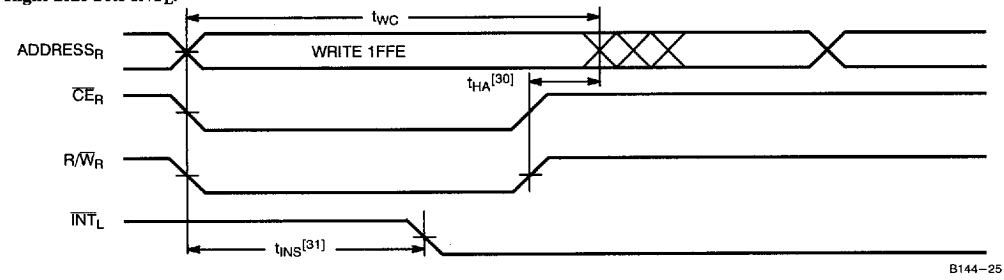
Left Side Sets $\overline{INT}_R$:



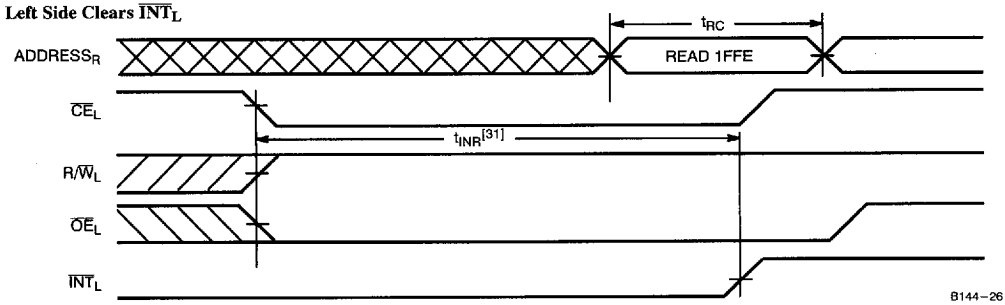
Right Side Clears $\overline{INT}_R$:



Right Side Sets $\overline{INT}_L$:



Left Side Clears $\overline{INT}_L$



Architecture

The CY7B144/5 consists of a an array of 8K words of 8/9 bits each of dual-port RAM cells, I/O and address lines, and control signals ($\overline{CE}$, $\overline{OE}$, R/$\overline{W}$). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a $\overline{BUSY}$ pin is provided on each port. Two interrupt ($\overline{INT}$) pins can be utilized for port-to-port communication. Two semaphore ($\overline{SEM}$) control pins are used for allocating shared resources. With the M/$\overline{S}$ pin, the CY7B144/5 can function as a Master ($\overline{BUSY}$ pins are outputs) or as a slave ($\overline{BUSY}$ pins are inputs). The CY7B144/5 has an automatic power-down feature controlled by $\overline{CE}$. Each port is provided with its own output enable control ($\overline{OE}$), which allows data to be read from the device.

Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/$\overline{W}$ in order to guarantee a valid write. A write operation is controlled by either the $\overline{OE}$ pin (see Write Cycle No.1 waveform) or the R/$\overline{W}$ pin (see Write Cycle No. 2 waveform). Data can be written to the device t_{HZOE} after the $\overline{OE}$ is deasserted or t_{HZWE} after the falling edge of R/$\overline{W}$. Required inputs for non-contention operations are summarized in *Table 1*.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must be met before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port t_{DDD} after the data is presented on the other port.

Read Operation

When reading the device, the user must assert both the $\overline{OE}$ and $\overline{CE}$ pins. Data will be available t_{ACE} after $\overline{CE}$ or t_{DOE} after $\overline{OE}$ are asserted. If the user of the CY7B144/5 wishes to access a semaphore flag, then the $\overline{SEM}$ pin must be asserted instead of the $\overline{CE}$ pin.

Interrupts

The interrupt flag ($\overline{INT}$) permits communications between ports. When the left port writes to location 1FFF, the right port's interrupt flag ($\overline{INT_R}$) is set. This flag is cleared when the right port reads that same location. Setting the left port's interrupt flag ($\overline{INT_L}$) is accomplished when the right port writes to location 1FFE. This flag is cleared when the left port reads location 1FFE. The message at 1FFF or 1FFE is user-defined. See *Table 2* for input requirements for $\overline{INT}$. $\overline{INT_R}$ and $\overline{INT_L}$ are push-pull outputs and do not require pull-up resistors to operate.

Busy

The CY7B144/5 provides on-chip arbitration to alleviate simultaneous memory location access (contention). If both ports' $\overline{CE}$s are asserted and an address match occurs within t_{PS} of each other the Busy logic will determine which port has access. If t_{PS} is violated, one port will definitely gain permission to the location, but it is not guaranteed which one. $\overline{BUSY}$ will be asserted t_{BLA} after an address match or t_{BLC} after $\overline{CE}$ is taken LOW. $\overline{BUSY_L}$ and $\overline{BUSY_R}$ in master mode are push-pull outputs and do not require pull-up resistors to operate.

Master/Slave

An M/$\overline{S}$ pin is provided in order to expand the word width by configuring the device as either a master or a slave. The $\overline{BUSY}$ output of the master is connected to the $\overline{BUSY}$ input of the slave. This will allow the device to interface to a master device with no external components. Writing of slave devices must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the slave chip may begin a write cycle during a contention situation. When presented a HIGH input, the M/$\overline{S}$ pin allows the device to be used as a master and therefore the $\overline{BUSY}$ line is an output. $\overline{BUSY}$ can then be used to send the arbitration outcome to a slave.

Semaphore Operation

The CY7B144/5 provides eight semaphore latches which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a 0 to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, $\overline{SEM}$ or $\overline{OE}$ must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value will be available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a 0), it assumes control over the shared resource, otherwise (reads a 1) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a 1), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a 1 is written to cancel its request.

Semaphores are accessed by asserting $\overline{SEM}$ LOW. The $\overline{SEM}$ pin functions as a chip enable for the semaphore latches ($\overline{CE}$ must remain HIGH during $\overline{SEM}$ LOW). A_{0-2} represents the semaphore address. $\overline{OE}$ and R/$\overline{W}$ are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a 0 is written to the left port of an unused semaphore, a 1 will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing 0 (the left port in this case). If the left port now relinquishes control by writing a 1 to the semaphore, the semaphore will be set to 1 for both sides. However, if the right port had requested the semaphore (written a 0) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. *Table 3* shows sample semaphore operations.

When reading a semaphore, all eight data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{SPS} of each other, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Initialization of the semaphore is not automatic and must be reset during initialization program at power-up. all Semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

Table 1. Non-Contending Read/Write

Inputs				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O_{0-7}	Operation
H	X	X	H	High Z	Power-Down
H	H	L	L	Data Out	Read Data in Semaphore
X	X	H	X	High Z	I/O Lines Disabled
H	⌐	X	L	Data In	Write to Semaphore
L	H	L	H	Data Out	Read
L	L	X	H	Data In	Write
L	X	X	L		Illegal Condition

Table 2. Interrupt Operation Example (assumes $\overline{BUSY}_L$=$\overline{BUSY}_R$=HIGH)

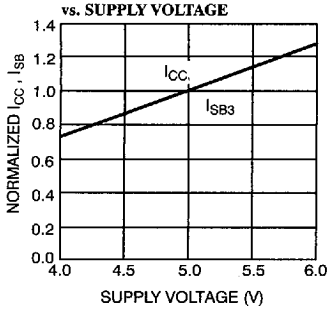
	Left Port					Right Port				
Function	R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	A_{0-12}	$\overline{INT}$	R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	A_{0-12}	$\overline{INT}$
Set Left $\overline{INT}$	X	X	X	X	L	L	L	X	1FFE	X
Reset Left $\overline{INT}$	X	L	L	1FFE	H	X	L	L	X	X
Set Right $\overline{INT}$	L	L	X	1FFF	X	X	X	X	X	L
Reset Right $\overline{INT}$	X	X	X	X	X	X	L	L	1FFF	H

Table 3. Semaphore Operation Example

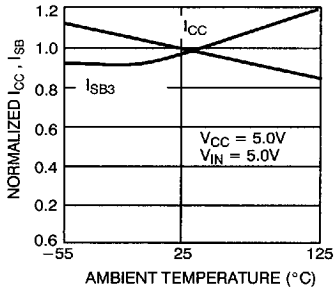
Function	I/O_0 Left	I/O_0 Right	Status
No action	1	1	Semaphore free
Left port writes semaphore	0	1	Left port obtains semaphore
Right port writes 0 to semaphore	0	1	Right side is denied access
Left port writes 1 to semaphore	1	0	Right port is granted access to semaphore
Left port writes 0 to semaphore	1	0	No change. Left port is denied access
Right port writes 1 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore address
Right port writes 0 to semaphore	1	0	Right port obtains semaphore
Right port writes 1 to semaphore	1	1	No port accessing semaphore
Left port writes 0 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore

Typical DC and AC Characteristics

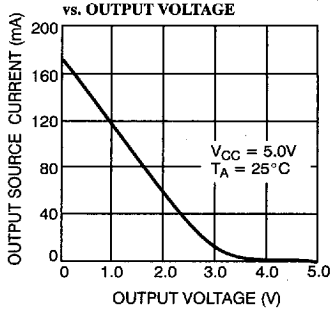
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



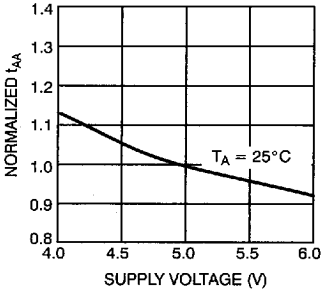
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



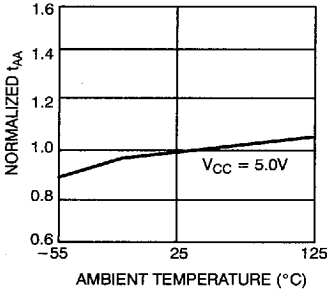
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



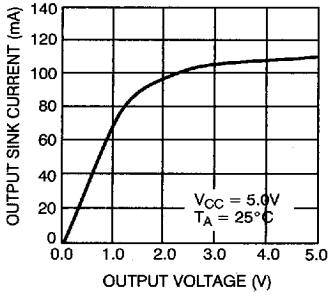
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



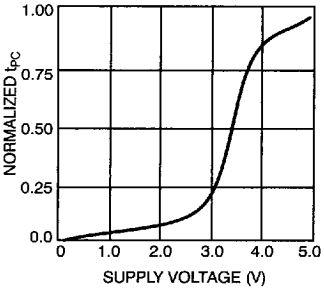
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



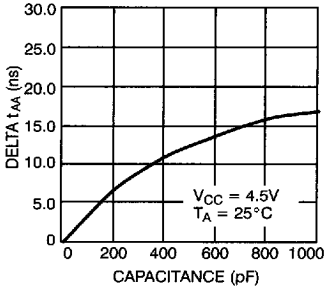
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



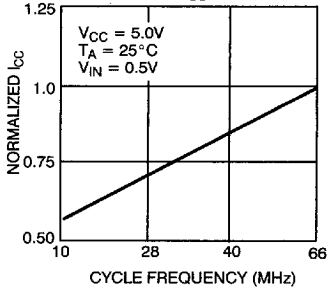
TYPICAL POWER−ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7B144–15AC	A65	64-Lead Thin Quad Flat Pack	Commercial
	CY7B144–15JC	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7B144–25AC	A65	64-Lead Thin Quad Flat Pack	Commercial
	CY7B144–25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B144–25AI	A65	64-Lead Thin Quad Flat Pack	Industrial
	CY7B144–25JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B144–25LMB	L81	68-Square Leadless Chip Carrier	Military
35	CY7B144–35AC	A65	64-Lead Thin Quad Flat Pack	Commercial
	CY7B144–35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B144–35AI	A65	64-Lead Thin Quad Flat Pack	Industrial
	CY7B144–35JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B144–35LMB	L81	68-Square Leadless Chip Carrier	Military
55	CY7B144–55AC	A65	64-Lead Thin Quad Flat Pack	Commercial
	CY7B144–55JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B144–55AI	A65	64-Lead Thin Quad Flat Pack	Industrial
	CY7B144–55JI	J81	68-Lead Plastic Leaded Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7B145–15AC	A80	80-Lead Thin Quad Flat Pack	Commercial
	CY7B145–15JC	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7B145–25AC	A80	80-Lead Thin Quad Flat Pack	Commercial
	CY7B145–25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B145–25AI	A80	80-Lead Thin Quad Flat Pack	Industrial
	CY7B145–25JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B145–25LMB	L81	68-Square Leadless Chip Carrier	Military
35	CY7B145–35AC	A80	80-Lead Thin Quad Flat Pack	Commercial
	CY7B145–35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B145–35AI	A80	80-Lead Thin Quad Flat Pack	Industrial
	CY7B145–35JI	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B145–35LMB	L81	68-Square Leadless Chip Carrier	Military
55	CY7B145–55AC	A80	80-Lead Thin Quad Flat Pack	Commercial
	CY7B145–55JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7B145–55AI	A80	80-Lead Thin Quad Flat Pack	Industrial
	CY7B145–55JI	J81	68-Lead Plastic Leaded Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
BUSY/INTERRUPT TIMING	
t_{BLA}	7, 8, 9, 10, 11
t_{BHA}	7, 8, 9, 10, 11
t_{BLC}	7, 8, 9, 10, 11
t_{BHC}	7, 8, 9, 10, 11
t_{PS}	7, 8, 9, 10, 11
t_{INS}	7, 8, 9, 10, 11
t_{INR}	7, 8, 9, 10, 11
BUSY TIMING	
t_{WB}	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{BDD}	7, 8, 9, 10, 11
t_{DDD}	7, 8, 9, 10, 11
t_{WDD}	7, 8, 9, 10, 11

Document #: 38-00163-G