



PSMN1R1-40BS

N-channel 40 V 1.3 m Ω standard level MOSFET in D2PAK

Rev. 2 — 29 February 2012

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in D2PAK (SOT404) package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive sources

1.3 Applications

- DC-to-DC convertors
- Motor control
- Load switching
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference data

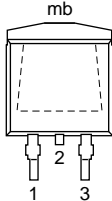
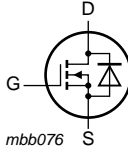
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|--|---|-------|------|-----|------------|
| V _{DS} | drain-source voltage | T _j ≥ 25 °C; T _j ≤ 175 °C | - | - | 40 | V |
| I _D | drain current | T _{mb} = 25 °C; V _{GS} = 10 V; see Figure 1 | [1] - | - | 120 | A |
| P _{tot} | total power dissipation | T _{mb} = 25 °C; see Figure 2 | - | - | 306 | W |
| T _j | junction temperature | | -55 | - | 175 | °C |
| Static characteristics | | | | | | |
| R _{DSon} | drain-source on-state resistance | V _{GS} = 10 V; I _D = 25 A; T _j = 100 °C; see Figure 12 ; see Figure 13 | - | 1.68 | 2 | m Ω |
| | | V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; see Figure 13 | - | 1.16 | 1.3 | m Ω |
| Dynamic characteristics | | | | | | |
| Q _{GD} | gate-drain charge | V _{GS} = 10 V; I _D = 75 A; V _{DS} = 20 V; see Figure 14 ; see Figure 15 | - | 32 | - | nC |
| Q _{G(tot)} | total gate charge | | - | 136 | - | nC |
| Avalanche ruggedness | | | | | | |
| E _{DS(AL)S} | non-repetitive drain-source avalanche energy | V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 120 A; V _{sup} ≤ 40 V; unclamped; R _{GS} = 50 Ω ; t _p = 0.1 ms | - | - | 1.4 | J |

[1] Continuous current is limited by package



2. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|----------------------|---|---|
| 1 | G | gate |  |  |
| 2 | D | drain ^[1] | | |
| 3 | S | source | | |
| mb | D | drain | | |

SOT404 (D2PAK)

[1] It is not possible to make connection to pin 2.

3. Ordering information

Table 3. Ordering information

| Type number | Package | | Version |
|--------------|---------|--|---------|
| | Name | Description | |
| PSMN1R1-40BS | D2PAK | plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) | SOT404 |

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit | |
|--------------|----------------------------|---|-----|------|------|---|
| V_{DS} | drain-source voltage | $T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$ | - | 40 | V | |
| V_{DGR} | drain-gate voltage | $T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}; R_{GS} = 20\text{ k}\Omega$ | - | 40 | V | |
| V_{GS} | gate-source voltage | | -20 | 20 | V | |
| I_D | drain current | $V_{GS} = 10\text{ V}; T_{mb} = 100\text{ °C}$ | [1] | - | 120 | A |
| | | $V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C};$ see Figure 1 | [1] | - | 120 | A |
| I_{DM} | peak drain current | pulsed; $t_p \leq 10\text{ }\mu\text{s}; T_{mb} = 25\text{ °C};$ see Figure 3 | - | 1320 | A | |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C};$ see Figure 2 | - | 306 | W | |
| T_{stg} | storage temperature | | -55 | 175 | °C | |
| T_j | junction temperature | | -55 | 175 | °C | |
| $T_{sld(M)}$ | peak soldering temperature | | - | 260 | °C | |

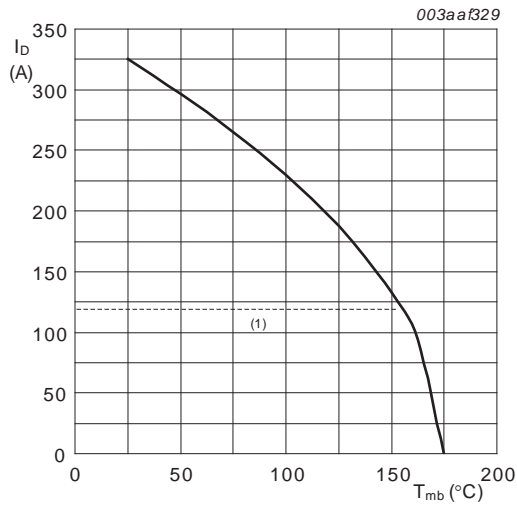
Source-drain diode

| | | | | | | |
|----------|---------------------|---|-----|---|------|---|
| I_S | source current | $T_{mb} = 25\text{ °C}$ | [1] | - | 120 | A |
| I_{SM} | peak source current | pulsed; $t_p \leq 10\text{ }\mu\text{s}; T_{mb} = 25\text{ °C}$ | - | - | 1320 | A |

Avalanche ruggedness

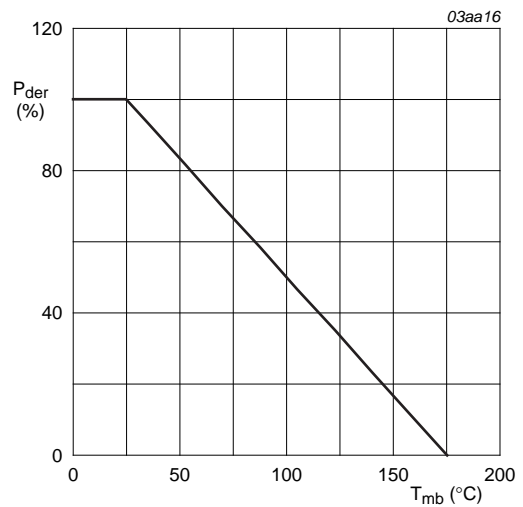
| | | | | | | |
|---------------|--|---|---|---|-----|---|
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C}; I_D = 120\text{ A}; V_{sup} \leq 40\text{ V};$ unclamped; $R_{GS} = 50\text{ }\Omega; t_p = 0.1\text{ ms}$ | - | - | 1.4 | J |
|---------------|--|---|---|---|-----|---|

[1] Continuous current is limited by package.



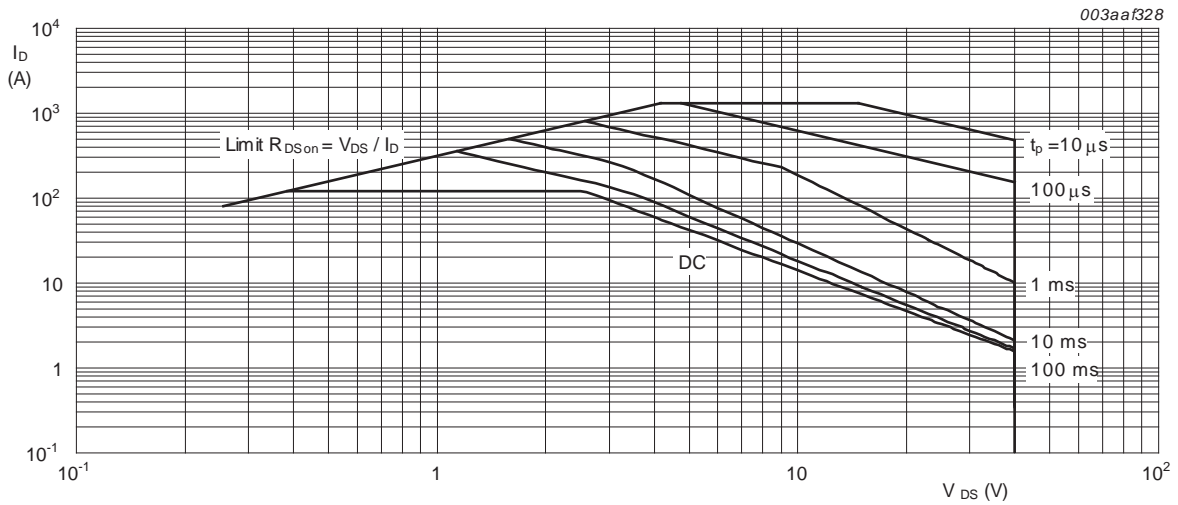
$V_{GS} \geq 10$ V; (1) Capped at 120 A due to package

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



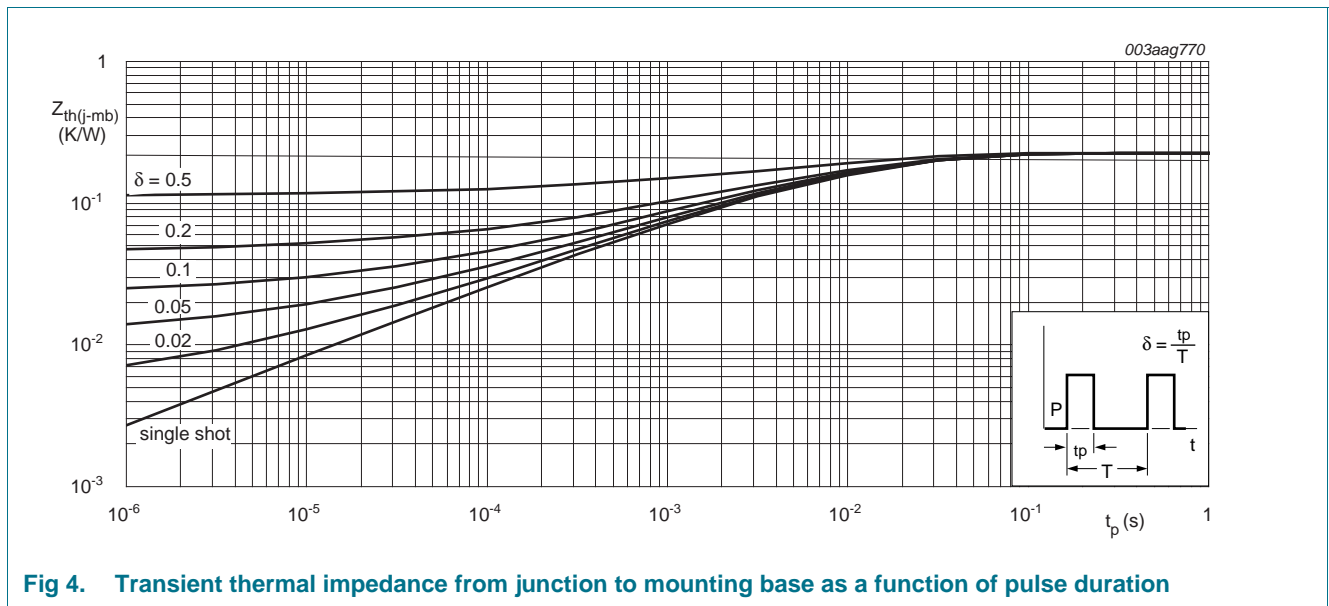
$T_{mb} = 25$ °C; I_{DM} is a single pulse; Capped at 120 A due to package

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|---|---|-----|------|------|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | see Figure 4 | - | 0.22 | 0.49 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | minimum footprint; mounted on a printed-circuit board | - | 50 | - | K/W |



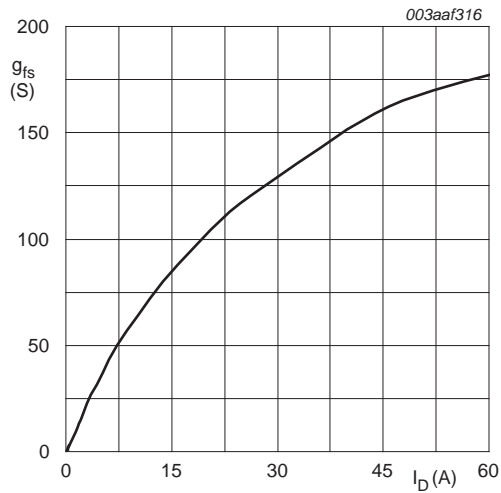
6. Characteristics

Table 6. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|-----------------------------------|--|-----|------|-----|---------|
| Static characteristics | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$ | 36 | - | - | V |
| | | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$ | 40 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$; see Figure 10 | - | - | 4.6 | V |
| | | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C$; see Figure 10 | 1 | - | - | V |
| | | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$; see Figure 11 ; see Figure 10 | 2 | 3 | 4 | V |
| I_{DSS} | drain leakage current | $V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$ | - | 0.02 | 10 | μA |
| | | $V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 \text{ }^\circ C$ | - | - | 500 | μA |
| I_{GSS} | gate leakage current | $V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$ | - | 10 | 100 | nA |
| | | $V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$ | - | 10 | 100 | nA |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 10 V; I_D = 25 A; T_j = 100 \text{ }^\circ C$; see Figure 12 ; see Figure 13 | - | 1.68 | 2 | mΩ |
| | | $V_{GS} = 10 V; I_D = 25 A; T_j = 175 \text{ }^\circ C$; see Figure 12 ; see Figure 13 | - | 2.3 | 2.8 | mΩ |
| | | $V_{GS} = 10 V; I_D = 25 A; T_j = 25 \text{ }^\circ C$; see Figure 13 | - | 1.16 | 1.3 | mΩ |
| R_G | internal gate resistance (AC) | $f = 1 \text{ MHz}$ | - | 1.1 | - | Ω |
| Dynamic characteristics | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$ | - | 133 | - | nC |
| | | $I_D = 75 A; V_{DS} = 20 V; V_{GS} = 10 V$; see Figure 14 ; see Figure 15 | - | 136 | - | nC |
| Q_{GS} | gate-source charge | | - | 52 | - | nC |
| $Q_{GS(th)}$ | pre-threshold gate-source charge | | - | 30 | - | nC |
| $Q_{GS(th-pl)}$ | post-threshold gate-source charge | | - | 22 | - | nC |
| Q_{GD} | gate-drain charge | | - | 32 | - | nC |
| $V_{GS(pl)}$ | gate-source plateau voltage | $I_D = 75 A; V_{DS} = 20 V$; see Figure 14 ; see Figure 15 | - | 6.1 | - | V |
| C_{iss} | input capacitance | $V_{DS} = 20 V; V_{GS} = 0 V; f = 1 \text{ MHz}$; | - | 9710 | - | pF |
| C_{oss} | output capacitance | $T_j = 25 \text{ }^\circ C$; see Figure 16 | - | 2042 | - | pF |
| C_{rss} | reverse transfer capacitance | | - | 994 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS} = 20 V; R_L = 0.8 \text{ } \Omega; V_{GS} = 5 V$; | - | 45 | - | ns |
| t_r | rise time | $R_{G(ext)} = 4.7 \text{ } \Omega$ | - | 66 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 111 | - | ns |
| t_f | fall time | | - | 53 | - | ns |

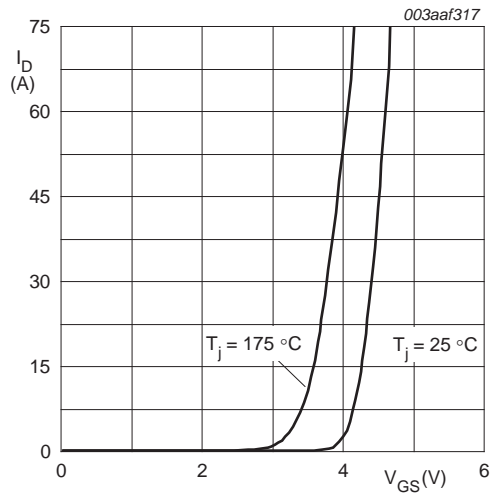
Table 6. Characteristics ...continued

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------|-----------------------|--|-----|-----|-----|------|
| Source-drain diode | | | | | | |
| V_{SD} | source-drain voltage | $I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$; see Figure 17 | - | 0.8 | 1.2 | V |
| t_{rr} | reverse recovery time | $I_S = 25\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; | - | 64 | - | ns |
| Q_r | recovered charge | $V_{DS} = 20\text{ V}$ | - | 117 | - | nC |



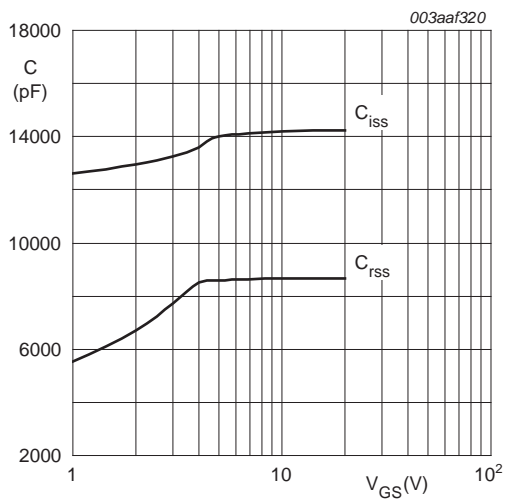
$T_j = 25\text{ °C}; V_{DS} = 25\text{ V}$

Fig 5. Forward transconductance as a function of drain current; typical values



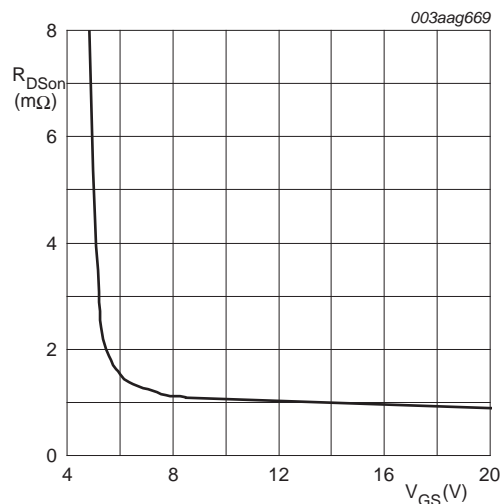
$V_{DS} > I_D \times R_{DS(on)}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



$V_{DS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 7. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



$T_j = 25\text{ °C}; V_{DS} = 25\text{ V}$

Fig 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

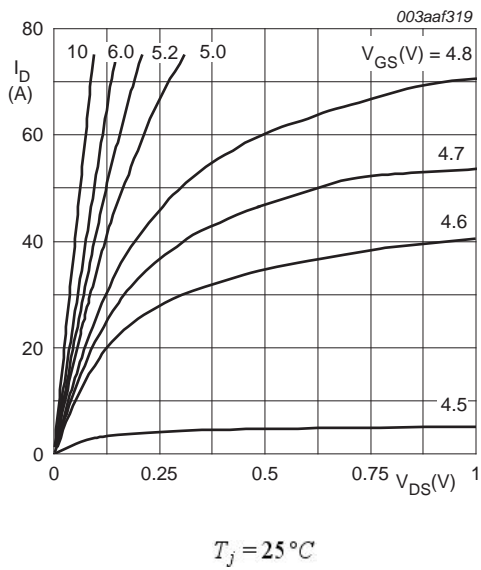


Fig 9. Output characteristics: drain current as a function of drain-source voltage; typical values

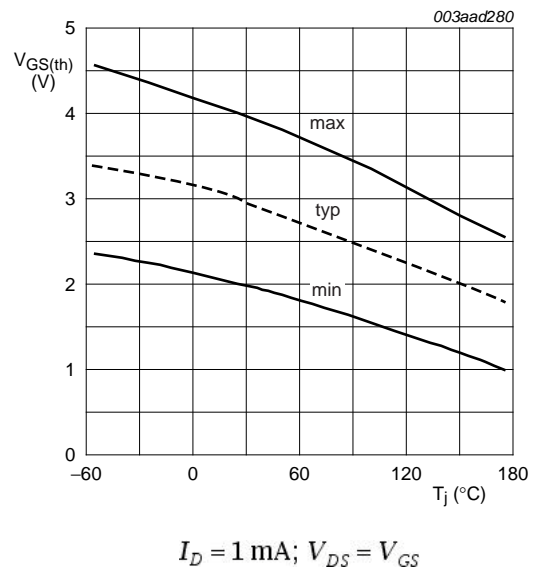


Fig 10. Gate-source threshold voltage as a function of junction temperature

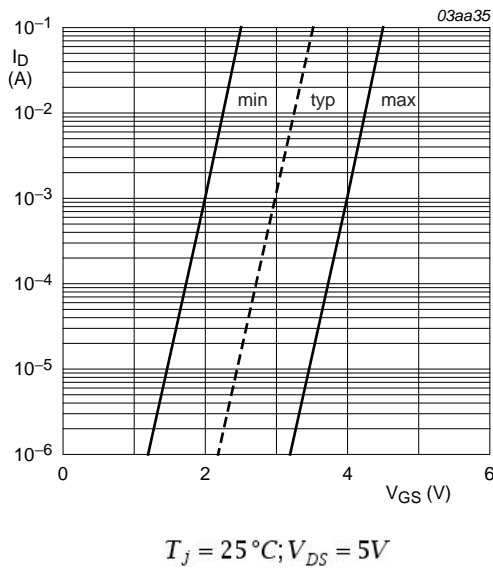


Fig 11. Sub-threshold drain current as a function of gate-source voltage

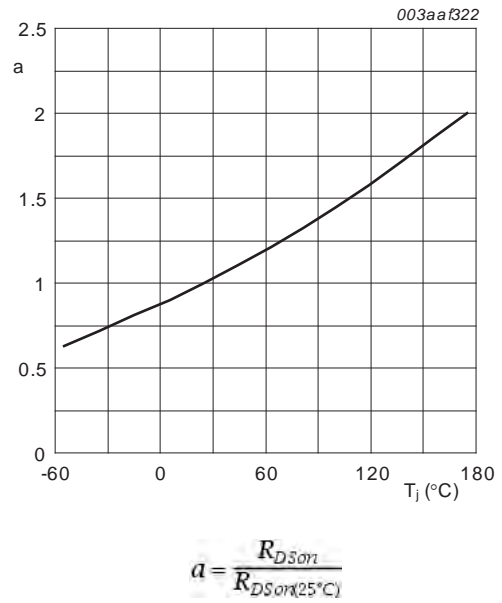
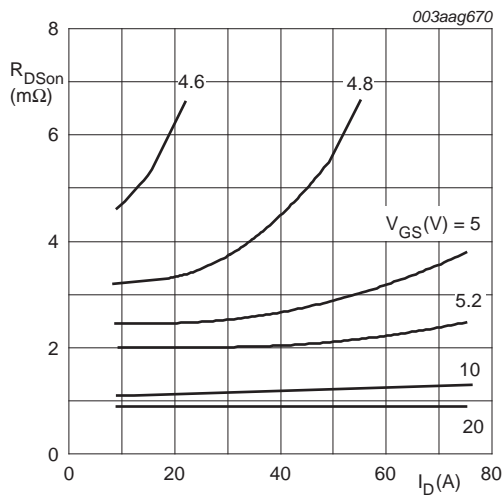


Fig 12. Normalized drain-source on state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)@25^\circ C}}$$



$T_j = 25^\circ C$

Fig 13. Drain-source on-state resistance as a function of drain current; typical values

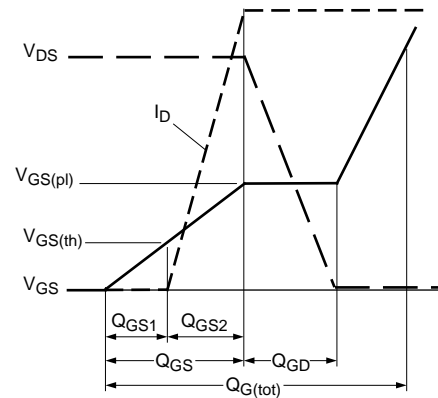
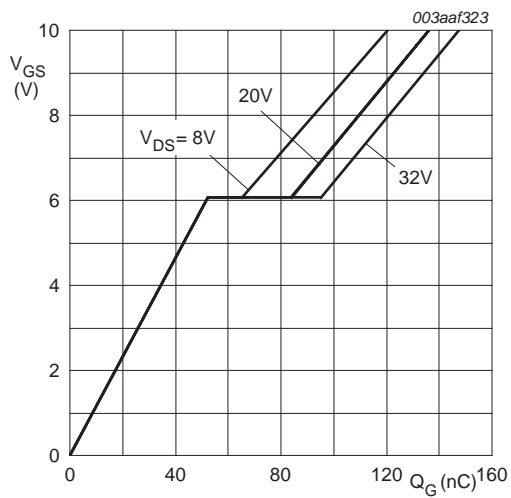
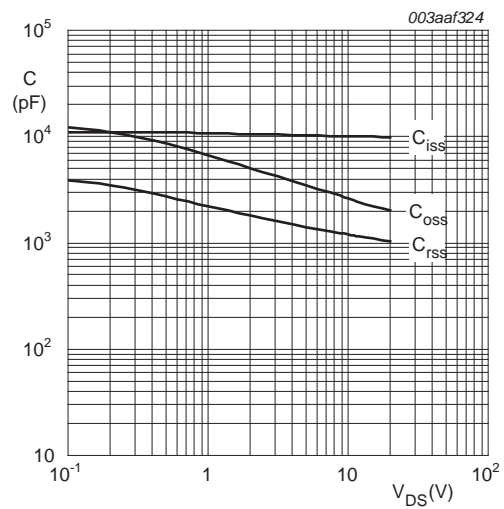


Fig 14. Gate charge waveform definitions



$I_D = 75 A$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0V; f = 1MHz$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

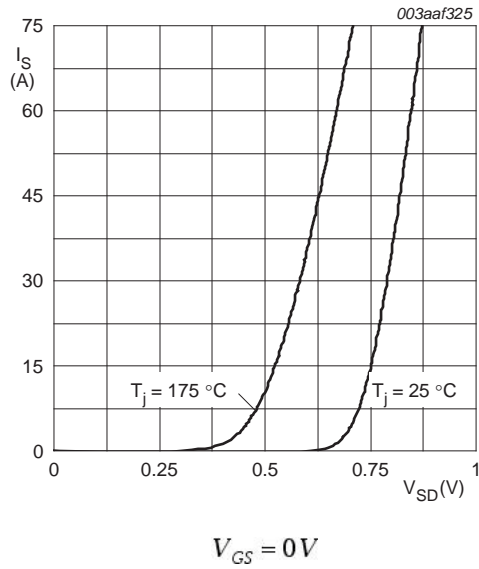


Fig 17. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404



Fig 18. Package outline SOT404 (D2PAK)

8. Revision history

Table 7. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|------------------|---|----------------------|---------------|------------------|
| PSMN1R1-40BS v.2 | 20120229 | Product data sheet | - | PSMN1R1-40BS v.1 |
| Modifications: | <ul style="list-style-type: none">• Status changed from objective to product.• Various changes to content. | | | |
| PSMN1R1-40BS v.1 | 20110929 | Objective data sheet | - | - |

9. Legal information

9.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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