CX77105

Power Amplifier Module for CDMA/AMPS (824–849 MHz)

The CX77105, a dual-mode, Code Division Multiple Access (CDMA) / Advanced Mobile Phone Service (AMPS) Power Amplifier Module (PAM), is a fully matched, 10-pin surface mount module developed for cellular handsets and wireless local loop applications. This small and efficient power amplifier module packs a full 824–849 MHz bandwidth coverage into a single compact package. The device meets the stringent IS95 CDMA linearity requirements to and exceeding 28 dBm output power, and can be driven to levels beyond 31 dBm for high efficiency in FM mode operation. A low current digital pin (VCONT) provides improved efficiency for the low RF power range of operation.

The single Gallium Arsenide (GaAs) Microwave Monolithic Integrated Circuit (MMIC) contains all active circuitry in the module. The MMIC contains on-board bias circuitry, as well as input and interstage matching circuits. The output match is realized off-chip and within the module package to optimize efficiency and power performance into a 50 Ω load. This device is manufactured with Skyworks' GaAs Heterojunction Bipolar Transistor (HBT) process that provides for all positive voltage DC supply operation while maintaining high efficiency and good linearity. Primary bias to the CX77105 is supplied directly from a three-cell nickel cadmium, a single-cell lithium ion, or other suitable battery with an output in the 3–4 volt range. Power down is accomplished by setting the voltage on the low current reference pin to zero volts. No external supply side switch is needed as typical "off" leakage is a few microamperes with full primary voltage supplied from the battery.

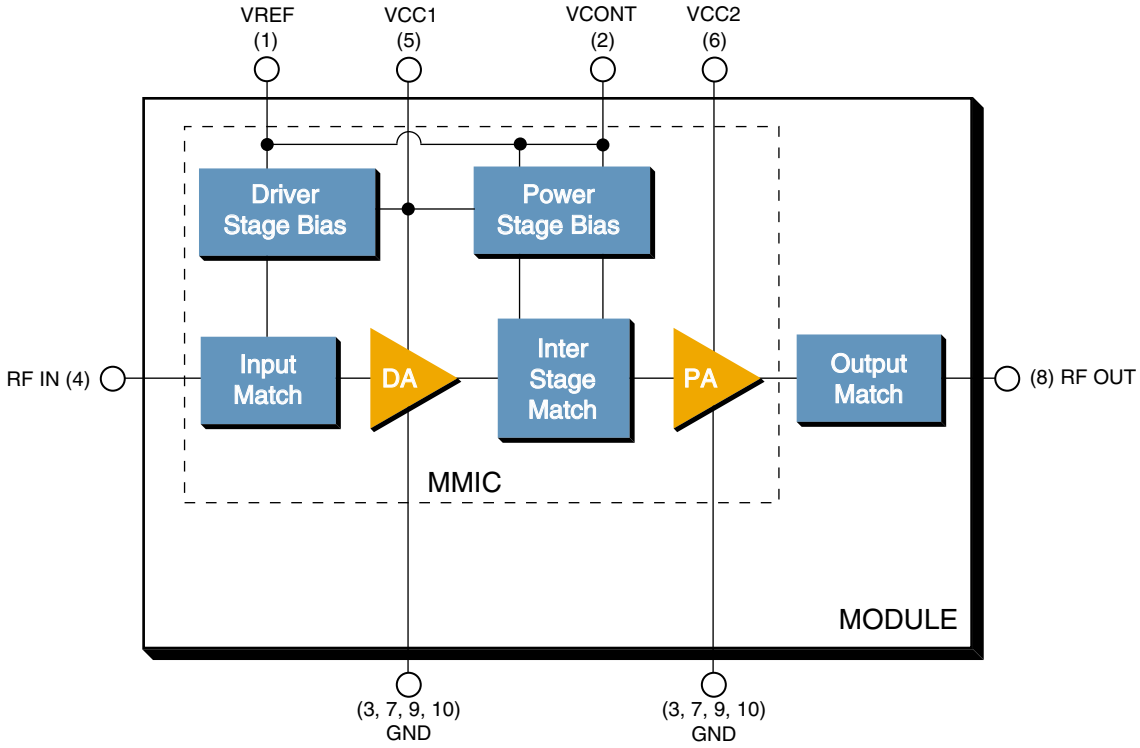
Distinguishing Features

- Low voltage positive bias supply (3.2 V to 4.2 V, typical)
- Good linearity
- High efficiency
- Dual mode operation
- Large dynamic range
- 10-pin package (4 x 4 x 1.5 mm)
- Power down control
- Low power-state control
- InGaP
- IS 95/CDMA2000

Applications

- Digital cellular (CDMA)
- Analog cellular (AMPS)
- Wireless local loop (WLL)

Functional Block Diagram



Electrical Specifications

The following tables list the electrical characteristics of the CX77105 Power Amplifier. Table 2 lists the recommended operating conditions for achieving the electrical performance listed in Table 4. Table 3 lists the electrical performance of the CX77105 Power Amplifier over the recommended operating conditions.

Table 1. Absolute Maximum Ratings(1)

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
RF Input Power	P_{IN}	—	4.0	7.0	dBm
Supply Voltage	V_{CC}	—	3.4	6.0	Volts
Reference Voltage	V_{REF}	—	3.0	3.1	Volts
Case Operating Temperature	T_C	–30	25	+110	°C
Storage Temperature	T_{STG}	–55	—	+125	°C

NOTE(S):
(1) No damage assuming only one parameter is set at limit at a time with all other parameters set at or below nominal value.

Table 2. Recommended Operating Conditions

Parameter		Symbol	Minimum	Nominal	Maximum	Unit
Supply Voltage		V_{CC}	3.2	3.4	4.2	Volts
Reference Voltage	PA On	V_{REF}	2.95	3.0	3.05	Volts
	PA Off	V_{REF}	—	—	0.5	
Mode Input Impedance >2.5 kΩ	High Bias	V_{CONT}	0.0	—	0.5	Volts
	Low Bias	V_{CONT}	2.5	—	3.0	
Operating Frequency		F_O	824.0	836.5	849.0	MHz
Operating Temperature		T_O	–30	—	+85	°C

Table 3. Power Range Truth Table

Power Mode	VREF	VCONT	Range
High Power	3.0 V	0.0–0.5 V	16 dBm–28 dBm
Low Power	3.0 V	2.5–3.0 V	≤ 16 dBm
Shut Down	0.0 V	0.0 V	—

Table 4. Electrical Specifications for CDMA / AMPS Nominal Operating Conditions[1]

Characteristics		Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain conditions	Digital Mode	G_{LOW}	$V_{CONT} \geq 2.5$ V, $P_O = 16$ dBm	25.0	27.0	28.0	dB
		G_{HIGH}	$V_{CONT} \leq 0.5$ V, $P_O = 28$ dBm	28.5	29.0	31.0	
	Analog Mode	G_P	$V_{CONT} \leq 0.5$ V, $P_O = 31$ dBm	27.5	29.0	31.0	
Power Added Efficiency	Digital Mode	PAE_{LOW}	$V_{CONT} \geq 2.5$ V, $P_O = 16$ dBm	7.6	8.5	—	%
		PAE_{HIGH}	$V_{CONT} \leq 0.5$ V, $P_O = 28$ dBm	37.0	40.0	—	
	Analog Mode	PAEa	$V_{CONT} \leq 0.5$ V, $P_O = 31$ dBm	48.0	55.0	—	
Total Supply Current		I_{CC_LOW}	$P_O = 16$ dBm	—	137	153	mA
		I_{CC_HIGH}	$P_O = 28$ dBm	—	490	500	
Quiescent Current		I_{Q_LOW}	$V_{CONT} \geq 2.5$ V	40	55	75	mA
		I_{Q_HIGH}	$V_{CONT} \leq 0.5$ V	60	78	105	
Reference Current		I_{REF}	—	—	2.5	5.0	mA
Control Current		I_{CTRL}	$V_{CONT} = 2.5$ V	200	235	500	µA
Total Supply current in Power-down Mode		I_{PD}	$V_{CC} = 3.4$ V, $V_{REF} = 0$ V	—	3.0	5.0	µA
Adjacent Channel Power[2][3]	885 kHz offset	$ACP1_{LOW}$	$V_{CONT} \geq 2.5$ V, $P_O \leq 16$ dBm	—	–49.0	–47.3	dBc
		$ACP1_{HIGH}$	$V_{CONT} \leq 0.5$ V, $P_O \leq 28$ dBm	—	–50.0	–47.0	
	1.98 MHz offset	$ACP2_{LOW}$	$V_{CONT} \geq 2.5$ V, $P_O \leq 16$ dBm or $V_{CONT} \leq 0.5$ V, $P_O \leq 28$ dBm	—	–65.0	–59.0	
		$ACP2_{HIGH}$		—	–60.0	–57.4	
Harmonic Suppression	Second	F_O2	$P_O \leq 28$ dBm	—	–38.0	–35.0	dBc
	Third	F_O3	$P_O \leq 28$ dBm	—	–59.0	–45.0	

Table 4. Electrical Specifications for CDMA / AMPS Nominal Operating Conditions(1)

Characteristics	Symbol	Condition	Minimum	Typical	Maximum	Unit
Noise Power in RX Band 869-894 MHz	RxBN	$P_O \leq 28$ dBm	—	–137	—	dBm/Hz
Noise Figure	NF	—	—	4.6	5.0	dB
Input Voltage Standing Wave Ratio	VSWR	—	—	—	1.9:1	—
Stability (Spurious output)	S	5:1 VSWR all phases	—	—	–60.0	dBc
Ruggedness—No damage(4)	Ru	$P_O \leq 28$ dBm	10:1	—	—	VSWR

NOTE(S):

(1) V_{CC} = +3.4 V, V_{REF} = +3.0 V, Freq = 836.5 MHz, T_C = 25 °C, unless otherwise specified.

(2) ACP is specified per IS95 as the ratio of the total in-band power (1.23 MHz BW) to adjacent power in a 30 kHz BW.

(3) CDMA2000 is configured as DCCH = 9600, SCHO = 9600, PCH (Walsh 0) = – 3.75 dB, and Peak-to-Average Ratio (CCDF = 1%) = 4.5 dB. For CDMA2000, 0.5 dB back-off in output power is required.

(4) All phases, time = 10 seconds.

Table 5. Electrical Specifications for CDMA / AMPS Recommended Operating Conditions(1)

Characteristics		Symbol	Condition	Minimum	Maximum	Unit
Gain conditions	Digital Mode	G_{LOW}	$V_{CONT} \geq 2.5$ V P_O = 16 dBm	24.0	28.5	dB
		G_{HIGH}	$V_{CONT} \leq 0.5$ V P_O = 28 dBm	27.1	32.4	
	Analog Mode	G_P	$V_{CONT} \leq 0.5$ V P_O = 31 dBm	24.0	33.0	
Adjacent Channel Power(2)(3)	1.25 MHz offset	$ACP1_{LOW}$	$V_{CONT} \geq 2.5$ V $P_O \leq 16$ dBm	—	–44	dBc
		$ACP1_{HIGH}$	$V_{CONT} \leq 0.5$ V $P_O \leq 28$ dBm	—	–44	dBc
	1.98 MHz offset	$ACP2_{LOW}$	$V_{CONT} \geq 2.5$ V $P_O \leq 16$ dBm or	—	–56	dBc
		$ACP2_{HIGH}$	$V_{CONT} \leq 0.5$ V $P_O \leq 28$ dBm	—	–56	dBc
Harmonic Suppression	Second	F_O2	$P_O \leq 28$ dBm	—	–30	dBc
	Third	F_O3	$P_O \leq 28$ dBm	—	–40	dBc

Table 5. Electrical Specifications for CDMA / AMPS Recommended Operating Conditions(1)

Characteristics	Symbol	Condition	Minimum	Maximum	Unit
Noise Power in RX Band 869-894 MHz	RxBN	$P_0 \leq 28$ dBm	—	–134.0	dBm/Hz
Noise Figure	NF	—	—	7.0	dB
Input Voltage Standing Wave Ratio (VSWR)	VSWR	—	—	2.0:1	—
Stability (Spurious output)	S	5:1 VSWR All phases	—	–60.0	dBc
Ruggedness – No damage(4)	Ru	$P_0 \leq 28$dBm	10:1	—	VSWR

NOTE(S):

(1) Per Table 2, unless otherwise specified.

(2) ACP is specified per IS95 as the ratio of the total in-band power (1.23 MHz BW) to adjacent power in a 30 kHz BW.

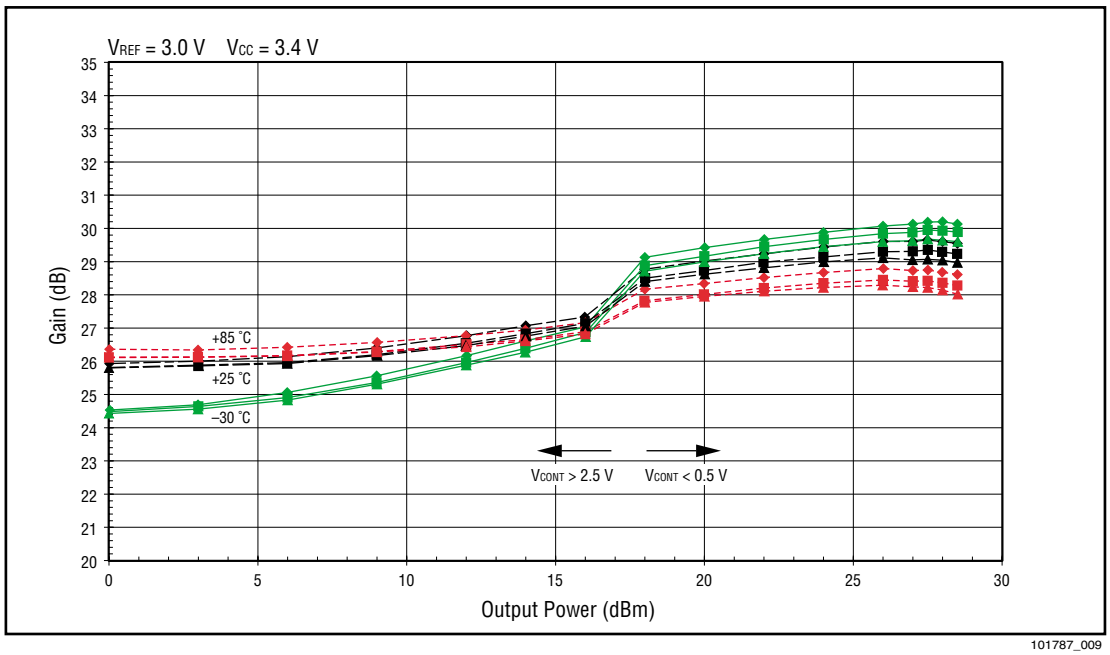
(3) CDMA2000 is configured as DCCH = 9600, SCHO = 9600, PCH (Walsh 0) = –3.75 dB, and Peak-to-Average Ratio (CCDF = 1%) = 4.5 dB. For CDMA2000, 0.5 dB back-off in output power is required.

(4) All phases, time = 10 seconds.

Characterization Data

The following graphs illustrate the characteristics of a typical CX77105 power amplifier designed for operation in the cellular frequency band (824–849 MHz). This amplifier was selected by characterizing a group of devices and then selecting a part with average electrical performance for both nominal and the full range of recommended operating conditions, including worst case limits. Figures 1 through 7 illustrate the digital signal characteristics of the CX77105. Shown are power sweep characteristics for key performance parameters, over temperature and frequency, up to 28.5 dBm output power. The data was taken up to and including 16 dBm output power with the bias mode control pin setting of V_{CONT} = 2.5 volts. Beyond 16 dBm output power, the V_{CONT} was set to 0 volts.

Figure 1. Digital Mode Gain vs. Output Power



101787_009

Legend

824 @ –30 °C	824 @ +25 °C	824 @ +85 °C
837 @ –30 °C	837 @ +25 °C	837 @ +85 °C
849 @ –30 °C	849 @ +25 °C	849 @ +85 °C

Figure 2. Primary Bias Current vs. Output Power

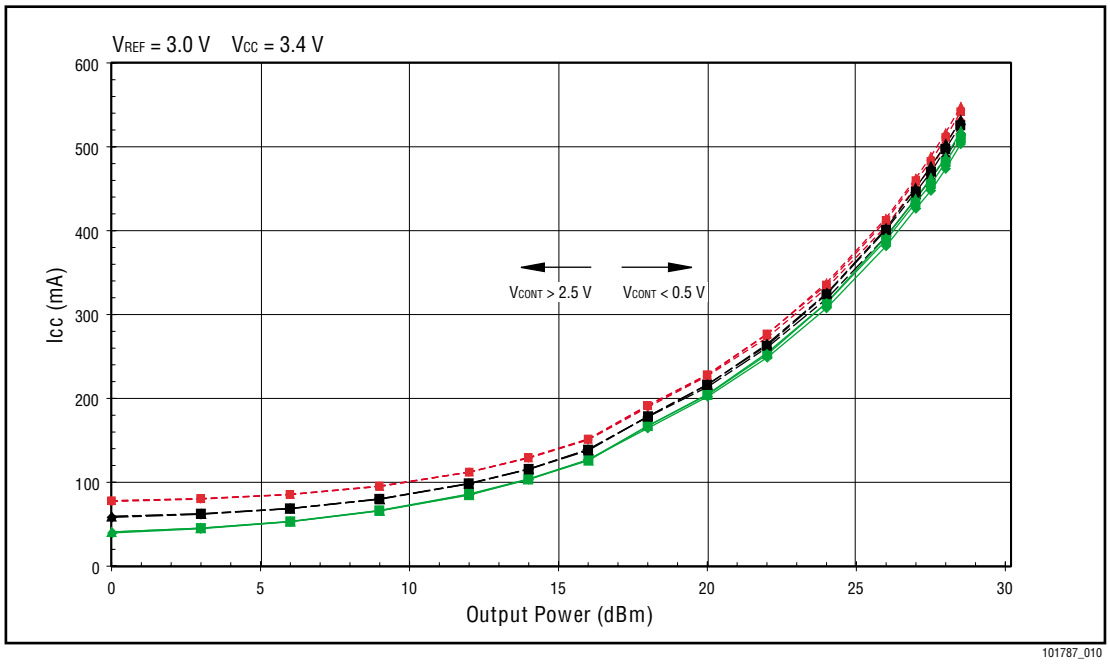
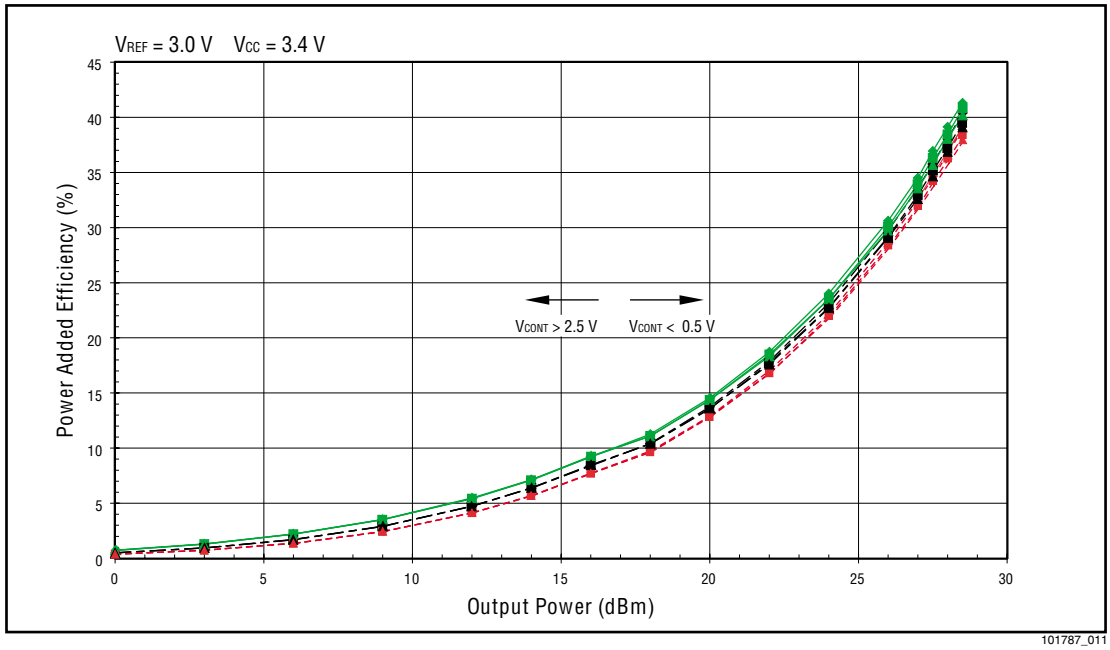


Figure 3. Power Added Efficiency vs. Output Power



Legend

824 @ –30 °C	824 @ +25 °C	824 @ +85 °C
837 @ –30 °C	837 @ +25 °C	837 @ +85 °C
849 @ –30 °C	849 @ +25 °C	849 @ +85 °C

Figure 4. Adjacent Channel Power for 885 kHz Offset Current vs. Output Power

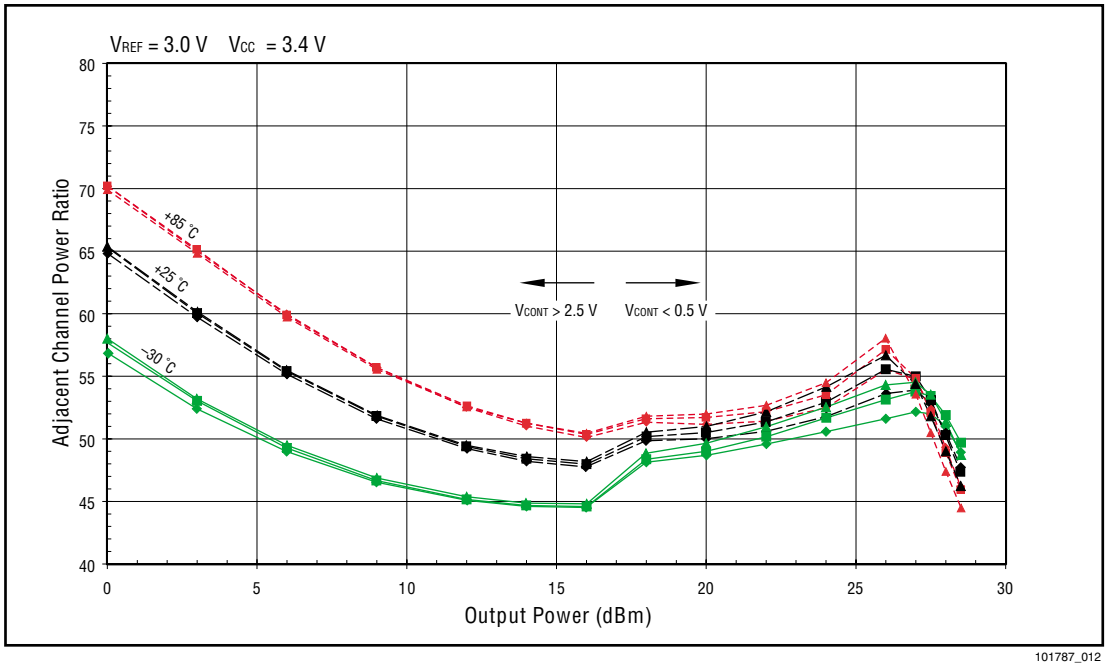
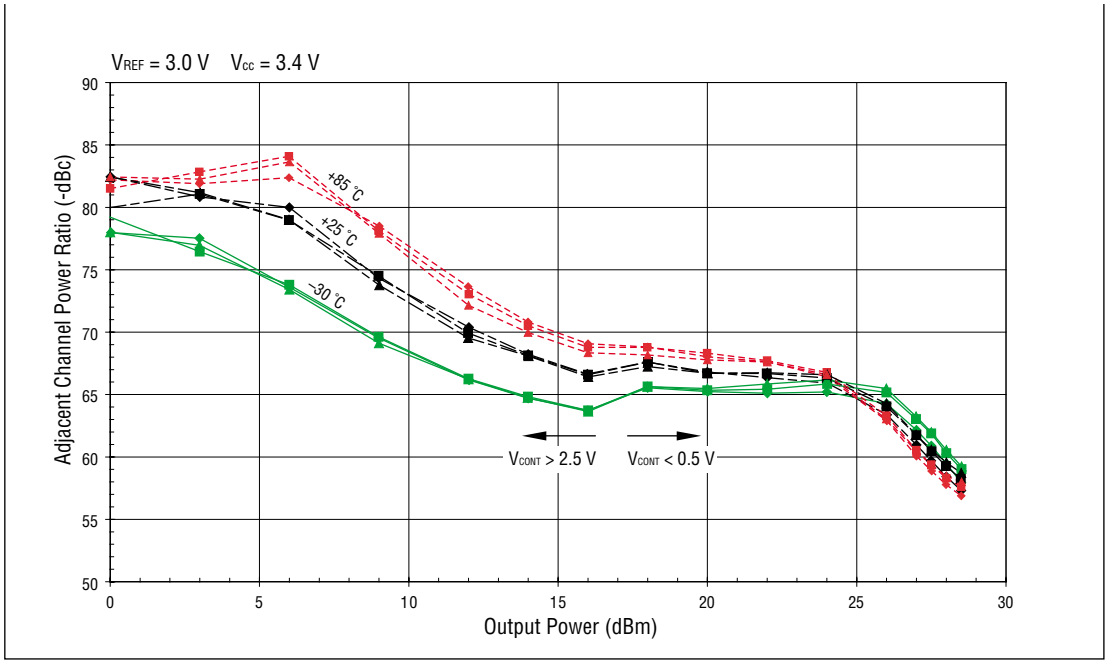


Figure 5. Adjacent Channel Power for 1.98 MHz Offset vs. Output Power



Legend

824 @ –30 °C	824 @ +25 °C	824 @ +85 °C
837 @ –30 °C	837 @ +25 °C	837 @ +85 °C
849 @ –30 °C	849 @ +25 °C	849 @ +85 °C

Figure 6. Second Harmonic Rejection vs. Output Power

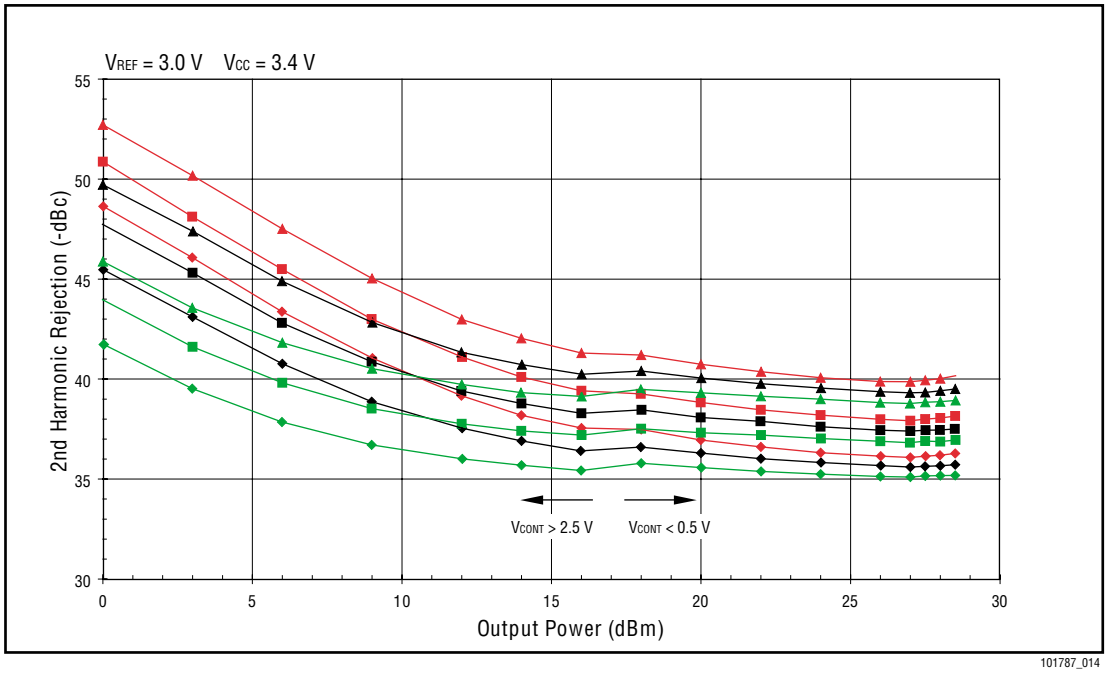
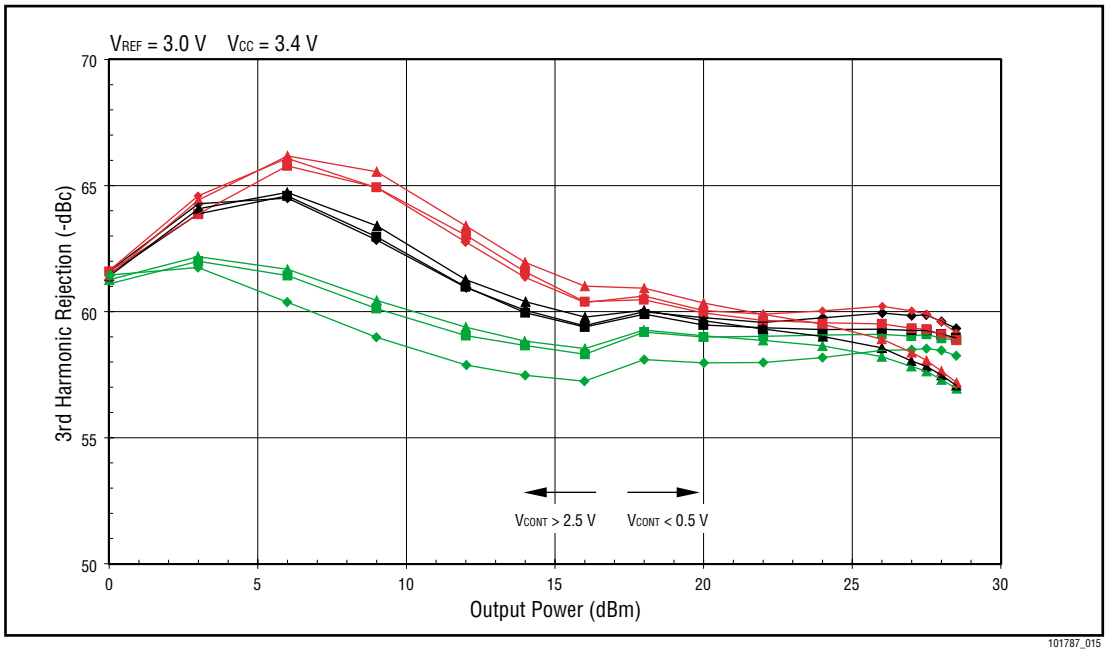


Figure 7. Third Harmonic Rejection vs. Output Power



Legend

824 @ –30 °C	824 @ +25 °C	824 @ +85 °C
837 @ –30 °C	837 @ +25 °C	837 @ +85 °C
849 @ –30 °C	849 @ +25 °C	849 @ +85 °C

Figure 8. Noise Figure as Function of Operating Conditions

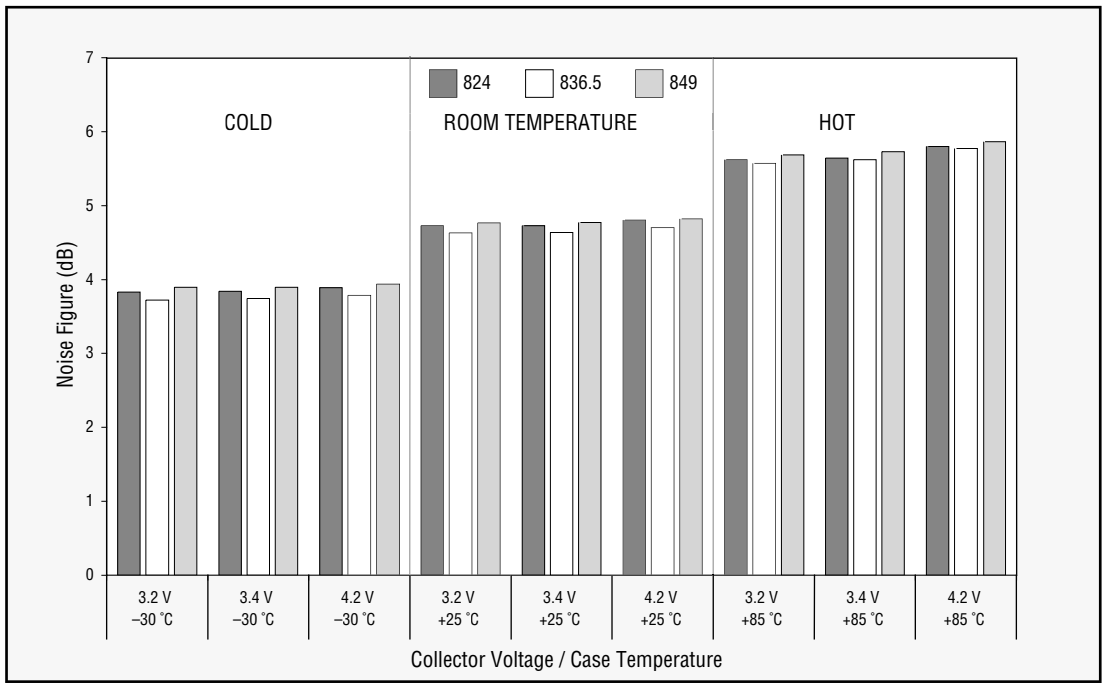
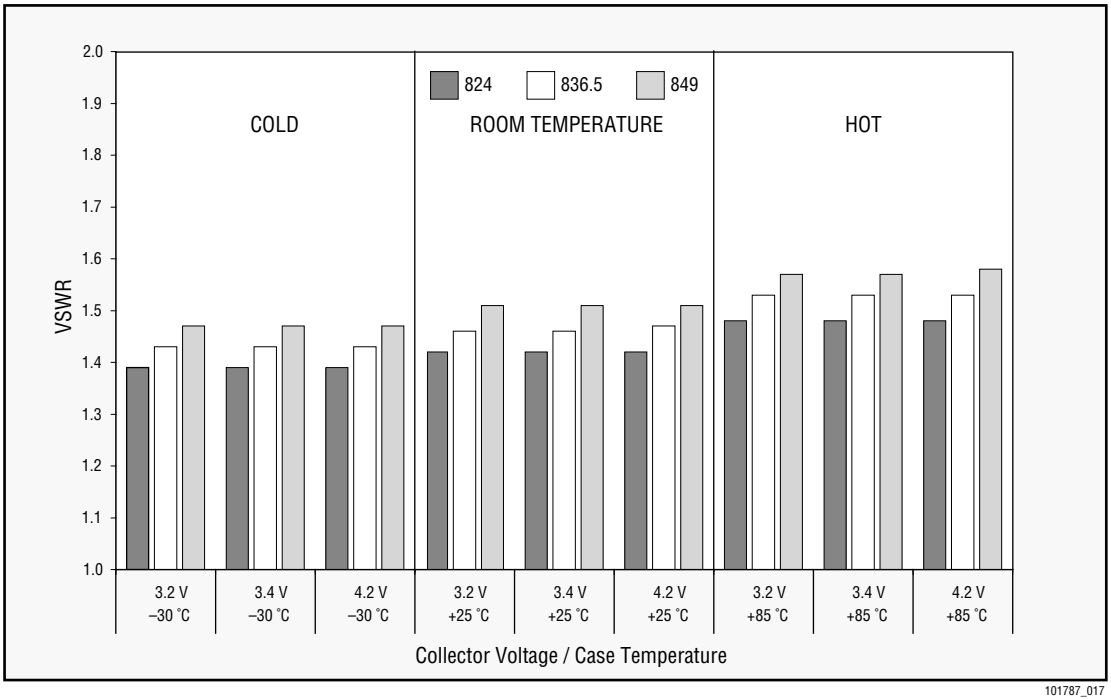


Figure 9. Input VSWR as Function of Operating Conditions



Evaluation Board Description

The evaluation board is a platform for testing and interfacing design circuitry. To accommodate the interface testing of the CX77105, the evaluation board schematic and diagrams are included for preliminary analysis and design. Figure 10 shows the basic schematic of the board for the 824 MHz to 849 MHz range.

Figure 10. Evaluation Board Schematic

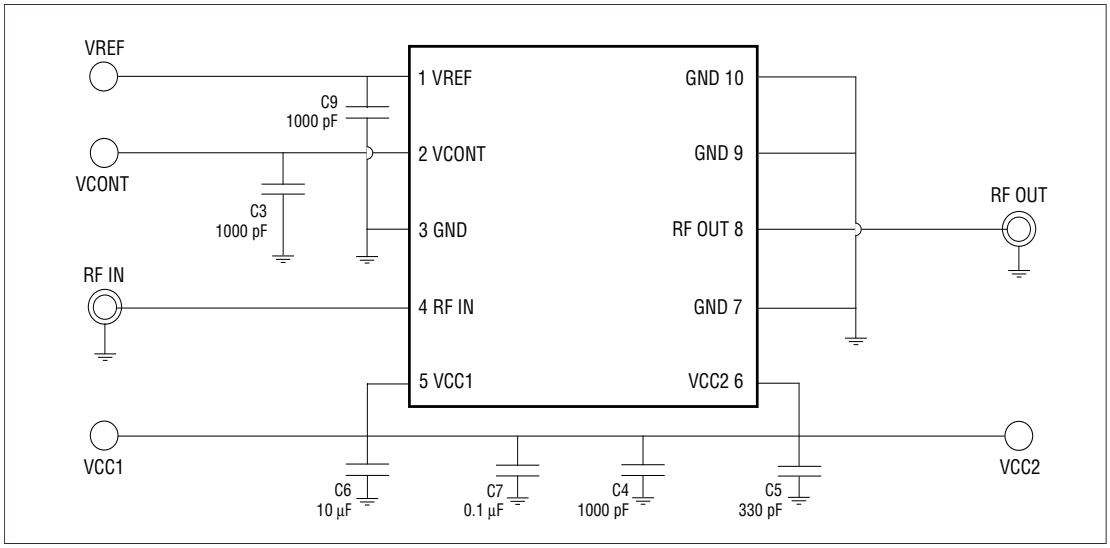
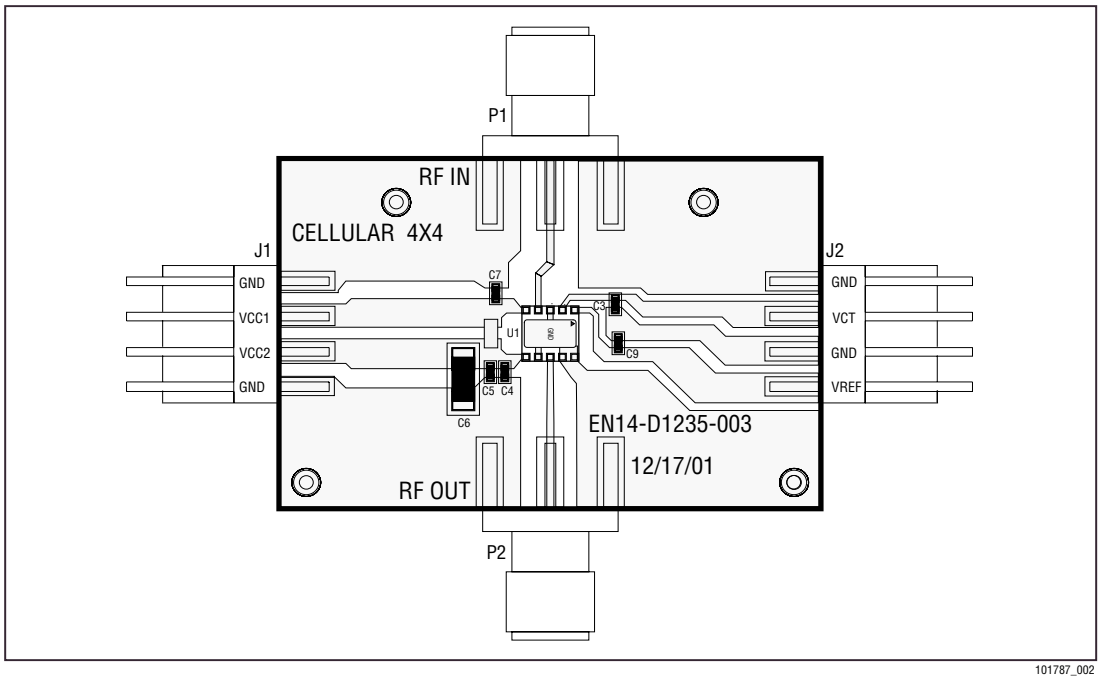


Figure 11. Evaluation Board Assembly Diagram



Package Dimensions and Pin Descriptions

The CX77105 is a multi-layer laminate base, overmold encapsulated modular package designed for surface mount solder attachment to a printed circuit board.

Figure 12 is a mechanical drawing of the pad layout for this package. The pin numbering convention starts with pin 1 in the upper left, as indicated in Figure 12, and increments counter-clockwise around the package. Table 6 describes each pin function and Figure 13 illustrates typical case markings.

Figure 12. CX77105 Package Dimensional Drawing

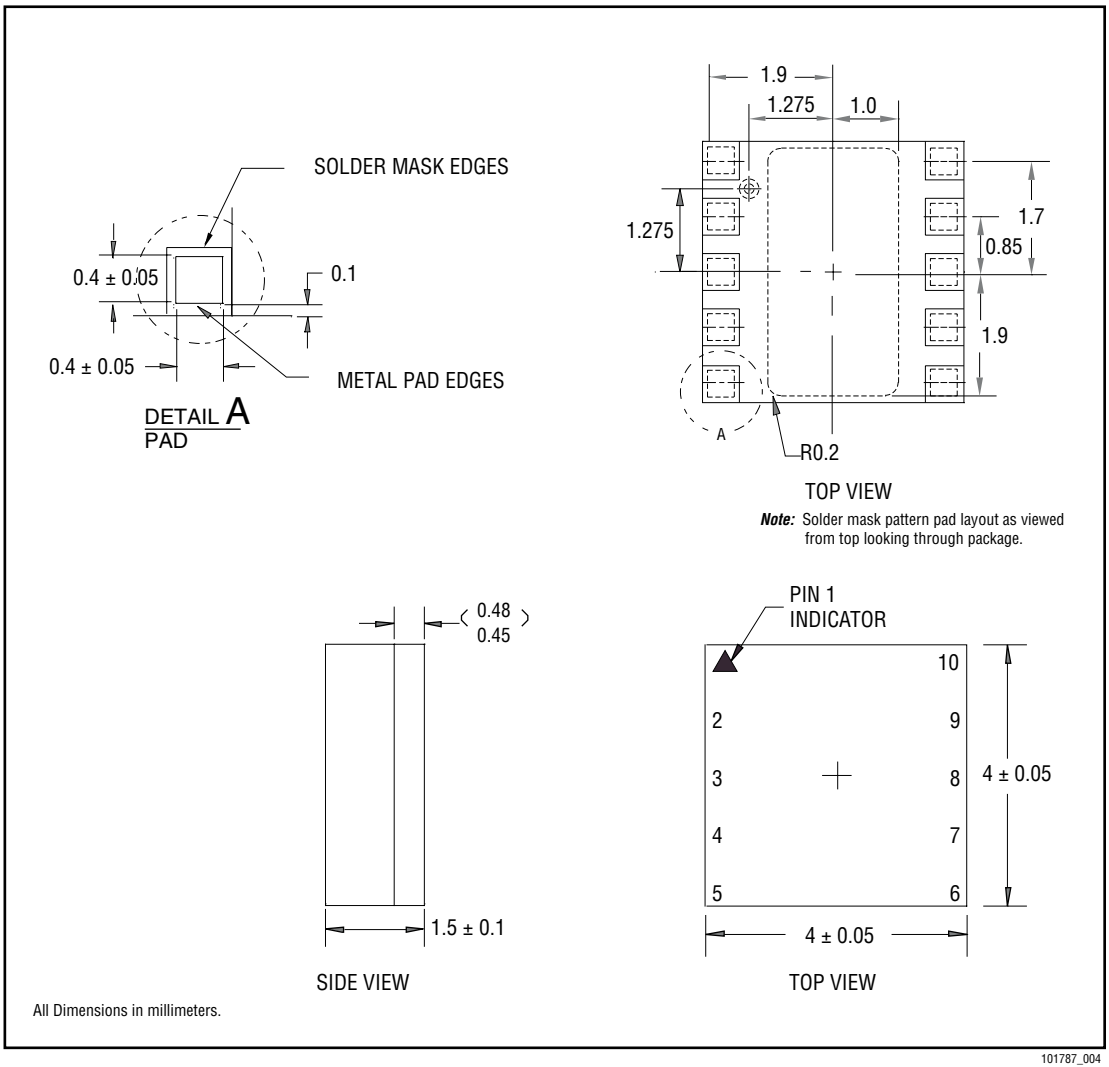
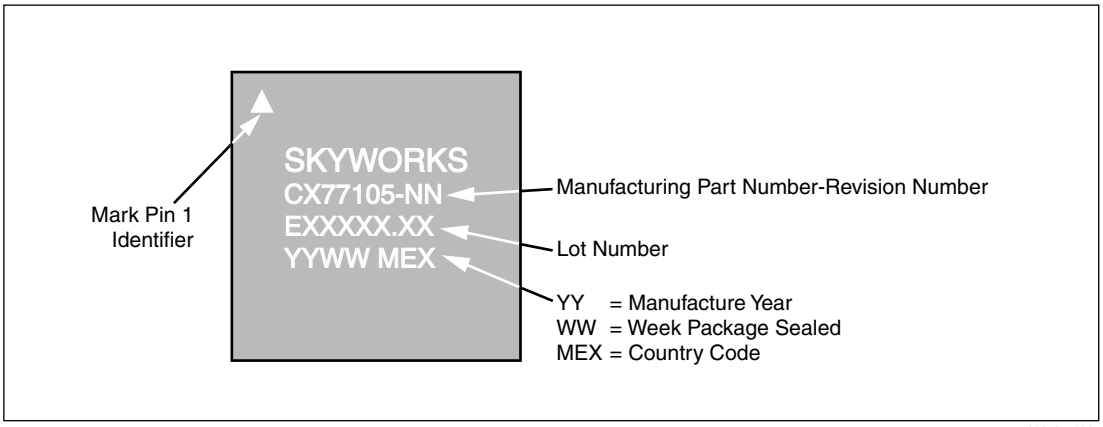


Table 6. Pin Descriptions

Pin #	Function	Pin #	Function	Pin #	Function
1	VREF	5	VCC1[1]	9	GND
2	VCONT	6	VCC2[1]	10	GND
3	GND	7	GND	GND PAD[2]	GND
4	RF IN	8	RF OUT		

NOTE(S):
(1) All supply pins may be connected together at the supply.
(2) GROUND PAD is package underside.

Figure 13. Typical Case Markings



Package and Handling Information

Because of its sensitivity to moisture absorption, this device package is baked and vacuum packed prior to shipment. Instructions on the shipping container label must be followed regarding exposure to moisture after the container seal is broken, otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

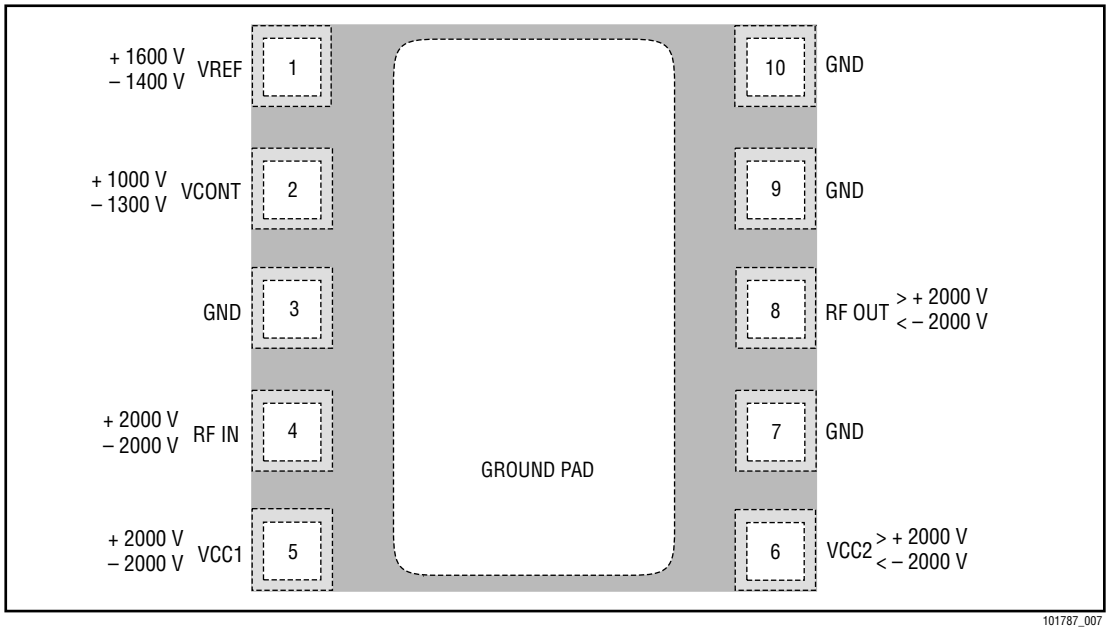
The CX77105 is capable of withstanding an MSL 3/240 °C solder reflow. Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. If the part is attached in a reflow oven, the temperature ramp rate should not exceed 5 °C per second; maximum temperature should not exceed 240 °C. If the part is manually attached, precaution should be taken to insure that the part is not subjected to temperatures exceeding 240 °C for more than 10 seconds. For details on both attachment techniques, precautions, and handling procedures recommended by Skyworks, please refer to *Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752*. Additional information on standard SMT reflow profiles can also be found in the *JEDEC Standard J–STD–020B*.

Production quantities of this product are shipped in the standard tape-and-reel format. For packaging details, refer to *Application Note: Tape and Reel, Document Number 101568.*

Electrostatic Discharge Sensitivity

The CX77105 is a Class I device. Figure 14 lists the Electrostatic Discharge (ESD) immunity level for each pin of the CX77105 product. The numbers in Figure 14 specify the ESD threshold level for each pin where the I-V curve between the pin and ground starts to show degradation. The ESD testing was performed in compliance with MIL-STD-883E Method 3015.7 using the Human Body Model. Since 2000 volts represents the maximum measurement limit of the test equipment used, pins marked > 2000 V pass 2000V ESD stress.

Figure 14. ESD Sensitivity Ares (Top View)



Various failure criteria can be utilized when performing ESD testing. Many vendors employ relaxed ESD failure standards which fail devices only after “the pin fails the electrical specification limits” or “the pin becomes completely non-functional”. Skyworks employs most stringent criteria, fails devices as soon as the pin begins to show any degradation on a curve tracer.

To avoid ESD damage, both latent and visible, it is very important that the product assembly and test areas follow the Class-1 ESD handling precautions listed in Table 7.

Table 7. Precautions for GaAs ICs with ESD Thresholds Greater Than 200 V But Less Than 2000 V

Personnel Grounding	**Facility**
Wrist Straps Conductive Smocks, Gloves and Finger Cots Antistatic ID Badges	Relative Humidity Control and Air Ionizers Dissipative Floors (less than 10^9 Ω to GND)
Protective Workstation	**Protective Packaging & Transportation**
Dissipative Table Tops Protective Test Equipment (Properly Grounded) Grounded Tip Soldering Irons Conductive Solder Suckers Static Sensors	Bags and Pouches (Faraday Shield) Protective Tote Boxes (Conductive Static Shielding) Protective Trays Grounded Carts Protective Work Order Holders

Ordering Information

Model Number	Manufacturing Part Number	Product Revision	Package	Operating Temperature
CX77105	CX77105-16P	16	4x4LM-10	–30 °C to +85 °C

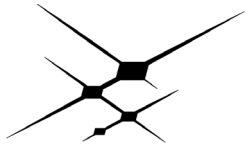
Revision History

Revision	Level	Date	Description
A		December 10, 2002	Initial Release

References

Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752.
Application Note: Tape and Reel, Document Number 101568
JEDEC Standard J–STD–020B.

General Information:
Skyworks Solutions, Inc.
4311 Jamboree Rd.
Newport Beach, CA. 92660-3007
www.skyworksinc.com



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