82541PI(ER) & 82562GZ(GX) Design Checklist v1.1

Project Name	
Fab Revision	
Date	
Designer	
Intel Contact	
Reviewer	

SECTION	CHECK ITEMS	REMARKS	√ DONE	COMMENTS
General	Have up-to-date product documentation and spec updates	Documents are subject to frequent change		
	Observe instructions for special pins needing pull-up or pull-down resistors	Do not connect pull-up or pull-down resistors to any pins marked No Connect.		
82562GZ(GX) LCI Device Option	Connect LCI signals to corresponding signals on ICH device.			
	Each of the four control pins TESTEN, ISOL_TCK, ISOL_TI, and ISOL_EXEC should be connected to a LAN disable circuit through 100 Ω resistors.	Contact Intel for latest LAN disable circuit recommendations. If the LOM disable function is not used, connect Ball A13 to ground through a 3.3 K resistor.		
	Verify LAN disable circuit.	Mode 0: see the related 82562ET(EM) and 82562GT(G) documentation. For Modes 1-4, see the related 82562GZ(GX) datasheet.		
	Use a 93C46 EEPROM for non-alerting applications or a 93C66 EEPROM for ASF 1.0. **Note:** DO NOT use a Catalyst 93C46 Revision H.	EEPROM for 82562GZ(GX) attaches to ICHx. Add decoupling capacitor. EEPROMs should be rated for at least 1 MHz.		
	Connect Ball B14 RBIAS10 to ground through a 619 Ω 1% resistor.	Recommended starting value. Measure PCB's output amplitude and adjust as required to meet IEEE specification. See the *82541PI(ER) and 82562GZ(GX) Dual Footprint LOM Design Guide* for more information.		
	Connect Ball B13 RBIAS100 to ground through a 649 Ω 1% resistor.	Recommended starting value. Measure PCB's output amplitude and adjust as required to meet IEEE specification. See the *82541PI(ER) and 82562GZ(GX) Dual Footprint LOM Design Guide* for more information.		

SECTION	CHECK ITEMS	REMARKS	√ DONE	COMMENTS
82541PI(ER) Controller Option	Connect 32-bit PCI interface pins to corresponding pins on system.			
	Connect Ball A9 LAN_PWR_GOOD to RSM_RST# or other voltage supervisor circuit.	Input should remain low until all power supplies are stable and for approximately 80ms. LAN_PWR_GOOD works like an auxiliary chip reset. It should be a clean, glitch-free signal. It is not intended for use as a LAN Disable. LAN_PWR_GOOD must be asserted during power down states to allow wakeup.		
	For the 82541PI, connect ball A6 PME# to system for wake up signaling.	Typical connection is PME# on ICHx.		
	Connect Ball J12 AUX_PWR signals correctly.	AUX_PWR is a logic input denoting that auxiliary power is connected to the device. AUX_PWR = 1 is a requirement for wakeup.		
	Connect Ball B9 RST# to RST# on system.			
	Bring out Ball B14's (IEEE_TEST+) and Ball D14's (IEEE_TEST-) traces as a differential pair and place a resistor pad between traces, but do not populate a resistor.	This is to facilitate IEEE testing.		
	Connect a 0.01 μF capacitor between Ball C2 M66EN and ground. M66EN should have a pull-up resistor somewhere in the system.	Capacitor per spec for signal integrity. This signal may be grounded anywhere on the segment for any PCI device incapable of 66 MHz operation.		
	Connect Ball G2 VIO to 5 V Standby or 3.3 V Standby to match PCI signaling voltage.	Use a 100 K resistor as a current limiter and a 0.1 μF bypass capacitor.		
	Ball H4 and G4 are connected to PLL_1.2 V.	Place appropriate stuffing options for each controller.		
	For the 82541ER, if a LAN disable function is required, drive Ball P9 FLSH_SO /LAN_ DISABLE#.	Use a Super I/O GP.		
	For the 82541ER, use a 93C46 EEPROM. **Note:** DO NOT use a Catalyst 93C46 Revision H.	For Microwire* EEPROMs, install a 100 pull-down resistor on Ball J4 EEMODE. Do not install a pull-down resistor on the EEDO pin. For SPI EEPROMs, use a 3.3 K pull-up resistor on write protect (WP#) and a 3.3 K pull-up resistor on HOLD#. Microwire EEPROMs should be rated for at least 1 MHz and SPI EEPROMs should be rated for at least 2 MHz.		

SECTION	CHECK ITEMS	REMARKS	√ DONE	COMMENTS
	For the 82541PI, use a 93C46 EEPROM for non-alerting applications, an AT25040 for ASF 1.0, or an AT25080 for ASF 2.0. **Note:** DO NOT use a Catalyst 93C46 Revision H	For Microwire* EEPROMs, install a 100 pull-down resistor on Ball J4 EEMODE. Do not install a pull-down resistor on the EEDO pin. For SPI EEPROMs, install a 1K pull-up resistor on ball J4 EEMODE, use a 3.3 K pull-up resistor on write protect (WP#) and a 3.3 K pull-up resistor on HOLD#. Microwire EEPROMs should be rated for at least 1 MHz and SPI EEPROMs should be rated for at least 2 MHz.		
	For the 82541PI, check reference schematic for connection of Software Defined Pins (SDPs).	Intel driver software may expect to use SDPs for special functions.		
	Connect Ball A13 TEST to ground, using a 1 K Ω resistor for dual layout designs with 82562GZ(GX).			
	For the 82541ER, connect Balls C9, A10, B10 to VCC.	1 K Ω pull-up resistors are reasonable values.		
	Provide a test point for IEEE PHY conformance testing. Depopulate the header for production.	This equates to a header between Balls B14 and D14 (differential clock output).		
Clock Source	Use 25 MHz 30 ppm accuracy @ 25° C clock source. Avoid components that introduce jitter.	Parallel resonant crystals are preferred.		
	Connect two 22 pF load caps to crystal.	Capacitance affects accuracy of the frequency. Must be matched to crystal specs, including estimated trace capacitance in calculation. Use low ESR caps.		
EEPROM and FLASH Memory	Use decoupling capacitor.	Applies to EEPROM or FLASH devices.		
	EEPROM ORG ties to 3.3 V for x16 access.	For Microwire EEPROMs. Depends on EEPROM used.		
	Consider whether to use FLASH memory.	Most LOM systems with boot ROM place the image in the system FLASH.		
	If FLASH memory is used, select the appropriate device.	The 82541PI(ER) uses serial FLASH.		

SECTION	CHECK ITEMS	REMARKS	√ DONE	COMMENTS
SMBus (82541PI)	If SMBus is not used, connect pull-up resistors to SMBCLK, SMBDATA, and SMB_ALERT#.	4.7 K Ω pull-ups are reasonable values.		
	If SMBus is used, system should have pull-up resistors.	SMBus signals are open-drain.		
	Connect Ball B10 SMB_ALERT# to the system LAN_PWR_GOOD signal or to Vcc through a 3.3 K W pull-up resistor.	Use 3.3 V, not 3.3 V AUX. Alternatively, ball B10 can be configured as an SMB_ALERT# output.		
Transmit and Receive Differential Pairs	82562GZ(GX) PLC devices use pairs of 54.9 Ω termination resistors.	Apply to both differential pairs.		
	82541(PI)ER controllers use pairs of 49.9 Ω termination resistors with 0.1 μF capacitors attached between center nodes and ground.	Apply to all four differential pairs.		
Magnetics Module (10/100/1000 Base-T Applications)	Integrated magnetics modules/RJ-45 connectors are available to minimize space requirements.	Modules with pin compatibility from 10/100 to Gigabit are available, containing internal jumpers for the unused pairs. Multivendor pin compatibility is possible. Contact manufacturers.		
	Qualify magnetics module carefully for Return Loss, Insertion Loss, Open Circuit Inductance, Common Mode Rejection, and Crosstalk Isolation	Magnetics module is critical to passing IEEE PHY conformance tests and EMI test.		
	82562GZ(GX) PLC devices use a 5-core model. The 82541(PI)ER controller uses a 12-core model.	Autotransformer models (10/100) provide better cable termination. All Gigabit models contain autotransformers.		
	For 82562GZ(GX) PLC devices that do not support MDI-X, use 0.1 μF capacitor on receive center tap.	Improves bit error rate.		
	For 82562GZ(GX) PLC devices that support MDI-X, do not use capacitor on receive center tap.	For severe EMI problems, a capacitor up to 22 pF can be used. Larger values will diminish signal strength and fail IEEE PHY conformance.		
	82562GZ(GX) PLC devices do not use capacitor on transmit center tap.	For severe EMI problems, a capacitor up to 22 pF can be used. Larger values will diminish signal strength and fail IEEE PHY conformance.		
	For 82541ER controller, supply 1.8 V to the transformer center taps and use 0.1 μF bypass capacitors.	These voltages bias the controller's output buffers. Magnetics with four center tap pins may have better characteristics than those with 1-2 center tap pins. Use capacitors with low Equivalent Series Resistance (ESR).		

SECTION	CHECK ITEMS	REMARKS	√ DONE	COMMENTS
Discrete Magnetics Module/RJ-45 Connector Option (10/100/1000 Base-T applications)	Bob Smith termination: use 4 x 75 Ω resistors for cable-side center taps and unused pins.	Terminates pair-to-pair common mode impedance of the CAT5 cable.		
	Bob Smith termination: use an EFT capacitor attached to the termination plane. Suggested values are 1500 pF/2KV or 1000 pF/3KV	For the 82541(PI)ER controller, maintain greater than 25 mil spacing from capacitor to traces and components.		
		For high-voltage isolation on 82562GZ(GX) designs, maintain greater than 70 mil spacing from capacitor to traces and components. Round all acute metal-fill angles to remove corners.		
	Connect signal pairs correctly to RJ-45 connector.	The differential pairs use pins 1-2 (Transmit in 10/100), 3-6 (Receive in 10/100), 4-5 (Gigabit only), and 7-8 (Gigabit only). Take care not to reverse the polarity.		
Power Supply and Signal Ground	For the 82541PI(ER) controller, connect external PNP transistors to the regulator control CTRL12 and CTRL18 outputs to supply 1.2 V and 1.8 V, respectively. The connections and transistor parameters are critical.	Alternatively, provide external regulators to generate these voltages. If the internal voltage regulator control circuit is not used, the CTRL pins may be left unconnected.		
	For the 82541PI, consider using two 0.5 Ω resistors in parallel to the emitter path of the 1.2 V power supply PNP transistor for regulator power dissipation.			
	For 82541PI(ER) controllers and 82562GZ(GX) PLC devices, provide a 3.3 V supply.	The 82562GZ(GX) is a single-voltage PLC device.		
	Design with power supplies that start up properly.	A good guideline is that all voltages should ramp to within their control bands in 20 ms. or less. It is desirable that voltages ramp in sequence and that the voltage rise be monotonic.		
	For the 82541ER, ensure that there is adequate capacitance on the PNPs.	Please check the reference schematic.		
	Use auxiliary power supplies.	Auxiliary power is necessary to support wake up from power down states.		

SECTION	CHECK ITEMS	REMARKS	√ DONE	COMMENTS
	Use decoupling and bulk capacitors generously.	Use approximately 12 bypass capacitors for the 82541ER controller. Add approximately 20-30 µF of bulk capacitance per voltage rail, typically using 10 µF capacitors. If power is distributed on traces, bulk capacitors should be used at both ends. If power is distributed on cards, bulk capacitors should be used at the connector.		
Chassis Ground (10/100/1000 Base-T applications)	If possible, provide a separate chassis ground to connect the shroud of the RJ-45 connector and to terminate the line side of the magnetics module.	This design improves EMI behavior.		
	Place pads for approximately four "stitching" capacitors to bridge the gap from chassis ground to signal ground.	Typical values range from 0.1 µF to 4.7 µF. Determine experimentally.		
Termination Plane	For designs with non-integrated magnetics modules, lay out Bob Smith termination plane. Term plane floats over chassis ground.	Splits in ground plane should be at least 50 mils to prevent arcing during hi-pot tests.		
LED Circuits	Basic recommendation is a single green LED for Activity and a dual (bi-color) LED for Speed. Many other configurations are possible.	A two-LED configuration is compatible with integrated magnetics modules. For the Link/Activity LED, connect the anode to the ACTIVITY#/ACTLED# pin (Ball C11) and the cathode to the LINK_LED/LINK_UP#/LILED# pin (Ball A12). For the bi-color speed LED pair, have the Link 100#/SPDLED# signal drive one end. The other end should be connected to 3.3 V for the 82562GZ(GX) PLC device or to LINK1000# for the 82541ER device (use 0 Ω resistors for dual footprint designs.)		
	Connect LEDs to 3.3 V as indicated in reference schematics.	Use 3.3 V AUX for designs supporting wakeup. Consider adding 1-2 filtering capacitors per LED for extremely noisy situations. Suggested starting value 470 pF.		
	Add current limiting resistors to LED paths.	Typical current limiting resistors are 250 to 330 Ω (300 to 330 Ω for the 82541PI) when using a 3.3 V supply. Current limiting resistors are typically included with integrated magnetics modules.		

SECTION	CHECK ITEMS	REMARKS	√ DONE	COMMENTS
Mfg Test	82541PI(ER) controller uses a JTAG Test Access Port.	Place 100 Ω pull-down resistors on Ball L13 JTAG_TRST# and Ball L14 JTAG_TCK. These connections hold the TAP controller in an inactive state. For 82562GZ(GX) PLC devices, depopulate the pull-down resistors.		