32-Tap Digitally Programmable Potentiometer (DPP™) with Buffered Wiper

FEATURES

- 32-position linear taper potentiometer
- Non-volatile EEPROM wiper storage; buffered wiper
- Low power CMOS technology
- Single supply operation: 2.5V - 6.0V
- Increment up/down serial interface
- Resistance values: 10kΩ, 50kΩ and 100kΩ
- Available in PDIP, SOIC, TSSOP and MSOP packages

APPLICATIONS

- Automated product calibration
- Remote control adjustments
- Offset, gain and zero control
- Tamper-proof calibrations
- Contrast, brightness and volume controls
- Motor controls and feedback systems
- Programmable analog functions

For Ordering Information details, see page 10.

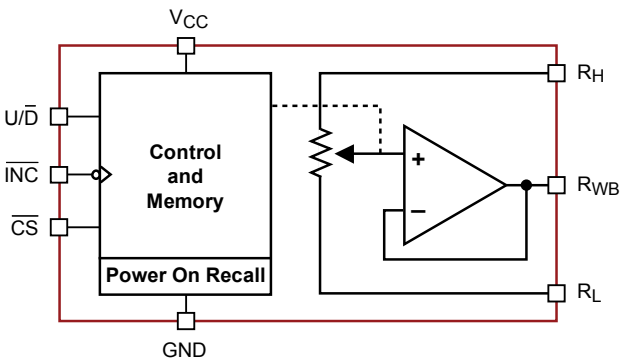
DESCRIPTION

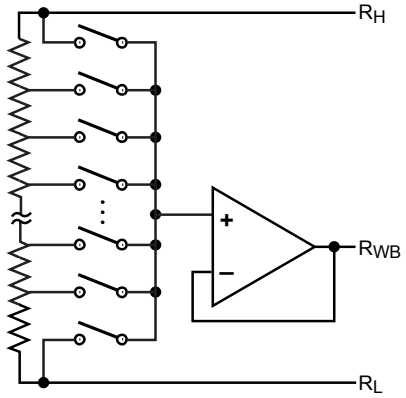
The CAT5112 is a single digitally programmable potentiometer (DPP™) designed as a electronic replacement for mechanical potentiometers. Ideal for automated adjustments on high volume production lines, they are also well suited for applications where equipment requiring periodic adjustment is either difficult to access or located in a hazardous or remote environment.

The CAT5112 contains a 32-tap series resistor array connected between two terminals R_H and R_L. An up/down counter and decoder that are controlled by three input pins, determines which tap is connected to the wiper, R_{WB}. The CAT5112 wiper is buffered by an op amp that operates rail to rail. The wiper setting, stored in non-volatile memory, is not lost when the device is powered down and is automatically recalled when power is returned. The wiper can be adjusted to test new system values without effecting the stored setting. Wiper-control of the CAT5112 is accomplished with three input control pins, $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$. The $\overline{INC}$ input increments the wiper in the direction which is determined by the logic state of the U/$\overline{D}$ input. The $\overline{CS}$ input is used to select the device and also store the wiper position prior to power down.

The digitally programmable potentiometer can be used as a buffered voltage divider. For applications where the potentiometer is used as a 2-terminal variable resistor, please refer to the CAT5114. The buffered wiper of the CAT5112 is not compatible with that application.

FUNCTIONAL DIAGRAM

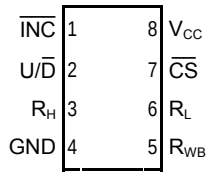




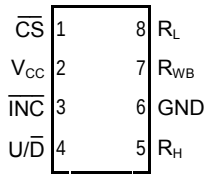
Electronic Potentiometer Implementation

PIN CONFIGURATION

PDIP 8-Lead (L)
SOIC 8 Lead (V)
MSOP 8 Lead (Z)



TSSOP 8 Lead (Y)



PIN DESCRIPTIONS

Name	Function
$\overline{INC}$	Increment Control
U/$\overline{D}$	Up/Down Control
R_H	Potentiometer High Terminal
GND	Ground
R_{WB}	Buffered Wiper Terminal
R_L	Potentiometer Low Terminal
$\overline{CS}$	Chip Select
V_{CC}	Supply Voltage

PIN DESCRIPTION

$\overline{INC}$: Increment Control Input

The $\overline{INC}$ input (on the falling edge) moves the wiper in the up or down direction determined by the condition of the U/$\overline{D}$ input.

U/$\overline{D}$: Up/Down Control Input

The U/$\overline{D}$ input controls the direction of the wiper movement. When in a high state and $\overline{CS}$ is low, any high-to-low transition on $\overline{INC}$ will cause the wiper to move one increment toward the R_H terminal. When in a low state and $\overline{CS}$ is low, any high-to-low transition on $\overline{INC}$ will cause the wiper to move one increment towards the R_L terminal.

R_H: High End Potentiometer Terminal

R_H is the high end terminal of the potentiometer. It is not required that this terminal be connected to a potential greater than the R_L terminal. Voltage applied to the R_H terminal cannot exceed the supply voltage, V_{CC} or go below ground, GND.

R_{WB}: Wiper Potentiometer Terminal (Buffered)

R_{WB} is the buffered wiper terminal of the potentio–meter. Its position on the resistor array is controlled by the control inputs, $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$.

R_L: Low End Potentiometer Terminal

R_L is the low end terminal of the potentiometer. It is not required that this terminal be connected to a potential less than the R_H terminal. Voltage applied to the R_L terminal cannot exceed the supply voltage, V_{CC} or go below ground, GND. R_L and R_H are electrically interchangeable.

$\overline{CS}$: Chip Select

The chip select input is used to activate the control input of the CAT5112 and is active low. When in a high state, activity on the $\overline{INC}$ and U/$\overline{D}$ inputs will not affect or change the position of the wiper.

DEVICE OPERATION

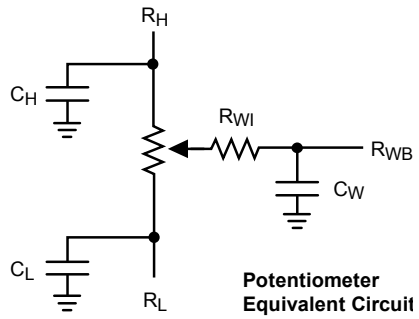
The CAT5112 operates like a digitally controlled potentiometer with R_H and R_L equivalent to the high and low terminals and R_{WB} equivalent to the mecha–nical potentiometer's wiper. There are 32 available tap positions including the resistor end points, R_H and R_L. There are 31 resistor elements connected in series between the R_H and R_L terminals. The wiper terminal is connected to one of the 32 taps and controlled by three inputs, $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$. These inputs control a five-bit up/down counter whose output is decoded to select the wiper position. The selected wiper position can be stored in nonvolatile memory using the INC and $\overline{CS}$ inputs.

With $\overline{CS}$ set LOW the CAT5112 is selected and will respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ wil increment or decrement the wiper (depending on the state of the U/$\overline{D}$ input and five-bit counter). The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. The value of the counter is stored in nonvolatile memory whenever $\overline{CS}$ transitions HIGH while the $\overline{INC}$ input is also HIGH. When the CAT5112 is powered-down, the last stored wiper counter position is maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the counter is set to the value stored.

With $\overline{INC}$ set low, the CAT5112 may be deselected and powered down without storing the current wiper position in nonvolatile memory. This allows the system to always power up to a preset value stored in non-volatile memory.

OPERATION MODES

$\overline{INC}$	$\overline{CS}$	U/$\overline{D}$	Operation
High to Low	Low	High	Wiper toward R_H
High to Low	Low	Low	Wiper toward R_L
High	Low to High	X	Store Wiper Position
Low	Low to High	X	No Store, Return to Standby
X	High	X	Standby



Potentiometer Equivalent Circuit

ABSOLUTE MAXIMUM RATINGS[1]

Parameters	Ratings	Units
Supply Voltage V_{CC} to GND	-0.5 to +7V	V
Inputs $\overline{CS}$ to GND	-0.5 to V_{CC} +0.5	V
$\overline{INC}$ to GND	-0.5 to V_{CC} +0.5	V
U/$\overline{D}$ to GND	-0.5 to V_{CC} +0.5	V
R_H to GND	-0.5 to V_{CC} +0.5	V
R_L to GND	-0.5 to V_{CC} +0.5	V
R_{WB} to GND	-0.5 to V_{CC} +0.5	V

Parameters	Ratings	Units
Operating Ambient Temperature Commercial ('C' or Blank suffix)	0 to 70	ºC
Industrial ('I' suffix)	-40 to +85	ºC
Junction Temperature	+150	ºC
Storage Temperature	-65 to 150	ºC
Lead Soldering (10s max)	+300	ºC

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Test Method	Min	Typ	Max	Units
V_{ZAP}[2]	ESD Susceptibility	MIL-STD-883, Test Method 3015	2000			V
I_{LTH}[2] [3]	Latch-Up	JEDEC Standard 17	100			mA
T_{DR}	Data Retention	MIL-STD-883, Test Method 1008	100			Years
N_{END}	Endurance	MIL-STD-883, Test Method 1003	1,000,000			Stores

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +2.5V to +6V unless otherwise specified

Power Supply

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Operating Voltage Range		2.5	–	6	V
I_{CC1}	Supply Current (Increment)	V_{CC} = 6V, f = 1MHz, I_W = 0	–	–	200	µA
		V_{CC} = 6V, f = 250kHz, I_W = 0	–	–	100	µA
I_{CC2}	Supply Current (Write)	Programming, V_{CC} = 6V	–	–	1000	µA
		V_{CC} = 3V	–	–	500	µA
I_{SB1}[3]	Supply Current (Standby)	$\overline{CS}$ = V_{CC} - 0.3V U/$\overline{D}$, $\overline{INC}$ = V_{CC} - 0.3V or GND	–	75	150	µA

Notes:

(1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

(2) This parameter is tested initially and after a design or process change that affects the parameter.

(3) Latch-up protection is provided for stresses up to 100mA on address and data pins from -1V to V_{CC} + 1V

(4) I_W = source or sink

(5) These parameters are periodically sampled and are not 100% tested.

Logic Inputs

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IH}	Input Leakage Current	$V_{IN} = V_{CC}$	–	–	10	µA
I_{IL}	Input Leakage Current	$V_{IN} = 0V$	–	–	-10	µA
V_{IH1}	TTL High Level Input Voltage	$4.5V \le V_{CC} \le 5.5V$	2	–	V_{CC}	V
V_{IL1}	TTL Low Level Input Voltage		0	–	0.8	V
V_{IH2}	CMOS High Level Input Voltage	$2.5V \le V_{CC} \le 6V$	V_{CC} x 0.7	–	V_{CC} + 0.3	V
V_{IL2}	CMOS Low Level Input Voltage		-0.3	–	V_{CC} x 0.2	V

Potentiometer Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{POT}	Potentiometer Resistance	-10 Device		10		kΩ
		-50 Device		50		
		-00 Device		100		
	Pot. Resistance Tolerance				±20	%
V_{RH}	Voltage on R_H pin		0		V_{CC}	V
V_{RL}	Voltage on R_L pin		0		V_{CC}	V
	Resolution			1		%
INL	Integral Linearity Error	$I_W \le 2µA$		0.5	1	LSB
DNL	Differential Linearity Error	$I_W \le 2µA$		0.25	0.5	LSB
R_{OUT}	Buffer Output Resistance	$0.05V_{CC} \le V_{WB} \le 0.95V_{CC}$, $V_{CC} = 5V$			1	Ω
I_{OUT}	Buffer Output Current	$0.05V_{CC} \le V_{WB} \le 0.95V_{CC}$, $V_{CC} = 5V$			3	mA
TC_{RPOT}	TC of Pot Resistance			300		ppm/ºC
TC_{RATIO}	Ratiometric TC			20		ppm/ºC
$C_{RH}/C_{RL}/C_{RW}$	Potentiometer Capacitances			8/8/25		pF
fc	Frequency Response	Passive Attenuator, 10kΩ		1.7		MHz
$V_{WB(SWING)}$	Output Voltage Range	$I_{OUT} \le 100µA$, $V_{CC} = 5V$	$0.01V_{CC}$		$0.99V_{CC}$	

AC CONDITIONS OF TEST

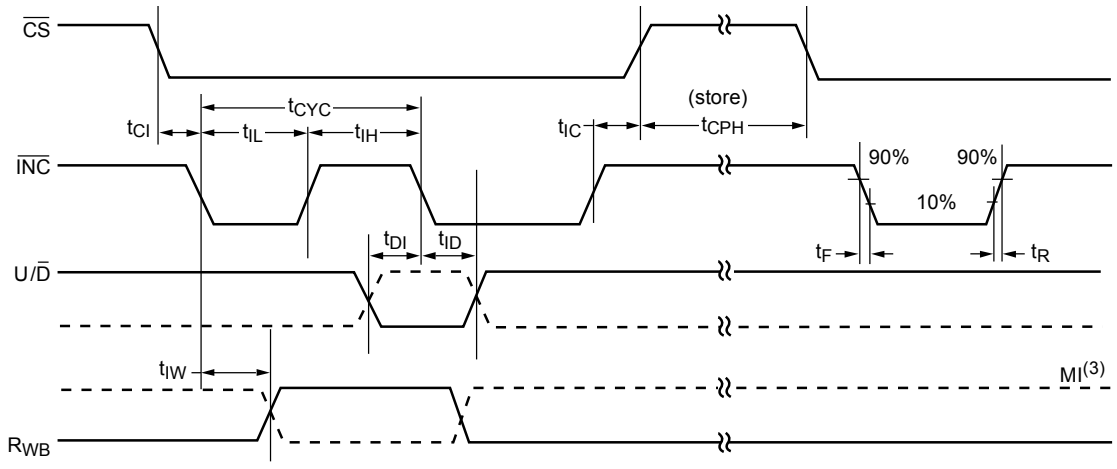
V_{CC} Range	$2.5V \le V_{CC} \le 6V$
Input Pulse Levels	$0.2V_{CC}$ to $0.7V_{CC}$
Input Rise and Fall Times	10ns
Input Reference Levels	$0.5V_{CC}$

AC OPERATING CHARACTERISTICS

V_{CC} = +2.5V to +6.0V, $V_H = V_{CC}$, V_L = 0V, unless otherwise specified

Symbol	Parameter	Min	Typ(1)	Max	Units
t_{CI}	$\overline{CS}$ to $\overline{INC}$ Setup	100	–	–	ns
t_{DI}	U/$\overline{D}$ to $\overline{INC}$ Setup	50	–	–	ns
t_{ID}	U/$\overline{D}$ to $\overline{INC}$ Hold	100	–	–	ns
t_{IL}	$\overline{INC}$ LOW Period	250	–	–	ns
t_{IH}	$\overline{INC}$ HIGH Period	250	–	–	ns
t_{IC}	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	1	–	–	µs
t_{CPH}	$\overline{CS}$ Deselect Time (NO STORE)	100	–	–	ns
t_{CPH}	$\overline{CS}$ Deselect Time (STORE)	10	–	–	ms
t_{IW}	$\overline{INC}$ to V_{OUT} Change	–	1	5	µs
t_{CYC}	$\overline{INC}$ Cycle Time	1	–	–	µs
t_R, t_F(2)	$\overline{INC}$ Input Rise and Fall Time	–	–	500	µs
t_{PU}(2)	Power-up to Wiper Stable	–	–	1	ms
t_{WR}	Store Cycle	–	5	10	ms

A.C. TIMING

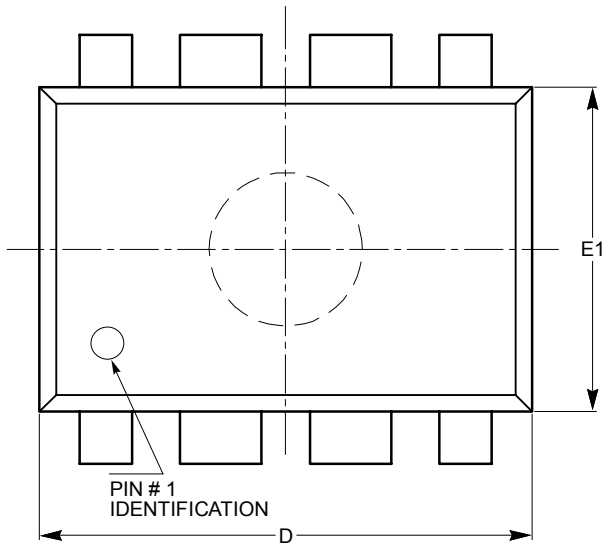


Notes:

(1) Typical values are for T_A = 25ºC and nominal supply voltage.
(2) This parameter is periodically sampled and not 100% tested.
(3) MI in the A.C. Timing diagram refers to the minimum incremental change in the W output due to a change in the wiper position.

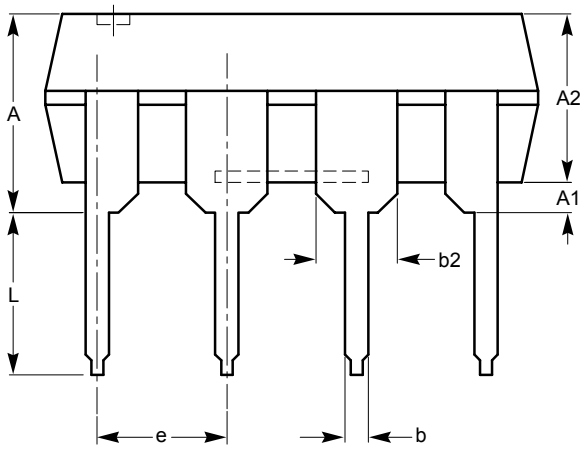
PACKAGE OUTLINE DRAWINGS

PDIP 8-Lead 300mil (L) (1)(2)

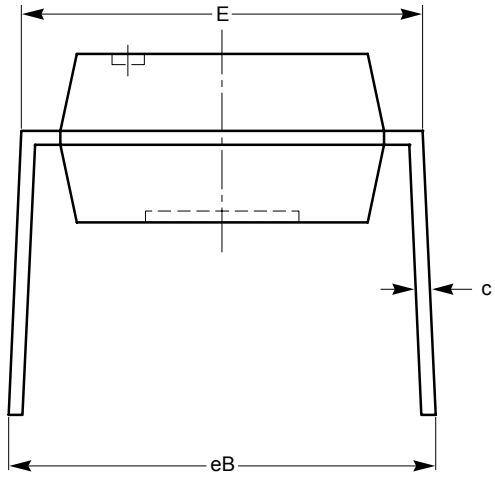


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.25
e		2.54 BSC	
E1	6.10	6.35	7.11
eB	7.87		10.92
L	2.92	3.30	3.80



SIDE VIEW

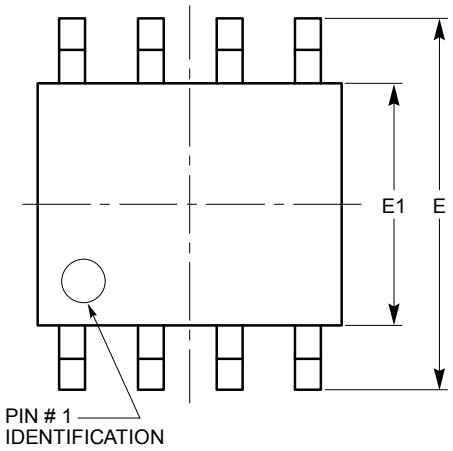


END VIEW

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

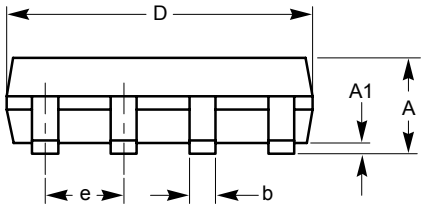
Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC Specification MS-001.

SOIC 8-LEAD Narrow Body (150mil) (V) [1][2]

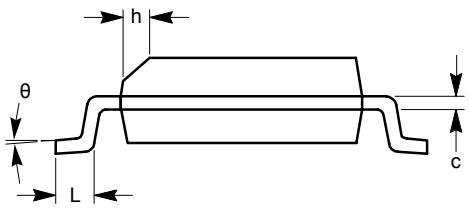


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW

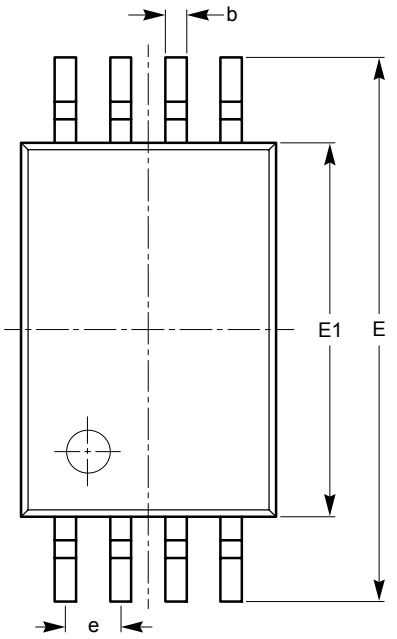


END VIEW

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

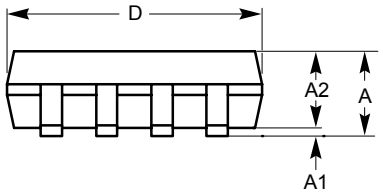
Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC Specification MS-012.

TSSOP 8-Lead (Y) (1)(2)

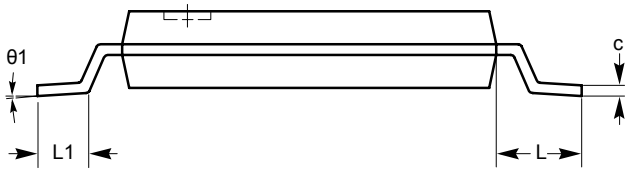


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e		0.65 BSC	
L		1.00 REF	
L1	0.50	0.60	0.75
θ1	0°		8°



SIDE VIEW

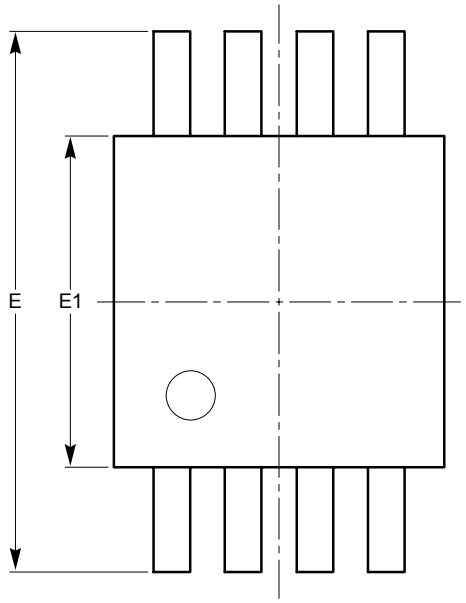


END VIEW

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

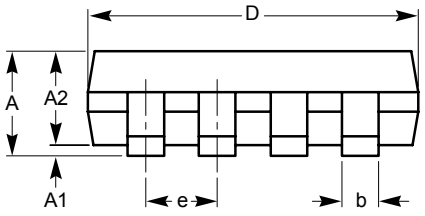
Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC Standard MO-153

MSOP 8-Lead (Z) (1)(2)

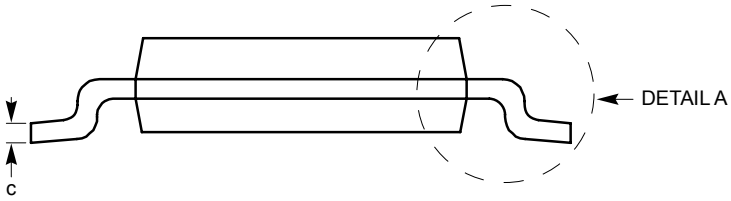


TOP VIEW

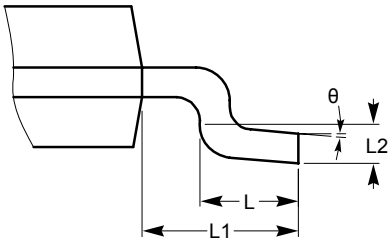
SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05	0.10	0.15
A2	0.75	0.85	0.95
b	0.22		0.38
c	0.13		0.23
D	2.90	3.00	3.10
E	4.80	4.90	5.00
E1	2.90	3.00	3.10
e		0.65 BSC	
L	0.40	0.60	0.80
L1		0.95 REF	
L2		0.25 BSC	
θ	0º		6º



SIDE VIEW



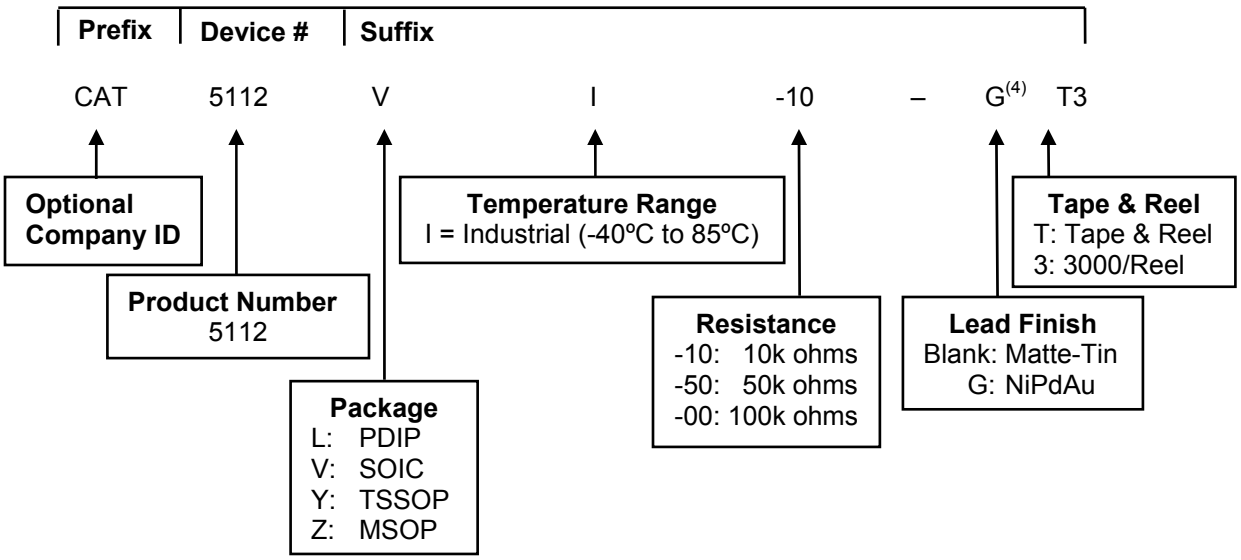
END VIEW



DETAIL A

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC Specification MS-187.

EXAMPLE OF ORDERING INFORMATION



ORDERING PART NUMBER
CAT5112LI-10-G
CAT5112LI-50-G
CAT5112LI-00-G
CAT5112VI-10-G
CAT5112VI-50-G
CAT5112VI-00-G
CAT5112YI-10-G
CAT5112YI-50-G
CAT5112YI-00-G
CAT5112ZI-10-G
CAT5112ZI-50-G
CAT5112ZI-00-G

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:
(1) All packages are RoHS-compliant (Lead-free, Halogen-free).
(2) The standard lead finish is NiPdAu.
(3) This device used in the above example is a CAT5112VI-10-GT3 (SOIC, Industrial Temperature, 10kΩ, NiPdAu, Tape & Reel).
(4) For Matte-Tin finish, contact factory.

REVISION HISTORY

Date	Rev.	Description
10-Mar-07	J	Updated Potentiometer Parameters
29-Mar-04	K	Change Green Package marking for SOIC from W to V
12-Apr-04	L	Update Reel Ordering Information
04-Jun-07	M	Add Package Outline Drawings Update Example of Ordering Information Add MD- to the Document Number
20-Nov-08	N	Update Package Outline Drawings Change logo and fine print to ON Semiconductor

PUBLICATION ORDERING INFORMATION
LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center:
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative