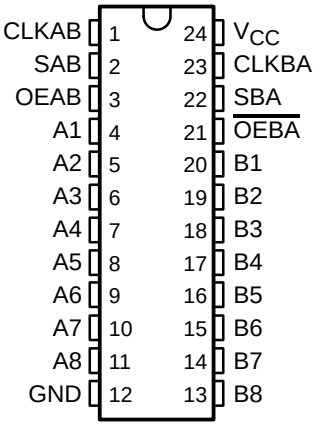
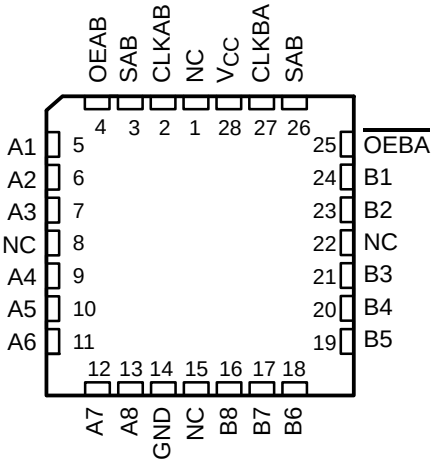
- **Operating Voltage Range of 4.5 V to 5.5 V**
- **Low Power Consumption, 80-μA Max $I_{CC}$**
- **Typical $t_{pd}$ = 12 ns**
- **±6-mA Output Drive at 5 V**
- **Low Input Current of 1 μA Max**
- **Inputs Are TTL-Voltage Compatible**
- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **True Data Paths**
- **High-Current 3-State Outputs Can Drive Up To 15 LSTTL Loads**

**SN54HCT652 . . . JT OR W PACKAGE**
**SN74HCT652 . . . DW OR NT PACKAGE**
**(TOP VIEW)**




**SN54HCT652 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description/ordering information

The ’HCT652 devices consist of bus-transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select real-time or stored data transfer. A low input level selects real-time data; a high input level selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with these devices.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | PDIP – NT | Tube | SN74HCT652NT | SN74HCT652NT |
| | SOIC – DW | Tube | SN74HCT652DW | HCT652 |
| | | Tape and reel | SN74HCT652DWR | |
| –55°C to 125°C | CDIP – JT | Tube | SNJ54HCT652JT | SNJ54HCT652JT |
| | CFP – W | Tube | SNJ54HCT652W | SNJ54HCT652W |
| | LCCC – FK | Tube | SNJ54HCT652FK | SNJ54HCT652FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## description/ordering information (continued)

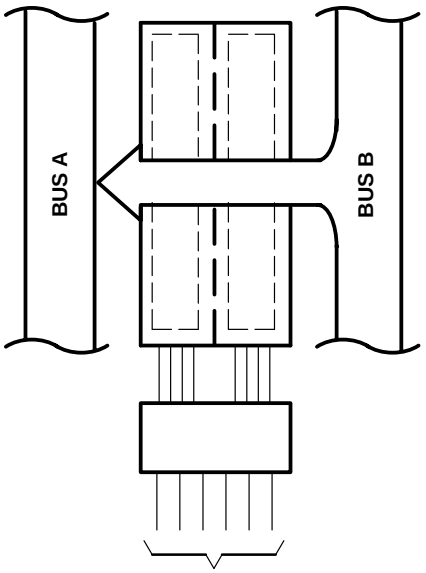
Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) terminals, regardless of the select- or output-control terminals. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input. When all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OEBA}}$ should be tied to $V_{CC}$ through a pullup resistor and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

**FUNCTION TABLE**

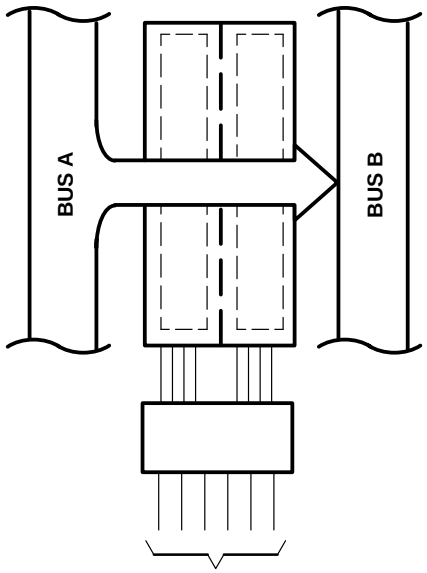
| INPUTS | | | | | | DATA I/O† | | OPERATION OR FUNCTION |
|---|---|---|---|---|---|---|---|---|
| OEAB | $\overline{\text{OEBA}}$ | CLKAB | CLKBA | SAB | SBA | A1–A8 | B1–B8 | |
| L | H | H or L | H or L | X | X | Input | Input | Isolation |
| L | H | ↑ | ↑ | X | X | Input | Input | Store A and B data |
| X | H | ↑ | H or L | X | X | Input | Unspecified‡ | Store A, hold B |
| H | H | ↑ | ↑ | X‡ | X | Input | Output | Store A in both registers |
| L | X | H or L | ↑ | X | X | Unspecified‡ | Input | Hold A, store B |
| L | L | ↑ | ↑ | X | X‡ | Output | Input | Store B in both registers |
| L | L | X | X | X | L | Output | Input | Real-time B data to A bus |
| L | L | X | H or L | X | H | Output | Input | Stored B data to A bus |
| H | H | X | X | L | X | Input | Output | Real-time A data to B bus |
| H | H | H or L | X | H | X | Input | Output | Stored A data to B bus |
| H | L | H or L | H or L | H | H | Output | Output | Stored A data to B bus and stored B data to A bus |

† The data-output functions can be enabled or disabled by a variety of level combinations at OEAB or $\overline{\text{OEBA}}$. Data-input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition on the clock inputs.
‡ Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered to load both registers.



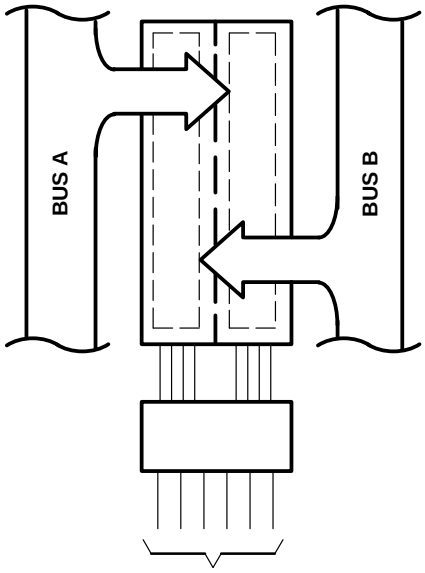

| 3 | 21 | 1 | 23 | 2 | 22 |
|---|---|---|---|---|---|
| OEAB | $\overline{\text{OEBA}}$ | CLKAB | CLKBA | SAB | SBA |
| L | L | X | X | X | L |

**REAL-TIME TRANSFER**
**BUS B TO BUS A**



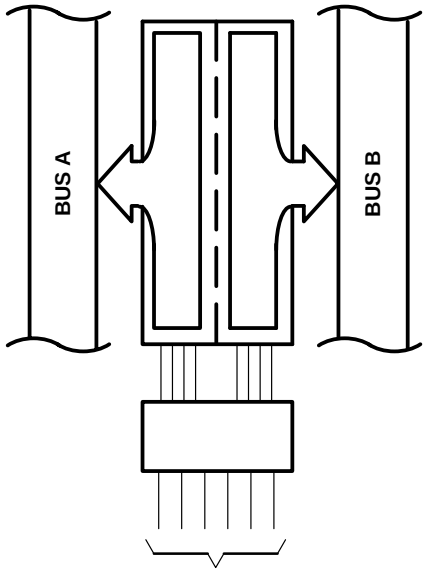

| 3 | 21 | 1 | 23 | 2 | 22 |
|---|---|---|---|---|---|
| OEAB | $\overline{\text{OEBA}}$ | CLKAB | CLKBA | SAB | SBA |
| H | H | X | X | L | X |

**REAL-TIME TRANSFER**
**BUS A TO BUS B**




| 3 | 21 | 1 | 23 | 2 | 22 |
|---|---|---|---|---|---|
| OEAB | $\overline{\text{OEBA}}$ | CLKAB | CLKBA | SAB | SBA |
| X | H | ↑ | X | X | X |
| L | X | X | ↑ | X | X |
| L | H | ↑ | ↑ | X | X |

**STORAGE FROM**
**A, B, OR A AND B**



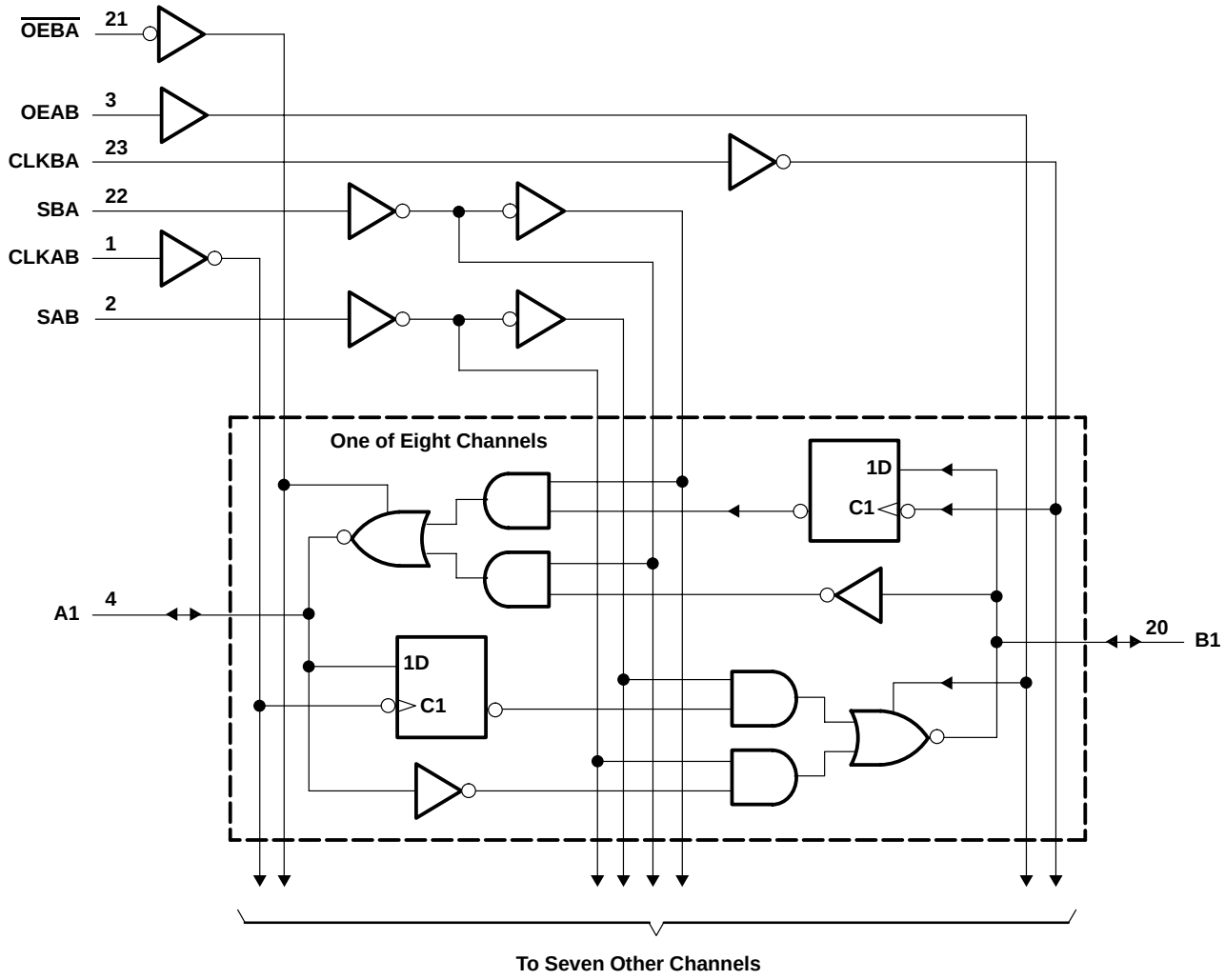

| 3 | 21 | 1 | 23 | 2 | 22 |
|---|---|---|---|---|---|
| OEAB | $\overline{\text{OEBA}}$ | CLKAB | CLKBA | SAB | SBA |
| H | L | H or L | H or L | H | H |

**TRANSFER STORED DATA**
**TO A AND/OR B**

Pin numbers shown are for the DW, JT, NT, and W packages.

**Figure 1. Bus-Management Functions**

## logic diagram (positive logic)




Pin numbers shown are for the DW, JT, NT, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input clamp current, $I_{IK}$ ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O = 0$ to $V_{CC}$) . . . . . ±35 mA
Continuous current through $V_{CC}$ or GND . . . . . ±70 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DW package . . . . . 46°C/W
(see Note 3): NT package . . . . . 67°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-3.

## recommended operating conditions (see Note 4)

| | | | SN54HCT652 | | | SN74HCT652 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $t_t$ | Input transition (rise and fall) time | | | | 500 | | | 500 | ns |
| $T_A$ | Operating free-air temperature | | –55 | | 125 | –40 | | 85 | °C |

NOTE 4: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | $T_A$ = 25°C | | | SN54HCT652 | | SN74HCT652 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –20 μA | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | V |
| | | | $I_{OH}$ = –6 mA | | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| $V_{OL}$ | | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20 μA | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | V |
| | | | $I_{OL}$ = 6 mA | | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| $I_I$ | Control inputs | $V_I$ = $V_{CC}$ or 0 | | 5.5 V | | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA |
| $I_{OZ}$ | A or B | $V_O$ = $V_{CC}$ or 0, $V_I$ = $V_{IH}$ or $V_{IL}$, Data = $V_{CC}$ or 0 | | 5.5 V | | | ±0.01 | ±0.5 | | ±10 | | ±5 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or 0, $I_O$ = 0 | | 5.5 V | | | 8 | | 160 | | 80 | μA |
| $\Delta I_{CC}$† | | One input at 0.5 V or 2.4 V, Other inputs at 0 or $V_{CC}$ | | 5.5 V | | 1.4 | 2.4 | | 3 | | 2.9 | mA |
| $C_i$ | Control inputs | | | 4.5 V to 5.5 V | | 3 | 10 | | 10 | | 10 | pF |

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or $V_{CC}$.

## timing requirements over recommended operating free-air temperature range (unless otherwise noted)

| | | $V_{CC}$ | $T_A$ = 25°C | | SN54HCT652 | | SN74HCT652 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | 4.5 V | | 25 | | 17 | | 20 | MHz |
| | | 5.5 V | | 28 | | 19 | | 22 | |
| $t_w$ | Pulse duration, CLKBA or CLKAB high or low | 4.5 V | 20 | | 30 | | 25 | | ns |
| | | 5.5 V | 18 | | 27 | | 23 | | |
| $t_{su}$ | Setup time, A before CLKAB↑ or B before CLKBA↑ | 4.5 V | 15 | | 23 | | 19 | | ns |
| | | 5.5 V | 14 | | 21 | | 17 | | |
| $t_h$ | Hold time, A after CLKAB↑ or B after CLKBA↑ | 4.5 V | 5 | | 5 | | 5 | | ns |
| | | 5.5 V | 5 | | 5 | | 5 | | |

### switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | $T_A$ = 25°C | | | SN54HCT652 | | SN74HCT652 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 4.5 V | 25 | 35 | | 17 | | 20 | | MHz |
| | | | 5.5 V | 28 | 40 | | 19 | | 22 | | |
| $t_{pd}$ | CLKBA or CLKAB | A or B | 4.5 V | | 18 | 36 | | 54 | | 45 | ns |
| | | | 5.5 V | | 16 | 32 | | 49 | | 41 | |
| | A or B | B or A | 4.5 V | | 14 | 27 | | 41 | | 34 | |
| | | | 5.5 V | | 12 | 24 | | 37 | | 31 | |
| | SBA or SAB† | A or B | 4.5 V | | 20 | 38 | | 57 | | 48 | |
| | | | 5.5 V | | 17 | 34 | | 51 | | 43 | |
| $t_{en}$ | $\overline{OEBA}$ or OEAB | A or B | 4.5 V | | 25 | 49 | | 74 | | 61 | ns |
| | | | 5.5 V | | 22 | 44 | | 67 | | 55 | |
| $t_{dis}$ | $\overline{OEBA}$ or OEAB | A or B | 4.5 V | | 25 | 49 | | 74 | | 61 | ns |
| | | | 5.5 V | | 22 | 44 | | 67 | | 55 | |
| $t_t$ | | Any | 4.5 V | | 9 | 12 | | 18 | | 15 | ns |
| | | | 5.5 V | | 7 | 11 | | 16 | | 14 | |

† These parameters are measured with the internal output state of the storage register opposite that of the bus input.

### switching characteristics over recommended operating free-air temperature range, $C_L$ = 150 pF (unless otherwise noted) (see Figure 2)

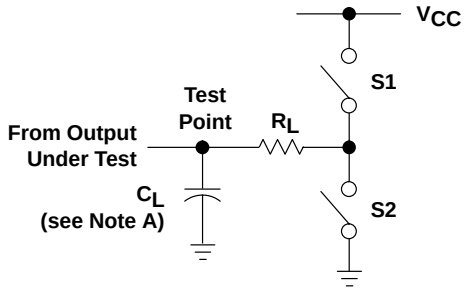
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | $T_A$ = 25°C | | | SN54HCT652 | | SN74HCT652 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | CLKBA or CLKAB | A or B | 4.5 V | | 24 | 53 | | 80 | | 66 | ns |
| | | | 5.5 V | | 22 | 47 | | 72 | | 60 | |
| | A or B | B or A | 4.5 V | | 22 | 44 | | 70 | | 55 | |
| | | | 5.5 V | | 20 | 39 | | 60 | | 50 | |
| | SBA or SAB† | A or B | 4.5 V | | 26 | 55 | | 83 | | 69 | |
| | | | 5.5 V | | 24 | 49 | | 74 | | 62 | |
| $t_{en}$ | $\overline{OEBA}$ or OEAB | A or B | 4.5 V | | 33 | 66 | | 100 | | 82 | ns |
| | | | 5.5 V | | 30 | 59 | | 90 | | 74 | |
| $t_t$ | | Any | 4.5 V | | 17 | 42 | | 63 | | 53 | ns |
| | | | 5.5 V | | 14 | 38 | | 57 | | 48 | |

† These parameters are measured with the internal output state of the storage register opposite that of the bus input.

### operating characteristics, $T_A$ = 25°C

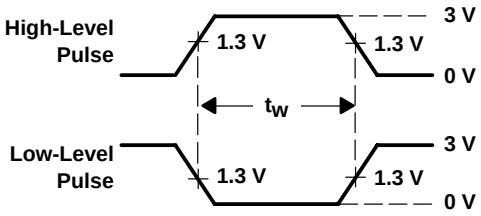
| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load | 50 | pF |

## PARAMETER MEASUREMENT INFORMATION

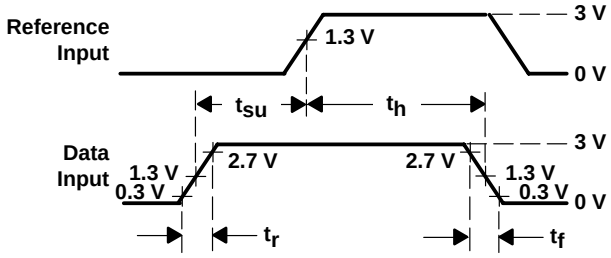



LOAD CIRCUIT

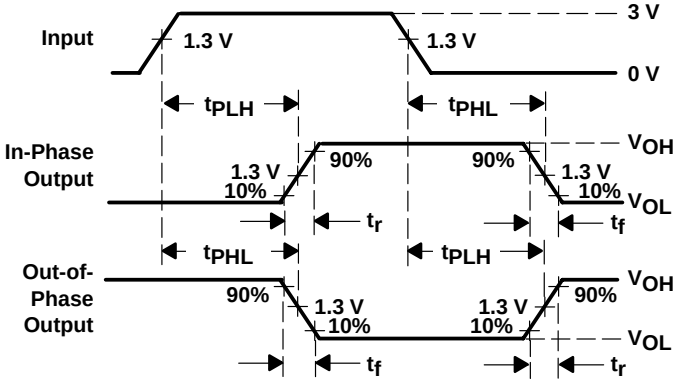
| PARAMETER | | $R_L$ | $C_L$ | S1 | S2 |
|---|---|---|---|---|---|
| $t_{en}$ | $t_{PZH}$ | 1 kΩ | 50 pF or 150 pF | Open | Closed |
| | $t_{PZL}$ | | | Closed | Open |
| $t_{dis}$ | $t_{PHZ}$ | 1 kΩ | 50 pF | Open | Closed |
| | $t_{PLZ}$ | | | Closed | Open |
| $t_{pd}$ or $t_t$ | | –– | 50 pF or 150 pF | Open | Open |



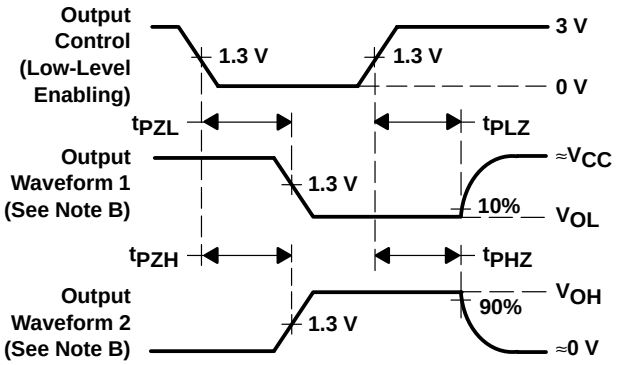

VOLTAGE WAVEFORMS
PULSE DURATIONS




VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. $C_L$ includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 6 ns, $t_f$ = 6 ns.
D. For clock inputs, $f_{max}$ is measured when the input duty cycle is 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
G. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
H. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| SN74HCT652DW | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HCT652DWE4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HCT652DWR | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HCT652DWRE4 | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HCT652NT | ACTIVE | PDIP | NT | 24 | 15 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74HCT652NTE4 | ACTIVE | PDIP | NT | 24 | 15 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |

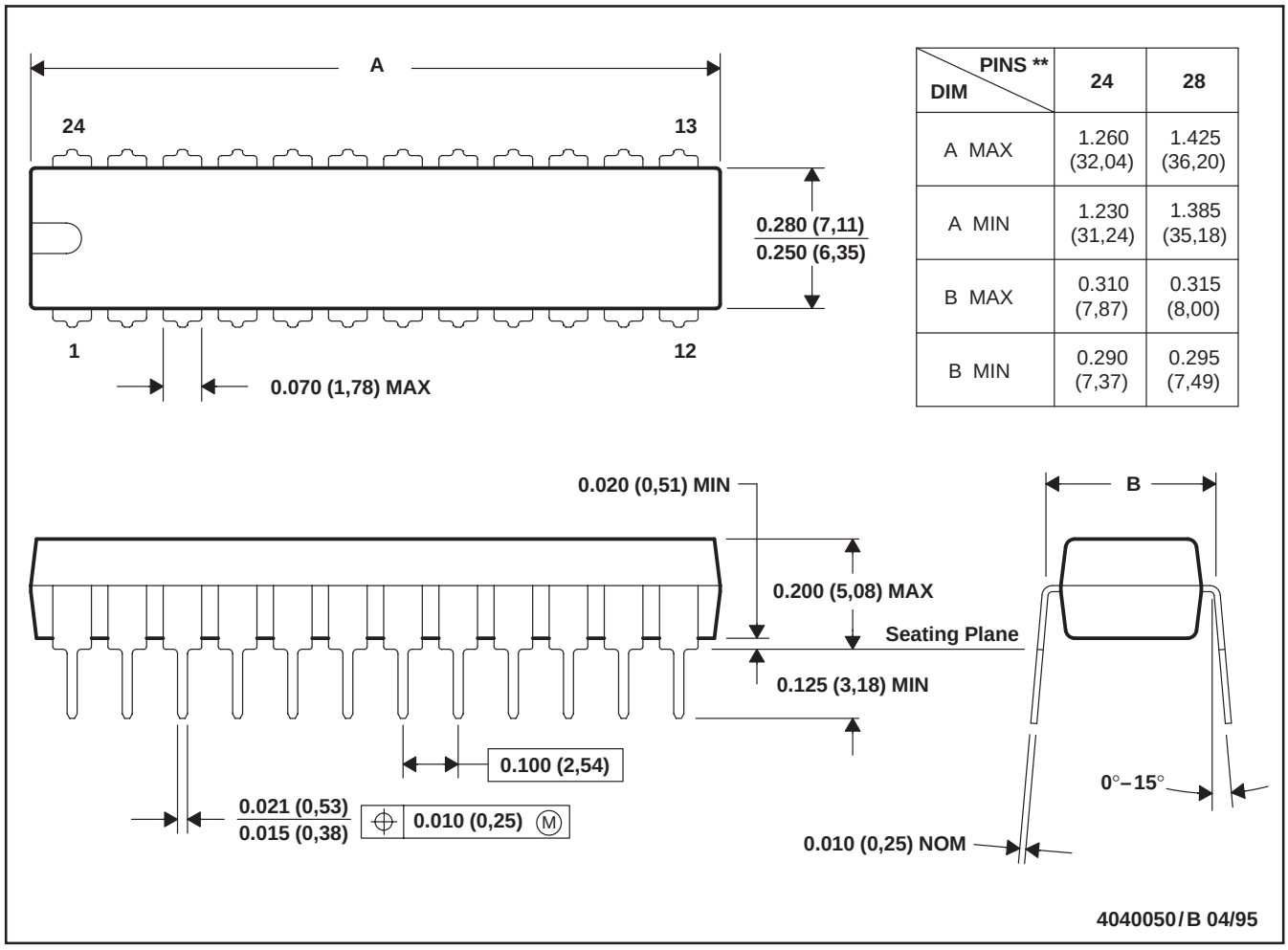
[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**NT (R-PDIP-T**)** **PLASTIC DUAL-IN-LINE PACKAGE**

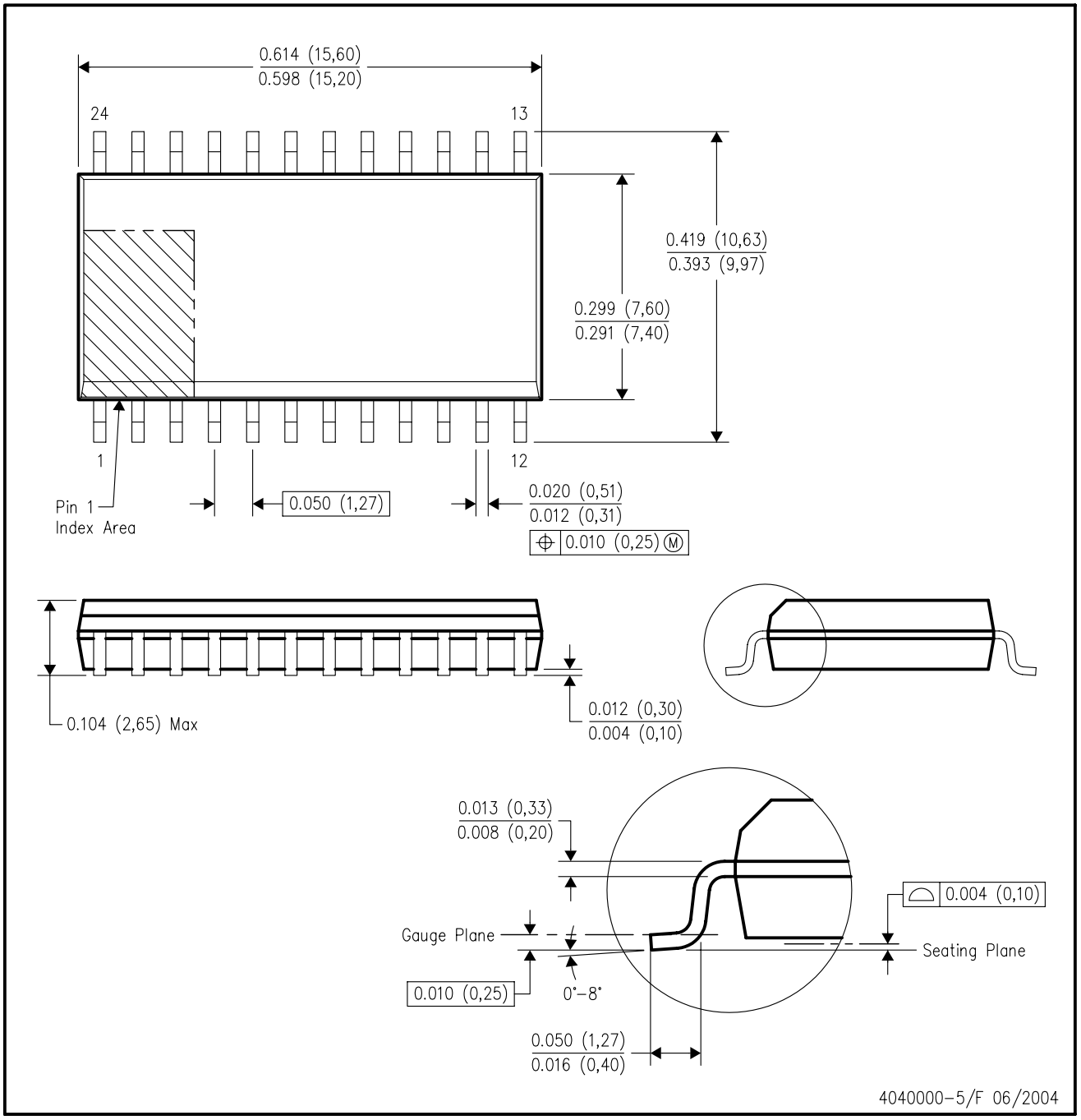
**24 PINS SHOWN**




| DIM \ PINS ** | 24 | 28 |
|---|---|---|
| A MAX | 1.260 (32,04) | 1.425 (36,20) |
| A MIN | 1.230 (31,24) | 1.385 (35,18) |
| B MAX | 0.310 (7,87) | 0.315 (8,00) |
| B MIN | 0.290 (7,37) | 0.295 (7,49) |

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

## DW (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265