

3.3 V 16 K / 32 K × 36 FLE^x36[®] Synchronous Dual-Port Static RAM

Features

- True dual-ported memory cells which allow simultaneous access of the same memory location
- Two flow-through/pipelined devices
 - 16 K × 36 organization (CY7C09569V)
 - 32 K × 36 organization (CY7C09579V)
- 0.25-micron CMOS for optimum speed/power
- Three modes
 - Flow-through
 - Pipelined
 - Burst
- Bus-matching capabilities on right port (× 36 to × 18 or × 9)
- Byte-select capabilities on left port
- 100-MHz pipelined operation
- High-speed clock to data access 5/6 ns
- 3.3 V low operating power
 - Active = 250 mA (typical)
 - Standby = 10 μA (typical)
- Fully synchronous interface for ease of use
- Burst counters increment addresses internally
 - Shorten cycle times
 - Minimize bus noise
 - Supported in flow-through and pipelined modes
- Counter address read back via I/O lines
- Single chip enable
- Automatic power-down
- Commercial and industrial temperature ranges
- Compact package
 - 144-pin TQFP (20 × 20 × 1.4 mm)
 - 144-pin Pb-free TQFP (20 × 20 × 1.4 mm)
 - 172-ball BGA (1.0-mm pitch) (15 × 15 × 0.51 mm)

Functional Description

The CY7C09569V and CY7C09579V are high-speed 3.3 V synchronous CMOS 16 K and 32 K × 36 dual-port static RAMs. Two ports are provided, permitting independent, simultaneous access for reads and writes to any location in memory. Registers on control, address, and data lines allow for minimal set-up and hold times. In pipelined output mode, data is registered for decreased cycle time. Clock to data valid $t_{CD2} = 5$ ns (pipelined). Flow-through mode can also be used to bypass the pipelined output register to eliminate access latency. In flow-through mode data will be available $t_{CD1} = 12.5$ ns after the address is clocked into the device. Pipelined output or flow-through mode is selected via the $\overline{FT}/\text{Pipe}$ pin.

Each port contains a burst counter on the input address register. The internal write pulse width is independent of the external R/W LOW duration. The internal write pulse is self-timed to allow the shortest possible cycle times.

A HIGH on $\overline{CE}$ for one clock cycle will power down the internal circuitry to reduce the static power consumption. In the pipelined mode, one cycle is required with $\overline{CE}$ LOW to reactivate the outputs.

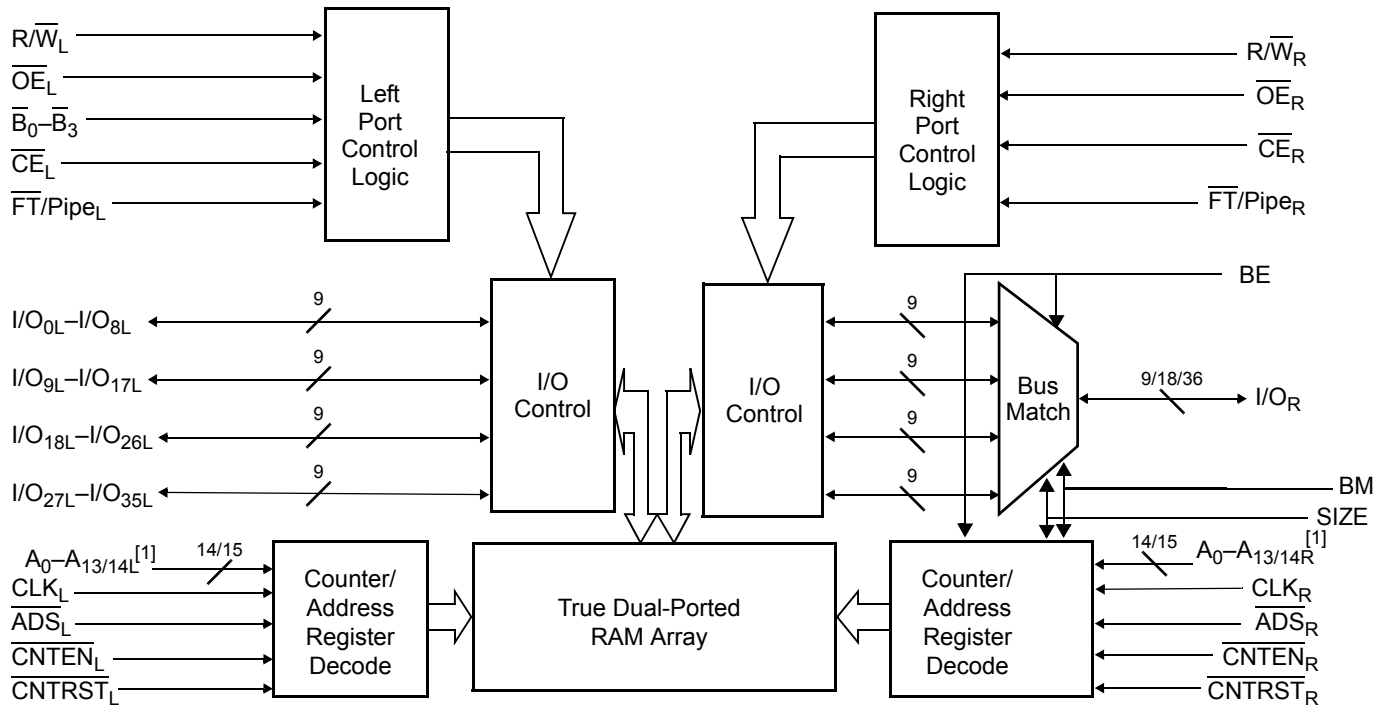
Counter Enable Inputs are provided to stall the operation of the address input and utilize the internal address generated by the internal counter for fast interleaved memory applications. A port's burst counter is loaded with the port's Address Strobe (ADS). When the port's Count Enable (CNTEN) is asserted, the address counter will increment on each LOW-to-HIGH transition of that port's clock signal. This will read/write one word from/into each successive address location until CNTEN is deasserted. The counter can address the entire memory array and will loop back to the start. Counter Reset (CNTRST) is used to reset the burst counter.

Parts are available in 144-pin Thin Quad Plastic Flatpack (TQFP), 144-pin Pb-free Thin Quad Plastic Flatpack (TQFP) and 172-ball Ball Grid Array (BGA) packages.

Selection Guide

Description	CY7C09569V / CY7C09579V		Unit
	-100	-83	
f_{MAX2} (pipelined)	100	83	MHz
Maximum access time (clock to data, pipelined)	5	6	ns
Typical operating current I_{CC}	250	240	mA
Typical standby current for I_{SB1} (both ports TTL level)	30	25	mA
Typical standby current for I_{SB3} (both ports CMOS level)	10	10	μA

Logic Block Diagram



Note

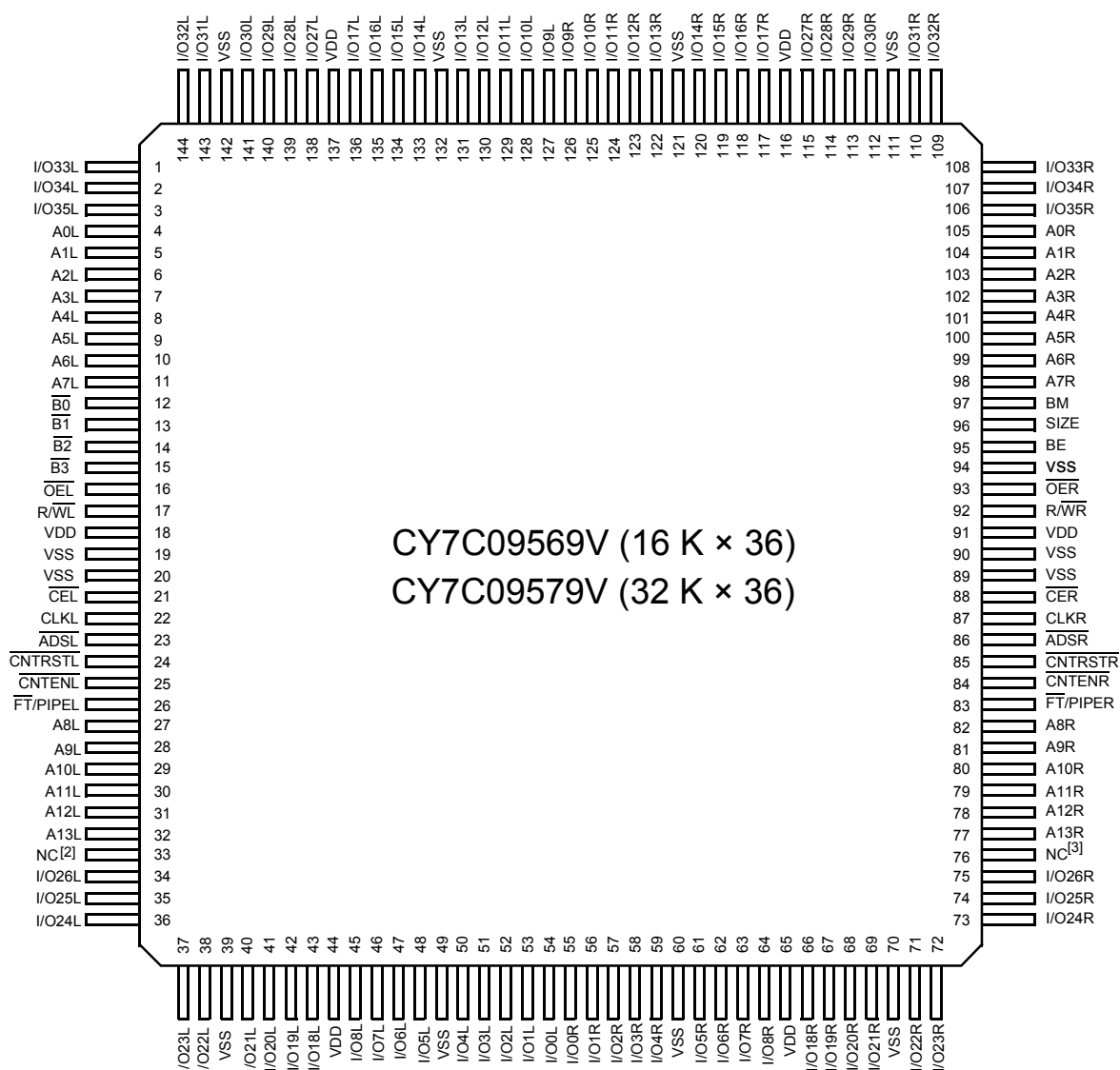
1. A_0-A_{13} for 16K; A_0-A_{14} for 32 K devices.

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Pin Configurations

Figure 1. 144-pin TQFP (20 × 20 × 1.4 mm) pinout (Top View)



Notes

2. This pin is A14L for CY7C09579V.
3. This pin is A14R for CY7C09579V.

Pin Configurations

Figure 2. 172-ball BGA (15 × 15 × 1.25 mm) pinout (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	I/O32L	I/O30L	NC	VSS	I/O13L	VDD	I/O11L	I/O11R	VDD	I/O13R	VSS	NC	I/O30R	I/O32R
B	A0L	I/O33L	I/O29	I/O17L	I/O14L	I/O12L	I/O9L	I/O9R	I/O12R	I/O14R	I/O17R	I/O29R	I/O33R	A0R
C	NC	A1L	I/O31L	I/O27L	NC	I/O15L	I/O10L	I/O10R	I/O15R	NC	I/O27R	I/O31R	A1R	NC
D	A2L	A3L	I/O35L	I/O34L	I/O28L	I/O16L	VSS	VSS	I/O16R	I/O28R	I/O34R	I/O35R	A3R	A2R
E	A4L	A5L	NC	B0L	NC	NC			NC	NC	BM	NC	A5R	A4R
F	VDD	A6L	A7L	B1L	NC					NC	SIZE	A7R	A6R	VDD
G	OEL	B2L	B3L	CEL							CER	VSS	BE	OER
H	VSS	R/WL	A8L	CLKL							CLKR	A8R	R/WR	VSS
J	A9L	A10L	VSS	ADSL	NC					NC	ADSR	VSS	A10R	A9R
K	A11L	A12L	NC	CNTRSTL	NC	NC			NC	NC	CNTRSTR	NC	A12R	A11R
L	FT/PIPEL	A13L	CNTENL	I/O26L	I/O25L	I/O19L	VSS	VSS	I/O19R	I/O25R	I/O26R	CNTENR	A13R	FT/PIPER
M	NC	NC ^[4]	I/O22L	I/O18L	NC	I/O7L	I/O2L	I/O2R	I/O7R	NC	I/O18R	I/O22R	NC ^[5]	NC
N	I/O24L	I/O20L	I/O8L	I/O6L	I/O5L	I/O3L	I/O0L	I/O0R	I/3R	I/O5R	I/O6R	I/O8R	I/O20R	I/O24R
P	I/O23L	I/O21L	NC	VSS	I/O4L	VDD	I/O1L	I/O1R	VDD	I/O4R	VSS	NC	I/O21R	I/O23R

Notes

4. This pin is A14L for CY7C09579V.
5. This pin is A14R for CY7C09579V.

Pin Definitions

Left Port	Right Port	Description
A _{0L} –A _{13/14L}	A _{0R} –A _{13/14R}	Address Inputs (A ₀ –A ₁₃ for 16 K, A ₀ –A ₁₄ for 32 K devices).
ADS _L	ADS _R	Address Strobe Input. Used as an address qualifier. This signal should be asserted LOW to assert the part using the externally supplied address on Address Pins. To load this address into the Burst Address Counter both ADS and CNTEN have to be LOW. ADS is disabled if CNTRST is asserted LOW.
$\overline{\text{CE}}_{\text{L}}$	$\overline{\text{CE}}_{\text{R}}$	Chip Enable Input.
CLK _L	CLK _R	Clock Signal. This input can be free-running or strobed. Maximum clock input rate is f _{MAX} .
CNTEN _L	CNTEN _R	Counter Enable Input. Asserting this signal <u>LOW</u> increments the <u>burst address</u> counter of its respective port on each rising edge of CLK. CNTEN is disabled if CNTRST is asserted LOW.
CNTRST _L	CNTRST _R	Counter Reset Input. Asserting this signal LOW resets the <u>burst address</u> counter of its respective port to zero. CNTRST is not disabled by asserting ADS or CNTEN.
I/O _{0L} –I/O _{35L}	I/O _{0R} –I/O _{35R}	Data Bus Input/Output
$\overline{\text{OE}}_{\text{L}}$	$\overline{\text{OE}}_{\text{R}}$	Output Enable Input. This signal must be asserted LOW to enable the I/O data pins during read operations.
R/ $\overline{\text{W}}_{\text{L}}$	R/ $\overline{\text{W}}_{\text{R}}$	Read/Write Enable Input. This signal is asserted LOW to write to the dual port memory array. For read operations, assert this pin HIGH.
$\overline{\text{FT/PIPE}}_{\text{L}}$	$\overline{\text{FT/PIPE}}_{\text{R}}$	Flow-Through/Pipelined Select Input. For flow-through mode operation, assert this pin LOW. For pipelined mode operation, assert this pin HIGH.
$\overline{\text{B}}_{0\text{L}}$ – $\overline{\text{B}}_{3\text{L}}$	–	Byte Select Inputs. Asserting these signals enable read and write operations to the corresponding bytes of the memory array.
–	BM, SIZE	Select Pins for Bus Matching. See Bus Matching for details.
–	BE	Big Endian Pin. See Bus Matching for details.
V _{SS}		Ground Input.
V _{DD}		Power Input.

Maximum Ratings

Exceeding maximum ratings^[6] may shorten the useful life of the device. User guidelines are not tested.

Storage temperature -65 °C to +150 °C

Ambient temperature with power applied -55 °C to +125 °C

Supply voltage to ground potential -0.5 V to +4.6 V

DC voltage applied to outputs in High Z state -0.5 V to $V_{DD} + 0.5 V$

DC input voltage -0.5 V to $V_{DD} + 0.5 V$ ^[7]

Output current into outputs (LOW) 20 mA

Static discharge voltage > 2001 V

Latch-up current > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}
Commercial	0 °C to +70 °C	3.3 V ± 165 mV

Electrical Characteristics

Over the Operating Range

Parameter	Description	CY7C09569V / CY7C09579V						Unit
		-100			-83			
		Min	Typ	Max	Min	Typ	Max	
V _{OH}	Output HIGH Voltage (V _{DD} = Min., I _{OH} = −4.0 mA)	2.4	–	–	2.4	–	–	V
V _{OL}	Output LOW Voltage (V _{DD} = Min., I _{OL} = +4.0 mA)	–	–	0.4	–	–	0.4	V
V _{IH}	Input HIGH Voltage	2.0	–	–	2.0	–	–	V
V _{IL}	Input LOW Voltage	–	–	0.8	–	–	0.8	V
I _{OZ}	Output Leakage Current	−10	–	10	−10	–	10	μA
I _{CC}	Operating Current (V _{DD} = Max., I _{OUT} = 0 mA) Outputs Disabled	–	250	385	–	240	360	mA
I _{SB1}	Standby Current (Both Ports TTL Level) CE _L & CE _R ≥ V _{IH} , f = f _{MAX}	–	30	75	–	25	70	mA
I _{SB2}	Standby Current (One Port TTL Level) CE _L CE _R ≥ V _{IH} , f = f _{MAX}	–	170	220	–	160	210	mA
I _{SB3}	Standby Current (Both Ports CMOS Level) CE _L & CE _R ≥ V _{DD} − 0.2 V, f = 0	–	0.01	1	–	0.01	1	mA
I _{SB4}	Standby Current (One Port CMOS Level) CE _L CE _R ≥ V _{IH} , f = f _{MAX}	–	150	200	–	140	190	mA

Capacitance

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	$T_A = 25 \text{ °C}$, $f = 1 \text{ MHz}$, $V_{DD} = 3.3 \text{ V}$	10	pF
C_{OUT}	Output capacitance		10	pF

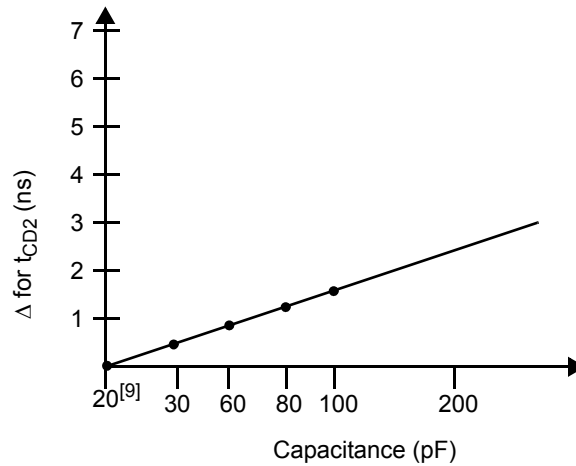
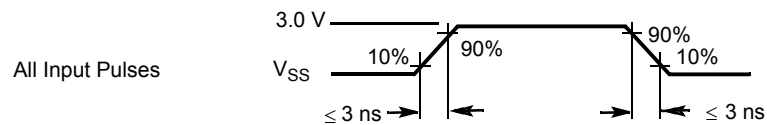
Notes

6. The voltage on any input or I/O pin can not exceed the power pin during power-up.

7. Pulse width < 20 ns.

AC Test Load and Waveforms

Figure 3. AC Test Load and Waveforms



(b) Load Derating Curve

Notes

8. External AC Test Load Capacitance = 10 pF.
9. (Internal I/O pad Capacitance = 10 pF + AC Test Load.

Switching Characteristics

Over the Operating Range

Parameter	Description	CY7C09569V/CY7C09579V				Unit
		-100		-83		
		Min	Max	Min	Max	
f _{MAX1}	f _{Max} Flow-Through	–	67	–	45	MHz
f _{MAX2}	f _{Max} Pipelined	–	100	–	83	MHz
t _{CYC1}	Clock Cycle Time – Flow-Through	15	–	22	–	ns
t _{CYC2}	Clock Cycle Time – Pipelined	10	–	12	–	ns
t _{CH1}	Clock HIGH Time – Flow-Through	6.5	–	7.5	–	ns
t _{CL1}	Clock LOW Time – Flow-Through	6.5	–	7.5	–	ns
t _{CH2}	Clock HIGH Time – Pipelined	4	–	5	–	ns
t _{CL2}	Clock LOW Time – Pipelined	4	–	5	–	ns
t _R	Clock Rise Time	–	3	–	3	ns
t _F	Clock Fall Time	–	3	–	3	ns
t _{SA}	Address Set-Up Time	3.5	–	4	–	ns
t _{HA}	Address Hold Time	0.5	–	0.5	–	ns
t _{SB}	Byte Select Set-Up Time	3.5	–	4	–	ns
t _{HB}	Byte Select Hold Time	0.5	–	0.5	–	ns
t _{SC}	Chip Enable Set-Up Time	3.5	–	4	–	ns
t _{HC}	Chip Enable Hold Time	0.5	–	0.5	–	ns
t _{SW}	R/W Set-Up Time	3.5	–	4	–	ns
t _{HW}	R/W Hold Time	0.5	–	0.5	–	ns
t _{SD}	Input Data Set-Up Time	3.5	–	4	–	ns
t _{HD}	Input Data Hold Time	0.5	–	0.5	–	ns
t _{SAD}	ADS Set-Up Time	3.5	–	4	–	ns
t _{HAD}	ADS Hold Time	0.5	–	0.5	–	ns
t _{SCN}	CNTEN Set-Up Time	3.5	–	4	–	ns
t _{HCN}	CNTEN Hold Time	0.5	–	0.5	–	ns
t _{SRST}	CNTRST Set-Up Time	3.5	–	4	–	ns
t _{HRST}	CNTRST Hold Time	0.5	–	0.5	–	ns
t _{OE}	Output Enable to Data Valid	–	8	–	9	ns
t _{OLZ} ^[10, 11]	OE to Low Z	2	–	2	–	ns
t _{OHZ} ^[10, 11]	OE to High Z	1	7	1	7	ns
t _{CD1}	Clock to Data Valid – Flow-Through	–	12.5	–	18	ns
t _{CD2}	Clock to Data Valid – Pipelined	–	5	–	6	ns
t _{CA1}	Clock to Counter Address Valid – Flow-Through	–	12.5	–	18	ns
t _{CA2}	Clock to Counter Address Valid – Pipelined	–	9	–	10	ns
t _{DC}	Data Output Hold After Clock HIGH	2	–	2	–	ns
t _{CKHZ} ^[10, 11]	Clock HIGH to Output High Z	2	6	2	7	ns
t _{CKLZ} ^[10, 11]	Clock HIGH to Output Low Z	2	–	2	–	ns

Notes

10. This parameter is guaranteed by design, but it is not production tested.
11. Test conditions used are Load 2.

Switching Characteristics *(continued)*

Over the Operating Range

Parameter	Description	CY7C09569V/CY7C09579V				Unit
		-100		-83		
		Min	Max	Min	Max	
Port to Port Delays						
t _{CWDD}	Write Port Clock HIGH to Read Data Delay	–	30	–	35	ns
t _{CCS}	Clock to Clock Set-Up Time	–	9	–	10	ns

Switching Waveforms

Figure 4. Read Cycle for Flow-Through Output ($\overline{\text{FT/PIPE}} = V_{\text{IL}}$) [12, 13, 14, 15]

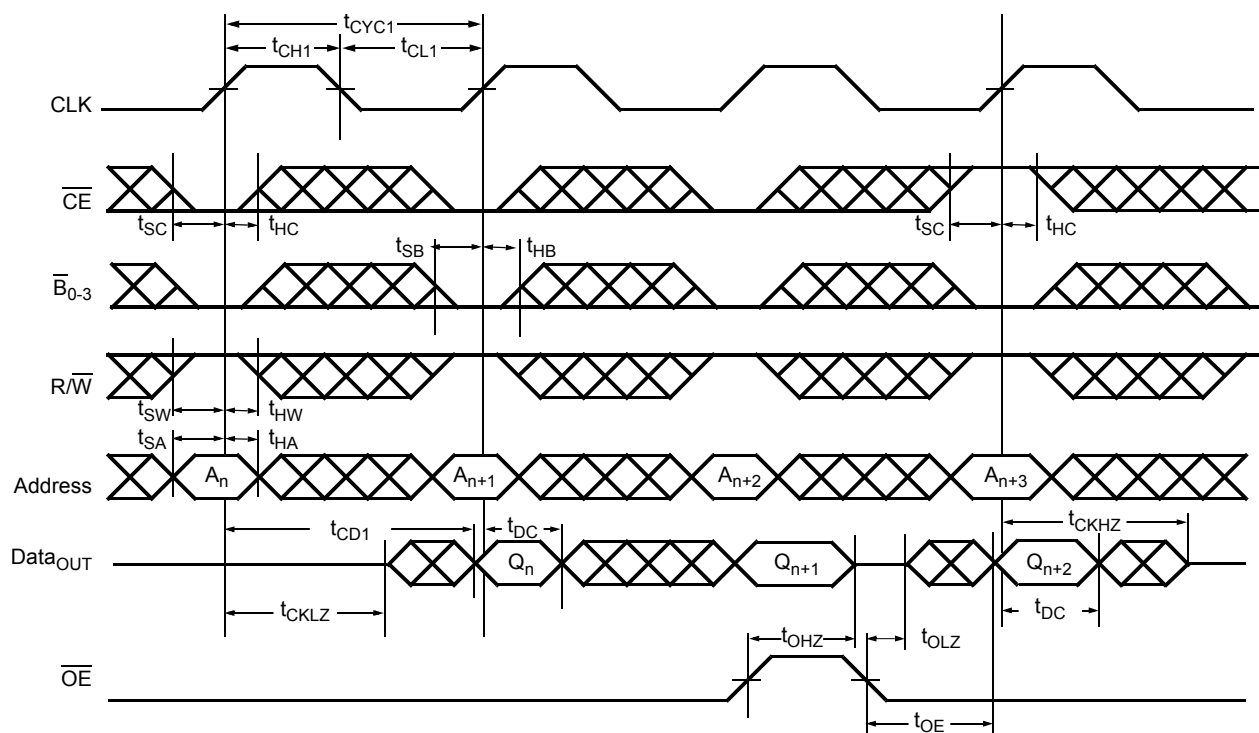
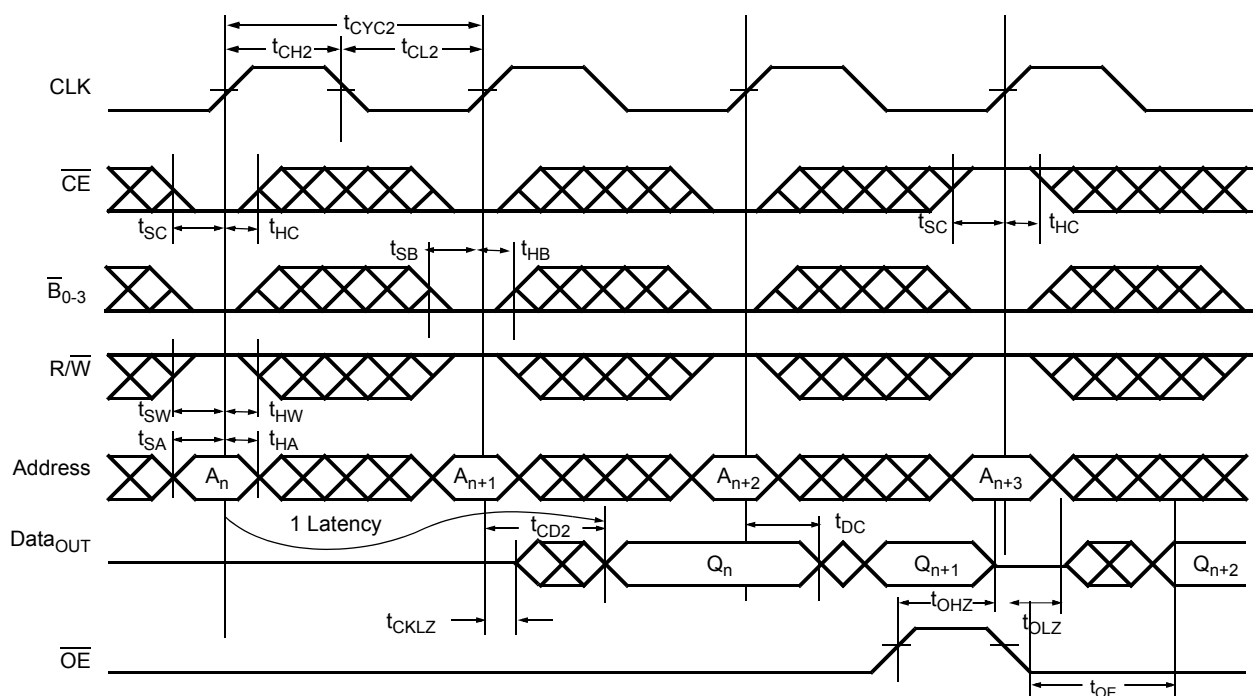


Figure 5. Read Cycle for Pipelined Operation ($\overline{\text{FT/PIPE}} = V_{\text{IH}}$) [12, 13, 14, 15]



Notes

12. $\overline{\text{OE}}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.

13. $\text{ADS} = V_{\text{IL}}$, $\text{CNTEN} = V_{\text{IL}}$ and $\text{CNTRST} = V_{\text{IH}}$.

14. The output is disabled (high-impedance state) by $\overline{\text{CE}} = V_{\text{IH}}$ following the next rising edge of the clock.

15. Addresses do not have to be accessed sequentially since $\text{ADS} = V_{\text{IL}}$ constantly loads the address on the rising edge of the CLK. Numbers are for reference only.

Switching Waveforms (continued)

Figure 6. Bus Match Read Cycle for Flow-Through Output ($\overline{\text{FT}}/\text{PIPE} = V_{\text{IL}}$) [16, 17, 18, 19, 20]

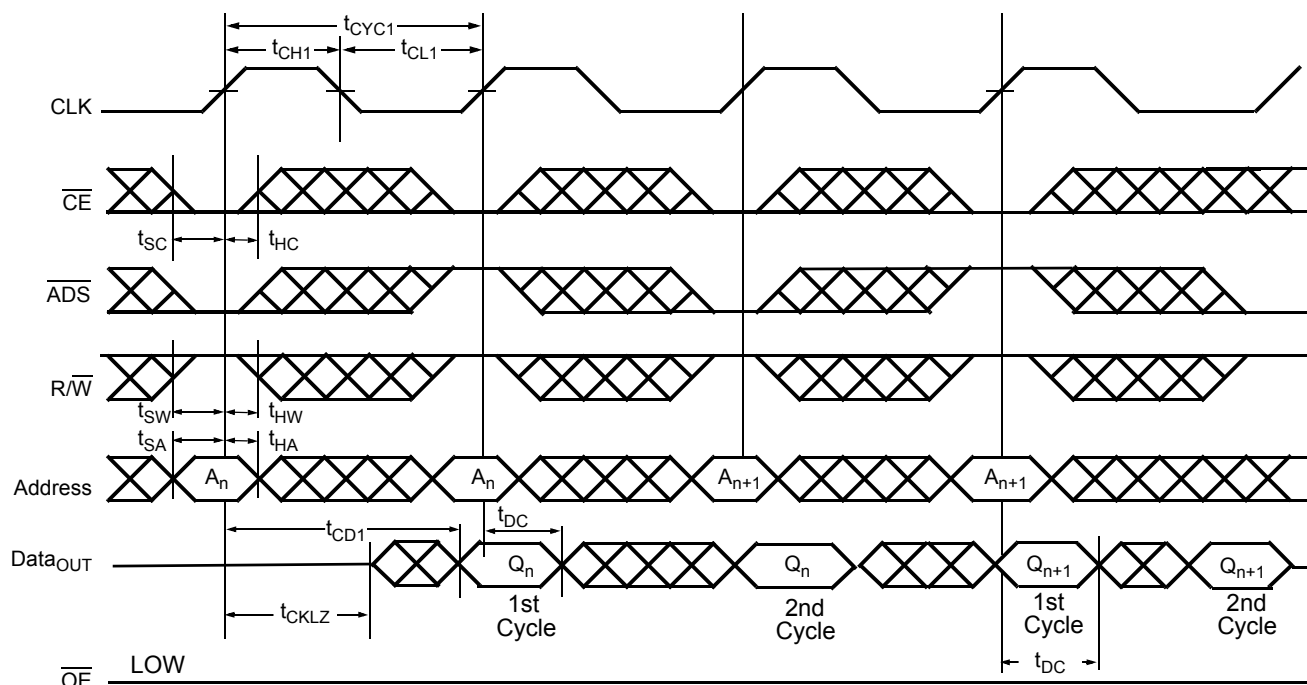
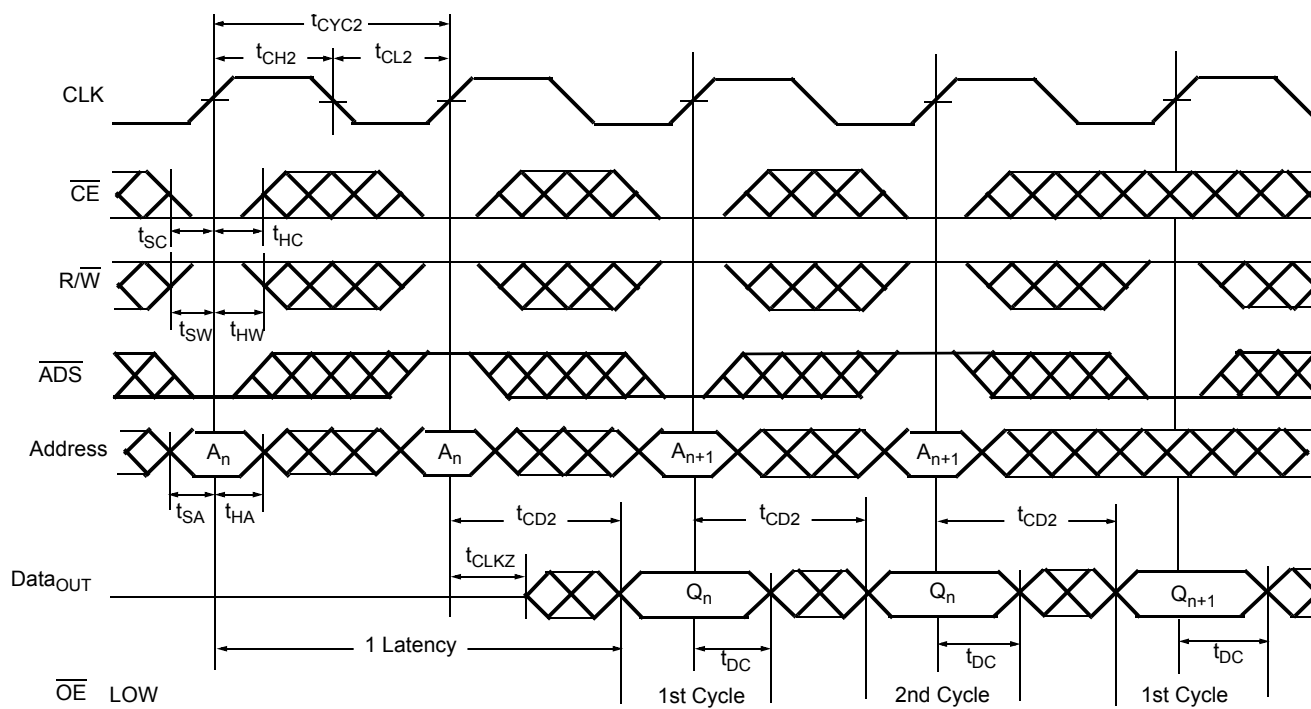


Figure 7. Bus Match Read Cycle for Pipelined Operation ($\overline{\text{FT}}/\text{PIPE} = V_{\text{IH}}$) [16, 17, 18, 19, 20]



Notes

16. OE is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
17. The output is disabled (high-impedance state) by $\text{CE} = V_{\text{IH}}$ following the next rising edge of the clock.
18. Timing shown is for x18 bus matching; x9 bus matching is similar with 4 cycles between address inputs.
19. See table "Right Port Operation" for data output on first and subsequent cycles.
20. $\text{CNTEN} = V_{\text{IL}}$. In x9 and x18 Bus Matching Burst Mode operations (Write or Read), $\overline{\text{ADS}}$ can toggle on the rising edge of every clock cycle or it can be at V_{IH} level all the time except when loading the initial external address (i.e. $\overline{\text{ADS}} = V_{\text{IL}}$ only required when reading or writing the first Byte or Word).

Switching Waveforms (continued)

Figure 8. Bank Select Pipelined Read [21, 22]

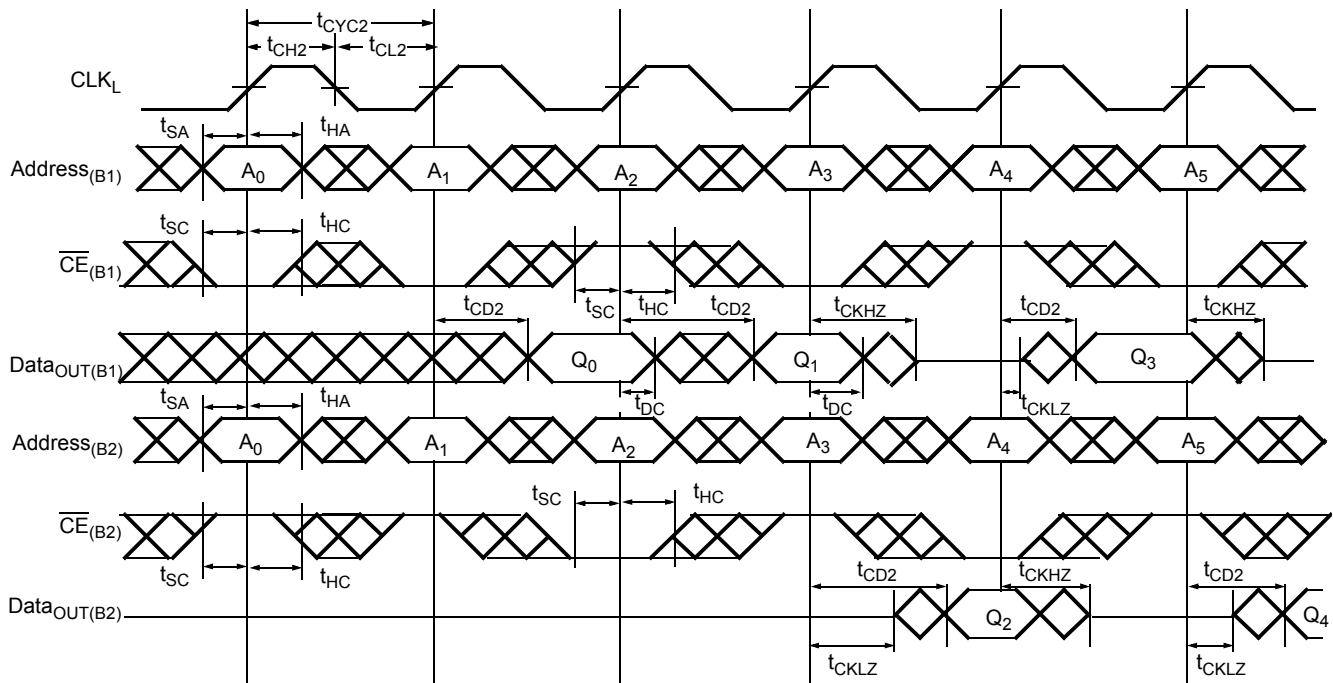
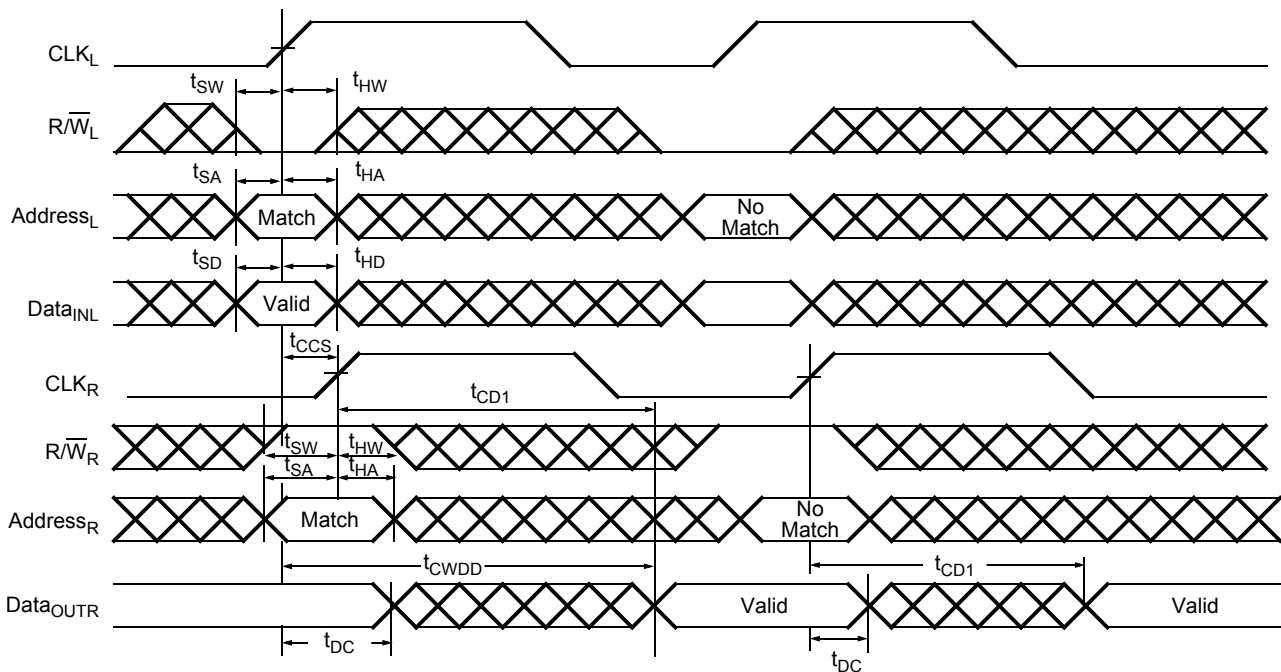


Figure 9. Left Port Write to Flow-Through Right Port Read [22, 23, 24, 25, 26]

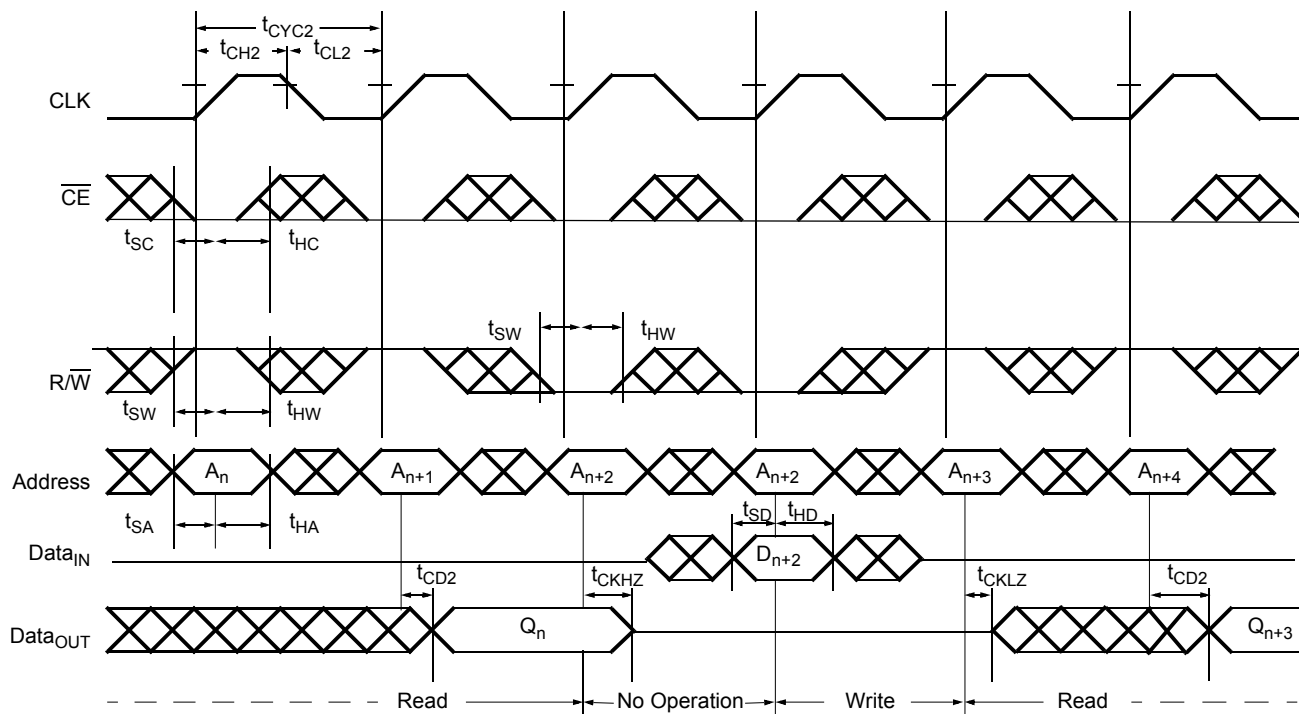


Notes

21. In this depth expansion example, B1 represents Bank #1 and B2 is Bank #2; Each Bank consists of one Cypress dual-port device from this data sheet.
22. $\overline{ADDRESS}_{(B1)} = \overline{ADDRESS}_{(B2)}$.
23. The same waveforms apply for a right port write to flow-through left port read.
24. $\overline{CE} = B0 = B1 = B2 = B3 = ADS = \overline{CNTEN} = V_{IL}$; $\overline{CNTRST} = V_{IH}$.
25. $OE = V_{IL}$ for the right port, which is being read from. $OE = V_{IH}$ for the left port, which is being written to.
26. If $t_{CCS} \leq$ maximum specified, then data from right port READ is not valid until the maximum specified for t_{CWDD} . If $t_{CCS} >$ maximum specified, then data is not valid until $t_{CCS} + t_{CD1}$ (t_{CWDD} does not apply in this case).

Switching Waveforms (continued)

Figure 10. Pipelined Read-to-Write-to-Read ($\overline{OE} = V_{IL}$) [27, 28, 29, 30]

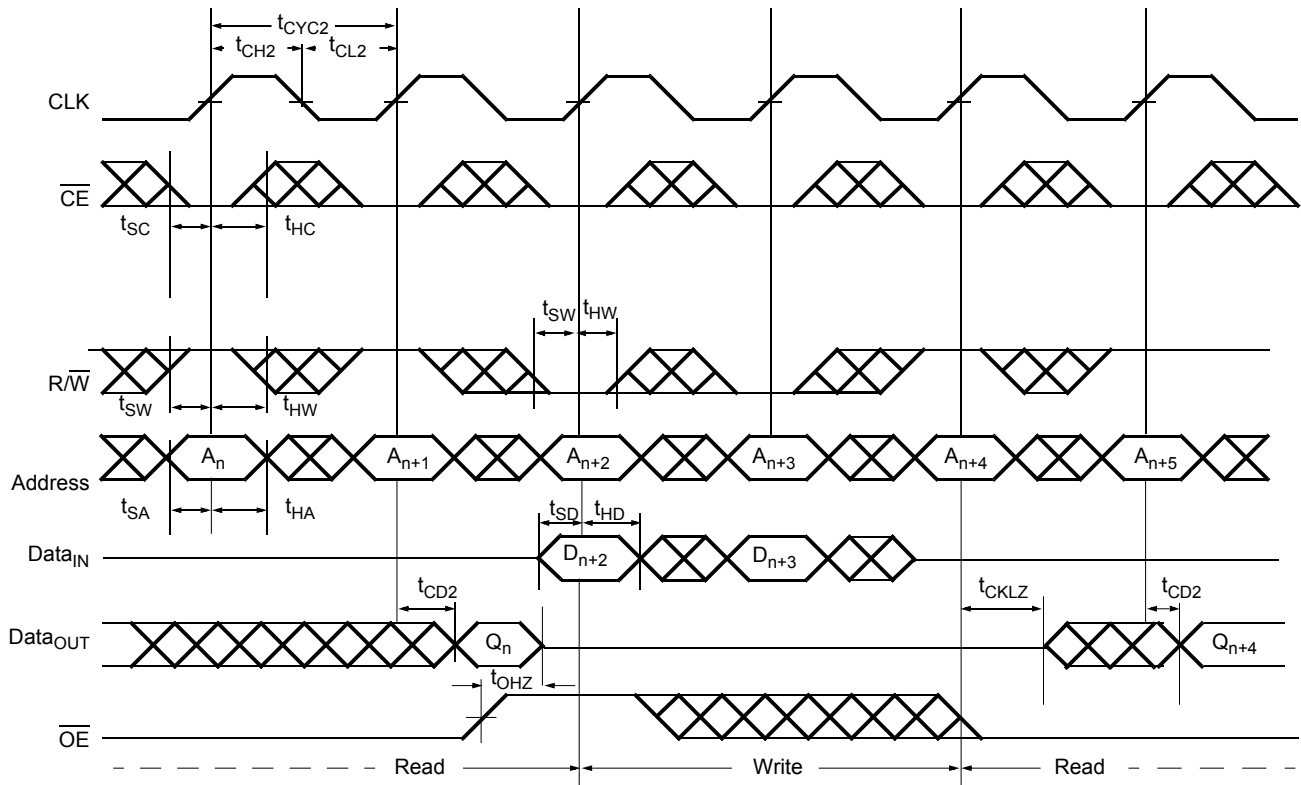


Notes

27. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK. Numbers are for reference only.
28. Output state (HIGH, LOW, or High-Impedance) is determined by the previous cycle control signals.
29. $\overline{CE} = \overline{ADS} = \overline{CNTEN} = V_{IL}$; $\overline{CNTRST} = V_{IH}$.
30. During "No Operation," data in memory at the selected address may be corrupted and should be rewritten to ensure data integrity.

Switching Waveforms (continued)

Figure 11. Pipelined Read-to-Write-to-Read ($\overline{OE}$ Controlled) [31, 32, 33, 34]

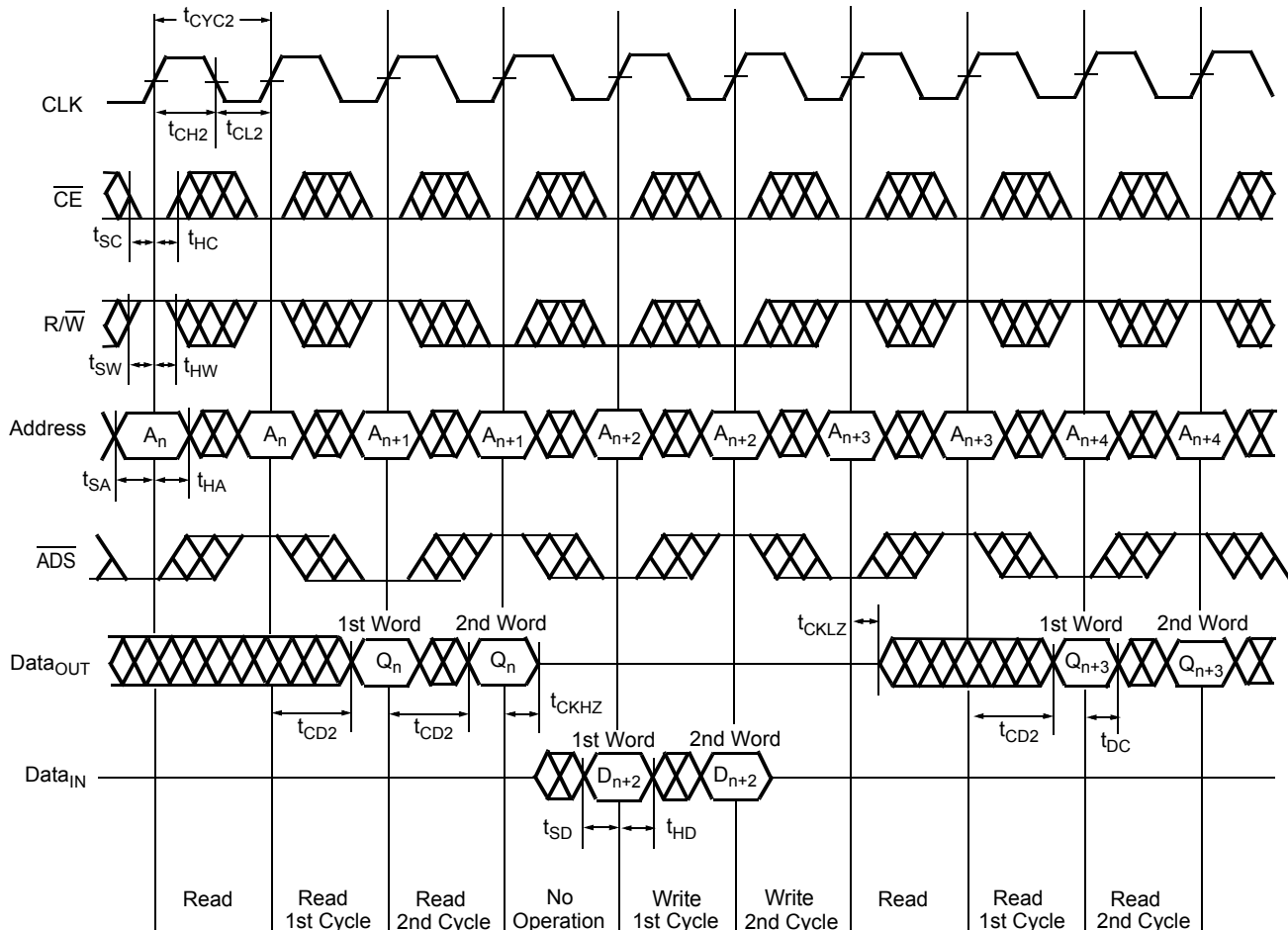


Notes

31. Test conditions used are Load 2.
32. Output state (HIGH, LOW, or High-Impedance) is determined by the previous cycle control signals.
33. $\overline{CE} = \overline{ADS} = \overline{CNTEN} = V_{IL}$; $\overline{CNTRST} = V_{IH}$.
34. During "No Operation," data in memory at the selected address may be corrupted and should be rewritten to ensure data integrity.

Switching Waveforms (continued)

Figure 12. Bus Match Pipelined Read-to-Write-to-Read ($\overline{OE} = V_{IL}$) [35, 36, 37, 38, 39, 40, 41]



Notes

35. Test conditions used are Load 2.
36. Timing shown is for x18 bus matching; x9 bus matching is similar with 4 cycles between address inputs.
37. See table "Right Port Operation" for data output on first and subsequent cycles.
38. $\overline{CNTEN} = V_{IL}$. In x9 and x18 Bus Matching Burst Mode operations (Write or Read), $\overline{ADS}$ can toggle on the rising edge of every clock cycle or it can be at V_{IH} level all the time except when loading the initial external address (i.e. $\overline{ADS} = V_{IL}$ only required when reading or writing the first Byte or Word).
39. $\overline{CE} = \overline{ADS} = \overline{CNTEN} = V_{IL}$; $\overline{CNTRST} = V_{IH}$.
40. During "No Operation," data in memory at the selected address may be corrupted and should be rewritten to ensure data integrity.
41. BM, SIZE, and BE must be reconfigured 1 cycle before operation is guaranteed. BM, SIZE, and BE should remain static for any particular port configuration.

Switching Waveforms (continued)

Figure 13. Flow-Through Read-to-Write-to-Read ($\overline{OE} = V_{IL}$) [42, 43, 44, 45, 46, 47]

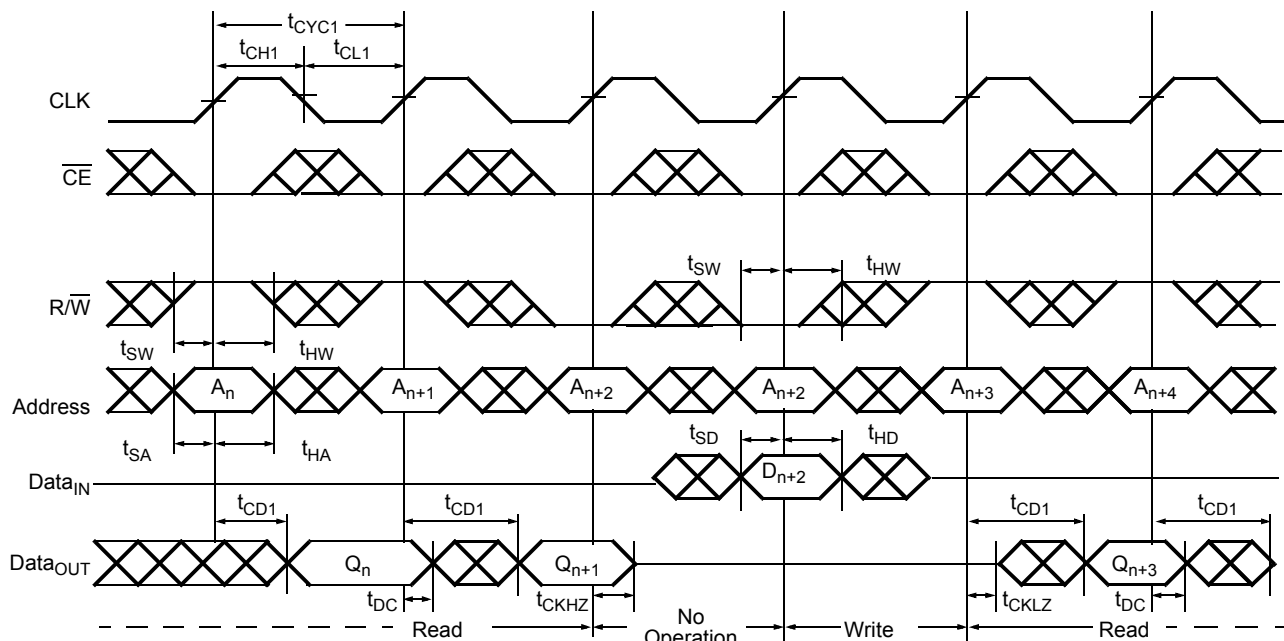
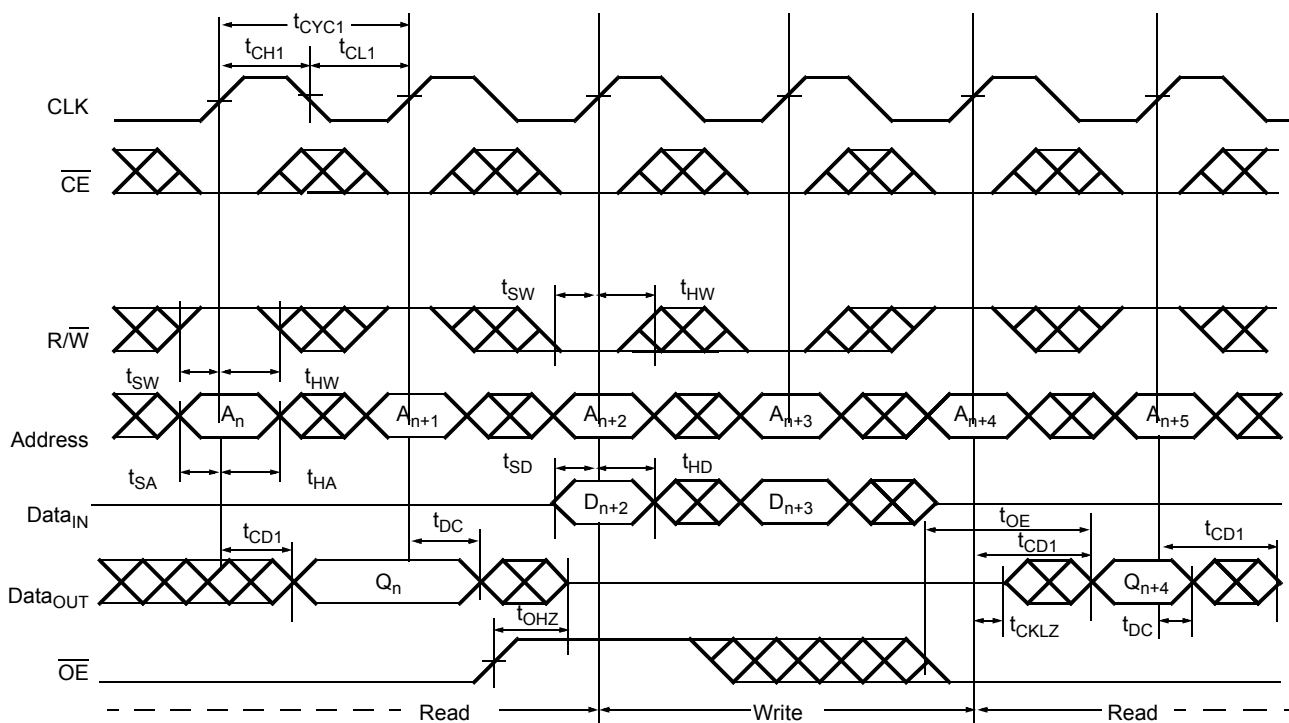


Figure 14. Flow-Through Read-to-Write-to-Read ($\overline{OE}$ Controlled) [42, 43, 46, 47, 48]

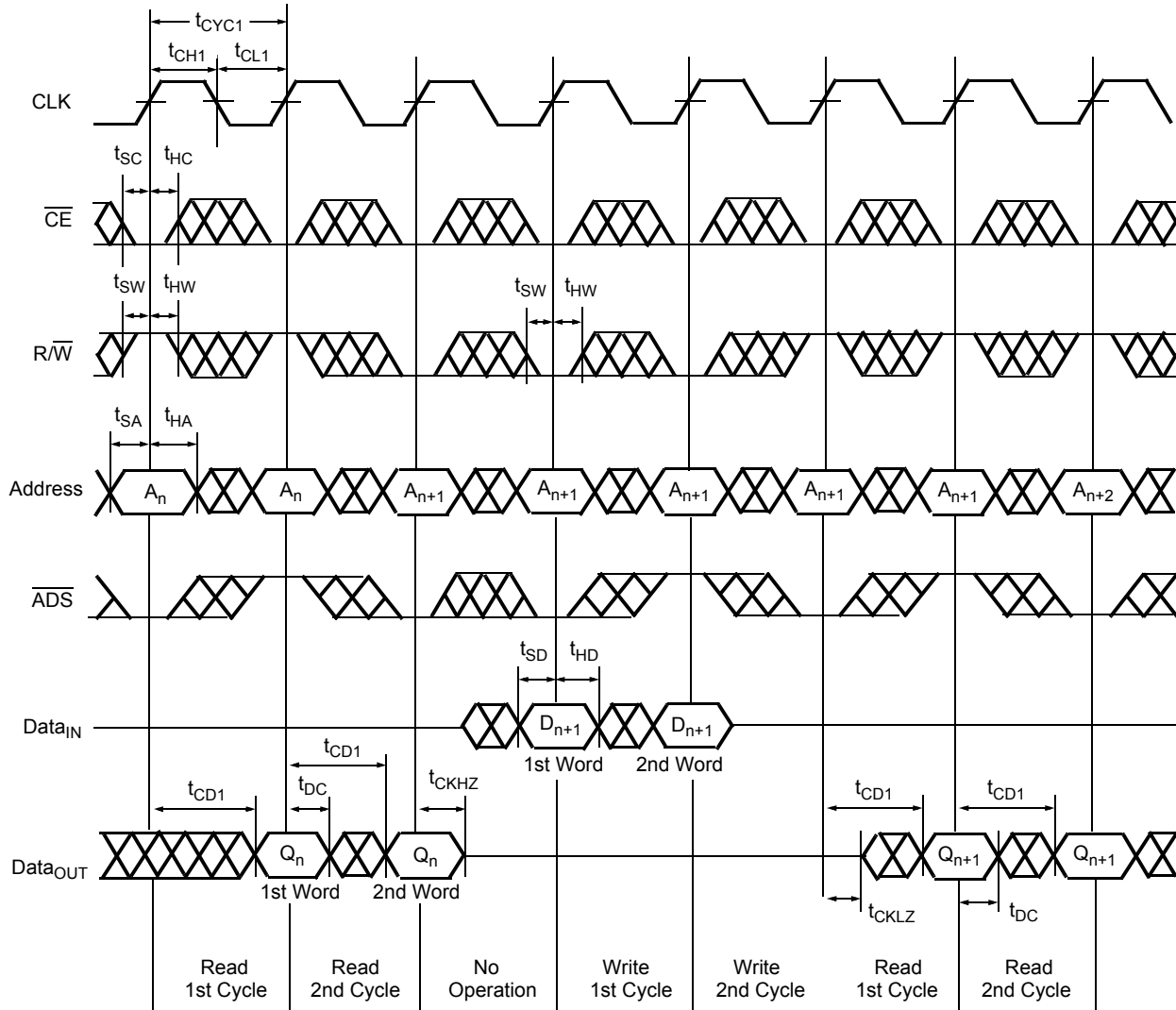


Notes

42. $\overline{ADS} = V_{IL}$, $\overline{CNTEN} = V_{IL}$, and $\overline{CNTRST} = V_{IH}$.
43. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK. Numbers are for reference only.
44. Timing shown is for x18 bus matching; x9 bus matching is similar with 4 cycles between address inputs.
45. See table "Right Port Operation" for data output on first and subsequent cycles.
46. $\overline{CE} = \overline{ADS} = \overline{CNTEN} = V_{IL}$; $\overline{CNTRST} = V_{IH}$.
47. During "No Operation," data in memory at the selected address may be corrupted and should be rewritten to ensure data integrity.
48. Output state (HIGH, LOW, or High-Impedance) is determined by the previous cycle control signals.

Switching Waveforms (continued)

Figure 15. Bus Match Flow-Through Read-to-Write-to-Read ($\overline{OE} = V_{IL}$) [49, 50, 51, 52, 53, 54, 55]



Notes

49. Test conditions used are Load 2.

50. Timing shown is for x 18 bus matching; x 9 bus matching is similar with 4 cycles between address inputs.

51. See table "Right Port Operation" for data output on first and subsequent cycles.

52. $\text{CNTEN} = V_{IL}$. In x9 and x18 Bus Matching Burst Mode operations (Write or Read), $\overline{ADS}$ can toggle on the rising edge of every clock cycle or it can be at V_{IH} level all the time except when loading the initial external address (i.e. $\text{ADS} = V_{IL}$ only required when reading or writing the first Byte or Word).

53. $\overline{CE} = \overline{ADS} = \text{CNTEN} = V_{IL}$; $\text{CNTRST} = V_{IH}$.

54. During "No Operation," data in memory at the selected address may be corrupted and should be rewritten to ensure data integrity.

55. BM, SIZE, and BE must be reconfigured 1 cycle before operation is guaranteed. BM, SIZE, and BE should remain static for any particular port configuration.

Switching Waveforms (continued)

Figure 16. Pipelined Read with Address Counter Advance ^[56]

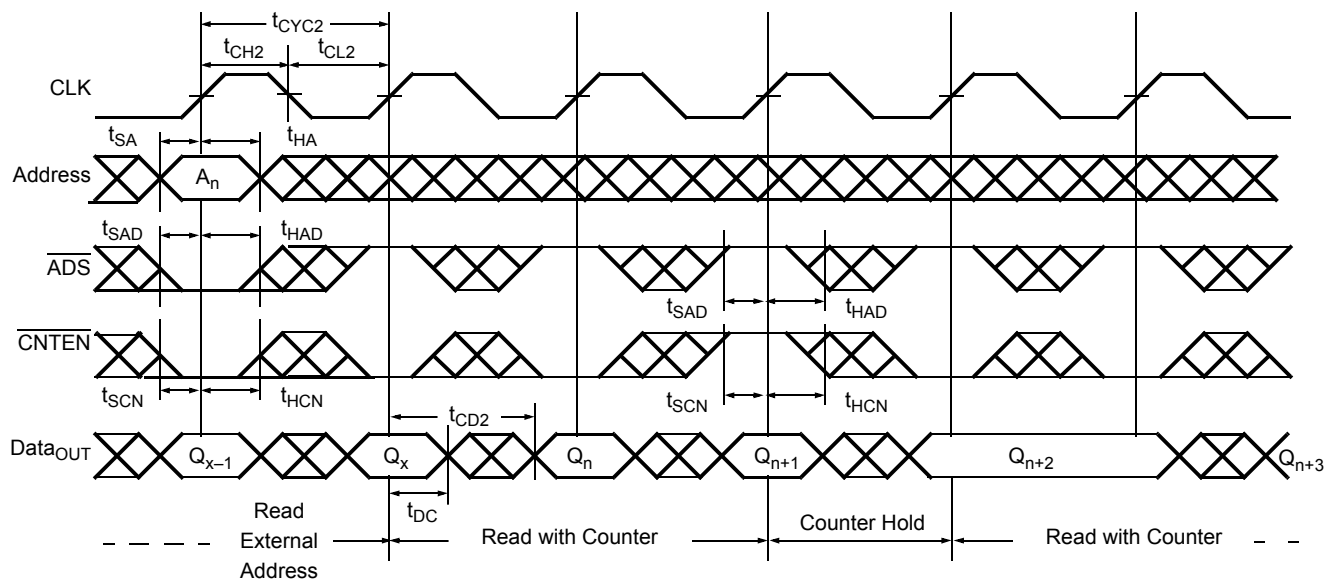
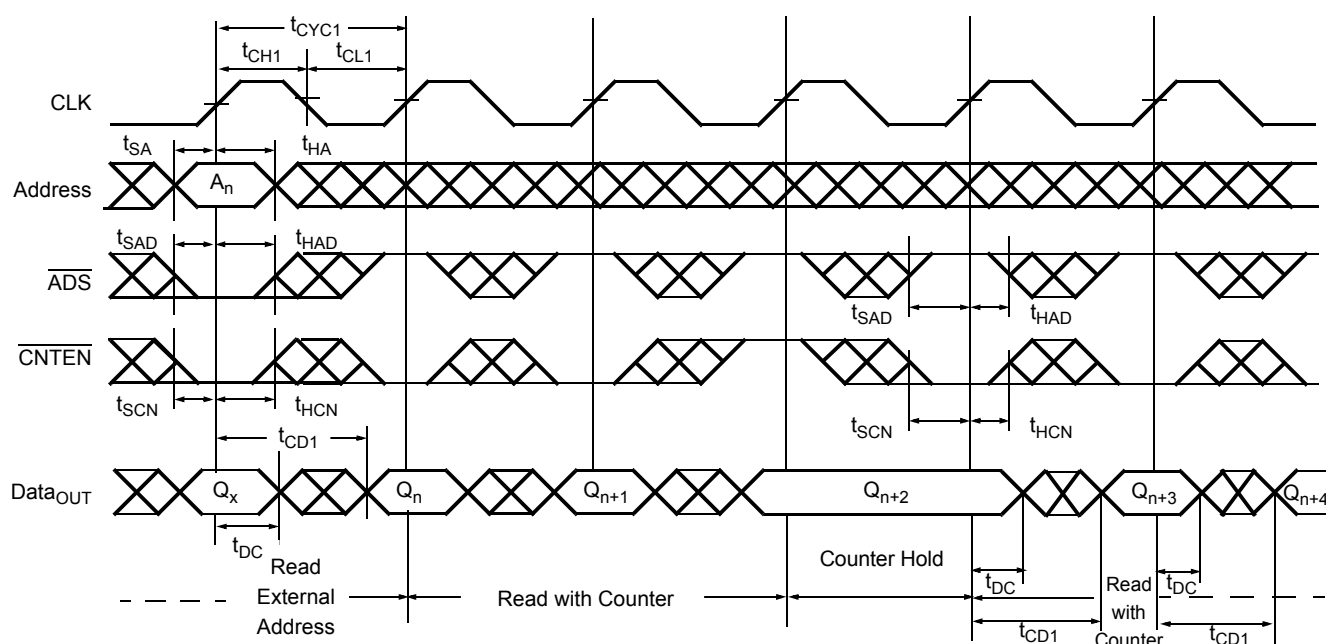


Figure 17. Flow-Through Read with Address Counter Advance ^[56]

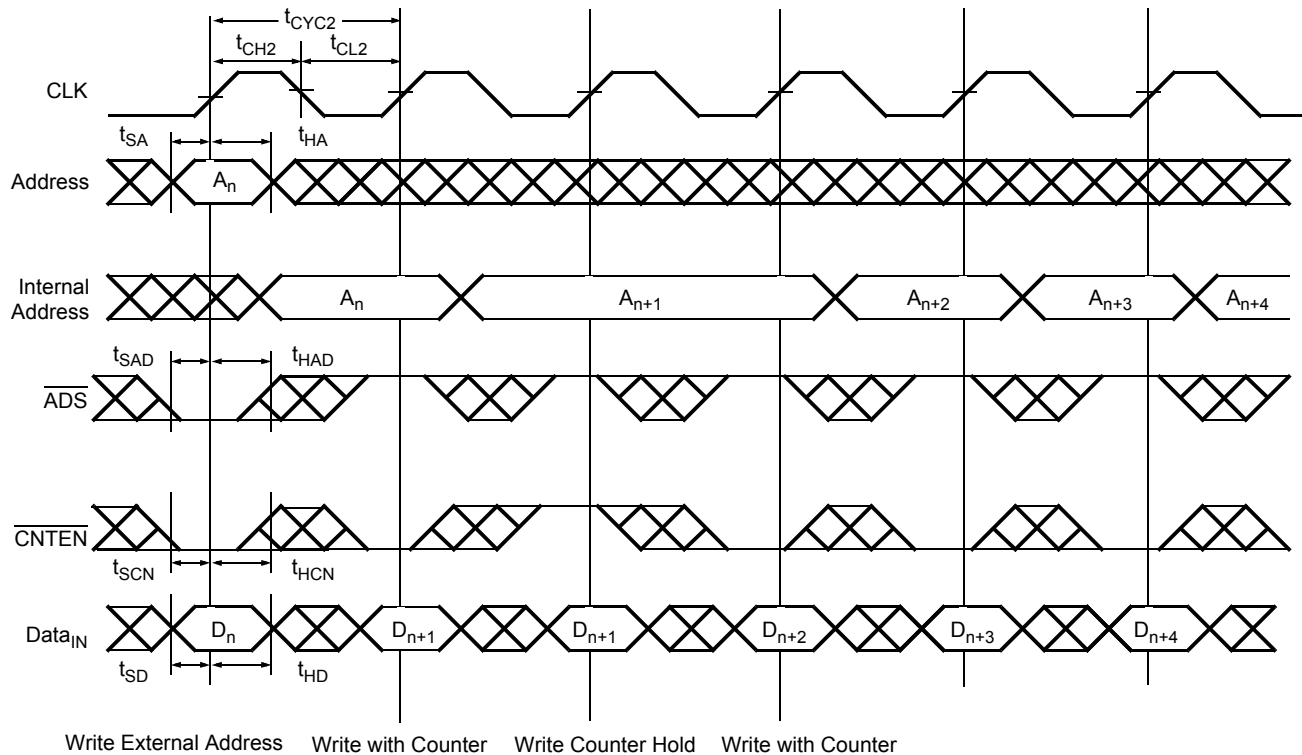


Note

56. $\overline{CE} = \overline{OE} = V_{IL}$; $R/\overline{W} = \overline{CNTRST} = V_{IH}$.

Switching Waveforms (continued)

Figure 18. Write with Address Counter Advance (Flow-Through or Pipelined Outputs) [57, 58]



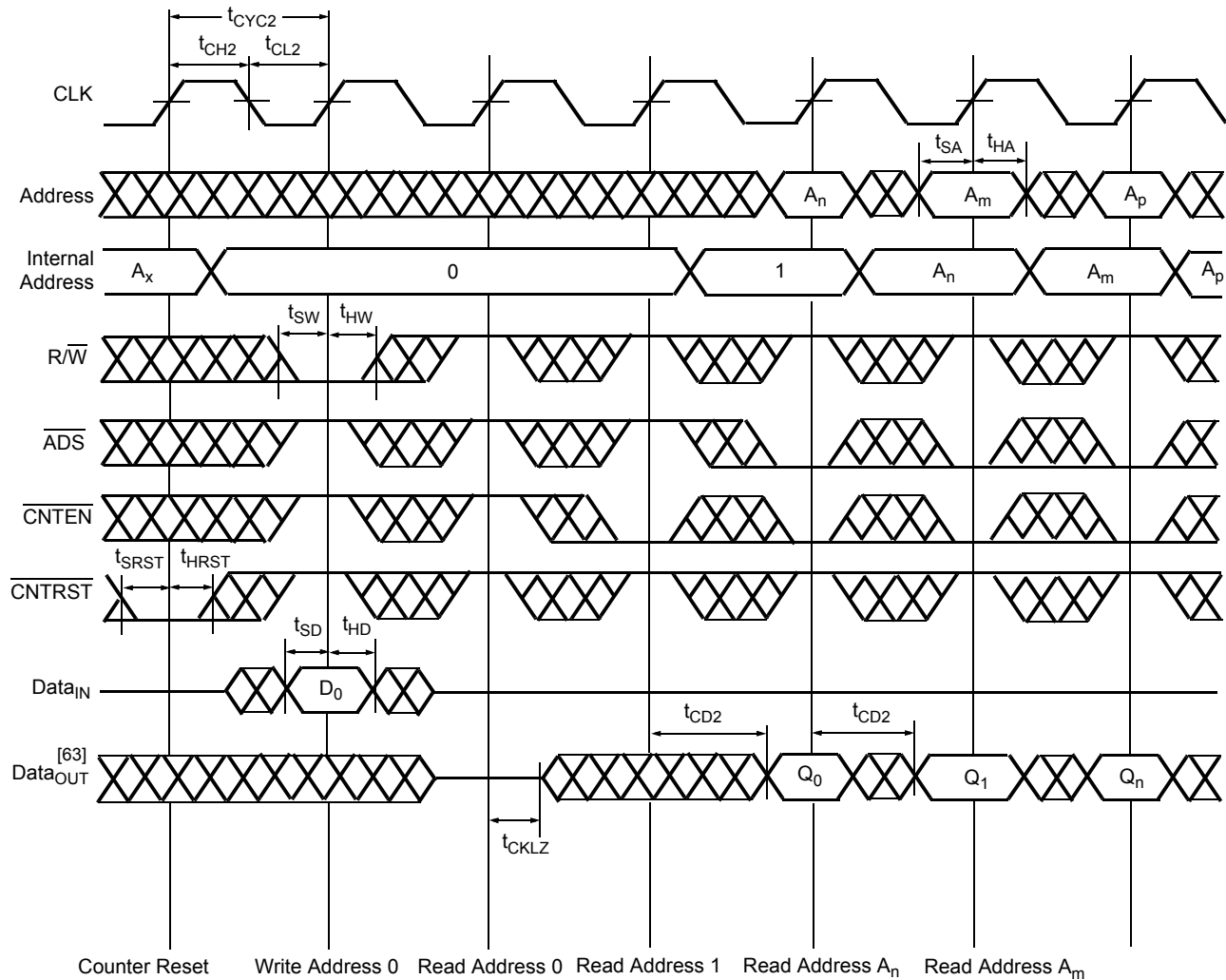
Notes

57. $\overline{CE} = \overline{B0} = \overline{B1} = \overline{B2} = \overline{B3} = R/\overline{W} = V_{IL}$; $\overline{CNTNST} = V_{IH}$.

58. The "Internal Address" is equal to the "External Address" when $\overline{ADS} = \overline{CNTEN} = V_{IL}$ and $\overline{CNTNST} = V_{IH}$.

Switching Waveforms (continued)

Figure 19. Counter Reset (Pipelined Outputs) [59, 60, 61, 62, 63]

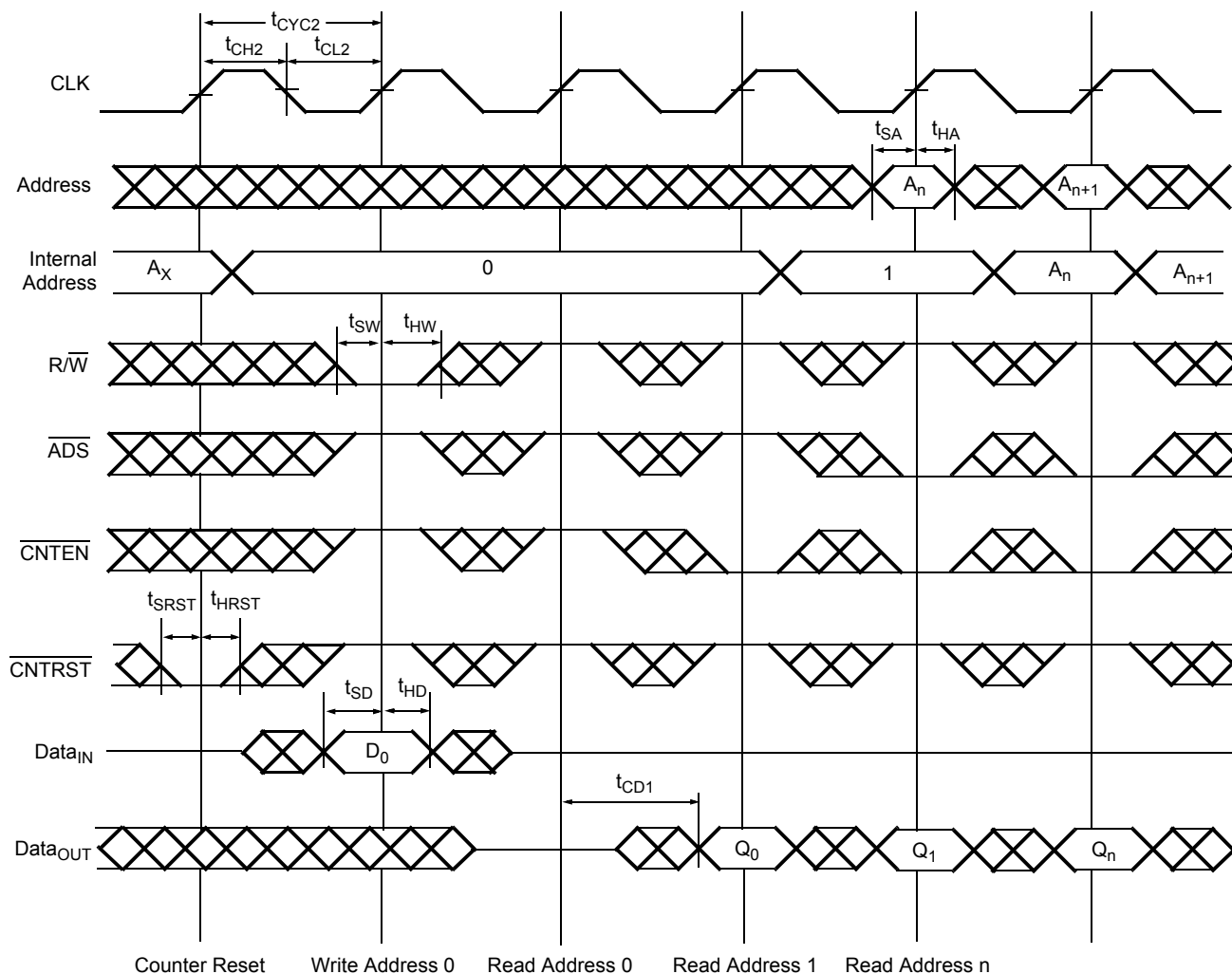


Notes

59. Test conditions used are Load 2.
60. Output state (HIGH, LOW, or High-Impedance) is determined by the previous cycle control signals.
61. $CE = B0 = B1 = B2 = B3 = V_{IL}$.
62. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset.
63. Output state (HIGH, LOW, or High-Impedance) is determined by the previous cycle control signals. Ideally, $DATA_{OUT}$ should be in the High-Impedance state during a valid WRITE cycle.

Switching Waveforms (continued)

Figure 20. Counter Reset (Flow-Through Outputs) [64, 65, 66, 67, 68]



Notes

64. Output state (HIGH, LOW, or High-Impedance) is determined by the previous cycle control signals.
65. During "No Operation," data in memory at the selected address may be corrupted and should be rewritten to ensure data integrity.
66. $CE = B0 = B1 = B2 = B3 = V_{IL}$.
67. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset.
68. Output state (HIGH, LOW, or High-Impedance) is determined by the previous cycle control signals. Ideally, $DATA_{OUT}$ should be in the High-Impedance state during a valid WRITE cycle.

Switching Waveforms (continued)

Figure 21. Pipelined Read of State of Address Counter [69, 70, 71]

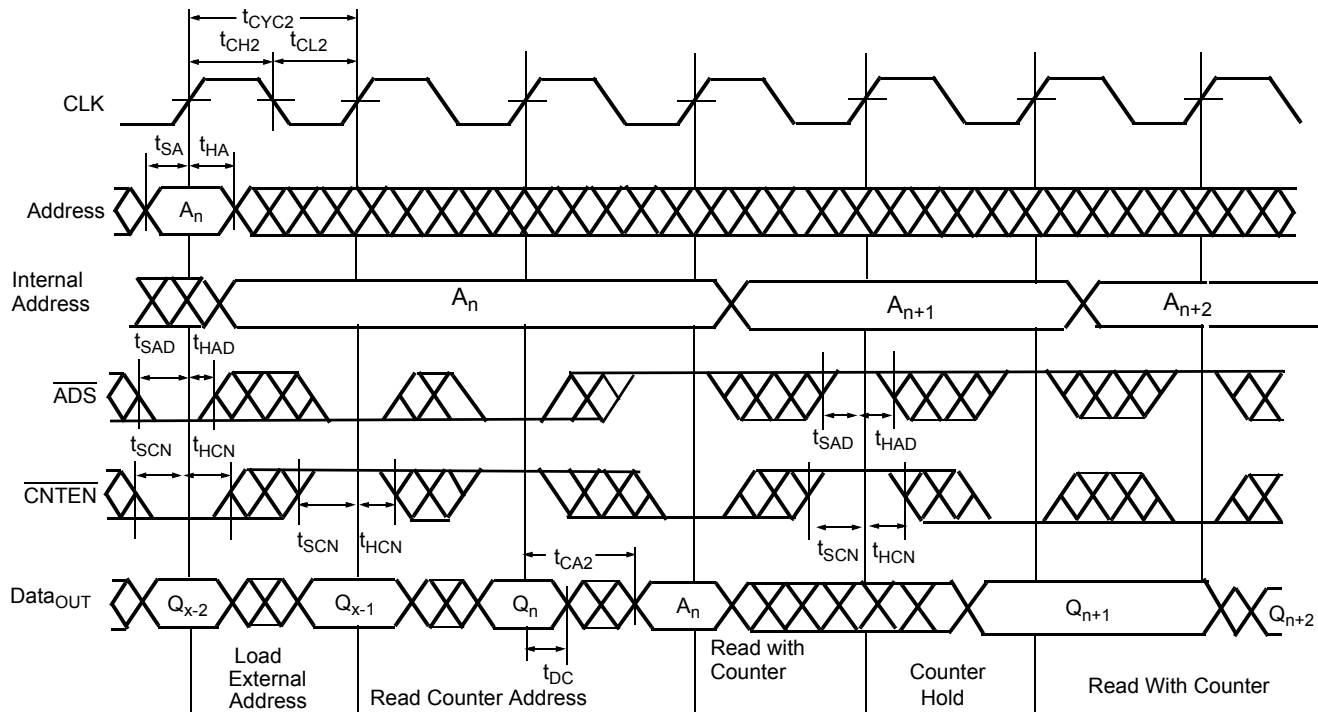
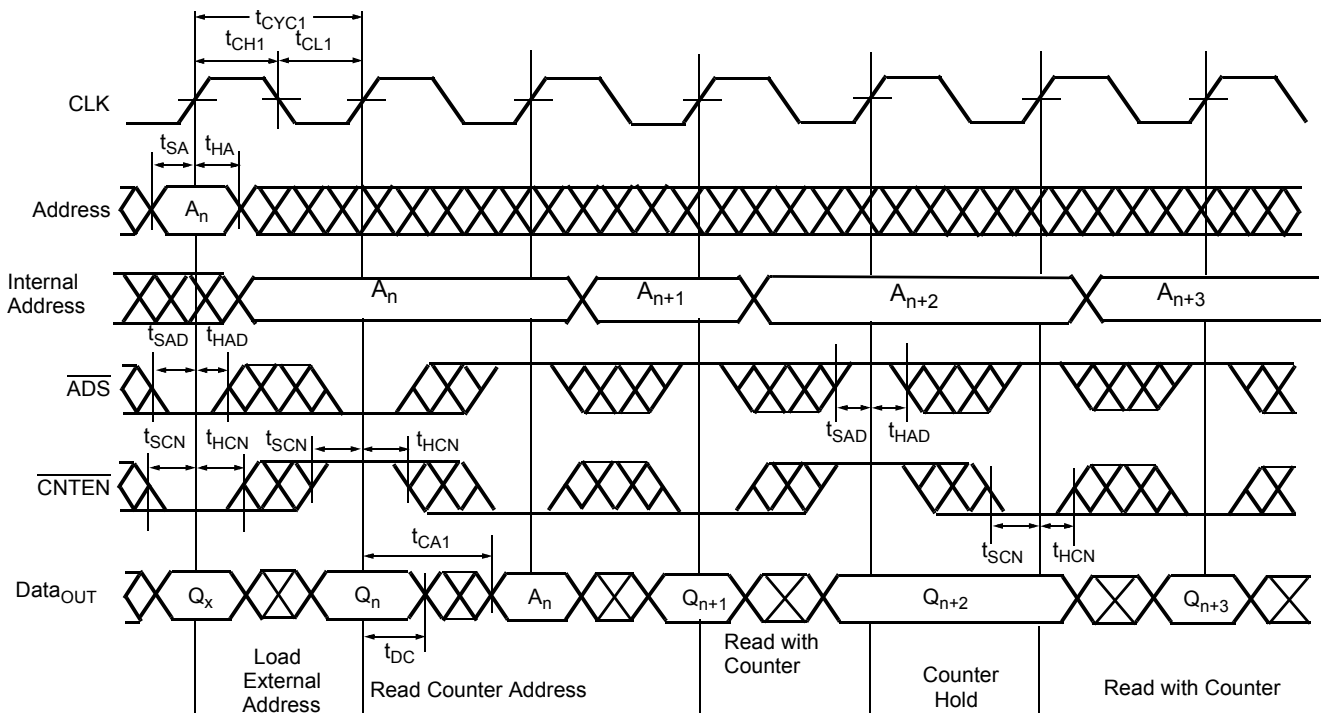


Figure 22. Flow-Through Read of State of Address Counter [69, 70, 72]



Notes

69. $\overline{CE} = \overline{OE} = V_{IL}$; $R/\overline{W} = \overline{CNT\overline{RST}} = V_{IH}$.

70. When reading ADDRESS_{OUT} in x 9 Bus Match mode, readout of A_n is extended by 1 cycle.

71. For Pipelined address counter read, signals from address counter operation table must be valid for 2 consecutive cycles for x 36 and x 18 mode and for 3 consecutive cycles for x 9 mode.

72. For flow-through address counter read, signals from address counter operation table must be valid for consecutive cycles for x 36.

Read/Write and Enable Operation

The Read/Write and Enable Operation is described as follows. [73, 74, 75]

Inputs				Outputs	Operation
OE	CLK	CE	R/W	I/O ₀ –I/O ₃₅	
X		H	X	High Z	Deselected [76]
X		L	L	D _{IN}	Write
L		L	H	D _{OUT}	Read [76]
H	X	L	X	High Z	Outputs disabled

Address Counter Control Operation

The Address Counter Control Operation is described as follows. [73, 77]

Address	Previous Address	CLK	OE	R/W	ADS	CNTEN	CNTRST	Mode	Operation
X	X		X	X	X	X	L	Reset	Counter reset
A _n	X		X	X	L	L	H	Load	Address load into counter
A _n	A _n		L	H	L	H	H	Hold + Read	External address blocked – counter address readout
X	A _n		X	X	H	H	H	Hold	External address blocked – counter disabled
X	A _n		X	X	H	L	H	Increment	Counter increment

Notes

73. "X" = "Don't Care," "H" = V_{IH}, "L" = V_{IL}.

74. ADS, CNTEN, CNTRST = "Don't Care."

75. OE is an asynchronous input signal.

76. When CE changes state in the pipelined mode, deselection and read happen in the following clock cycle.

77. Counter operation is independent of CE.

Right Port Configuration

The Right Port Configuration is described as follows. [78, 79]

BM	SIZE	Configuration	I/O Pins used
0	0	× 36	I/O _{0R–35R}
1	0	× 18	I/O _{0R–17R}
1	1	× 9	I/O _{0R–8R}

Right Port Operation

The Right Port Operation is described as follows. [80]

Configuration	BE	Data on 1st Cycle	Data on 2nd Cycle	Data on 3rd Cycle	Data on 4th Cycle
× 18	0	Q _{0R–17R}	Q _{18R–35R}	–	–
× 18	1	Q _{18R–35R}	Q _{0R–17R}	–	–
× 9	0	Q _{0R–8R}	Q _{9R–17R}	Q _{18R–26R}	Q _{27R–35R}
× 9	1	Q _{27R–35R}	Q _{18R–26R}	Q _{9R–17R}	Q _{0R–8R}

Readout of Internal Address Counter

The Readout of Internal Address Counter is described as follows. [81]

Configuration	Address on 1st Cycle	I/O Pins used on 1st Cycle	Address on 2nd Cycle	I/O Pins used on 2nd Cycle
Left Port × 36	A _{0L–14L}	I/O _{3L–17L}	–	–
Right Port × 36	A _{0R–14R}	I/O _{3R–17R}	–	–
Right Port × 18	WA, A _{0R–14R}	I/O _{2R–17R}	–	–
Right Port × 9	A _{6R–14R}	I/O _{0R–8R}	BA, WA, A _{0R–5R}	I/O _{1R–8R}

Left Port Operation

The Left Port Operation is described as follows.

Control Pin	Effect
B0	I/O _{0–8} Byte Control
B1	I/O _{9–17} Byte Control
B2	I/O _{18–26} Byte Control
B3	I/O _{27–35} Byte Control

Notes

78. BM, SIZE, and BE must be reconfigured 1 cycle before operation is guaranteed. BM, SIZE, and BE should remain static for any particular port configuration.

79. In x36 mode, BE input is a "Don't Care."

80. DQ represents data output of the chip.

81. x18 and x9 configuration apply to right port only.

Counter Operation

The CY7C09569V/CY7C09579V Dual-Port RAM (DPRAM) contains on-chip address counters (one for each port) for the synchronous members of the product family. Besides the main $\times 36$ format, the right port allows bus matching ($\times 18$ or $\times 9$, user-selectable). An internal sub-counter provides the extra addresses required to sequence out the 36-bit word in 18-bit or 9-bit increments. The sub-counter counts up in the “Little Endian” mode, and counts down if the user has chosen the “Big Endian” mode. The address counter is required to be in increment mode in order for the sub-counter to sequence out the second word (in $\times 18$ mode) or the remaining three bytes (in $\times 9$ mode).

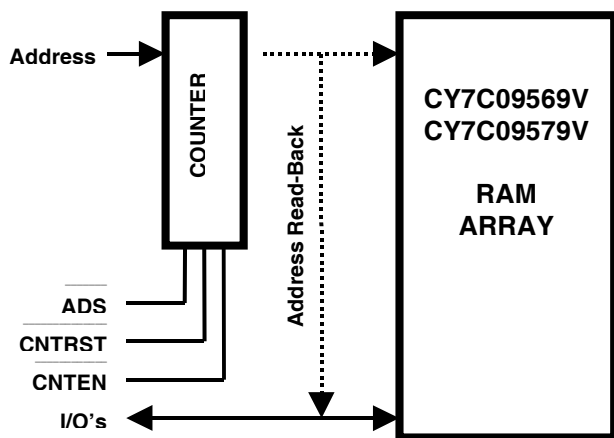
For a $\times 36$ format (the only active format on the left port), each address counter in the CY7C09579V uses addresses (A_{0-14}).

For the right port (allowing for the bus-matching feature), a maximum of two address bits (out of a 2-bit sub-counter) are added.

1. $\overline{ADS}_{L/R}$ (pin #23/86) is a port's address strobe, allowing the loading of that port's burst counters if the corresponding $\overline{CNTEN}_{L/R}$ pin is active as well.
2. $\overline{CNTEN}_{L/R}$ (pin #25/84) is a port's count enable, provided to stall the operation of the address input and utilize the internal address generated by the internal counter for fast interleaved memory applications; when asserted, the address counter will increment on each positive transition of that port's clock signal.
3. $\overline{CNTRST}_{L/R}$ (pin #24/85) is a port's burst counter reset.

A new read-back (Hold+Read Mode) feature has been added, which is different between the left and right port due to the bus matching feature provided only for the right port. In read-back mode the internal address of the counter will be read from the data I/Os as shown in Figure 23.

Figure 23. Counter Operation Diagram



Bus Match Operation

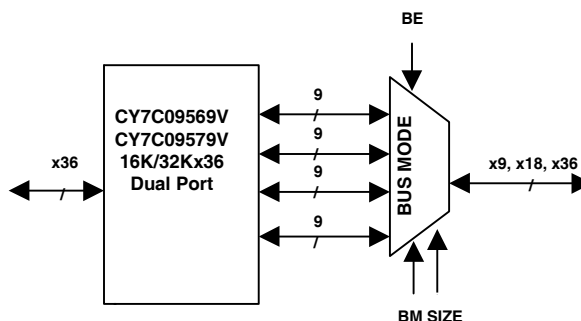
The right port of the CY7C09569V/CY7C09579V 16 K / 32 K $\times$ 36 dual-port SRAM can be configured in a 36-bit

Note

82. Even though a logic level applied to a “Don't Care” input will not change the logical operation of the dual-port, inputs that are temporarily a “Don't Care” (along with unused inputs) must not be allowed to float. They must be forced either HIGH or LOW.

long-word, 18-bit word, or 9-bit byte format for data I/O. The data lines are divided into four lanes, each consisting of 9 bits (byte-size data lines).

Figure 24. Bus Match Operation Diagram



The Bus Match Select (BM) pin works with Bus Size Select (SIZE) and Big Endian Select (BE) to select the bus width (long-word, word, or byte) and data sequencing arrangement for the right port of the dual-port device. A logic LOW applied to both the Bus Match Select (BM) pin and to the Bus Size Select (SIZE) pin will select long-word (36-bit) operation. A logic HIGH level applied to the Bus Match Select (BM) pin will enable whether byte or word bus width operation on the right port I/Os depending on the logic level applied to the SIZE pin. The level of Bus Match Select (BM) must be static throughout normal device operation.

The Bus Size Select (SIZE) pin selects either a byte or word data arrangement on the right port when the Bus Match Select (BM) pin is HIGH. A logic HIGH on the SIZE pin when the BM pin is HIGH selects a byte bus (9-bit) data arrangement. A logic LOW on the SIZE pin when the BM pin is HIGH selects a word bus (18-bit) data arrangement. The level of the Bus Size Select (SIZE) must also be static throughout normal device operation.

The Big Endian Select (BE) pin is a multiple-function pin during word or byte bus selection ($BM = 1$). BE is used in Big Endian Select mode to determine the order by which bytes (or words) of data are transferred through the right data port. A logic LOW on the BE pin will select Little Endian data sequencing arrangement and a logic HIGH on the BE pin will select a Big Endian data sequencing arrangement. Under these circumstances, the level on the BE pin should be static throughout dual-port operation.

Long-Word (36-bit) Operation

Bus Match Select (BM) and Bus Size Select (SIZE) set to a logic LOW will enable standard cycle long-word (36-bit) operation. In this mode, the right port's I/O operates essentially in an identical fashion to the left port of the dual-port SRAM. However no Byte Select control is available. All 36 bits of the long-word are shifted into and out of the right port's I/O buffer stages. All read and write timing parameters may be identical with respect to the two data ports. When the right port is configured for a long-word size, Big-Endian Select (BE) pin has no application and their inputs are “Don't Care”^[82] for the external user.

Word (18-bit) Operation

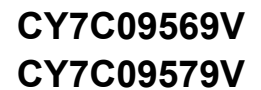
Word (18-bit) bus sizing operation is enabled when Bus Match Select (BM) is set to a logic HIGH and the Bus Size Select (SIZE) pin is set to a logic LOW. In this mode, 18 bits of data are ported through I/O_{0R–17R}. The level applied to the Big Endian (BE) pin determines the right port data I/O sequencing order (Big Endian or Little Endian).

During word (18-bit) bus size operation, a logic LOW applied to the BE pin will select Little Endian operation. In this case, the least significant data word is read from the right port first or written to the right port first. A logic HIGH on the BE pin during word (18-bit) bus size operation will select Big Endian operation resulting in the most significant data word being transferred through the right port first. Internally, the data will be stored in the appropriate 36-bit LSB or MSB I/O memory location. Device operation requires a minimum of two clock cycles to read or write during word (18-bit) bus size operation. An internal sub-counter automatically increments the right port multiplexer control when Little or Big Endian operation is in effect.

Byte (9-bit) Operation

Byte (9-bit) bus sizing operation is enabled when Bus Match Select (BM) is set to a logic HIGH and the Bus Size Select (SIZE) pin is set to a logic HIGH. In this mode, 9 bits of data are ported through I/O_{0R–8R}.

Big Endian and Little Endian data sequencing is available for dual-port operation. The level applied to the Big Endian pin (BE) under these circumstances will determine the right port data I/O sequencing order (Big or Little Endian). A logic LOW applied to the BE pin during byte (9-bit) bus size operation will select Little Endian operation. In this case, the least significant data byte is read from the right port first or written to the right port first. A logic HIGH on the BE pin during byte (9-bit) bus size operation will select Big Endian operation resulting in the most significant data word to be transferred through the right port first. Internally, the data will be stored in the appropriate 36-bit LSB or MSB I/O memory location. Device operation requires a minimum of four clock cycles to read or write during byte (9-bit) bus size operation. An internal sub-counter automatically increments the right port multiplexer control when Little or Big Endian operation is in effect. When transferring data in byte (9-bit) bus match format, the unused I/O pins (I/O_{9R–35R}) are three-stated.



16 K × 36 3.3 V Synchronous Dual-Port SRAM

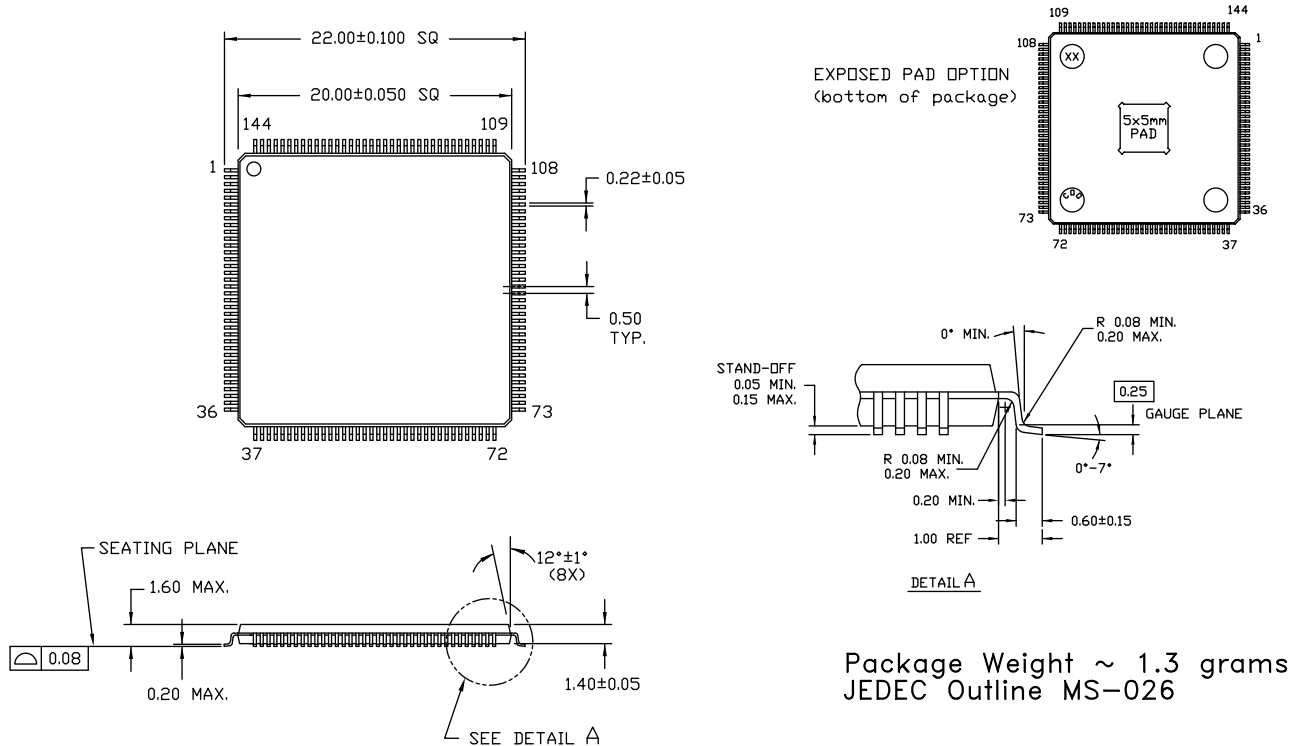
32K × 36 3.3 V Synchronous Dual-Port SRAM

Ordering Code Definitions



Package Diagrams

Figure 25. 144-pin TQFP (20 × 20 × 1.4 mm) A144SA Package Outline, 51-85047

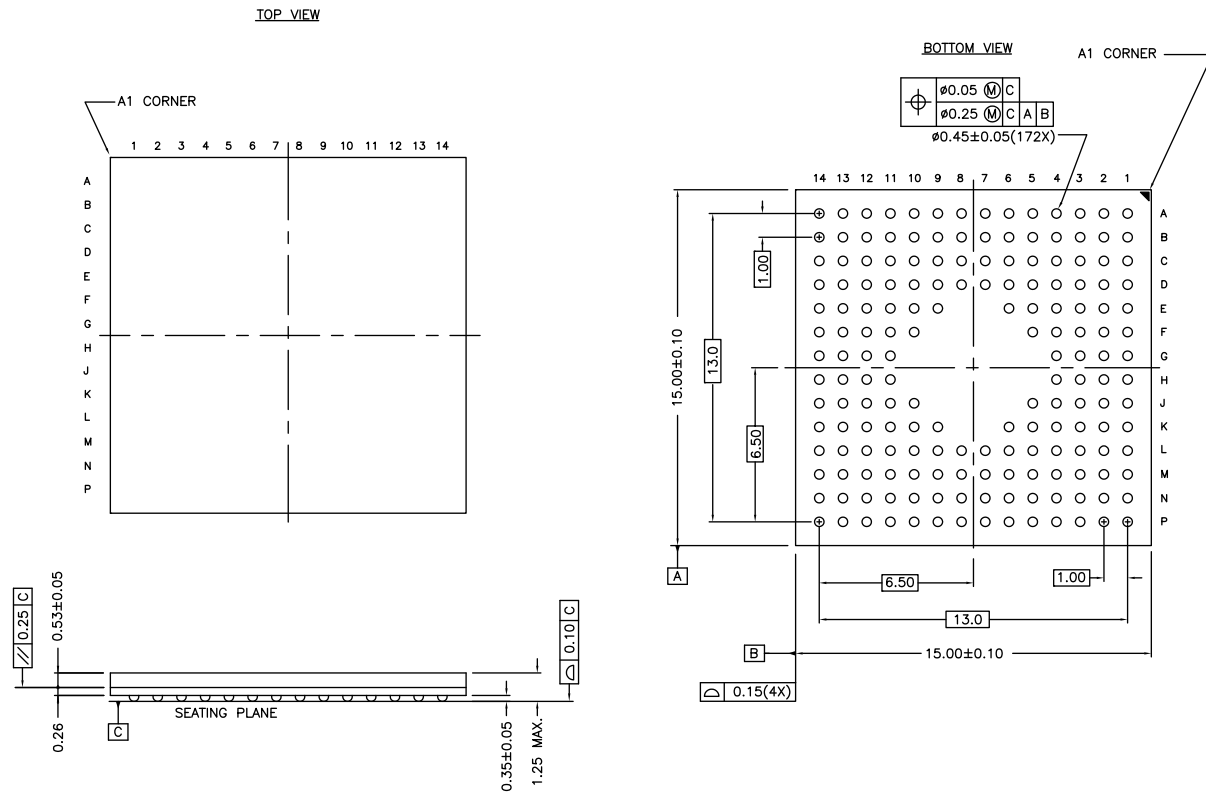


⟨DIMENSIONS ARE IN MILLIMETERS⟩

51-85047 *D

Package Diagrams *(continued)*

Figure 26. 172-ball FBGA (15 × 15 × 1.25 mm) BB172 Package Outline, 51-85114



51-85114 *D

Acronyms

Acronym	Description
ADS	address strobe
BGA	ball grid array
$\overline{\text{CE}}$	chip enable
CMOS	complementary metal oxide semiconductor
$\overline{\text{CNTEN}}$	count enable
$\overline{\text{CNTRST}}$	counter reset
I/O	input/output
LSB	least significant bit
MSB	most significant bit
$\overline{\text{OE}}$	output enable
SRAM	static random access memory
TQFP	thin quad flat pack
TTL	transistor-transistor logic

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
mA	milliampere
mm	millimeter
ns	nanosecond
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C09569V/CY7C09579V, 3.3 V 16 K / 32 K × 36 FLEx36® Synchronous Dual-Port Static RAM Document Number: 38-06054				
Rev.	ECN	Orig. of Change	Submission Date	Description of Change
**	110213	SZV	12/16/01	Change from Spec number: 38-00743 to 38-06054
*A	122304	RBI	12/27/02	Updated Maximum Ratings (Added Power up requirements to Maximum Ratings Information).
*B	349775	RUY	See ECN	Updated Ordering Information (Added Pb-free Information).
*C	2897215	RAME	03/22/10	Updated Ordering Information (Removed inactive parts). Updated Package Diagrams .
*D	3110406	ADMU	12/14/10	Added Ordering Code Definitions . Minor edits and updated in new template.
*E	3162642	ADMU	02/04/11	Updated Selection Guide (Removed speed bin -67 related information). Updated Operating Range (Removed Industrial Temperature Range information). Updated Electrical Characteristics (Removed speed bin -67 related information). Updated Switching Characteristics (Removed speed bin -67 related information). Added Acronyms and Units of Measure .
*F	3352391	ADMU	08/23/11	Updated Package Diagrams (Spec 51-85047 (Changed revision from *C to *D)).
*G	3702863	SMCH	08/20/2012	Updated Logic Block Diagram (Aligned all the objects correctly). Updated Switching Waveforms (Updated Figure 18 (Aligned the naming of objects correctly), updated Figure 19 (Aligned the naming of objects correctly), updated Figure 20 (Aligned the naming of objects correctly)). Updated Right Port Operation (Updated the columns Data on 1st Cycle, Data on 2nd Cycle, Data on 3rd Cycle and Data on 4th Cycle). Updated Bus Match Operation (Updated Byte (9-bit) Operation (description)). Updated Package Diagrams (Spec 51-85114 (Changed revision from *C to *D)). Replaced Logic '0' with Logic LOW and replaced Logic '1' with Logic HIGH across the document.

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