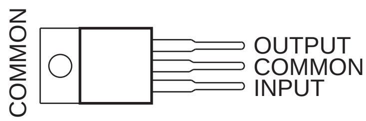
TL780 SERIES POSITIVE-VOLTAGE REGULATORS

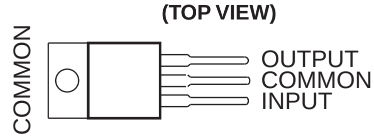
FEATURES

- **±1% Output Tolerance at 25°C**
- **±2% Output Tolerance Over Full Operating Range**
- **Thermal Shutdown**
- **Internal Short-Circuit Current Limiting**
- **Pinout Identical to μA7800 Series**
- **Improved Version of μA7800 Series**

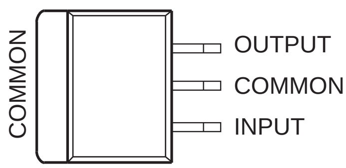
KC (TO-220) PACKAGE (TOP VIEW)



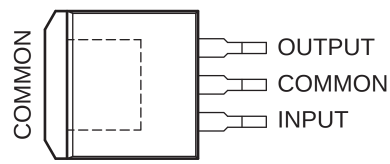
KCS (TO-220) PACKAGE (TOP VIEW)



KTE PACKAGE (TOP VIEW)



KTT (TO-263) PACKAGE (TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

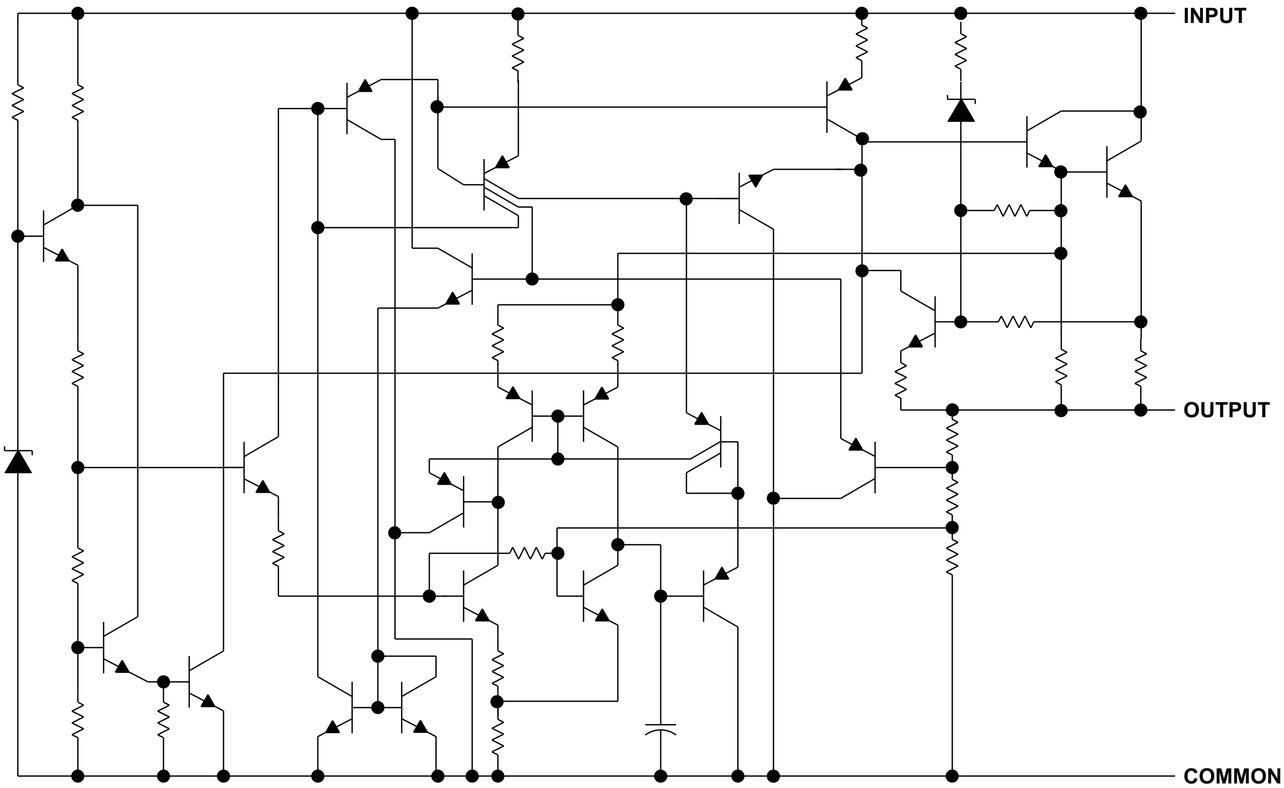
Each fixed-voltage precision regulator in the TL780 series is capable of supplying 1.5 A of load current. A unique temperature-compensation technique, coupled with an internally trimmed band-gap reference, has resulted in improved accuracy when compared to other three-terminal regulators. Advanced layout techniques provide excellent line, load, and thermal regulation. The internal current-limiting and thermal-shutdown features essentially make the devices immune to overload.

ORDERING INFORMATION

T_J	V_O TYP (V)	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 125°C	5	PowerFLEX™ – KTE	Reel of 2000	TL780-05CKTER	TL780-05C
		TO-220 – KC	Tube of 50	TL780-05CKC	TL780-05C
		TO-220, short shoulder – KCS	Tube of 20	TL780-05KCS	TL780-05
		TO-263 – KTT	Reel of 500	TL780-05CKTTR	TL780-05C
	12	TO-220 – KC	Tube of 50	TL780-12CKC	TL780-12C
		TO-220, short shoulder – KCS	Tube of 20	TL780-12KCS	TL780-12
	15	TO-220 – KC	Tube of 50	TL780-15CKC	TL780-15C
		TO-220, short shoulder – KCS	Tube of 20	TL780-15KCS	TL780-15

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

SCHEMATIC



Absolute Maximum Ratings[1]

over operating temperature ranges (unless otherwise noted)

		MIN	MAX	UNIT
V_I	Input voltage		35	V
T_J	Operating virtual junction temperature		150	°C
	Lead temperature 1,6 mm (1/16 in) from case for 10 s		260	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Package Thermal Data[1]

PACKAGE	BOARD	θ_{JP} [2]	θ_{JC}	θ_{JA}
PowerFLEX (KTE)	High K, JESD 51-5	2.7°C/W	11.6°C/W	23.3°C/W
TO-220 (KC/KCS)	High K, JESD 51-5	3°C/W	17°C/W	19°C/W
TO-263 (KTT)	High K, JESD 51-5	1.91°C/W	18°C/W	25.3°C/W

(1) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.
(2) For packages with exposed thermal pads, such as QFN, PowerPAD™, or PowerFLEX, θ_{JP} is defined as the thermal resistance between the die junction and the bottom of the exposed pad.

Recommended Operating Conditions

			MIN	MAX	UNIT
V_I	Input voltage	TL780-05C	7	25	V
		TL780-12C	14.5	30	
		TL780-15C	17.5	30	
I_O	Output current			1.5	A
T_J	Operating virtual junction temperature		0	125	°C

Electrical Characteristics

at specified virtual junction temperature, V_I = 10 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J (1)	TL780-05C MIN	TL780-05C TYP	TL780-05C MAX	UNIT
Output voltage	I_O = 5 mA to 1 A, P ≤ 15 W, V_I = 7 V to 20 V	25°C	4.95	5	5.05	V
		0°C to 125°C	4.9		5.1	
Input voltage regulation	V_I = 7 V to 25 V	25°C		0.5	5	mV
	V_I = 8 V to 12 V			0.5	5	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz	0°C to 125°C	70	85		dB
Output voltage regulation	I_O = 5 mA to 1.5 A	25°C		4	25	mV
	I_O = 250 mA to 750 mA			1.5	15	
Output resistance	f = 1 kHz	0°C to 125°C		0.0035		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		0.25		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		75		µV
Dropout voltage	I_O = 1 A	25°C		2		V
Input bias current		25°C		5	8	mA
Input bias-current change	V_I = 7 V to 25 V	0°C to 125°C		0.7	1.3	mA
	I_O = 5 mA to 1 A			0.003	0.5	
Short-circuit output current		25°C		750		mA
Peak output current		25°C		2.2		A

(1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.22-µF capacitor across the output.

Electrical Characteristics

at specified virtual junction temperature, V_I = 19 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J (1)	TL780-12C MIN	TL780-12C TYP	TL780-12C MAX	UNIT
Output voltage	I_O = 5 mA to 1 A, P ≤ 15 W, V_I = 14.5 V to 27 V	25°C	11.88	12	12.12	V
		0°C to 125°C	11.76		12.24	
Input voltage regulation	V_I = 14.5 V to 30 V	25°C		1.2	12	mV
	V_I = 16 V to 22 V			1.2	12	
Ripple rejection	V_I = 15 V to 25 V, f = 120 Hz	0°C to 125°C	65	80		dB
Output voltage regulation	I_O = 5 mA to 1.5 A	25°C		6.5	60	mV
	I_O = 250 mA to 750 mA			2.5	36	
Output resistance	f = 1 kHz	0°C to 125°C		0.0035		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		0.6		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		180		µV
Dropout voltage	I_O = 1 A	25°C		2		V
Input bias current		25°C		5.5	8	mA
Input bias-current change	V_I = 14.5 V to 30 V	0°C to 125°C		0.4	1.3	mA
	I_O = 5 mA to 1 A			0.03	0.5	
Short-circuit output current		25°C		350		mA
Peak output current		25°C		2.2		A

(1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.22-µF capacitor across the output.

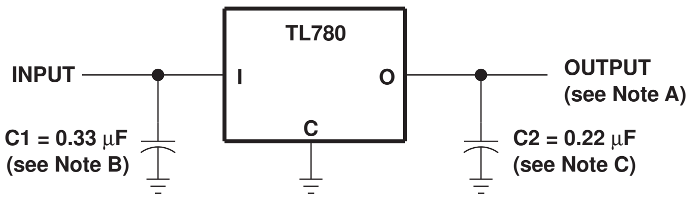
Electrical Characteristics

at specified virtual junction temperature, V_I = 23 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J (1)	TL780-15C MIN	TL780-15C TYP	TL780-15C MAX	UNIT
Output voltage	I_O = 5 mA to 1 A, P ≤ 15 W, V_I = 17.5 V to 30 V	25°C	14.85	15	15.15	V
		0°C to 125°C	14.7		15.3	
Input voltage regulation	V_I = 17.5 V to 30 V	25°C		1.5	15	mV
	V_I = 20 V to 26 V			1.5	15	
Ripple rejection	V_I = 18.5 V to 28.5 V, f = 120 Hz	0°C to 125°C	60	75		dB
Output voltage regulation	I_O = 5 mA to 1.5 A	25°C		7	75	mV
	I_O = 250 mA to 750 mA			2.5	45	
Output resistance	f = 1 kHz	0°C to 125°C		0.0035		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		0.62		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		225		µV
Dropout voltage	I_O = 1 A	25°C		2		V
Input bias current		25°C		5.5	8	mA
Input bias-current change	V_I = 17.5 V to 30 V	0°C to 125°C		0.4	1.3	mA
	I_O = 5 mA to 1 A			0.02	0.5	
Short-circuit output current		25°C		230		mA
Peak output current		25°C		2.2		A

(1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.22-µF capacitor across the output.

PARAMETER MEASUREMENT INFORMATION



A. Permanent damage can occur when OUTPUT is pulled below ground.

B. C1 is required when the regulator is far from the power-supply filter.

C. C2 is not required for stability; however, transient response is improved.

Figure 1. Test Circuit

APPLICATION INFORMATION

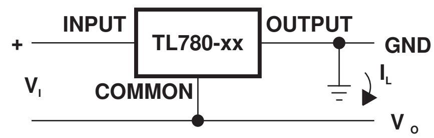
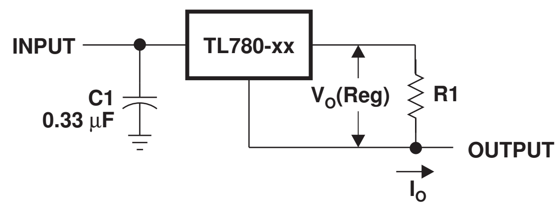


Figure 2. Positive Regulator in Negative Configuration (V_I Must Float)



I_O = (V_O/R1) + I_O Bias Current

Figure 3. Current Regulator

Operation With a Load Common to a Voltage of Opposite Polarity

In many cases, a regulator powers a load that is not connected to ground, but instead, is connected to a voltage source of opposite polarity (e.g., operational amplifiers, level-shifting circuits, etc.). In these cases, a clamp diode should be connected to the regulator output as shown in Figure 4. This protects the regulator from output polarity reversals during startup and short-circuit operation.

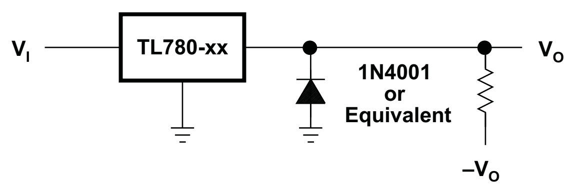


Figure 4. Output Polarity-Reversal-Protection Circuit

Reverse-Bias Protection

Occasionally, the input voltage to the regulator can collapse faster than the output voltage. This, for example, could occur when the input supply is crowbarred during an output overvoltage condition. If the output voltage is greater than approximately 7 V, the emitter-base junction of the series pass element (internal or external) could break down and be damaged. To prevent this, a diode shunt can be employed, as shown in Figure 5.

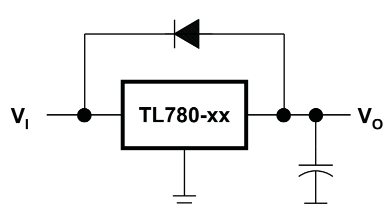


Figure 5. Reverse-Bias-Protection Circuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL780-05CKTTR	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 125	TL780-05C	Samples
TL780-05CKTTRG3	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 125	TL780-05C	Samples
TL780-05KCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	TL780-05	Samples
TL780-05KCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	TL780-05	Samples
TL780-12KCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	TL780-12	Samples
TL780-12KCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	TL780-12	Samples
TL780-15KCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	TL780-15	Samples
TL780-15KCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	TL780-15	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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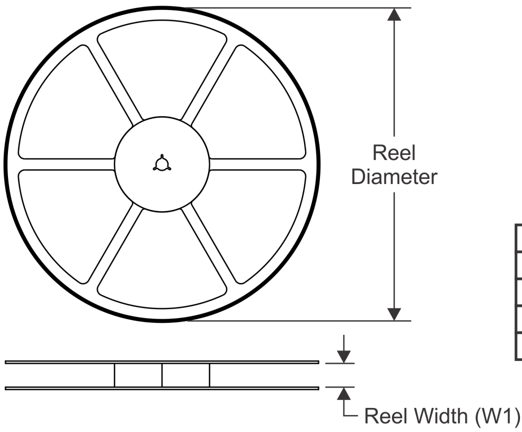
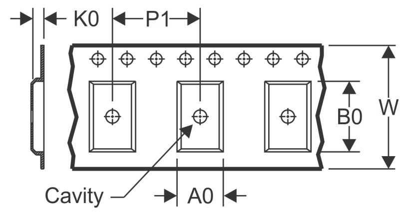
TAPE AND REEL INFORMATION

REEL DIMENSIONS

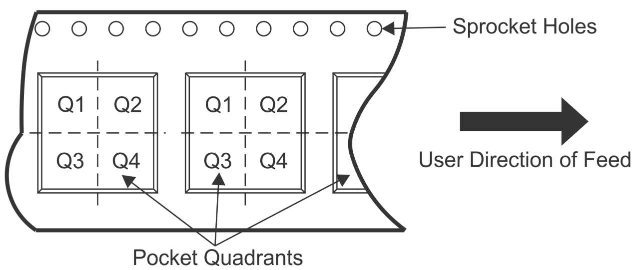


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

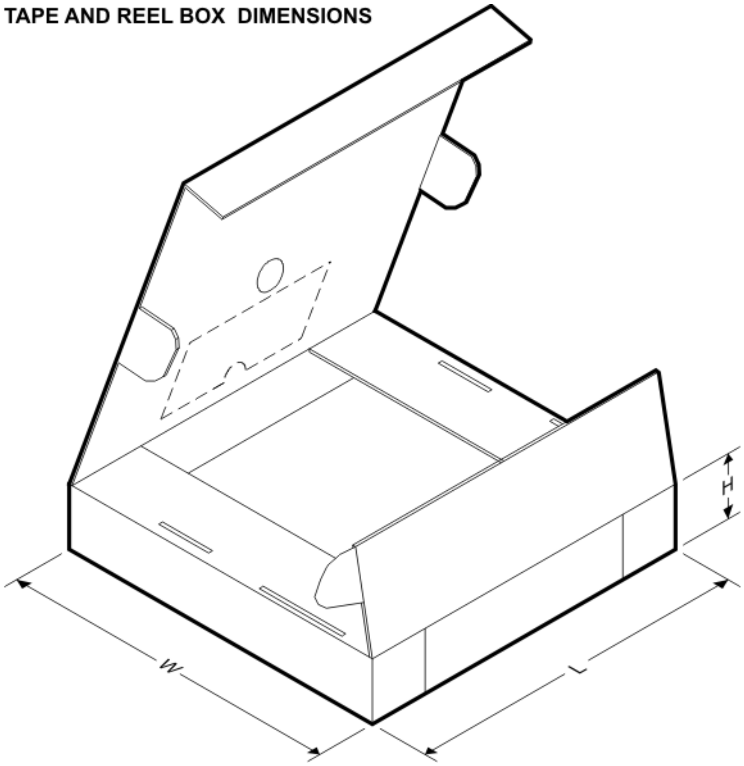
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

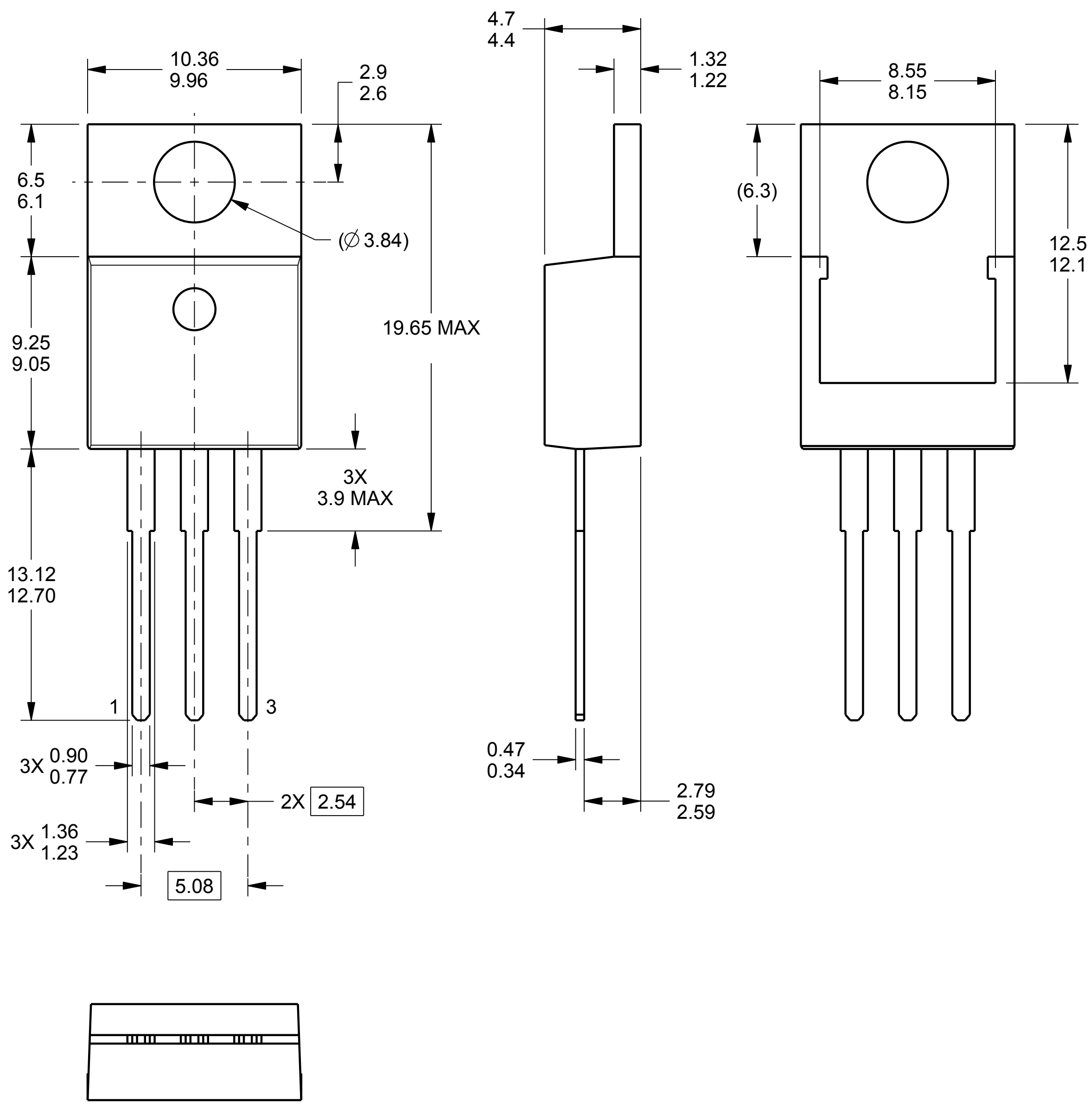
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL780-05CKTTR	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL780-05CKTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0



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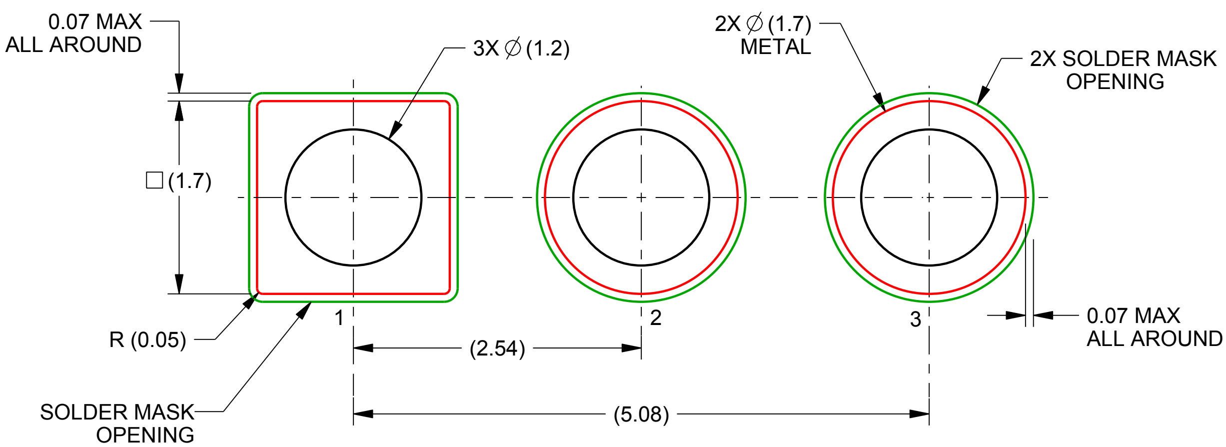
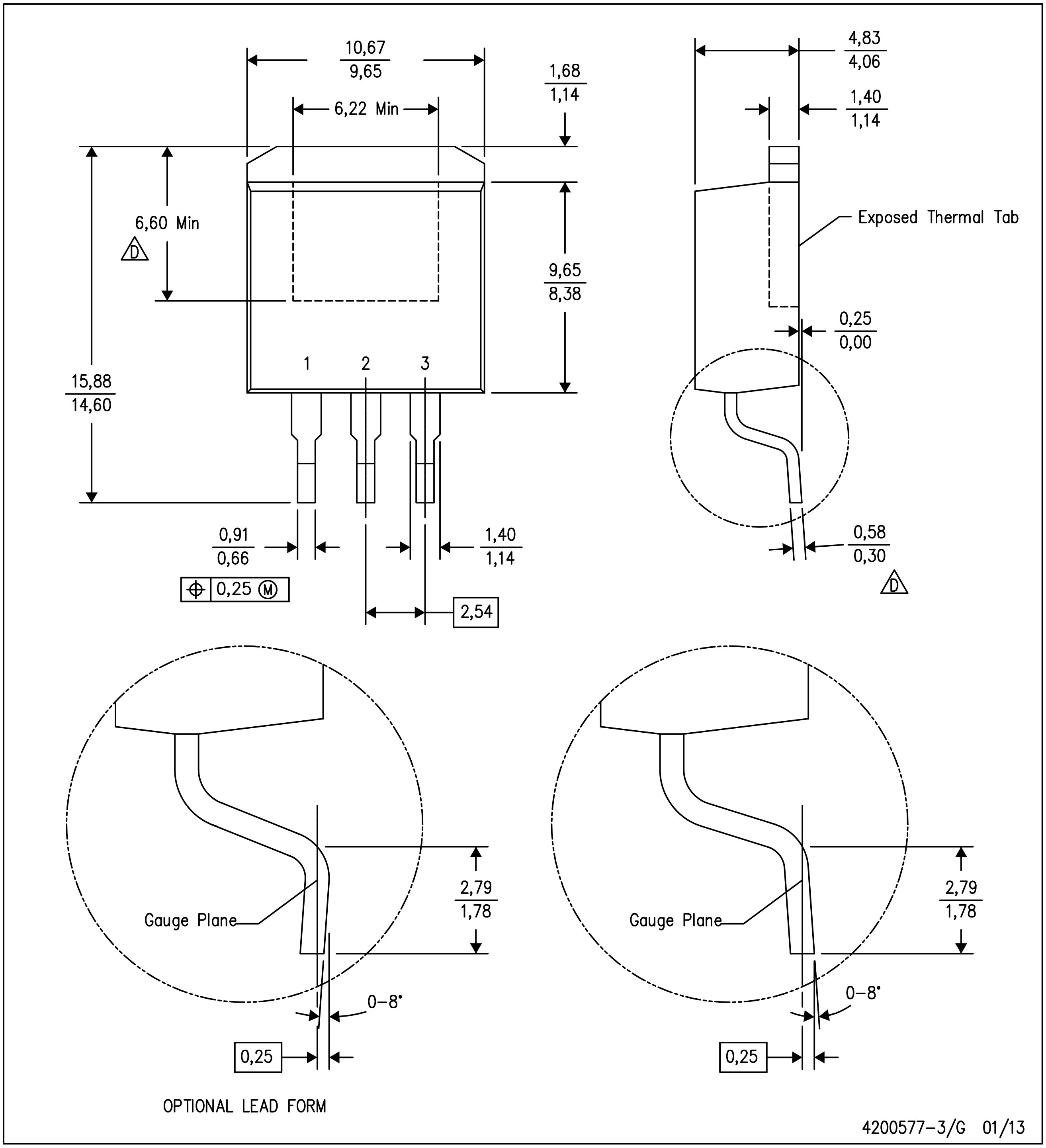
NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-220.



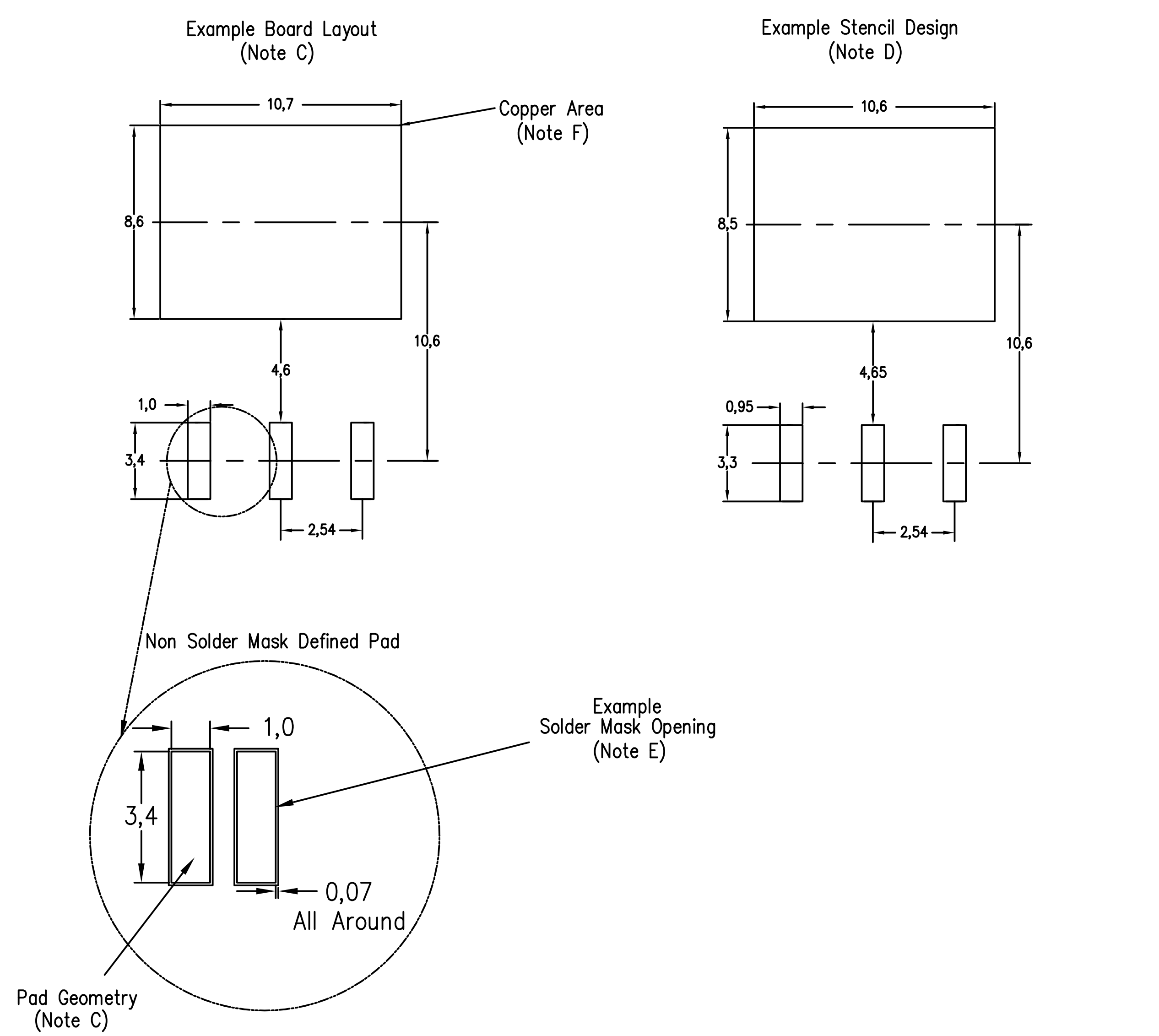
LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:15X

KTT (R-PSFM-G3) PLASTIC FLANGE-MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO-263 variation AA, except minimum lead thickness and minimum exposed pad length.

KTT (R-PSFM-G3) PLASTIC FLANGE-MOUNT PACKAGE



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NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-SM-782 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
- F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

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