AC/DC Drivers

Power Factor Correction and Quasi-Resonant DC/DC converter IC

BM1C001F

General Description

The compounded LSI of the Power Factor Correction (PFC) converter and Quasi-Resonant (QR) controller type AC/DC converter IC provides an optimum system for all products that include an electrical outlet. BM1C001F has a built in HV starter circuit that tolerates 650V and contributes to low power consumption and high speed start.

The PFC part is a Boundary Conduction Mode (BCM). It reduces the switching loss and the switching noise. This IC has adopted the voltage control mode, a solution that achieves no auxiliary winding and reduces external parts and the bias current.

The DC/DC part is Quasi-Resonant controlled. This control enables soft switching and helps to keep the EMI low. With MOSFET for switching and current detection resistors as external devices, a higher degree of design freedom is achieved.

This IC has over voltage protection for the PFC's output terminal, which protects electrolytic capacitors by stopping switching and makes the standby power consumption low by the PFC ON/OFF control function. The IC includes various protective functions such as VCC over voltage protection, external latch protection, brown out protection, soft start function, per-cycle current limiter and over load protection.

Features

- PFC+QR Combo IC
- Built-in 650V tolerance start circuit
- VCC pin: under and over voltage protection
- Brown out function
- External latch terminal function
- PFC boundary current mode (voltage control)
- PFC Zero Cross Detection
- PFC variable max frequency (up to 400kHz)
- PFC Dynamic & Static OVP function
- PFC Output level setting function
- PFC ON/OFF level setting
- QR low power when load is light (Burst operation) and frequency decrease function
- QR maximum frequency control (120kHz)
- QR_CS pin open protection and OCP function
- QR Over-Current Protection with AC compensation
- QR Soft Start function
- QR secondary side protection circuit of over-current
- QR_ZT pin 2 step timeout function and OVP function

Applications

AC adapters and Household appliances (Printer, TV, Vacuum cleaners, Air cleaners, Air conditioners, IH cooking heaters, Rice cookers, etc.).

Key Specifications

Operating Power Supply:	VCC	8.9V to 26.0V
Voltage Range:	VH_IN	80V to 600V
Operating Current:	Normal	1.2mA (Typ)
	Burst	0.6mA (Typ)
Max frequency:	PFC	400kHz (Max)
	QR	120kHz (Typ)
The range of temperature:		-40°C to +85°C

Package W(Typ) x D(Typ) x H(Max)

SOP18 11.20mm × 7.80mm × 2.01mm pitch 1.27mm

SOP18

Typical Application Circuit

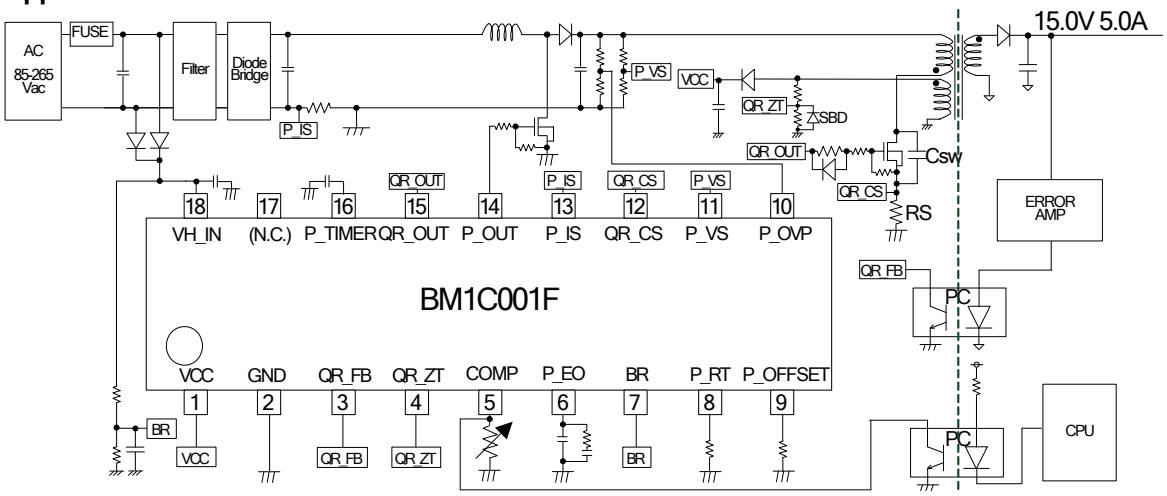


Figure 1. Application circuit

Pin Configuration

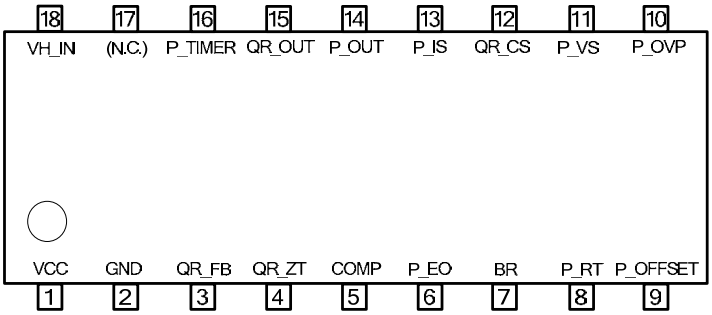


Figure 2. Pin Layout (Top View)

Pin Description

Table 1. I/O Pin Functions

Pin Name	I/O	Pin No.	Function	ESD Diode	
				VCC	GND
VCC	I/O	1	[General] Power supply pin	-	○
GND	I/O	2	[General] GND pin	○	-
QR_FB	I	3	[QR] Feedback detection pin	−	○
QR_ZT	I	4	[QR] Zero cross detection pin	-	○
COMP	I	5	[General] External latch input pin	−	○
P_EO	O	6	[PFC] Error amplifier output pin	−	○
BR	I	7	[General] Input AC voltage monitor pin	−	○
P_RT	I	8	[PFC] Max frequency setting pin	−	○
P_OFFSET	I	9	[PFC] ON/OFF setting voltage	−	○
P_OVP	I	10	[PFC] Over voltage detection pin	−	○
P_VS	I	11	[PFC] Feedback signal input pin	−	○
QR_CS	I	12	[QR] Over-current detection pin	−	○
P_IS	I	13	[PFC] Zero cross detection pin	−	○
P_OUT	O	14	[PFC] External MOS drive pin	○	○
QR_OUT	O	15	[QR] External MOS drive pin	○	○
P_TIMER	I	16	[PFC] OFF time setting pin	−	○
N.C.	-	17	-	-	-
VH_IN	I	18	[General] Starter circuit pin	-	○

Block Diagram

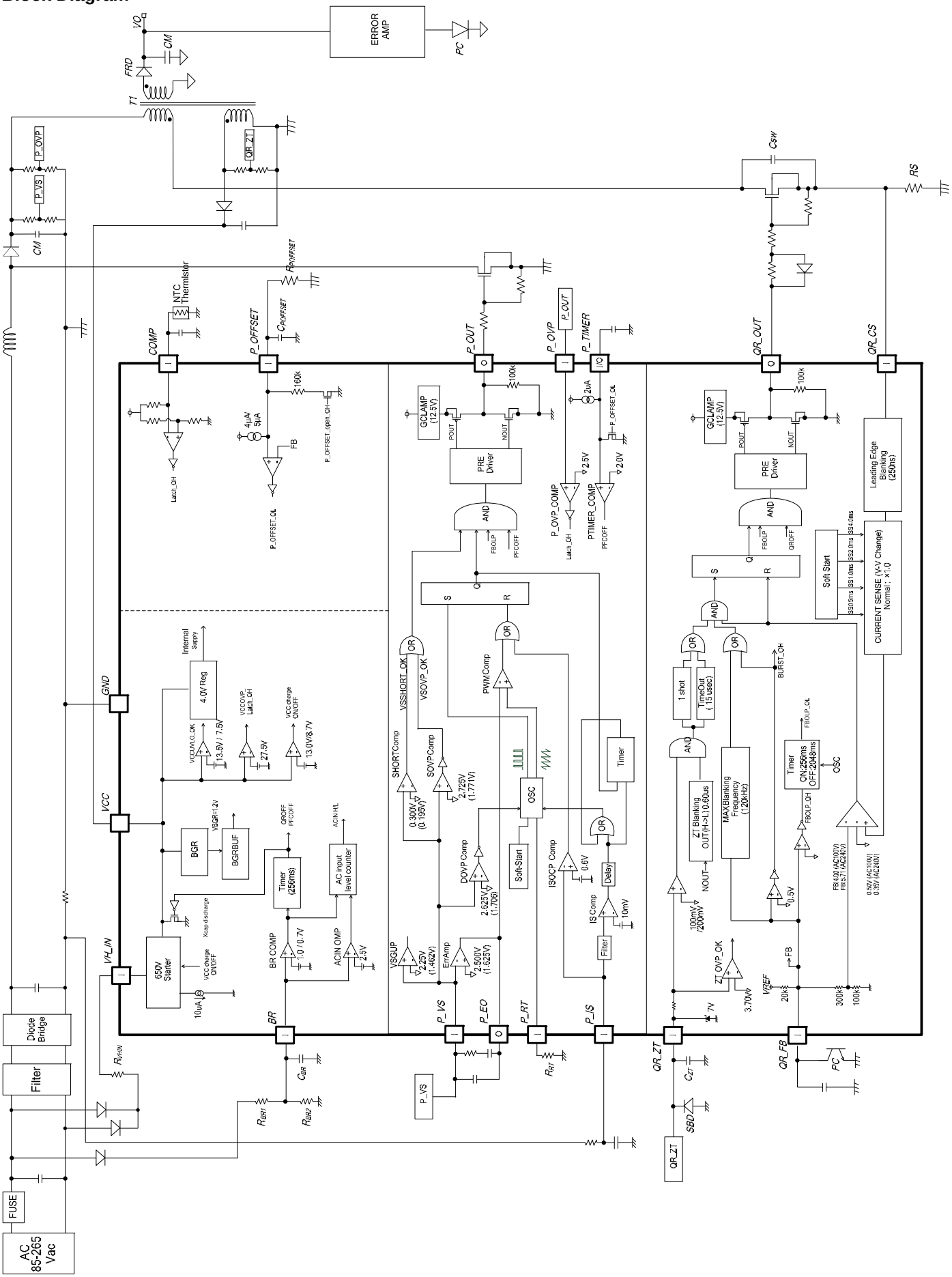


Figure 3. Block Diagram

Description of Blocks

(1) Starter Block (VH_IN Pin)

The built-in starter circuit tolerates 650V and enables low standby mode current consumption and high speed starting. After starting, current consumption is idle I_{START3} (typ=10uA).
This function is shown in Figure 4 and Figure 5. To supply electric power from AC supply to VHIN, rectification is inputed from both ends of AC waveform to VHIN for stable works (Refer to Figure6).

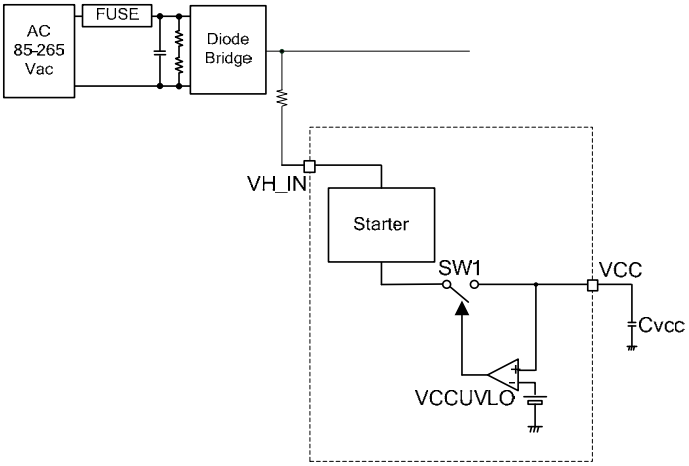


Figure 4. Starter Circuit Block Diagram

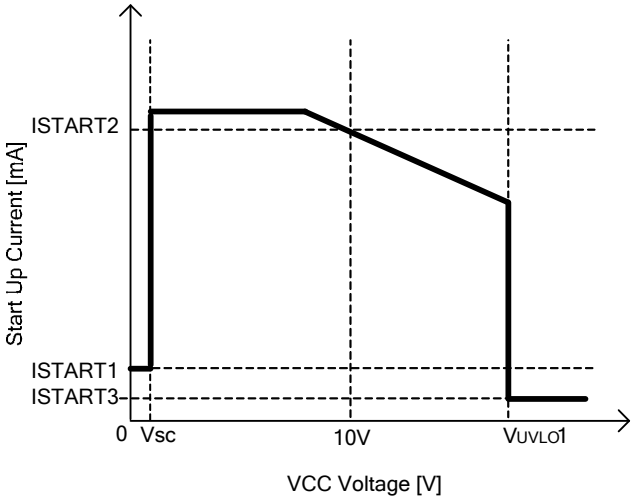


Figure 5. Start-up Current vs VCC Voltage

In addition, VH_IN pin has a Cap discharge function. (Refer to Figure 6). If the input voltage of the BR pin goes below 1.0V, discharge starts after waiting 256ms. (However during Light load mode, the OLP state of the secondary side output, if there is no power supply from the auxiliary winding, when the IC is in recharge operation, discharge begins after removing the AC outlet without waiting for the timer (256ms), with the current consumption of the internal circuitry of the IC. (Path: Figure 6 (a)))

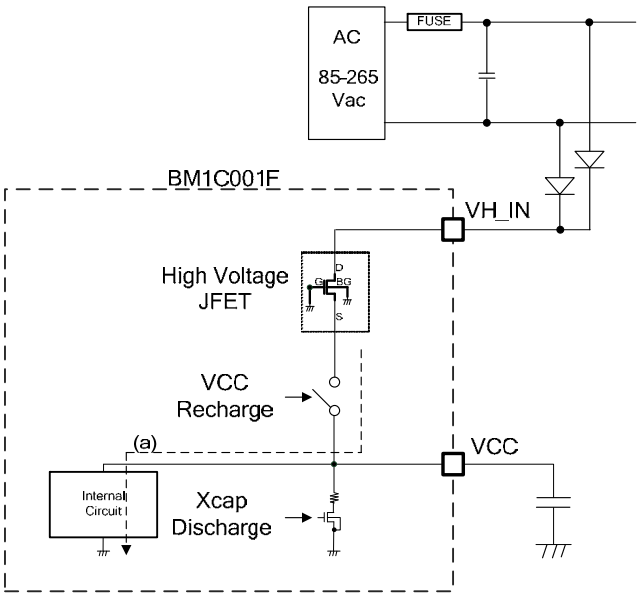


Figure 6. Starter Circuit Block Diagram

(2) Start-Up Sequence
(Soft Start Operation, Light Load Operation, Over Load Operation, Auto Recovery Operation)

The start up sequence is showed at Figure 7; the DC/DC part operates first, followed by the PFC part.

A: Input voltage VH_IN is applied.
B: Charge current flows from start circuit to the VCC pin capacitor. Then VCC pin voltage rises.
C: Monitor the AC voltage by BR pin. And confirm normal state by releasing brown out (BR pin>1.0V).
D: When V_{UVLO1} (typ.13.5V) < VCC pin, UVLO is released and this IC operates.
E: After rising, the internal regulator, DC/DC part, starts operation, and then VOUT voltage rises. When the DC/DC starts, the DC/DC output voltage is set to be the specified voltage to until t_{FOLP} (typ.256ms).

[QR Start-Up Operation]
F: This IC adjusts the over-current limiter of DC/DC part during the operation of soft start 1 against over voltage and current rising. This term continues for t_{ss1} (typ.0.5ms). This IC operates the state until maximum power of QR is 12%.
G: This IC adjusts the over-current limiter of DC/DC part during the operation of soft start 2 against over voltage and current rising. This term continues for t_{ss2} (typ.1.0ms). This IC operates the state until maximum power of QR is 25%.
H: This IC adjusts the over-current limiter of DC/DC part during the operation of soft start 3 against over voltage and current rising. This term continues for t_{ss2} (typ.2.0ms). This IC operates the state until maximum power of QR is 50%.
I: This IC adjusts the over-current limiter of DC/DC part during the operation of soft start 4 against over voltage and current rising. This term continues for t_{ss2} (typ.4.0ms). This IC operates the state until maximum power of QR is 75%.
J: If secondary voltage is value is set, the QR_FB voltage value corresponding to load current from photo coupler is constant. At normal state, QR_FB voltage is QR_FB<$V_{FBOLP1B}$ (typ.2.60V).

[PFC Start-Up Operation]
K: At the point in J or after the QR Soft-start ends (4ms≤), This IC recognizes that the DC/DC part operation is normal, the PFC part starts operation.
L: If P_VS pin voltage is greater than V_{P_SHORT} (typ.0.3V), the IC judges that short detection is normal.
M: To prevent an excessive current rise and excessive voltage rise in the PFC part, P_VS voltage rises from 0V. At this time, PFC's DUTY increase from 0% with P_EO voltage increasing. When P_VS>2.25V, the output voltage rise is slow, Then, P_VS is stable with voltage of 1.625V (ACIN L) or (ACIN H) 2.5V by the input state of the BR pin.

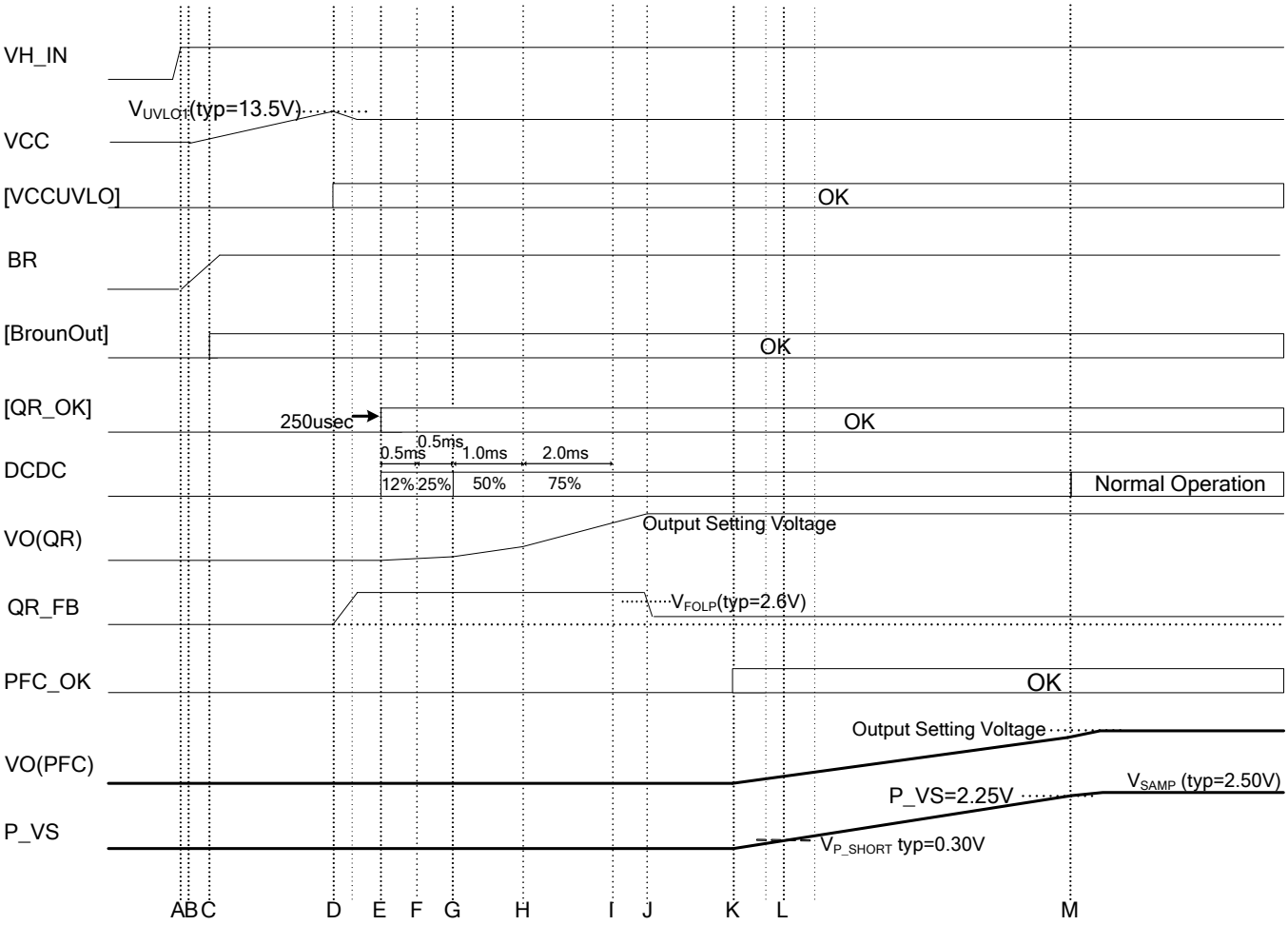


Figure 7. Start-up Sequence Timing Chart

(3) VCC Pin Protection Function

BM1C001F includes built-in V_{CC} low voltage protection function, VCC UVLO (Under Voltage Lock Out), V_{CC} over voltage protection function, VCC OVP (Over Voltage Protection), and VCC CHARGE function that operates in case the VCC voltage drops. VCC UVLO and VCC OVP monitor the VCC pin and prevent the VCC pin from destroying the switching MOSFET with abnormal voltage. VCC charge function stabilizes the secondary output voltage by charging it from the high voltage line using the starter circuit when the VCC voltage drops.

(3-1) VCC UVLO／VCC OVP Function

VCC UVLO is an auto recovery comparator that has voltage hysteresis. VCC OVP is also an auto recovery comparator that has voltage hysteresis. VCC OVP operates detection in case of continuing VCC pin voltage > V_{OVP} (typ.27.5V).

This function has built-in mask time of t_{LATCH}(typ.150us). By this function, this IC masks pin generated surge etc.

(3-2) VCC Charge Function

VCC charge function operates once the VCC pin >V_{UVLO1} and the DC/DC operation starts and then when the VCC pin voltage drops to <V_{CHG1}. At that time the VCC pin is charged from VH_IN pin through starter circuit. Therefore, this IC start up stability. At charging time, stop PFC output to stable charge. When the VCC pin voltage rises to VCC >V_{CHG2}, charging is stopped, and start PFC works. The operations are shown in figure 8.

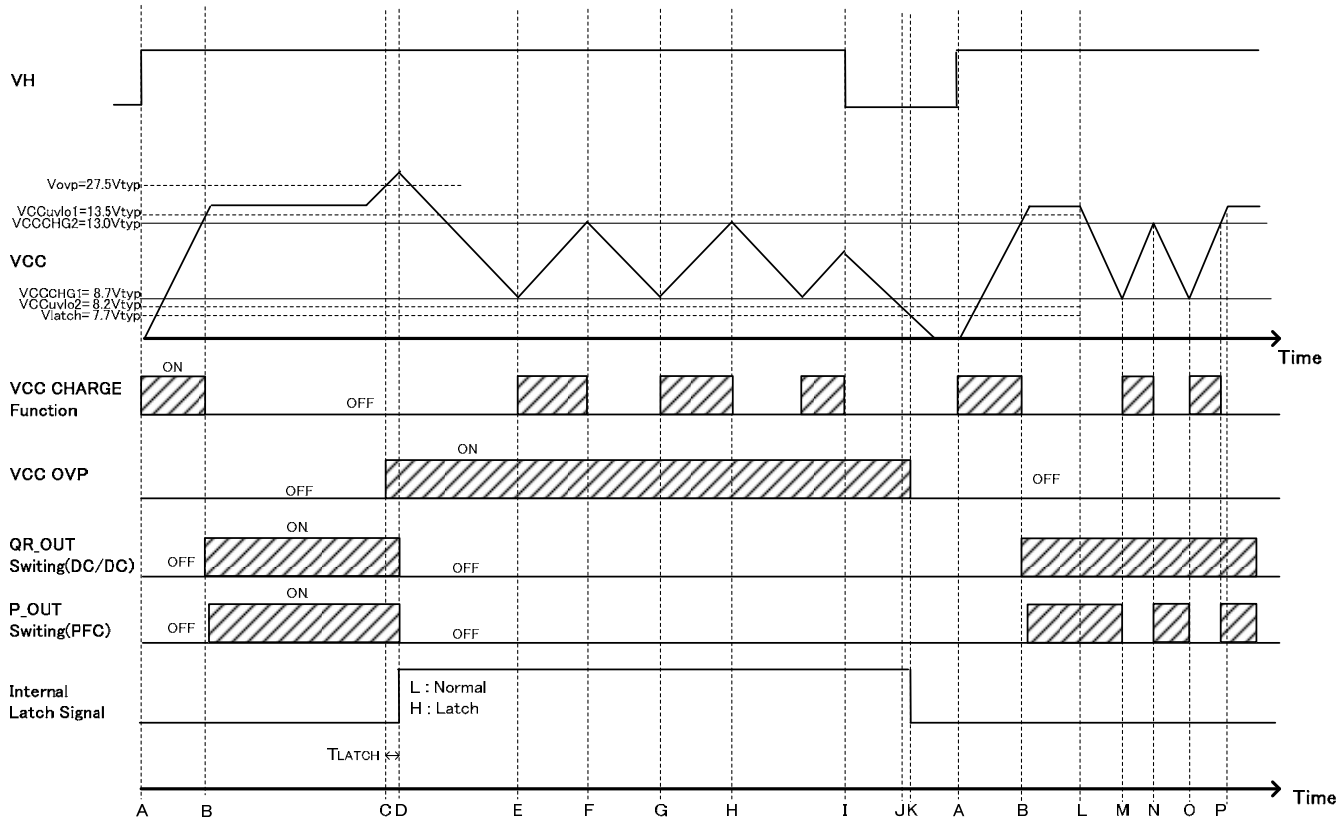


Figure 8. VCC UVLO / VCC OVP / VCC Charge Function Timing Chart

A: VH _IN pin voltage rises, VCC pin voltage starts rising.
B: VCC > V_{UVLO1}, VCC UVLO is released, DC/DC operation starts.
C: VCC > V_{OVP}, VCC OVP detects the overvoltage in the IC.
D: If the state of VCC < V_{OVP} continued t_{LATCH} (typ.100us) time, switching will stop by the OVP function. (Latch mode).
E: VCC < V_{CHG1}, VCC terminal voltage rises by VCC recharging function.
F: VCC > $V_{CHG2,}$ VCC recharge function stops.
G: (The same with E.)
H: (The same with F.)
I: Voltage of the high voltage line VH is reduced
J: VCC<V_{UVLO2}, VCC UVLO function starts.
K: VCC<V_{LATCH}, Latch is released.
L: Secondary output has no load, DCDC works burst operation. VCC pin voltage reduce because power does not supply from auxiliary coil
M:VCC<V_{CHG1} VCC terminal voltage rises by VCC recharging function. At that time, PFC switching stops.
N :VCC> V_{CHG2} VCC recharge function stops. PFC operation starts.
O:(The same with M.)
P:Increas a load, supply electric power from auxiliary coil

(4) COMP Pin (Outside Coercive Stop Function)

The COMP Pin is used for coercive stop function. When the COMP Pin is lower than V_{COMP} (typ.0.5V), PFC and DC/DC blocks stop. A detection timer t_{COMP} (typ.150us) is built inside to prevent detection errors caused by noise. The stop mode is latched.

The COMP pin is pulled up in RCOMP (typ.25.9kΩ), If the COMP pin is pulled down with a resistance value lower than R_T(3.70kΩ.typ), the IC will detect the abnormality. An application example is shown in Figure 9, 10, 11.

Overheating Protection by NTC Thermistor

A thermistor is attached to the COMP pin so that latching can be stopped when overheating occurs.
In the case of this application, it should be designed so that the thermistor resistance becomes R_T (typ.3.70kΩ) when overheating is detected.
(Figure 9, 10, 11 are application circuit examples in which latching occurs when Ta = 110°C.)

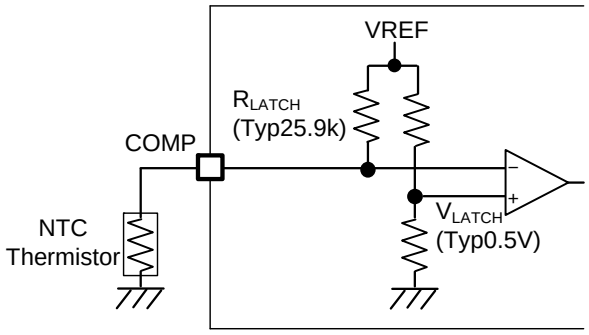


Figure 9. COMP Pin Overheating Protection Application

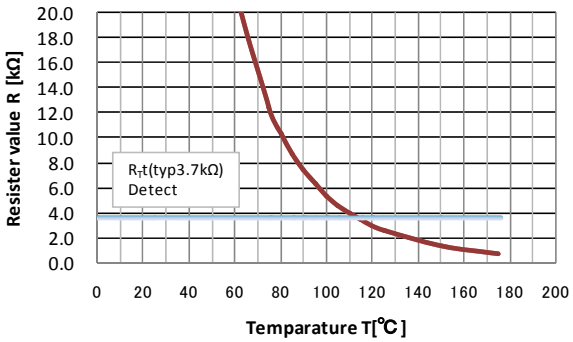


Figure 10. Temperature-Thermistor Resistance Value Characteristics

Secondary Output Voltage Overvoltage Protection

A photocoupler is attached to the COMP pin to perform detection of secondary output overvoltage.

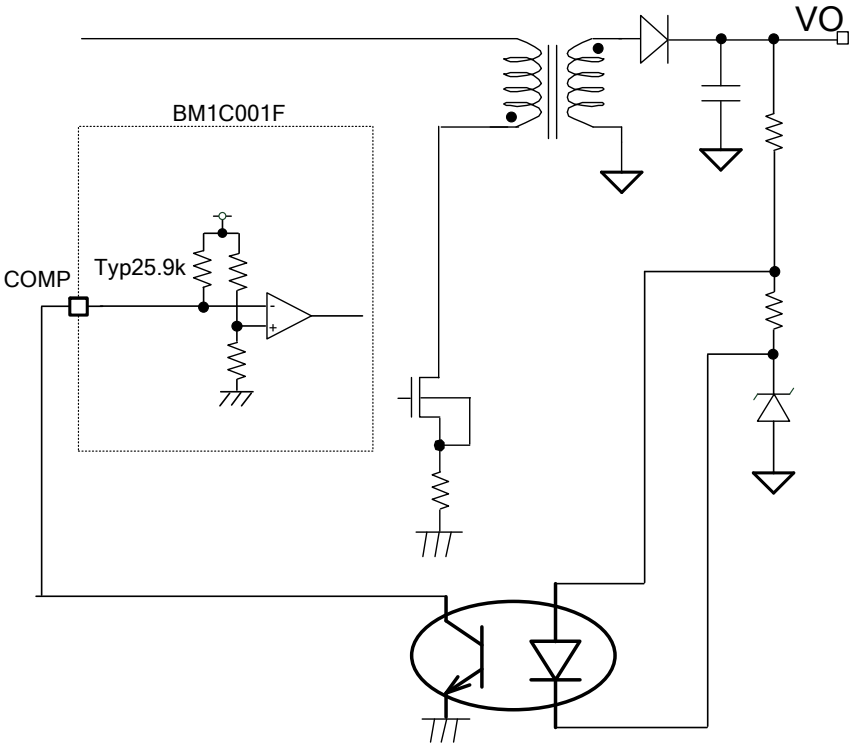


Figure 11. Output Overvoltage Protection Application

(5) BR Pin

The BR Pin has three functions as shown in Figure 12.
Function 1: Low AC voltage protection. (Blown IN/OUT)
Function 2: Detects AC voltage and discharges by VH_IN Pin.
Function 3: Detects AC input voltage, whether 240V or 100V, by the amplitude level input to the BR pin The output voltage of the PF" and voltage level of the CS over-current detection are switched to AC240V or AC100V based systems. (PFC Output = AC100V: 260V, AC240V:400V)

The Input to the BR pin is the full-wave / half-wave rectified AC waveform of 50Hz/60Hz voltage divided by resistance. In addition, in order to stabilize the input waveform, the capacitor (1000pF to 0.01uF) must be connected close to the BR pin.

(5-1) Low AC Voltage Protection (Blown IN/OUT)

When AC voltage is too low, blown out function can stop the PFC block and QR block. The AC input voltage connects to the BR pin through two divider resistors. When the voltage of the BR pin is higher than V_{BR} (1.0Vtyp), normal status is detected and DC/DC starts.

After DC/DC started, low voltage in BR pin can stop PFC and DCDC blocks when it`s lower than V_{BR}(typ.1.0V)and maintains the level for longer than t_{BR}(typ.256ms).

(5-2) X Capacitor Discharge Function

When AC voltage drop is detected after T_{BR}(typ.256ms), discharge function becomes possible.
Discharge happens when VCC recharge function works.

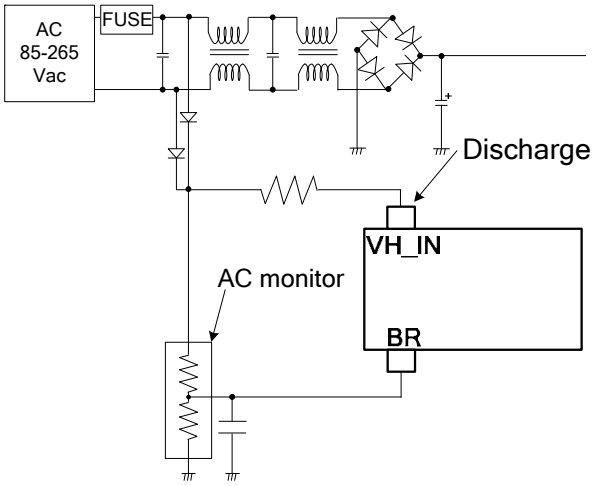
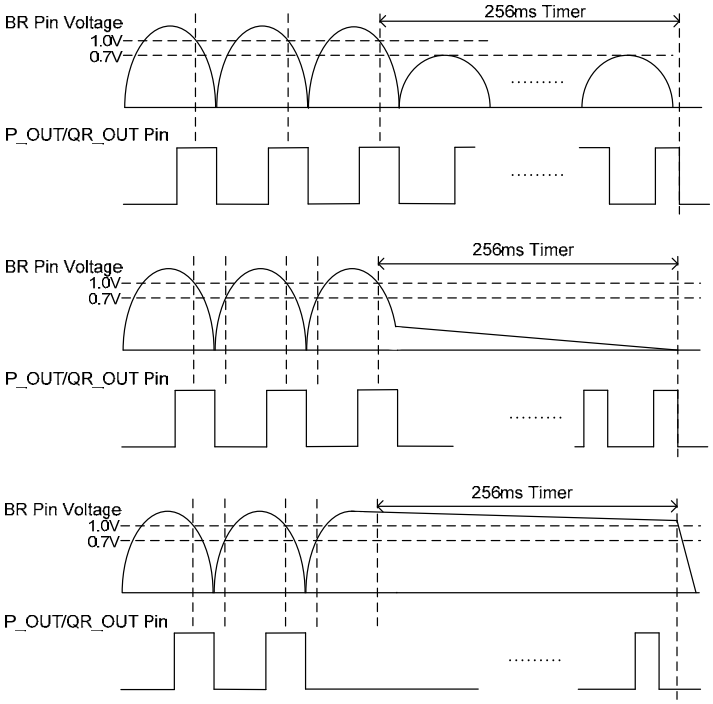


Figure 12. Blown IN/OUT Application Circuits



(1) If the AC input voltage drops,
Output is stopped if for more than 256ms the BR terminal voltage is lower than 1.0V.
In this case, Xcap discharge function operates.

(2) If the AC input voltage is lost, it was a low voltage,
Output will be stopped in 256ms after the point where the BR terminal voltage drops to 1.0V or less.
In this case, Xcap discharge function operates.

(3) If the AC input voltage is lost, it becomes a high voltage,
Output will be stopped in 256ms after the point where the BR terminal voltage rises to 0.75V or more.
In this case, Xcap discharge function operates.

Figure 13. BR Pin Timing Chart

(5-3) PFC Output Voltage Switching Function

For AC input voltage that varies by region, in order to be as constant as possible boosting ratio by changing the PFC output voltage, PFC is switching the output voltage by AC240V or AC100V-based systems. Thereby, PFC output voltage is changed from 400V to 260V in the case of AC100V-based input. As a result, efficiency is improved.

This feature will detect if the system is AC240V or AC100V based in number and voltage level of the AC waveform that is input to the BR pin. (Refer to Figure 14). See the timing chart of Figure 15, If the waveform (voltage higher than the voltage detection ACIN (Th.=2.5V)) of 9 cycles is entered continuously, The PFC determines the AC240V system. In that case, PFC changes the GM amplifier reference and the PFC output is changed to 400V from 260V.

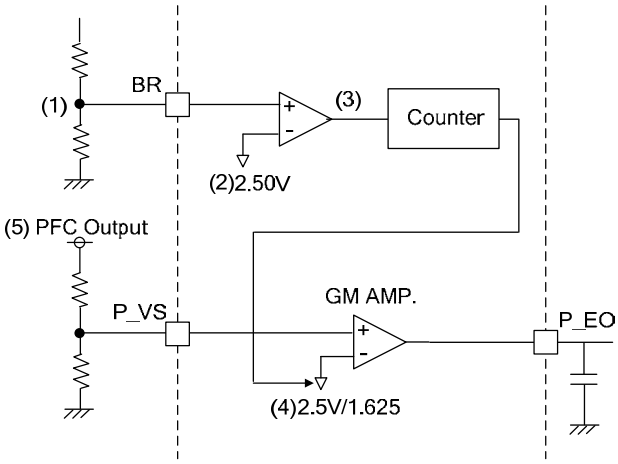


Figure 14. PFC output voltage switching function

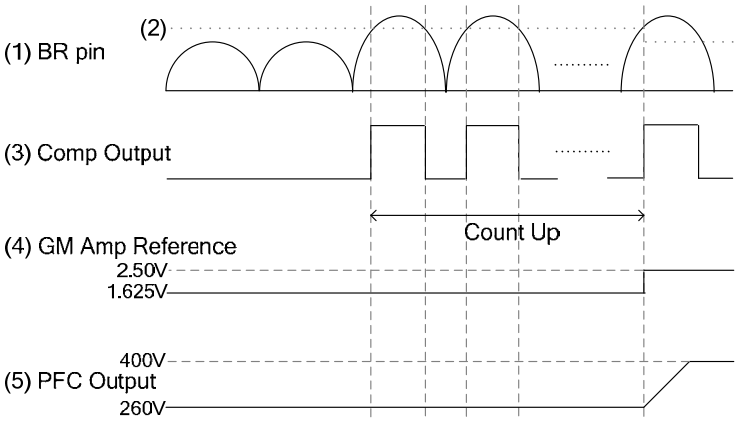


Figure 15. PFC output voltage switching Timing Chart

(6) The Quasi-Resonant DC/DC Driver

The IC operates with PFM (Pulse Frequency Modulation) mode method. By monitoring the QR_FB pin, QR_ ZT pin, and QR_ CS pin, the IC supplies optimum system for DC/DC operation. The IC controls ON width (Turn Off) of external MOSFET by QR_FB pin and QR_CS pin. The IC controls OFF width (Turn ON) of external MOSFET by QR_ZT pin. The details are shown below. (Refer to Figure 16)

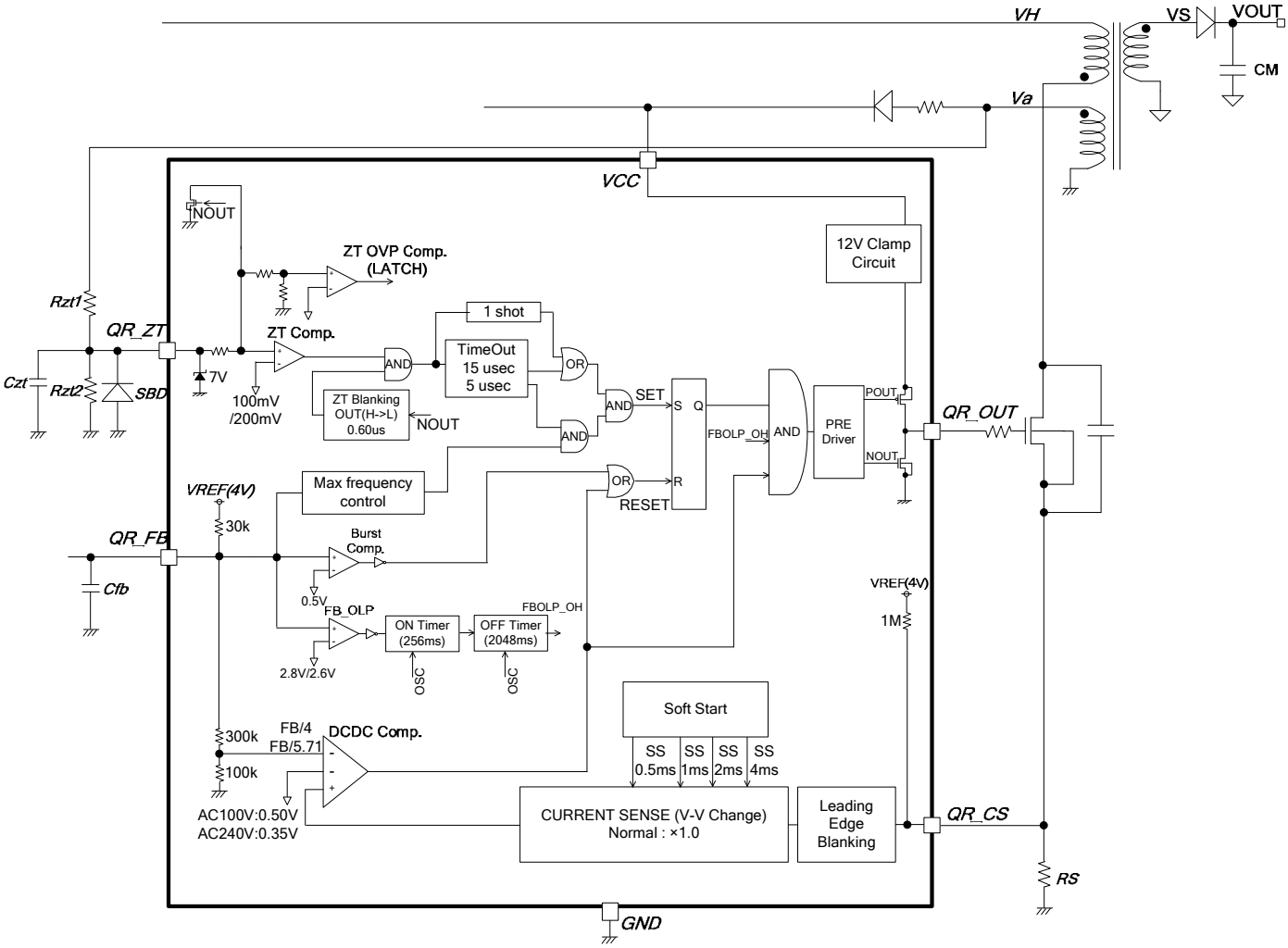


Figure 16. DC/DC Block Diagram

(6-1) Determination of ON width (Turn OFF)

ON width is controlled by QR_FB and QR_CS. The IC decides ON width by comparison between the value which divide QR_FB pin by V_{cs} (typ=4) voltage and QR_CS pin voltage. Besides, by comparison with Vlim1(typ.0.5V)voltage which is generated in IC, QR_CS comparator level is changed linearly to be shown in Figure 17.

QR_CS is shared with over-current limiter circuit per pulse.

IC changes over-current limiter level and max frequency by QR_ FB voltage.

mode1: Burst operation
mode2: Frequency reduction operation (reduce max frequency)
mode3: Max frequency operation
mode4: Over load operation (To detect over load state, IC stops switching)

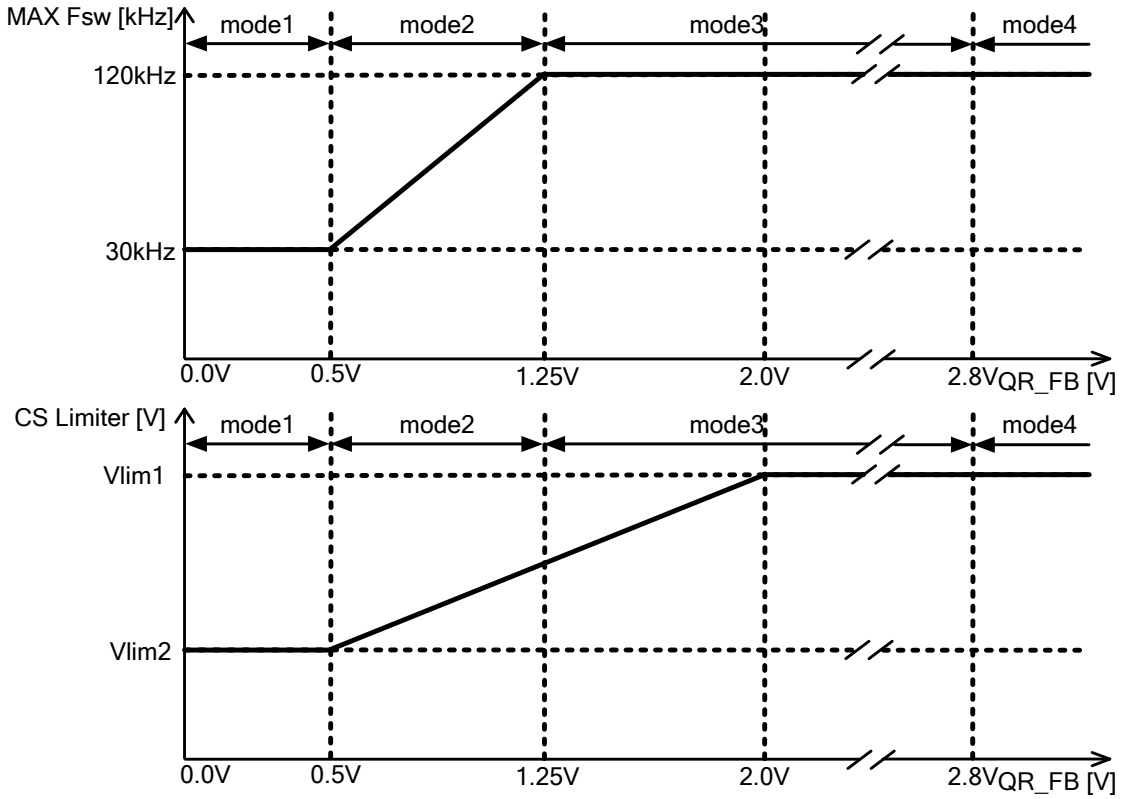


Figure 17. QR_FB Pin Voltage – Over-Current Limiter, Max Frequency Characteristics

To adjust over-current limiter level, CS Over-Current Protection voltage is switched in soft-start, AC voltage. Vlim1 and Vlim2 are changed below.

Table 2. Over-Current Protection Voltage Detail

Soft Start	AC=100V AC=240V(PFC=OFF)		AC=240V(PFC=ON)	
	Vlim1	Vlim2	Vlim1	Vlim2
Start to 0.5ms	0.063V (12%)	0.016V (3%)	0.044V (10%)	0.011V (2%)
0.5ms to 1ms	0.125V (25%)	0.032V (6%)	0.088V (20%)	0.022V (4%)
1ms to 2ms	0.250V (50%)	0.063V (12%)	0.175V (40%)	0.044V (9%)
2ms to 4ms	0.375V (75%)	0.094V (19%)	0.263V (60%)	0.066V (13%)
4ms ≤	0.500V (100%)	0.125V (25%)	0.350V (70%)	0.087V (18%)

* (percent) is shown comparative value with Vlim1(typ =0.5V)in normal operation.
The reason that distinguish between AC100V and AC230V is by CS over-current protection voltage switch function which is shown to(6-3).

(6-2) LEB (Leading Edge Blanking) Function

When a MOSFET for switching is turned ON, surge current occurs because of capacitance or rush current. Therefore, when QR_CS voltage rises temporarily, the over-current limiter circuit may result to miss detections. To prevent miss detections, the IC has a built-in blanking function which masks for t_{LEB} (typ.250ns) from switching QR_OUT pin from L to H. This blanking function enables to reduce noise filter of QR_CS pin.

(6-3) QR_CS Pin Over-Current Protection Switching Function

When input voltage (VH_IN) is higher, ON time is short, and the operating frequency increases. As a result, maximum capable power increases for constant over-current limiter. For that while monitoring BR pin (ACIN detect voltage) the IC switches the over-current detection of the IC. In case of high voltage (AC230V) and PFC working, IC changes over-current comparator level to ×0.7 multiple of normal level.

(6-4) Determination of OFF Width (Turn on)

OFF width is controlled at the QR_ZT pin. When QR_OUT is Low, the power stored in the coil is supplied to the secondary-side output capacitor. When this power supply ends, there is no more current flowing to the secondary side, so the drain pin voltage of switching MOSFET drops. Consequently, the voltage on the auxiliary coil side also drops. A voltage that was resistance-divided by Rzt1 and Rzt2 is applied to QR_ZT pin. When this voltage level drops to V_{ZT1} (typ.100mV) or below, MOSFET is turned ON by the ZT comparator. Since zero current status is detected at the QR_ZT pin, time constants are generated using Czt, Rzt1, and Rzt2. Additionally, a ZT trigger mask function (described in section 6-5) and a ZT timeout function (described in section 6-6) are built in IC.

In addition, Voltage auxiliary winding voltage (Vs) becomes negative while the switching is ON, There is a possibility that the surge voltage negative is input to the pin QR_ZT during the switching timing. For this reason, To avoid of-0.3V Contact Rating below, Please connect a Schottky diode between the pin and GND. (Refer to Figure 16)

(6-5) ZT Trigger Mask Function (Figure 18)

When switching is set from ON to OFF, superposition of noise may occur at the QR_ZT pin.
Then, the ZT comparator and ZTOVP comparator are masked for the T_{ZTMASK} time to prevent ZT comparator operation errors.

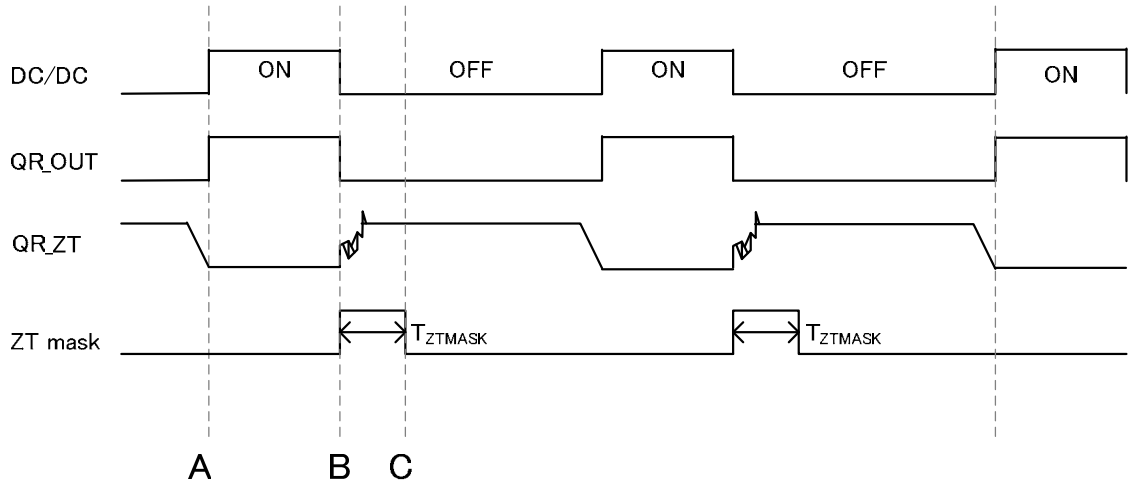


Figure 18. The Function of QR_ZT Trigger Mask.

A: DC/DC OFF => ON
B: DC/DC ON => OFF
C: Since a noise occurs to QR_ZT pin at B, IC masks ZT comparator and ZTOVP comparator detection for T_{ZTMASK} time.

(6-6) ZT Timeout Function (Figure 19)

(6-6-1) ZT Timeout Function 1

When QR_ZT pin voltage is not higher than V_{ZT2}(typ=200mV) for t_{ZTOUT1} such as start or low output voltage, QR_ ZT pin shorts to ground and IC turns on MOSFET by force.

(6-6-2) ZT Timeout Function 2

After ZT comparator detects low voltage level, when IC does not detect a following low voltage level within t_{ZTOUT2}, IC turns on MOSFET by force. After ZT comparator detects bottom at once, the function operates. For that, it does not operate at start or at low output voltage. When IC is not able to detect low voltage level by decreasing auxiliary coil voltage, the function operates.

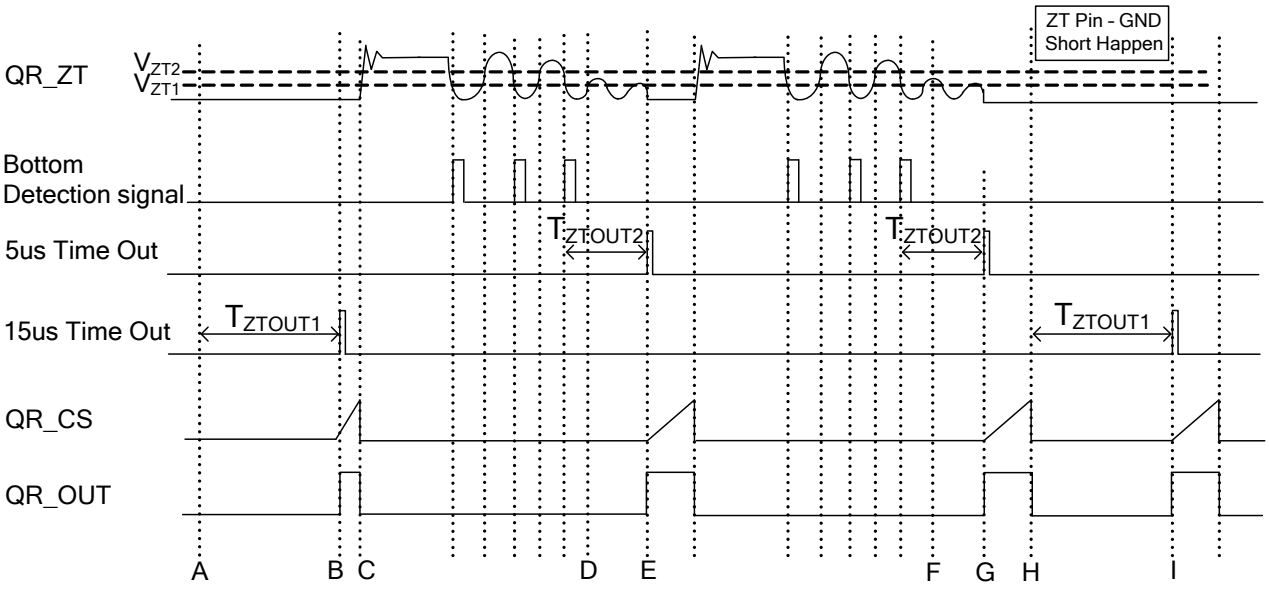


Figure 19. The Function of ZT Time Out.

A: When starting, IC starts to operate by ZT timeout function1 for QR_ZT=0V.
B: MOSFET turns ON
C: MOSFET turns OFF
D: QR_ZT voltage is lower than V_{ZT2} (typ.200mV) by QR_ZT dump decreasing.
E: MOSFET turns ON by ZT timeout fucntion2 after T_{ZT2} (typ.5us) from D point.
F: QR_ZT voltage is lower than V_{ZT2} (typ.200mV) by QR_ZT dump decreasing.
G: MOSFET turns ON by ZT timeout fucntion2 after T_{ZT2} (typ.5us) from F point.
H: QR_ZT pin is short to GND.
I : MOSFET turns ON by ZT timeout function1 after T_{ZTOUT1}(typ.15us).

(6-7) Soft Start Sequence

Normally, when AC voltage is applied there is a large amount of current flow then secondary the output voltage and current overshoot. To prevent it, the IC has a built-in soft-start function. When VCC pin voltage is lower than V_{UVLO2} (typ.8.2V), IC is reset. After that, when AC voltage is applied, the IC operates soft-start. The soft start function is shown below:

start to 0.5ms	=>	Set QR_CS limiter to 12.5% of normal operation.
0.5ms to 1ms	=>	Set QR_CS limiter to 25% of normal operation.
1ms to 2ms	=>	Set QR_CS limiter to 50% of normal operation.
2ms to 4ms	=>	Set QR_CS limiter to 75% of normal operation.
4ms ≤	=>	normal operation

(6-8) QR_ZT OVP (Over Voltage Protection)

The built-in OVP function to QR_ZT of the IC has a protection type that is latch mode. ZTOVP corresponds to DC voltage detection and pulse detection for QR_ZT pin.

When the QR_ZT pin voltage is over V_{ZTL} (typ=5.0V), IC starts to detect ZTOVP function.
To prevent ZT OVP from miss-detecting by surge noise, IC builds in 3count and t_{LATCH}(typ=100us) timer.
ZT OVP function operates in all states (normal state and over load state and burst state) after t_{ZTMASK}(0.6us).
For pulse detection, ZT OVP operation starts detection after t_{ZTMASK} delay time from QR_OUT: H->L

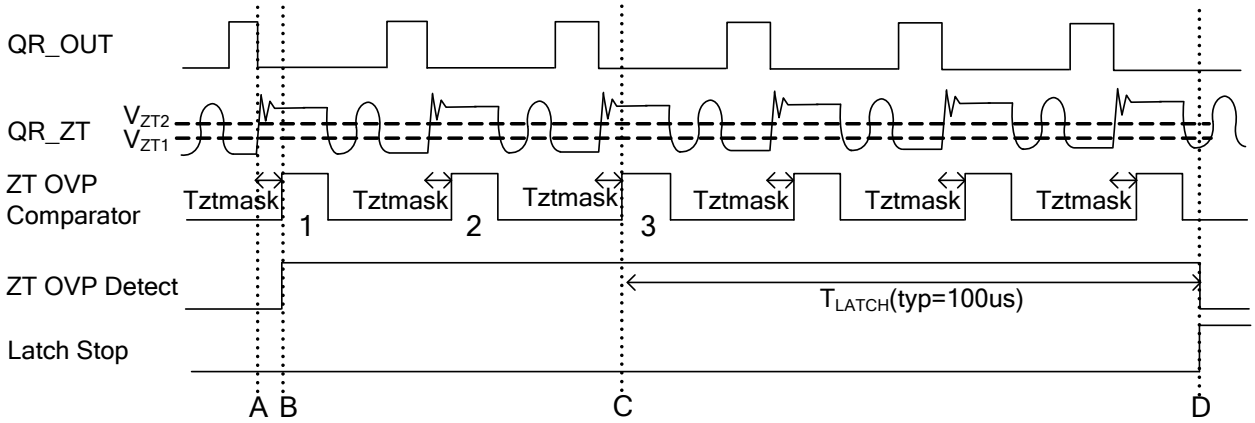


Figure 20. The Function of Latch Mask and ZT OVP

A: When QR_OUT voltage is changed from H to L, QR_ZT voltage is up. Then, surge pulse occurs to QR_ZT. For that, because IC builds in t_{ztmask} time (typ=0.6us), IC does not detect ZTOVP for t_{ztmask} time.
B: IC detects ZTOVP after t_{ztmask} time (typ=0.6us) when QR_ZT voltage > 5.0V.
C: When ZTOVP comparator counts 3 pulse, t_{LATCH} timer (typ=100us) operates.
D: When it takes for 100us from C, IC detects ZT OVP and IC carries out latch stop.

(6-9) QR_CS Open Protection

When QR_CS is OPEN, to prevent QR_OUT pin from changing to H by noise, IC builds in CS open protection. When QR_CS is open, QR_OUT switching is stopped by the function. (This is auto-recovery.)

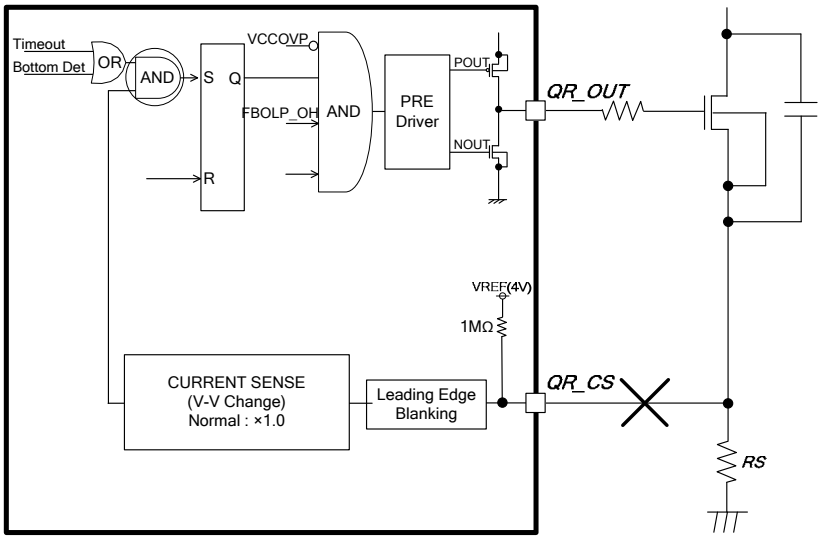


Figure 21. QR_CS Open Protection Circuit.

(6-10) OUTPUT Over Load Protection (FB OLP Comparator)

When secondary output is at over load, IC detects it by FB OLP, then the IC stops switching.
In OLP state, because the secondary photo-coupler has no current flow, QR_FB voltage is up.
When the condition continues for t_{FOLP} (typ =256ms), IC judges over load state, QR_OUT and P_OUT are fixed to low. After QR_FB voltage is over V_{FOLP1A} (typ =2.8V), when QR_FB voltage is lower than V_{FOLP1B} (typ =2.6V) within t_{FOLP} (typ =256ms), over load protection timer is reset.
In starting, because QR_FB is pull-up by a resistor to internal voltage, QR_FB voltage starts to operate in the state which is more than V_{FOLP1A} (typ =2.8V).
For that, please set the stable time of secondary output voltage within t_{FOLP} (typ =256ms).
After detecting over load, IC is stopped for t_{OLPST} (typ =2048ms), IC is on auto-recovery operation.
In stopping switching, though VCC voltage is not charged from auxiliary coil side, IC operates re-charge function from starter circuit, VCC voltage keeps VCC pin voltage > V_{UVLO2}.

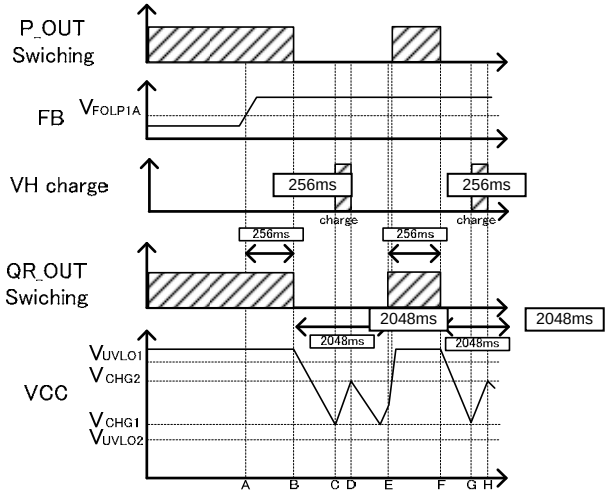


Figure 22. Auto Restart Operation by Over Load Protection.

A: When QR_FB voltage is over V_{FOLP1A} (typ.2.8V), FBOLP comparator detects over load.
B: When the state A continues for t_{FOLP} (typ.256ms), IC stops switching by over load protection.
C: During stopping switching by over load protection, VCC voltage drops. When VCC voltage is lower than V_{CHG}, VCC re-charge function operates, VCC voltage is up.
D: When VCC voltage is higher than V_{CHG2} by re-charge function, VCC recharge function is stopped.
E: From B, it takes for t_{OLPST} (typ.2048ms), IC starts switching with soft-start.
F: When over load state continues, QR_FB voltage is over V_{FOLP1A}. When it takes for t_{FOLP}(typ.256ms) from E, IC stops switching.
G: During stopping switching by over load protection, VCC voltage drops. When VCC voltage is lower than V_{CHG1}, VCC re-charge function operates, VCC voltage is up.
H: When VCC voltage is higher than V_{CHG2} by re-charge function, VCC recharge function is stopped.

(6-11) QR_OUT Pin Voltage Clamp Function

For the purpose of protecting the external MOSFET, H level of QR_OUT is clamped to V_{OUTH} (typ.12.5V)
It prevents gate destruction of MOSFET by rising VCC voltage. (refer to Figure 20) QR_OUT is pull-down R_{PDOUT} (typ.100kΩ).

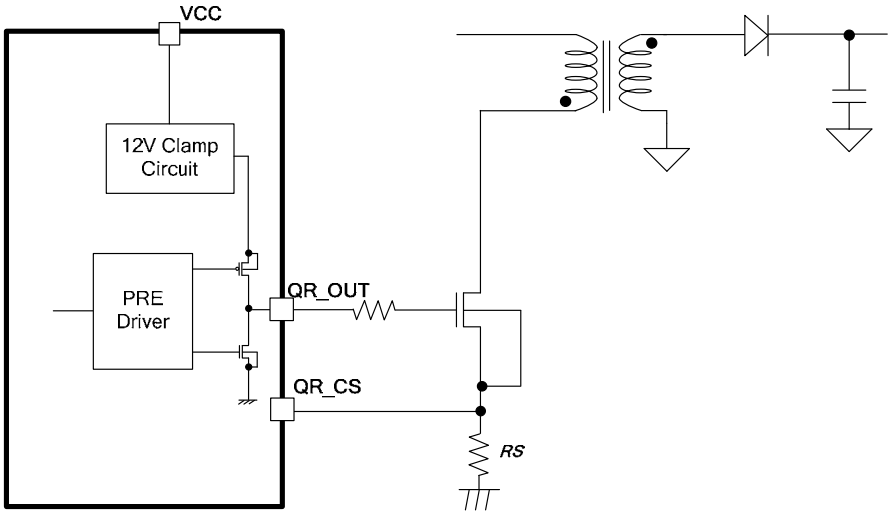


Figure 23. The Simple Circuit of QR_OUT Pin.

(7) Power Factor Correction (PFC: Power Factor Correction) Part

The Power Factor Correction Circuit is a voltage control method with the PFM boundary conduction mode. The operation circuit is shown is Figure 24 and Timing chart is shown in Figure 25.

Switching Operation

(1) Inductor current (I_L) increases after MOSFET changes to ON.
(2) The slope set by P_RT is compared with V_{P_EO} when MOSFET is turned ON, I_L increases current.
(3) MOSFET is set to be ON after P_IS terminal detects at the zero point.

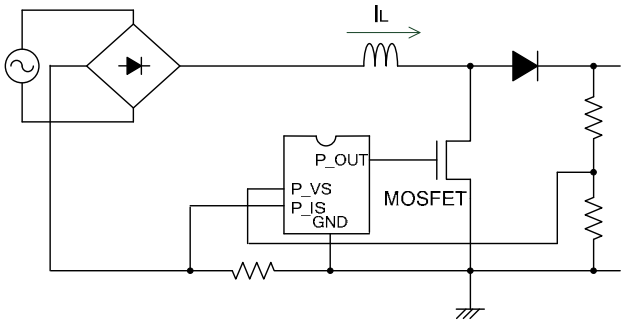


Figure 24. The Operation Circuit of PFC.

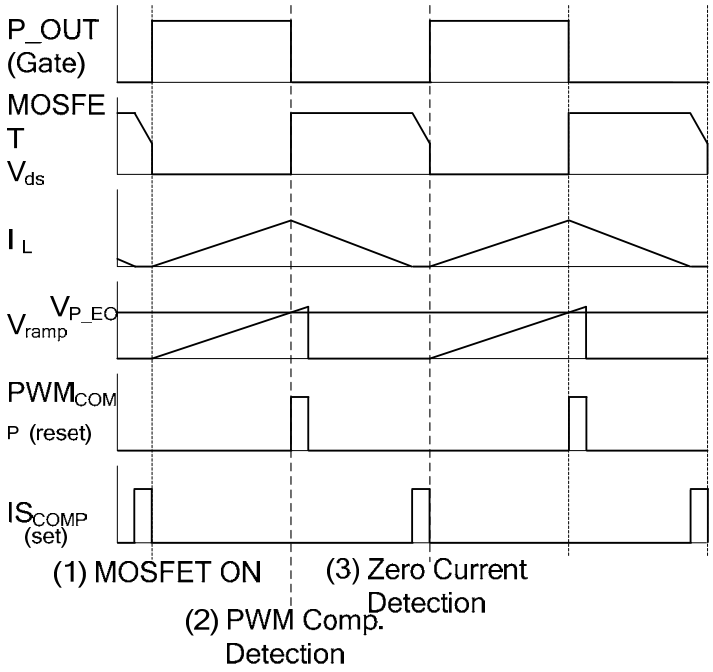


Figure 25. The Switching Timing Chart.

(7-1) gmAMP

P_VS pin monitors a voltage divided level between resistors of output voltage. P_VS pin has the piled up ripple voltage of AC frequency (50Hz/60Hz).

The gmAMP filters this ripple voltage and controls the voltage level of P_EO, by responding to error of P_VS pin voltage and internal reference voltage V_{P_VSAMP} (typ.2.5V (1.625V)).

Please set cut-off frequency of filter at P_EO pin showed in Figure 26, to about 5~10Hz.

Gm constant is designed 44uA / V.

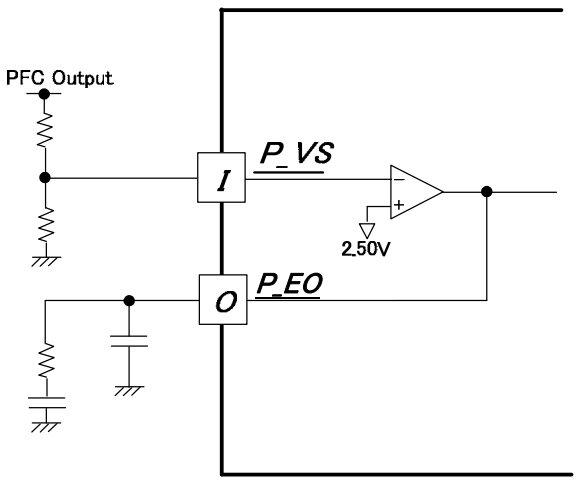


Figure 26. The Block Diagram of gmAMP.

(7-2) P_VS Short Protection

The PFC built-in short protection function at P_VS works by stopping switching at P_OUT when P_VS voltage < V_{P_SHORT} (typ:0.3V/0.195V: -92% voltage of PFC output). The operation is shown is Figure 27.

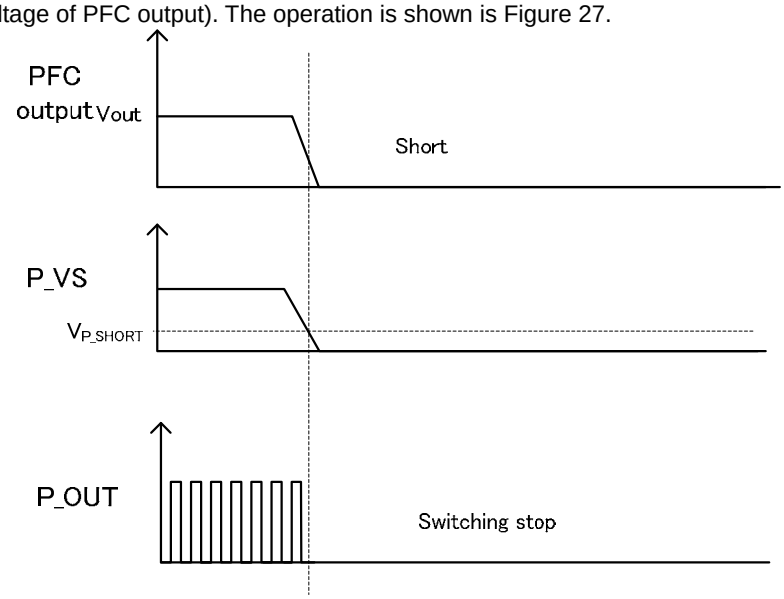


Figure 27. The Short Protection of P_VS Terminal..

(7-3) Gain Boost Function in P_VS low Voltage

There are instances where Dropping of output voltage by sudden load changes happens, because of slow PFC voltage response, output voltage is low for a long time. Therefore, PFC speeds up voltage control loop gain when P_VS pin voltage is low around V_{PGUP} (typ.2.25V) (Output voltage - 10%). In the operation, ON-duty at P_OUT pin increases, PFC prevents output voltage from dropping for a long time. This operation is stopped when P_VS pin voltage is higher than V_{GUP} (typ.2.25V).

(7-4) Gain Decrease Function in P_VS over Voltage (Dynamic OVP)

In case the output voltage is high by starting up or sudden output load changes, and because PFC voltage response is slow, output voltage is high for a long time. Therefore, PFC speeds up voltage control loop gain when P_VS pin voltage is high around V_{P_OVP1} (typ.2.625). In this operation, ON-duty at P_OUT pin decreases, PFC prevents output voltage from rising for a long time. This operation is stopped when P_VS pin voltage is lower than Vp_ovp1(typ.2.625V).

(7-5) P_VS Over Voltage Protection Function (Static OVP)

PFC has a second built-in over voltage protection, for the case that P_VS voltage exceeds over the first over voltage protection voltage V_{P_OVP1}. In case of auto recovery, P_VS pin voltage is exceeded V_{P_OVP2} (typ.2.725V), switching is stopped instantly. When P_VS pin voltage decrease lower than V_{P_OVP2} (typ.2.725V), switching operation is re-start. Refer to Figure 28.

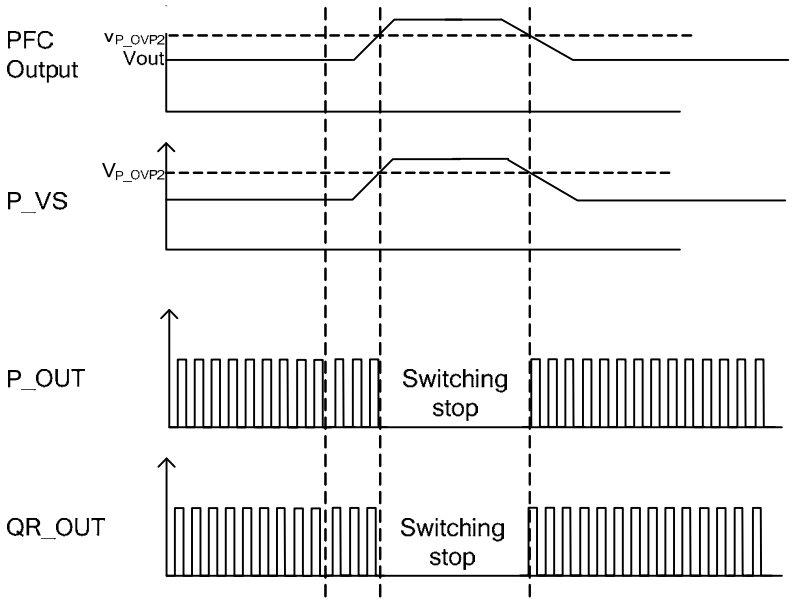


Figure 28. P_VS Over Voltage Protection (Auto Restart Mode).

(7-6) P_OVP Terminal Over Voltage Protection Function

P_OVP terminal has over voltage protection function to avoid P_OVP voltage increasing more than V_{P_OVP2} when P_VS feedback circuit is under abnormal condition and to stop PFC output (latch mode).
IC stops switching (latch mode) after timer count (16ms), P_OVP increases more than V_{P_OVP3} (typ.2.5V). Because of the timer, IC avoids detection error. The operation is shown is Figure 30.

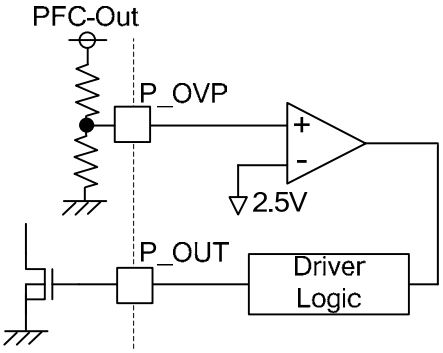


Figure 29. The Protection of P_POVP terminal(Latch mode).

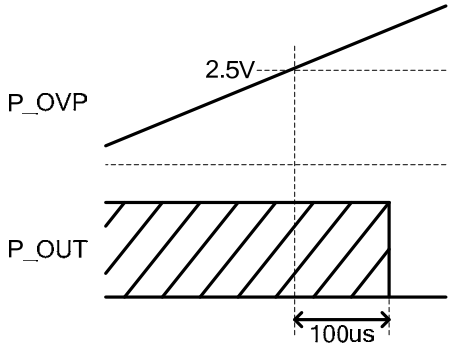


Figure 30. Timing Chart

(7-7) The P_IS Terminal Zero Current Detection and Over-Current Detection Function

Zero current detection circuit is used to sense the zero crossing of Inductor current (IL).
P_OUT output is set to be low after zero detection delay because P_IS voltage becomes more than zero current detection voltage. The over-current detection of an inductor current is set to be V_{th}=-0.6V (typ) of P_IS voltage.
To remove switching noise, we recommend additional CR filter in P_IS pin. The operation is shown is Figure 32.

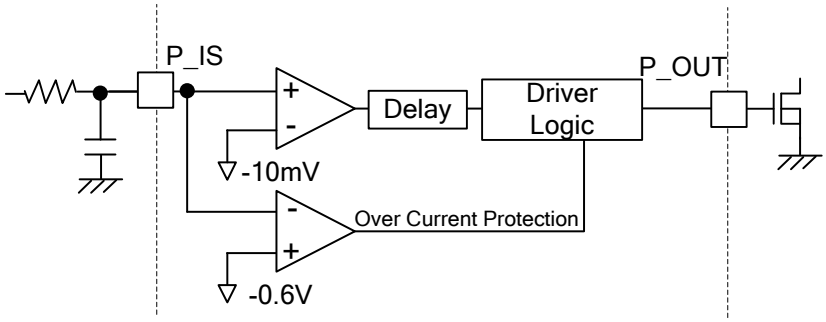


Figure 31. Current Detection Circuit of P_IS Terminal

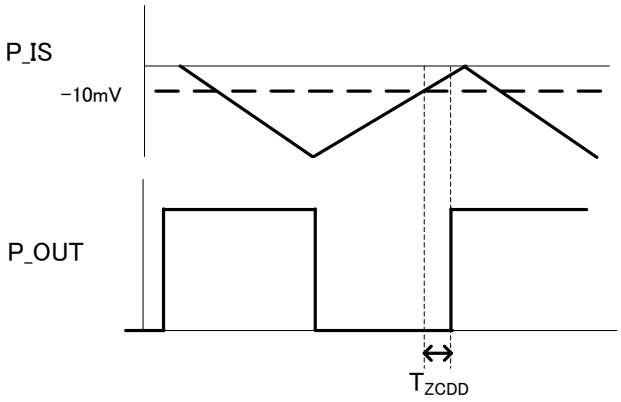


Figure 32. P_IS Zero Current Detection Delay Time

(7-8) P_RT Terminal

The frequency of the triangle waveform is generated by the oscillator block by external resistor on R_RT. The relationship of RT value and frequency is shown in Figure 34. The maximum ON width is calculated by the following expression on application.

$$T_{ON\_MAX}[s] = \frac{2 \times L \times P_O}{V_{ACMin}{}^2 \times \eta}$$

V_{AC}: Input power 、Inductor: L、Max output power(W)、Efficiency η

We recommend that the period set by P_RT terminal is to be more than max ON width (T_{ON_MAX}).
Also, to improve efficiency in light load mode, rising frequency is controlled by the frequency set by P_RT.
So the range of setting frequency is ≤400kHz(typ). External resistance range on the RT pin is 82kΩ≤390kΩ.
RT terminal can also set Delay time from the zero-crossing detection (Vth=-10mV) comparator output change point. (Refer to Figure 35).

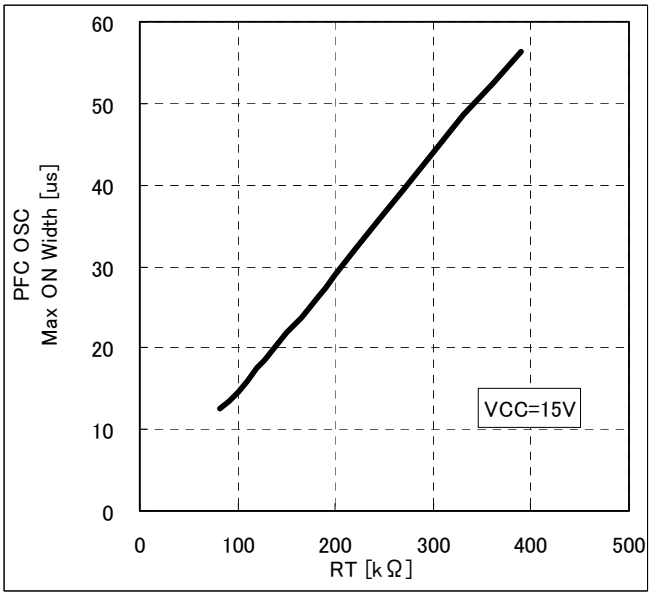


Figure 33. The Relationship of RT and Operation Frequency*

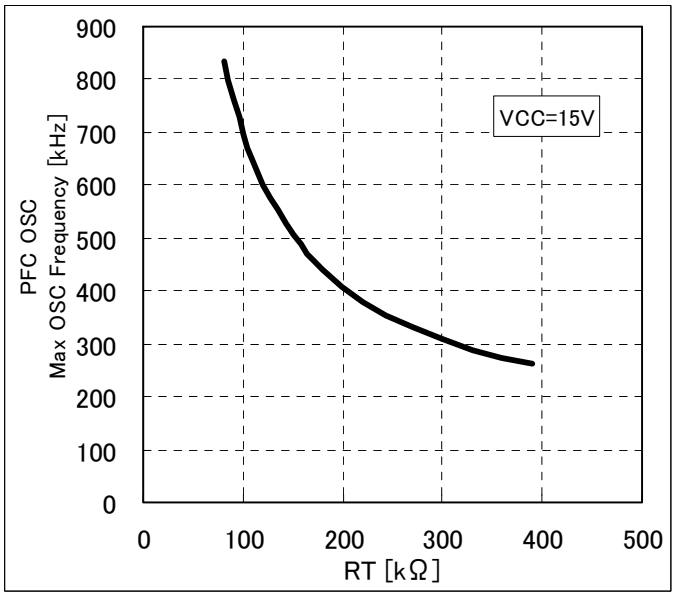


Figure 34. The Relationship of RT and ON Width*

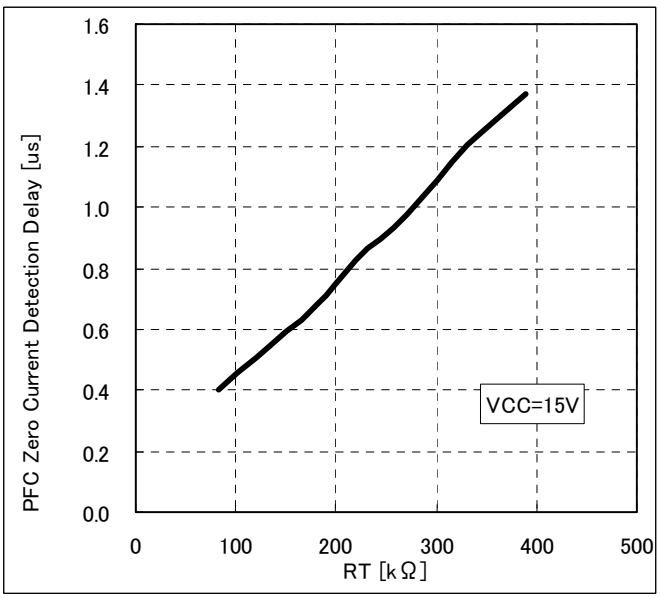


Figure 35. The Relationship of RT and PFC Zero Current Detection Delay*

*The above chart is for reference only. After confirmation of the actual device, please set the constant.

(7-9) PFC OFF Configuration Function

Figure 36 shows the operation circuit and Figure 37 shows timing chart. This function can be used to stop PFC block and to improve efficiency of the system for light load. The light load is detected when QR_FB`s voltage is low. The P_TIMER pin sets timer by capacitor's value to PFC stopping output from light load condition detection.

When QR_FB`s voltage is lower than P_OFFSET`s voltage in BM1C001F, the capacitor of P_TIMER pin starts to charge. When P_TIMER`s voltage is higher than 2.0V (typ), P_OUT is stopped. When QR_FB`s voltage is higher than P_OFFSET`s voltage, P_OUT starts again (Auto Restart).

For the stabilization of P_OFFSET pin voltage, connect a capacitor (1000pF≤) between the pin and GND. In addition, there is a need to connect a 140kΩ ≤ 400kΩ resistance to be connected to the P_OFFSET Pin. P_OFFSET pin and P_TIMER pin connect to GND if does not use PFC=OFF function. After start up, adjust VCC voltage not to change VCC recharge mode for stable work in light load mode.

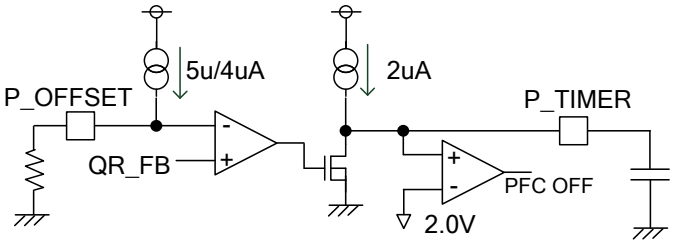


Figure 36. Operation Circuit

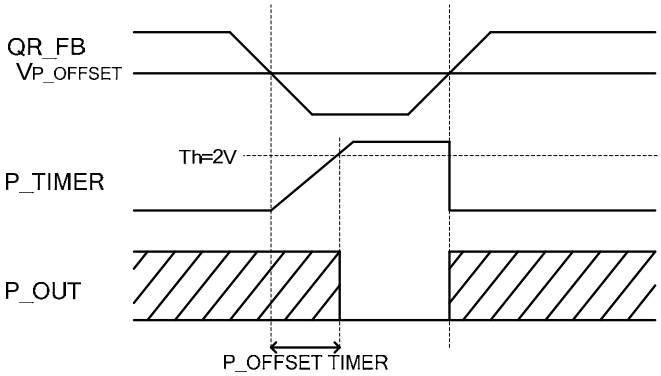


Figure 37. Timing Chart

Operation Mode of Protection Circuit

Operation mode of protection functions are shown in Table 3.

Table 3. Operation Mode of Protection Circuit.

Item	Comments	Operation Mode			
		Detection Method	Operation At Detection	Release Method	Operation At Release
VCCUVLO	VCC Pin Low Voltage Protection	VCC<8.2V （VCC Falling）	PFC Part, DC/DC Part STOP	VCC>13.5V （VCC Rising）	PFC Part, DC/DC Part Start Up Operation
VCCOVP	VCC Pin Over Voltage Protection	VCC>27.5V During 100us （VCC Rising）	PFC Part, DC/DC Part Latch STOP	VCC<7.7V （VCC Falling）	PFC Part, DC/DC Part Start Up Operation
Brown Out (PFC)	Input AC Voltage Low Voltage Protection	BR＜1.0V During 256ms （BR Falling）	PFC Part STOP, X-Cap Disharging	BR>1.0V （BR Rising）	Normal Operation
Brown Out (QR)	Input AC Voltage Low Voltage Protection	BR＜1.0V During 256ms （BR Falling）	DC/DC Part STOP	BR>1.0V （BR Rising）	Normal Operation
COMP	COMP Pin Protection	COMP<0.5V During 150us （COMP Falling）	PFC Part, DC/DC Part Latch Stop	VCC<7.7V （VCC Falling）	PFC Part, DC/DC Part Start Up Operation
QR_FB_OLP	QR_FB Pin Over-Current Protection	QR_FB>2.8V During 256ms （QR_FB Rising）	DC/DC ,PFC Parts STOP	QR_FB<2.6V During 2048ms （QR_FB Falling）	Normal Operation
QR_ZT OVP	QR_ZT Pin Over Voltage Protection	QR_ZT>5.0V During 100us （QR_QR_ZT Rising）	DC/DC, PFC Parts Latch Stop	VCC<7.7V （VCC Falling）	Normal Operation
P_IS OCP	P_IS Pin Short Protection	P_IS<-0.60V （P_IS Falling）	PFC Part Output STOP	P_IS>-0.60V （P_IS Rising）	Normal Operation
P_VS Short Protection 1(2)	P_VS Pin Short Protection	P_VS<0.300V(0.195V) （P_VS Falling）	PFC Part Operation STOP	P_VS>0.300V(0.195V) （P_VS Rising）	Normal Operation
P_VS Gain rise voltage1(2)	P_VS Pin Low Voltage Gain Boost Function	P_VS<2.250V(1.462V) （P_VS Falling）	Gm-Amp. GAIN Boost	P_VS>2.250V(1.462V) （P_VS Rising）	Normal Operation
P_VS Gain fall voltage1(2)	P_VS Pin Dynamic Over Voltage Protection	P_VS>2.625V(1.706V) （P_VS Rising）	Gm-Amp. GAIN Down	P_VS<2.625V(1.706V) （P_VS Falling）	Normal Operation
P_VS over voltage protection1(2)	P_VS Pin Static Over Voltage Protection	P_VS>2.725V(1.771V) （P_VS Rising）	PFC Part STOP	P_VS<2.600V(1.690V) （P_VS Falling）	Normal Operation
P_OVP OVP	P_OVP Pin Over Voltage Protection	P_OVP>2.5V （P_VS Rising）	PFC Part, DC/DC Part Latch Stop	VCC<8.2V （VCC Falling）	PFC Part, DC/DC Part Start Up Operation
P_TIMER	P_TIMER Pin Protection Function	P_TIMER>2.0V （P_TIMER Rising）	PFC Part STOP	FB>P_OFFSET (FB Rising)	Normal Operation

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit	Conditions
Maximum Applied Voltage 1	V_{max1}	-0.3 to +30.0	V	VCC
Maximum Applied Voltage 2	V_{max2}	-0.3 to +650	V	VH_IN
Maximum Applied Voltage 3	V_{max3}	-0.3 to +15.0	V	P_OUT, QR_OUT
Maximum Applied Voltage 4	V_{max4}	-0.3 to +6.5	V	QR_FB, COMP, P_VS, BR, P_OVP, P_RT, P_OFFSET, P_VS, QR_CS, P_TIMER
Maximum Applied Voltage 5	V_{max5}	-0.3 to +7.0	V	QR_ZT
Maximum Applied Voltage 6	V_{max6}	-6.5 to +0.3	V	P_IS
P_OUT Pin Output Peak Current 1	I_{P_OUT1}	-0.5	A	
P_OUT Pin Output Peak Current 2	I_{P_OUT2}	+1.0	A	
QR_OUT Pin Output Peak Current 1	I_{QR_OUT1}	-0.5	A	
QR_OUT Pin Output Peak Current 2	I_{QR_OUT2}	+1.0	A	
Allowable Dissipation	P_d	0.68 (Note1)	W	mounted
Operating Temperature Range	T_{opr}	-40 to +105	°C	
Storage Temperature Range	T_{str}	-55 to +150	°C	

(Note1) Derate by 5.5 mW/°C when operating above Ta = 25°C when mounted (on 70 mm × 70 mm, 1.6 mm thick, glass epoxy on single-layer substrate).
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta = 25°C)

Parameter	Symbol	Rating	Unit	Conditions
Power supply voltage range 1	V_{CC}	8.9 to 26.0	V	VCC Pin Voltage
Power supply voltage range 2	V_H	80 to 600	V	VH_IN Pin Voltage

Recommended External Parts (Ta = 25°C)

Parameter	Symbol	Rating	Unit
VCC Pin Capacitor	C_{VCC}	1.0 ≤	μF
BR Pin Capacitor	C_{BR}	0.1 to 100	nF
P_RT Pin Resistor	R_{P_RT}	82 to 390	kΩ
P_OFFSET Pin Capacitor	C_{P_OFFSET}	1000 ≤	pF
P_OFFSET Pin Resistor	R_{P_OFFSET}	140 ≤ (400)	kΩ

Electrical Characteristics (Unless otherwise noted, Ta=25°C, VCC=15V)

Parameter	Symbol	Specifications			Unit	Conditions
		Minimum	Standard	Maximum		
[Circuit Current]						
Circuit current (ON) 1	I_{ON1}	-	1.0	1.4	mA	PFC=OFF QR_FB=2.0V (During Pulse Operation)
Circuit current (ON) 2	I_{ON2}	-	1.2	1.7	mA	PFC=ON QR_FB=2.0V (During Pulse Operation)
Circuit current (ON) 3	I_{ON3}	-	600	780	μA	PFC=OFF FB=0.0V (During Burst Operation)
[Start-Up Circuit Block]						
Start current 1	I_{START1}	0.4	0.7	1.0	mA	VCC= 0V
Start current 2	I_{START2}	1	3	5	mA	VCC=10V
OFF Current	I_{START3}	-	10	20	μA	Input Current from VH _IN Terminal after Releasing UVLO
VH voltage switched start current	V_{SC}	0.8	1.5	2.1	V	
[VCC Pin Protection Function]						
VCC UVLO voltage1	V_{UVLO1}	12.5	13.5	14.5	V	VCC Rise
VCC UVLO voltage 2	V_{UVLO2}	7.5	8.2	8.9	V	VCC Drop
VCC UVLO hysteresis	V_{UVLO3}	-	5.3	-	V	V_{UVLO3} =V_{UVLO1} -V_{UVLO2}
VCC charge start voltage	V_{CHG1}	7.7	8.7	9.7	V	Start Circuit Operation Voltage
VCC charge end voltage	V_{CHG2}	12	13	14	V	Stop Voltage from V_{CHG1}
VCC OVP voltage 1	V_{OVP1}	26.0	27.5	29.0	V	VCC Rise
[BR Pin (7pin)]						
BR detect voltage1	V_{BR1}	0.92	1.00	1.08	V	BR Rise
BR detect voltage 2	V_{BR2}	-	0.70	-	V	BR Fall
BR hysteresis	V_{BRHYS}	-	0.30	-	V	
BR timer	$T_{BRTIMER}$	204	256	307	ms	PFC, DCDC Stop, Discharge Start
ACIN Detect Voltage	V_{ACIN1}	2.25	2.50	2.75	V	
[COMP Pin (5pin)]						
COMP pin detect voltage	V_{COMP}	0.37	0.50	0.63	V	
COMP pin pull-up resistor	R_{COMP}	19.4	25.9	32.3	kΩ	
Thermistor resistor detection value	R_T	3.32	3.70	4.08	kΩ	
Latch release voltage (VCC pin voltage)	$T_{BRTIMER}$	-	V_{UVLO}-0.5	-	V	
Latch mask time	T_{COMP}	-	150	240	μs	

Electrical Characteristics – continued (Unless otherwise noted, Ta=25, VCC=15V)

Parameter	Symbol	Specifications			Unit	Conditions
		Minimum	Standard	Maximum		
[P_OFFSET block]						
P_OFFSET source current 1	$I_{OFFSET1}$	3.6	4.0	4.4	μA	
P_OFFSET source current 2	$I_{OFFSET2}$	4.5	5.0	5.5	V	
P_OFFSET setting voltage	V_{p_OFFSET}	0.50	0.64	0.78	μA	P_OFFSET Pin = Open
P_OFFSET setting voltage hys	$V_{p\_OFFSET\ hys}$	0.12	0.16	0.20	V	P_OFFSET Pin = Open
[P_TIMER Pin]						
P_TIMER source current	I_{PTIMER}	1.6	2.0	2.4	μA	
P_TIMER detection voltage	$V_{P\ TIMER}$	1.9	2.0	2.1	V	P_TIMER Rise
[PFC Part Gm Amplifier Block]						
P_VS pin pull-up current	$I_{P\ VS}$	-	0.5	-	μA	
Gm Amp. normal voltage 1	$V_{P\ VSAMP1}$	2.46	2.50	2.56	V	
Gm Amp. normal voltage 2	$V_{P\ VSAMP2}$	1.544	1.625	1.706	V	
Gm Amp. trans conductance	$T_{P\ VS}$	30.8	44.0	59.2	μA/V	
Maximum Gm amplifier source current	$I_{P\_EO\_source}$	15	25	35	μA	P_VS=1.0V
Maximum Gm amplifier sink current	$I_{P\_EO\_sink}$	24	40	56	μA	P_VS=3.5V
[PFC Part OSC Block]						
Maximum ON width	$T_{MAXDUTY}$	24	30	36	μs	RT=220kΩ
Maximum oscillation frequency	$F_{MAXDUTY}$	320	400	480	kHz	RT=220kΩ
[PFC Part OSC Block]						
Zero current detection voltage	V_{ZCD}	-15m	-10m	-5m	V	
Zero current detection voltage Delay	T_{ZCDD}	-	0.85	1.70	μs	
IS over-current detection voltage	V_{IS_OCP}	-0.625	-0.600	-0.575	V	
[PFC Part protection Block]	**Figure of (%) is the ratio of VS standard voltage (1: 2.5V, 2:1.625V).**					
P_VS short protection voltage1	V_{P_SHORT1}	0.200 (-92%)	0.300 (-88%)	0.400 (-84%)	V	ACIN=H
P_VS short protection voltage2	V_{P_SHORT2}	0.130 (-92%)	0.195 (-88%)	0.260 (-84%)	V	ACIN=L
P_VS gain rise voltage1	V_{PGUP1}	2.050 (-18%)	2. 250 (-10%)	2.450 (-2%)	V	ACIN=H
P_VS gain rise voltage2	V_{PGUP2}	1.332 (-18%)	1.462 (-10%)	1.593 (-2%)	V	ACIN=L
P_VS gain fall voltage 1	V_{P_OVP1}	-	2.625 (+5%)	-	V	ACIN=H
P_VS gain fall voltage 2	V_{P_OVP2}	-	1.706 (+5%)	-	V	ACIN=L
P_VS over voltage protection detection voltage1 (auto recovery)	V_{P_OVP1}	-	2.725 (+9%)	-	V	ACIN=H
P_VS over voltage protection detection voltage2 (auto recovery)	V_{P_OVP2}	-	1.771 (+9%)	-	V	ACIN=L
[PFC Part OVP Block]						
PFC OVP pin detection voltage	V_{COMP}	2.43	2.50	2.57	V	
PFC OVP pin detection timer	T_{PFCOVP}	-	100	200	μsec	
[PFC Part OUT Block]						
P_OUT pin H voltage	V_{OUTH}	10.5	12.5	14.5	V	IO = -20mA
P_OUT pin L voltage	V_{OUTL}	-	-	1.00	V	IO = +20mA
P_OUT pin pull down resistor	R_{PDOUT}	75	100	125	kΩ	

* Definition of ACIN (L : BR Pin Voltage < 2.5V, H : BR Pin Voltage > 2.5V)

Electrical Characteristics – continued (Unless otherwise noted, Ta=25, VCC=15V)

Parameter	Symbol	Specifications			Unit	Conditions
		Minimum	Standard	Maximum		
[DC/DC Convertor Block (Turn Off)]						
FB pin pull-up resistor	R_{FB}	22.5	30.0	37.5	kΩ	
CS over-current detect voltage 1A	V_{lim1A}	0.475	0.500	0.525	V	FB=2.2V (ACIN=L)
CS over-current detect voltage 1B	V_{lim1B}	0.310	0.350	0.390	V	FB=2.2V (ACIN=H)
CS over-current detect voltage 2A	V_{lim2A}	0.100	0.125	0.150	V	FB=0.5V (ACIN=L)
CS over-current detect voltage 2B	V_{lim2B}	0.062	0.088	0.113	V	FB=0.5V (ACIN=H)
Voltage gain 1 (⊿VFB/⊿VCS)	AV_{CS1}	3.40	4.00	4.60	V/V	ACIN=L
Voltage gain 2 (⊿VFB/⊿VCS)	AV_{CS2}	4.86	5.71	6.57	V/V	ACIN=H
CS Leading Edge Blanking time	T_{LEB}	-	0.250	-	μs	
Turn off time	T_{OFF}	-	0.250	-	μs	PULSE is Applied to CS Pin
Minimum ON width	T_{min}	-	0.500	-	μs	$T_{LEB} + T_{OFF}$
Maximum ON width	T_{max}	29.0	43.0	57.2	μs	
[DC/DC Convertor Block (Turn Off)]						
Maximum operating frequency 1	F_{SW1}	108	120	132	kHz	FB=2.0V
Maximum operating frequency 2	F_{SW2}	22	30	39	kHz	FB=0.5V
Frequency reduction start FB voltage	V_{FBSW1}	1.10	1.25	1.40	V	
Frequency reduction end FB voltage	V_{FBSW2}	0.45	0.50	0.55	V	
ZT comparator voltage 1	V_{ZT1}	60	100	140	mV	ZT fall
ZT comparator voltage 2	V_{ZT2}	120	200	280	mV	ZT rise
ZT trigger mask time	T_{ZTMASK}	-	0.6	-	μs	OUT H to L, for Protection Noise
ZT trigger timeout period 1	T_{ZTOUT1}	11.7	17.5	23.2	μs	The Operation Without Bottom Detection
ZT trigger timeout period 2	T_{ZTOUT2}	3.9	5.8	7.7	μs	Count from Final ZT Trigger
[DC/DC Convertor Block (Protection)]						
Soft start time 1	T_{SS1}	0.35	0.50	0.65	ms	
Soft start time 2	T_{SS2}	0.70	1.00	1.30	ms	
Soft start time 3	T_{SS3}	1.40	2.00	2.60	ms	
Soft start time 4	T_{SS4}	2.80	4.00	5.20	ms	
FB burst voltage 1	V_{BURST1}	0.435	0.500	0.565	V	FB Fall
FB burst voltage 2	V_{BURST2}	0.479	0.550	0.621	V	FB Rise
FB OLP voltage a	V_{FOLP1A}	2.6	2.8	3.0	V	Over Load Detection (FB Fall)
FB OLP voltage b	V_{FOLP1B}	-	2.6	-	V	Over Load Detection (FB Rise)
FB OLP detection timer	T_{FOLP}	197	256	333	ms	
FB OLP stop timer	T_{OLPST}	1433	2048	2664	ms	
Latch release voltage (VCC pin voltage)	V_{LATCH}	-	V_{UVLO2} – 0.50	-	V	
Latch mask time	T_{LATCH}	50	100	200	μs	
ZT OVP voltage	V_{ZTL}	4.64	5.00	5.36	V	
[DC/DC OUT Block]						
QR_OUT Pin H Voltage	V_{QROUTH}	10.5	12.5	14.5	V	IO=-20mA
QR_OUT Pin L Voltage	V_{QROUTL}	-	-	1.00	V	IO=+20mA
QR_OUT Pin Pull-Down Res.	R_{QRDOUT}	75	100	125	kΩ	

* Definition of ACIN (L : BR Pin Voltage < 2.5V, H : BR Pin Voltage > 2.5V)

Power Dissipation

The thermal design should set operation for the following conditions.
(Since the temperature shown below is the guaranteed temperature, be sure to take a margin into account.)

1. The ambient temperature Ta must be 105°C or less.
2. The IC's loss must be within the allowable dissipation Pd.

The thermal abatement characteristics are as follows.
(PCB: 70 mm × 70 mm × 1.6 mm, mounted on glass epoxy substrate)

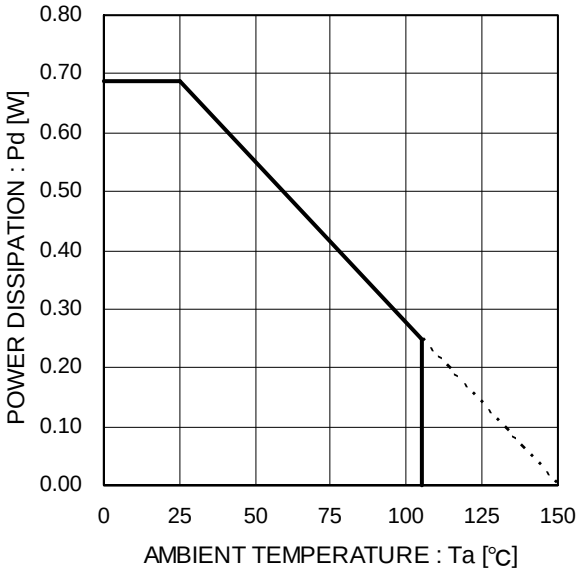


Figure 38. Thermal Abatement Characteristics

I/O Equivalence Circuits

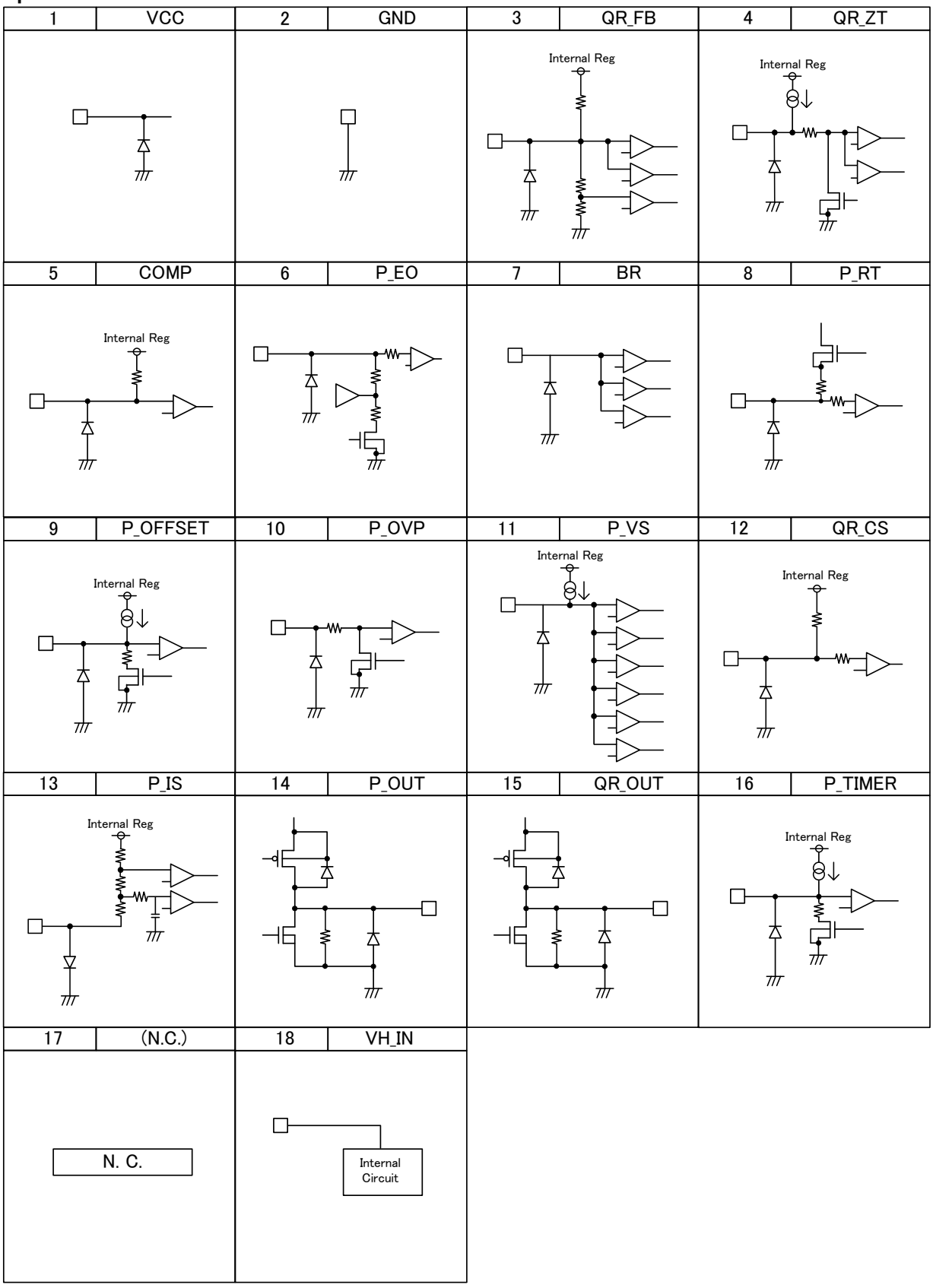


Figure 39. I/O Equivalent Circuit Diagram

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded, the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Rush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Terminals

Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

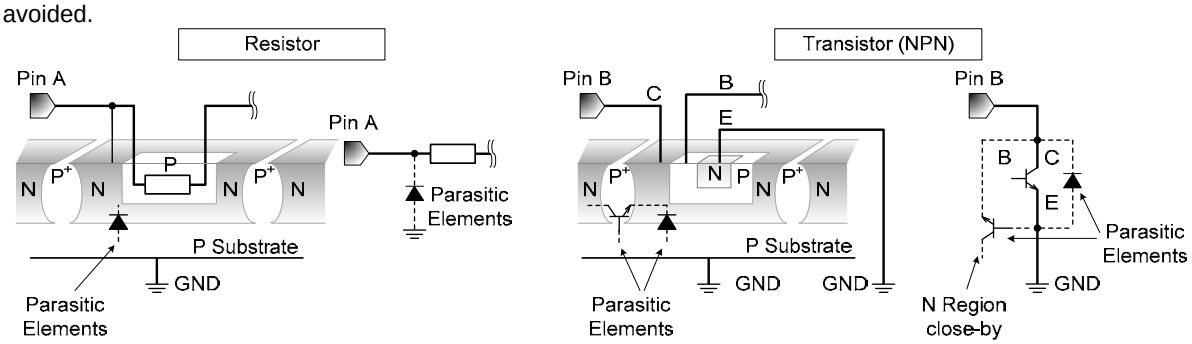


Figure 40. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

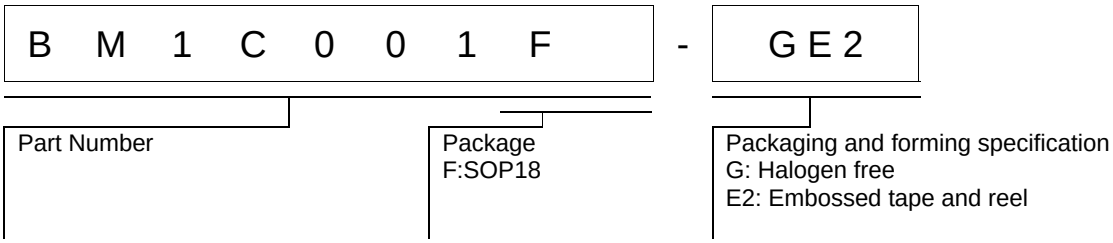
16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

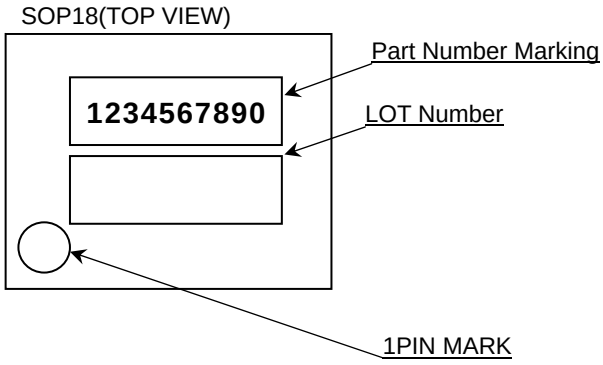
Status of this document
The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document formal version takes priority

Ordering Information



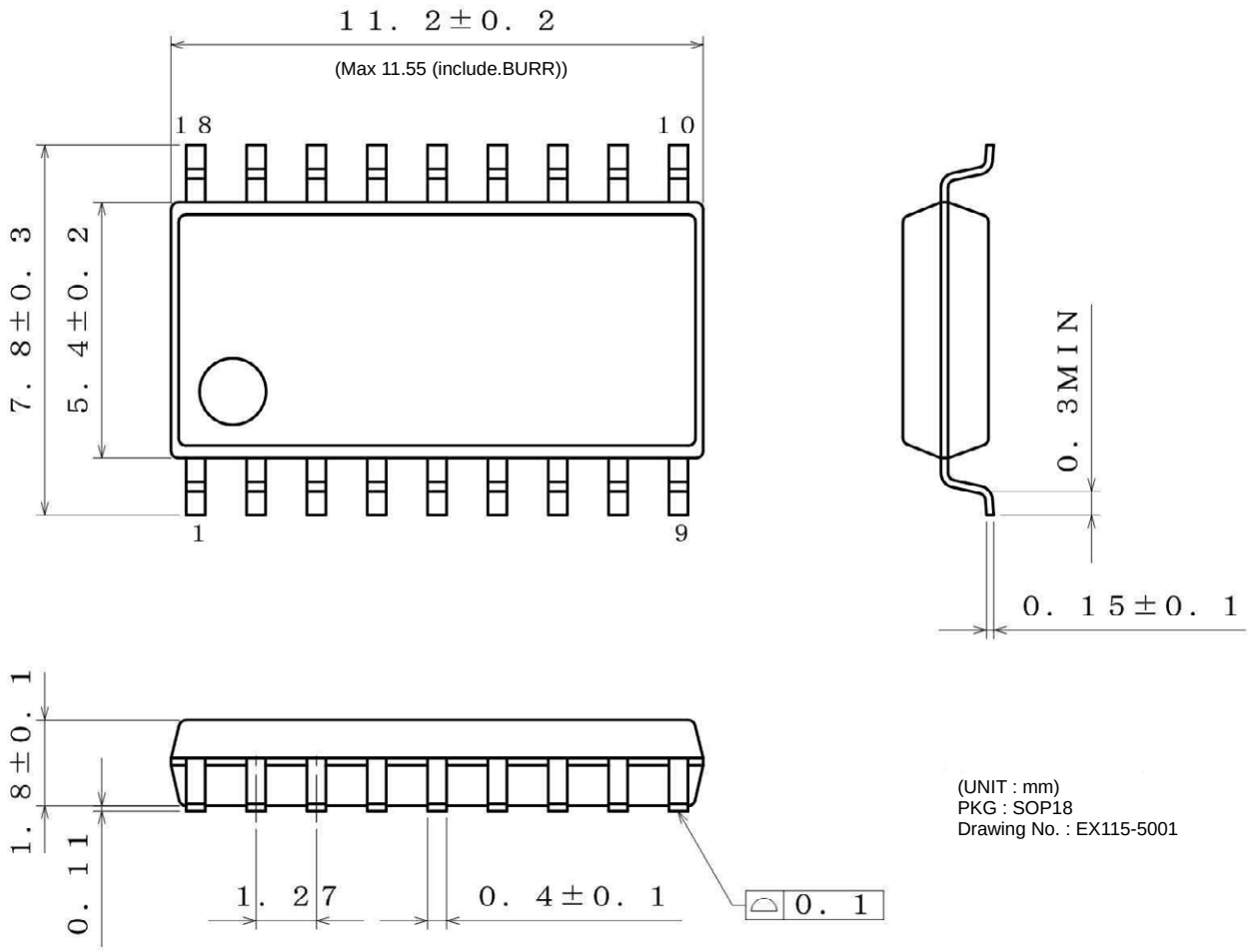
Marking Diagrams



Part Number Marking	Package	Orderable Part Number
BM1C001F	SOP18	BM1C001F-GE2

Physical Dimension, Tape and Reel Information

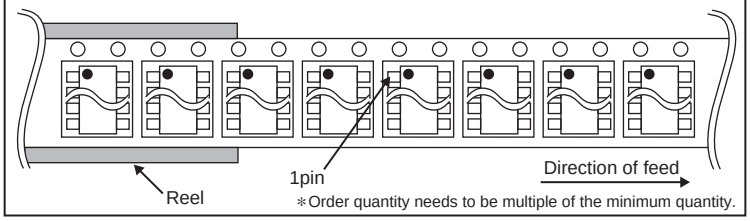
Package Name	SOP18



(UNIT : mm)
PKG : SOP18
Drawing No. : EX115-5001

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
5.Aug.2013	001	New Release
28.Aug.2013	002	Page 25. Maximum ON width: 30 / 42 / 54 -> 29.0 / 43.0 / 57.2 us ZT trigger timeout period 1: 10.5 / 15.0 /19.5 -> 11.7 / 17.5 / 23.2 us ZT trigger timeout period 2: 3.5 / 5.0 / 6.5 -> 3.9 / 5.8 / 7.7 us FB burst voltage 1: 0.450 / 0.500 / 0.550 -> 0.435 / 0.500 / 0.565 V FB burst voltage 2: 0.495 / 0.550 / 0.605 -> 0.479 / 0.550 / 0.621 V Page22. Absolute Maximum Ratings: “Caution” and “P_OVP” Pin Added. Others: Each figure appearance modification.
07.Mar.2014	003	Page04 Starter Block : correct a explanation Page06 VCC charge Function : correct a explanation Page06,07 Figure8 : correct a explanation Page11 Figure 17 : correct a explanation Page11 Table2 : correction Page12 QR_CS Pin Over-Current Protection Switching Function : correct a explanation Page14 OUTPUT Over Load Protection : correct a explanation

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1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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