

Octal D-type flip-flop; positive edge-trigger; 3-state**74LVC374****FEATURES**

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- Inputs accept voltages upto 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- 8-bit positive edge-triggered register
- Independent register and 3-state buffer operation
- Output drive capability 50 Ω transmission lines @ 85 °C

DESCRIPTION

The 74LVC374 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC374 is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The eight flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the eight flip-flops is available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops. The '374' is functionally identical to the '574', but the '574' has a different pin arrangement.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $t_r = t_f \leq 2.5\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	$C_L = 50\text{ pF}$ $V_{CC} = 3.3\text{ V}$	4.8	ns
f_{max}	maximum clock frequency		150	MHz
C_i	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	28	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is $V_i = \text{GND to } V_{CC}$.

ORDERING INFORMATION

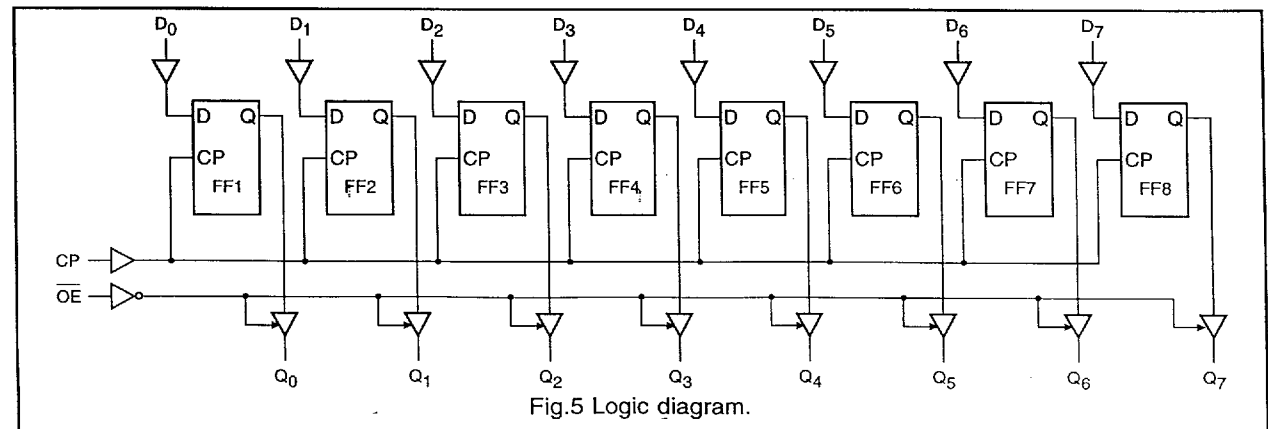
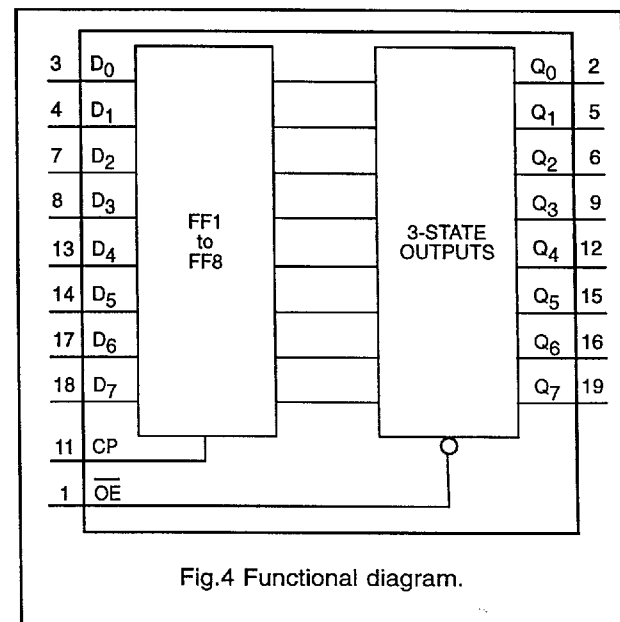
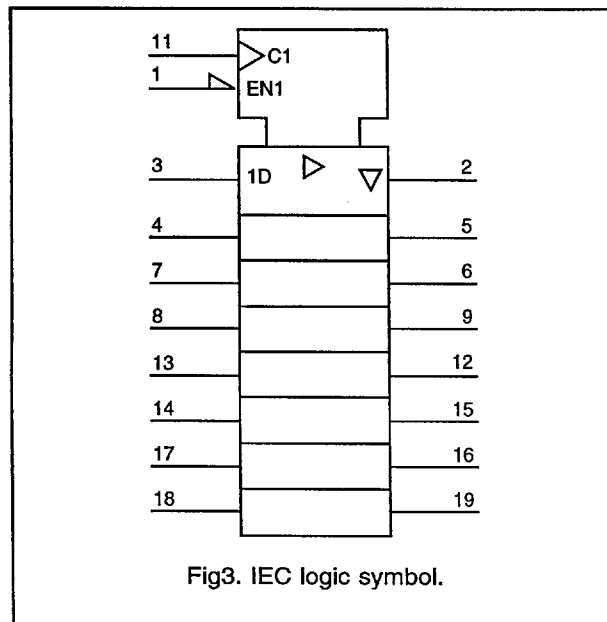
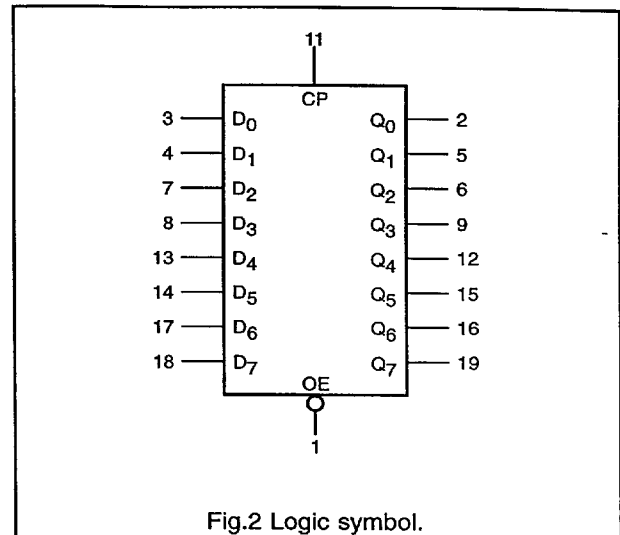
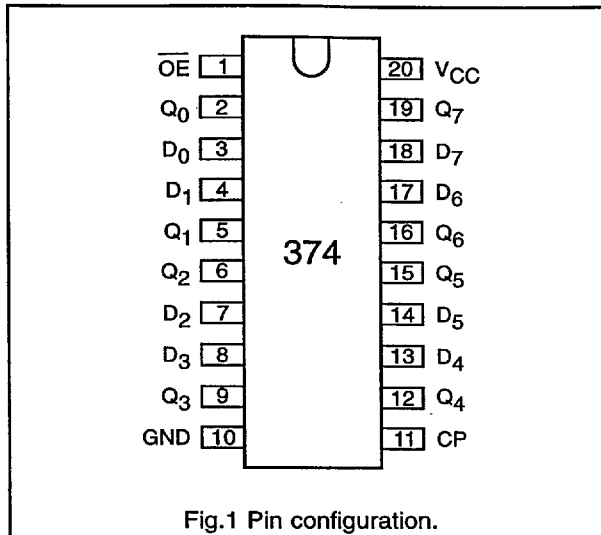
TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC374D	20	SO	plastic	SOT163-1
74LVC374DB	20	SSOP	plastic	SOT339-1
74LVC374PW	20	TSSOP	plastic	SOT360-1

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0 to Q_7	3-state flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	positive supply voltage

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FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS Q ₀ to Q ₇
	$\overline{OE}$	CP	D _n		
load and read register	L	↑	l	L	L
	L	↑	h	H	H
load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition

L = LOW voltage level

l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition

Z = high impedance OFF-state

↑ = LOW-to-HIGH clock transition

DC CHARACTERISTICS FOR 74LVC374

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74LVC374

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

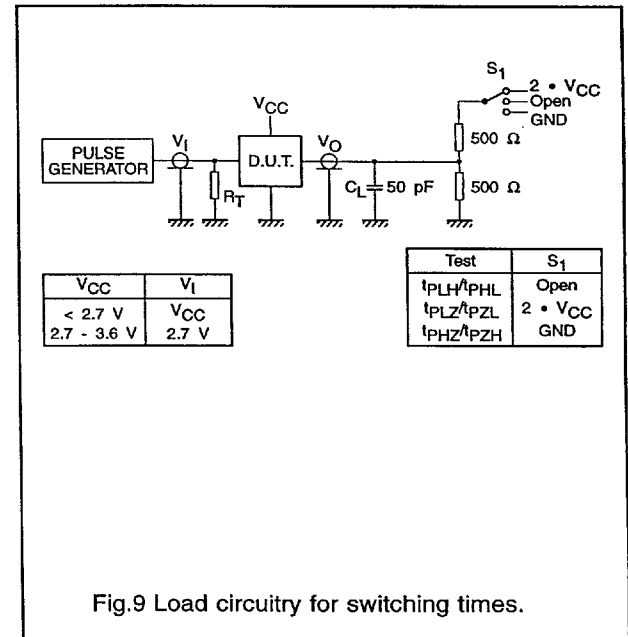
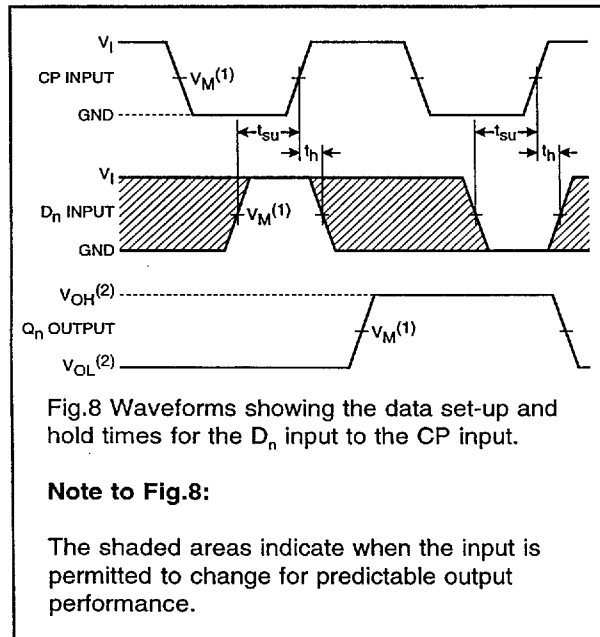
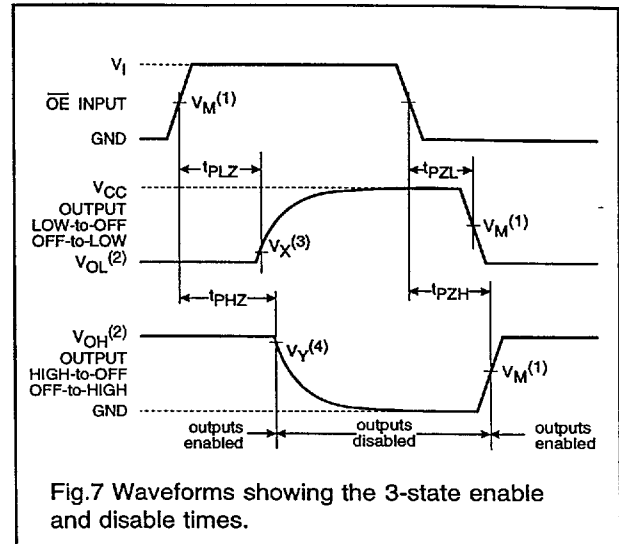
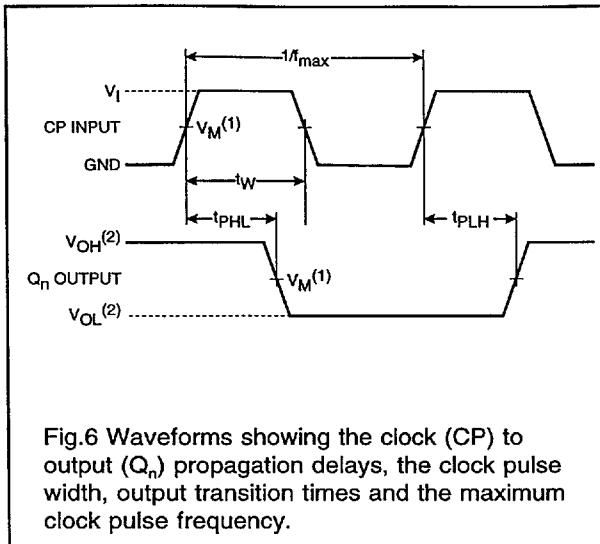
SYMBOL	PARAMETER	T _{amb} (°C)			UNIT	TEST CONDITIONS	
		-40 to +85				V _{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
t _{PHL} /t _{PLH}	propagation delay CP to Q _n	— 1.5 1.5	21 5.2 4.8*	— 9.5 8.5	ns	1.2 2.7 3.0 to 3.6	Figs 6, 9
t _{PZH} /t _{PZL}	3-state output enable time OE to Q _n	— 1.5 1.5	17 4.4 4.0*	— 8.0 7.5	ns	1.2 2.7 3.0 to 3.6	Figs 7, 9
t _{PHZ} /t _{PLZ}	3-state output disable time OE to Q _n	— 1.5 1.5	8.0 3.6 3.5*	— 6.5 6.0	ns	1.2 2.7 3.0 to 3.6	Figs 7, 9
t _w	clock pulse width HIGH or LOW	— —	3.0 3.0*	— —	ns	2.7 3.0 to 3.6	Fig.6
t _{su}	set-up time D _n to CP	— —	0.5 0.4*	— —	ns	2.7 3.0 to 3.6	Fig.8
t _h	hold time D _n to CP	1.0 1.0	-0.5 -0.4*	— —	ns	2.7 3.0 to 3.6	Fig.8
f _{max}	maximum clock pulse frequency	— 75	— 150*	— —	MHz	2.7 3.0 to 3.6	Fig.6

Notes: All typical values are measured at T_{amb} = 25 °C.* Typical values are measured at V_{CC} = 3.3 V.

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AC WAVEFORMS



- Notes:**
- (1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
 $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
 - (2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load
 - (3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
 $V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
 - (4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
 $V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V