

To all our customers

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Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

M66312P/FP

8-BIT LED DRIVER WITH SHIFTRREGISTER AND LATCHED 3-STATE OUTPUTS

DESCRIPTION

M66312 is a LED array driver having a 8-bit serial input and parallel output shiftrregister function with 3-state output latch.

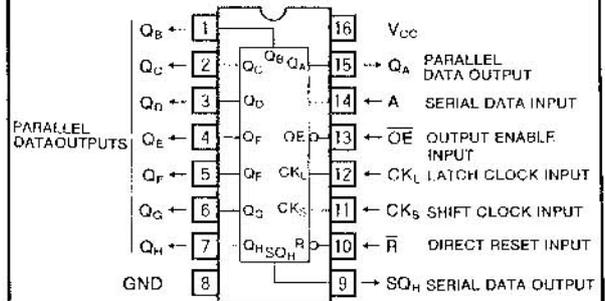
This product guarantees the output electric current of 16mA which is sufficient for LED drive, capable of flowing 8 bits continuously at the same time, and use either of cathode common LED and anode common LED.

In addition, as this product has been designed in complete CMOS, power consumption can be greatly reduced when compared with conventional BIPOLAR or Bi-CMOS products.

FEATURES

- High output current $I_{OL}=16\text{mA}$, $I_{OH}=-16\text{mA}$
- High speed (clock frequency) : 30MHz (typ)
($C_L=50\text{pF}$, $V_{CC}=5\text{V}$)
- Low power dissipation : 20 μW /package (max)
($V_{CC}=5\text{V}$, $T_a=25^\circ\text{C}$, quiescent state)
- 3-state output (except serial data output)
- Wide operating temperature range : $T_a=-40\sim+85^\circ\text{C}$

PIN CONFIGURATION (TOP VIEW)

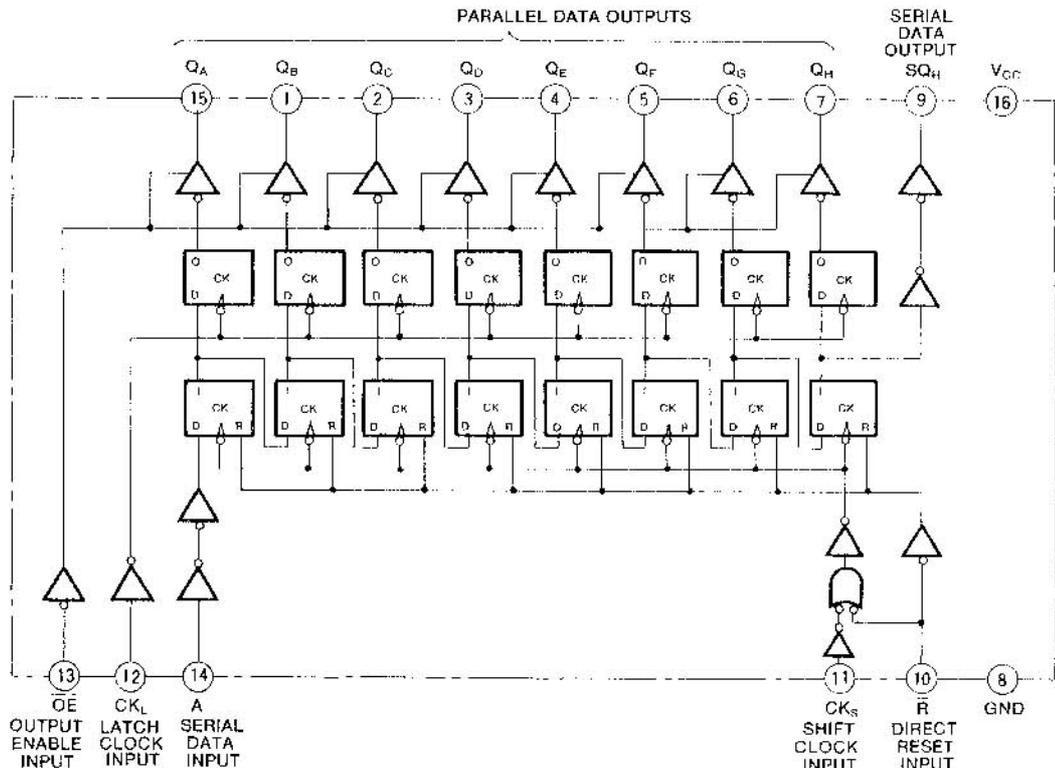


Outline 16P4
16P2N-A

APPLICATION

- LED array drive of PRINTER
- LED array drive of BUTTON TELEPHONE

LOGIC DIAGRAM



8-BIT LED DRIVER WITH SHIFTRREGISTER AND LATCHED 3-STATE OUTPUTS

FUNCTIONAL DESCRIPTION

As M66312 uses silicon gate CMOS process, it realizes high-speed and high-output currents sufficient for LED drive while maintaining low power consumption and allowance for high noises.

Each bit of a shiftrregister consists of two flip-flops having independent clocks for shifting and latching.

As for clock input, shift clock input CK_S and latch clock input CK_L are independent from each other, shift and latch operations being made when "L" changes to "H".

Serial data input A is the data input of the first-step shiftrregister and the signal of A shifts shiftrregisters one by one when a pulse is impressed to CK_S. When A is "H", the signal of "H" shifts. When A is "L", the signal of "L" shifts.

When the pulse is impressed to CK_L, the contents of the

shifting register at that time are stored in a latching register, and they appear in the output from Q_A through Q_H are 3-state outputs.

To extend the number of bits, serial data output SQ_H is used to output the 8-bit of the shift register.

By connecting CKs and CK_L, the shift register state delayed by 1 clock cycle is output at Q_A through Q_H.

When reset input \bar{R} is low, shift register and SQ_H will be reset. To reset Q_A through Q_H to low-level, CK_L must be changed from low-level to high-level after the shift register is reset by \bar{R} .

When output-enable input \overline{OE} is high, Q_A through Q_H will become high impedance state, but SQ_H is not changed. Even if \overline{OE} is changed, shift operation is not affected.

FUNCTION TABLE (Note : 1)

| Operation mode | | Input | | | | | Parallel data output | | | | | | | | Serial data output SQ _H |
|-----------------------|----------------------|-----------|-----------------|-----------------|---|-----------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|------------------------------------|
| | | \bar{R} | CK _S | CK _L | A | \overline{OE} | Q _A | Q _B | Q _C | Q _D | Q _E | Q _F | Q _G | Q _H | |
| Reset | Shift t ₁ | L | X | X | X | L | Q _A ⁰ | Q _B ⁰ | Q _C ⁰ | Q _D ⁰ | Q _E ⁰ | Q _F ⁰ | Q _G ⁰ | Q _H ⁰ | L |
| | Latch t ₂ | X | X | ↑ | X | L | L | L | L | L | L | L | L | L | L |
| Shift latch operation | Shift t ₁ | H | ↑ | X | H | L | Q _A ⁰ | Q _B ⁰ | Q _C ⁰ | Q _D ⁰ | Q _E ⁰ | Q _F ⁰ | Q _G ⁰ | Q _H ⁰ | q _A ⁰ |
| | Latch t ₂ | H | X | ↑ | X | L | H | q _A ⁰ | q _B ⁰ | q _C ⁰ | q _D ⁰ | q _E ⁰ | q _F ⁰ | q _G ⁰ | q _H ⁰ |
| | Shift t ₁ | H | ↑ | X | L | L | Q _A ⁰ | Q _B ⁰ | Q _C ⁰ | Q _D ⁰ | Q _E ⁰ | Q _F ⁰ | Q _G ⁰ | Q _H ⁰ | q _A ⁰ |
| | Latch t ₂ | H | X | ↑ | X | L | L | q _A ⁰ | q _B ⁰ | q _C ⁰ | q _D ⁰ | q _E ⁰ | q _F ⁰ | q _G ⁰ | q _H ⁰ |
| 3 state | | X | X | X | X | H | Z | Z | Z | Z | Z | Z | Z | Z | q _H |

- Note 1 : ↑ : Change from low-level to high-level
 Q⁰ : Output state Q before CK_L changed
 X : Irrelevant
 q⁰ : Contents of shift register before CK_S changed
 q : Contents of shift register
 t₁, t₂ : t₂ is set after t₁ is set
 Z : High impedance

8-BIT LED DRIVER WITH SHIFTRREGISTER AND LATCHED 3-STATE OUTPUTS

ABSOLUTE MAXIMUM RATINGS (T_a = -40 ~ +85°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Ratings | Unit |
|------------------|--------------------------------|----------------------------------|------------------------------|------|
| V _{CC} | Supply voltage | | -0.5 ~ +7.0 | V |
| V _I | Input voltage | | -0.5 ~ V _{CC} + 0.5 | V |
| V _O | Output voltage | | -0.5 ~ V _{CC} + 0.5 | V |
| I _{IK} | Input protection diode current | V _I < 0V | -20 | mA |
| | | V _I > V _{CC} | 20 | |
| I _{OK} | Output parasitic diode current | V _O < 0V | -20 | mA |
| | | V _O > V _{CC} | 20 | |
| I _O | Output current per output pin | Q _A ~ Q _H | ±35 | mA |
| | | SQ _H | ±25 | |
| I _{CC} | Supply/GND current | V _{CC} , GND | ±132 | mA |
| P _d | Power dissipation | (Note 2) | 500 | mW |
| T _{stg} | Storage temperature range | | -65 ~ +150 | °C |

Note 2 : M66312FP : T_a = -40 ~ +70°C, T_a = 70 ~ 85°C are derated at -6mW/°C.

RECOMMENDED OPERATING CONDITIONS (T_a = -40 ~ +85°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|-----------------|-------------------------------|------------------------|-----|-----------------|------|
| | | Min | Nom | Max | |
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | V |
| V _I | Input voltage | 0 | | V _{CC} | V |
| V _O | Output voltage | 0 | | V _{CC} | V |
| Topr | Operating temperature range | -40 | | +85 | °C |
| tr, tf | Input rising and falling time | V _{CC} = 4.5V | 0 | 500 | ns |
| | | V _{CC} = 5.5V | 0 | 400 | |

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 ~ 5.5V, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | | | Unit |
|------------------|---|--|--|---------------------------------|------------------------|---------------------------------|------------------------|------|
| | | | T _a = 25°C | | | | | |
| | | | Min | Typ | Max | Min | Max | |
| V _{IH} | High-level input voltage | V _O = 0.1V, V _{CC} = 0.1V I _O = 20μA | 0.70 × V _{CC} | | | 0.70 × V _{CC} | | V |
| V _{IL} | Low-level input voltage | V _O = 0.1V, V _{CC} = 0.1V I _O = 20μA | | | 0.30 × V _{CC} | | 0.30 × V _{CC} | V |
| V _{OZH} | High-level output voltage | V _I = V _{IH} , V _{IH} V _{CC} = 4.5V | I _{OH} = -20μA I _{OH} = -16mA | V _{CC} - 0.1 3.70 * | | V _{CC} - 0.1 3.55 * | | V |
| V _{OZH} | High-level output voltage | V _I = V _{IH} , V _{IL} V _{CC} = 4.5V | I _{OH} = -20μA I _{OH} = -4mA | V _{CC} - 0.1 4.0 | | V _{CC} - 0.1 3.9 | | V |
| V _{OL} | Low-level output voltage | V _I = V _{IH} , V _{IL} V _{CC} = 4.5V | I _{OL} = 20μA I _{OL} = 16mA | | 0.1 0.7 * | | 0.1 0.85 * | V |
| V _{OL} | Low-level output voltage | V _I = V _{IH} , V _{IL} V _{CC} = 4.5V | I _{OL} = 20μA I _{OL} = 4 mA | | 0.1 0.4 | | 0.1 0.5 | V |
| I _{IH} | High-level input current | V _I = V _{CC} , V _{CC} = 5.5V | | | 0.1 | | 1.0 | μA |
| I _{IL} | Low-level input current | V _I = GND, V _{CC} = 5.5V | | | -0.1 | | -1.0 | μA |
| I _{OZH} | Off state high-level output current Q _A ~ Q _H | V _I = V _{IH} , V _{IL} V _{CC} = 5.5V | V _O = V _{CC} | | 1.0 | | 10.0 | μA |
| I _{OZL} | Off state low-level output current Q _A ~ Q _H | V _I = V _{IH} , V _{IL} V _{CC} = 5.5V | V _O = GND | | -1.0 | | -10.0 | μA |
| I _{CC} | Quiescent supply current | V _I = V _{CC} , GND, V _{CC} = 5.5V | | | 4.0 | | 40.0 | μA |

* : Limits of single PIN operating state

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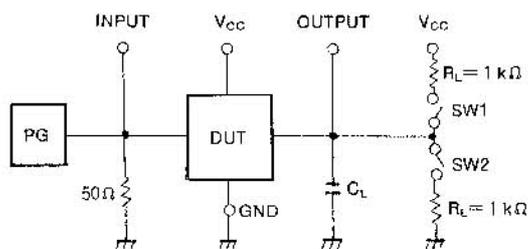
SWITCHING CHARACTERISTICS ($V_{CC}=5V$)

| Symbol | Parameter | Test conditions | Limits | | | | | Unit |
|-----------|---|-------------------------------|------------------------|-----|-----|--------------------------------|-----|------|
| | | | $T_a=25^\circ\text{C}$ | | | $T_a=-40\sim+85^\circ\text{C}$ | | |
| | | | Min | Typ | Max | Min | Max | |
| f_{max} | Maximum clock frequency | $C_L=50\text{pF}$ | 15 | | | 12 | | MHz |
| t_{PLH} | Low-level to high-level and high-level to low-level output propagation time $CK_S\text{-}SQ_{II}$ | $C_L=15\text{pF}$ (Note 3) | | | 70 | | 88 | ns |
| t_{PHL} | | | | | 70 | | 88 | ns |
| t_{PHL} | High-level to low-level output propagation time $\bar{R}\text{-}SQ_H$ | | | | 60 | | 76 | ns |
| t_{PLH} | Low-level to high-level and high-level to low-level output propagation time $CK_L\text{-}Q_A\sim Q_H$ | $C_L=50\text{pF}$ (Note 3) | | | 60 | | 76 | ns |
| t_{PHL} | | | | | 60 | | 76 | ns |
| t_{PLZ} | Output disable time from low-level and high-level | $C_L=5\text{pF}$ | | | 50 | | 64 | ns |
| t_{PHZ} | $OE\text{-}Q_A\sim Q_H$ | (Note 3) | | | 50 | | 64 | ns |
| t_{PZL} | Output enable time to low-level and high-level | $C_L=50\text{pF}$ | | | 56 | | 70 | ns |
| t_{PZH} | $OE\text{-}Q_A\sim Q_H$ | (Note 3) | | | 56 | | 70 | ns |

TIMING REQUIREMENTS ($V_{CC}=5V$)

| Symbol | Parameter | Test conditions | Limits | | | | | Unit |
|-----------|--|-----------------|------------------------|-----|-----|--------------------------------|-----|------|
| | | | $T_a=25^\circ\text{C}$ | | | $T_a=-40\sim+85^\circ\text{C}$ | | |
| | | | Min | Typ | Max | Min | Max | |
| t_w | CK_S, CK_L, \bar{R} pulse width | | 32 | | | 40 | | ns |
| t_{su} | A setup time with respect to CK_S | | 40 | | | 50 | | ns |
| t_{su} | CK_S setup time with respect to CK_L | | 40 | | | 50 | | ns |
| t_h | A hold time with respect to CK_S | | 10 | | | 10 | | ns |
| t_{rec} | \bar{R} recovery time with respect to CK_S | | 20 | | | 26 | | ns |

Note 3 : Test Circuit



| Item | SW1 | SW2 |
|--------------------|-------|-------|
| t_{PLH}, t_{PHL} | OPEN | OPEN |
| t_{PLZ} | CLOSE | OPEN |
| t_{PHZ} | OPEN | CLOSE |
| t_{PZL} | CLOSE | OPEN |
| t_{PZH} | OPEN | CLOSE |

- (1) The pulse generator (PG) has the following characteristics (10%~90%) : $t_r=6\text{ns}, t_f=6\text{ns}$
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

8-BIT LED DRIVER WITH SHIFTREGISTER AND LATCHED 3-STATE OUTPUTS

TIMING DIAGRAM

