

TC74AC574P, TC74AC574F, TC74AC574FW, TC74AC574FT**OCTAL D - TYPE FLIP - FLOP WITH 3 - STATE OUTPUT**

The TC74AC574 is an advanced high speed CMOS OCTAL FLIP - FLOP fabricated with silicon gate and double - layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

These 8 - bit D - type flip - flops are controlled by a clock input (CK) and a output enable input ($\overline{OE}$).

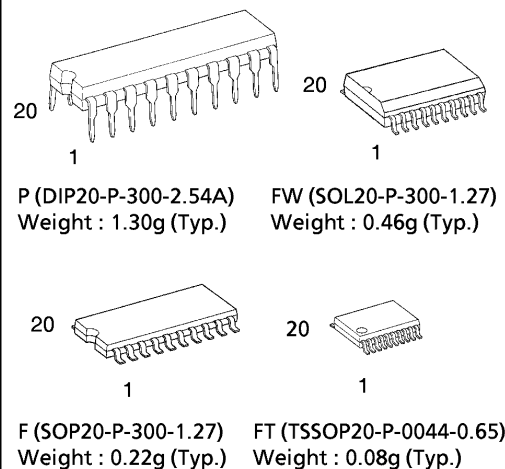
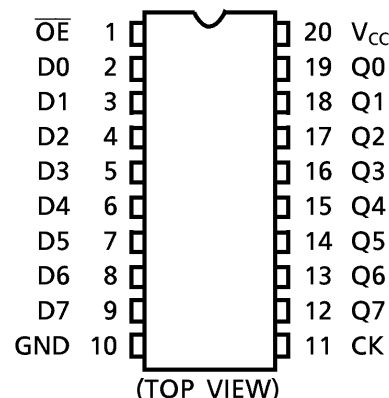
When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

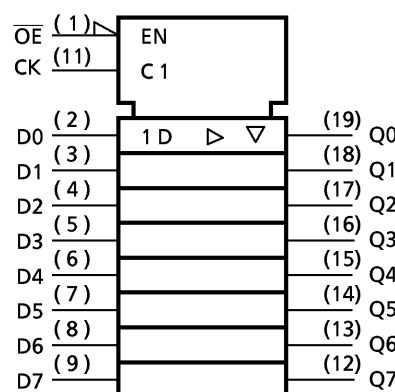
- High Speed..... $f_{MAX} = 180\text{MHz}(\text{typ.})$
at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 8\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC} (\text{Min.})$
- Symmetrical Output Impedance... $|I_{OH}| = |I_{OL}| = 24\text{mA}(\text{Min.})$
Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays..... $t_{PLH} \approx t_{PHL}$
- Wide Operating Voltage Range.... $V_{CC} (\text{opr}) = 2\text{V} \sim 5.5\text{V}$
- Pin and Function Compatible with 74F574

(Note) The JEDEC SOP (FW) is not available in Japan.

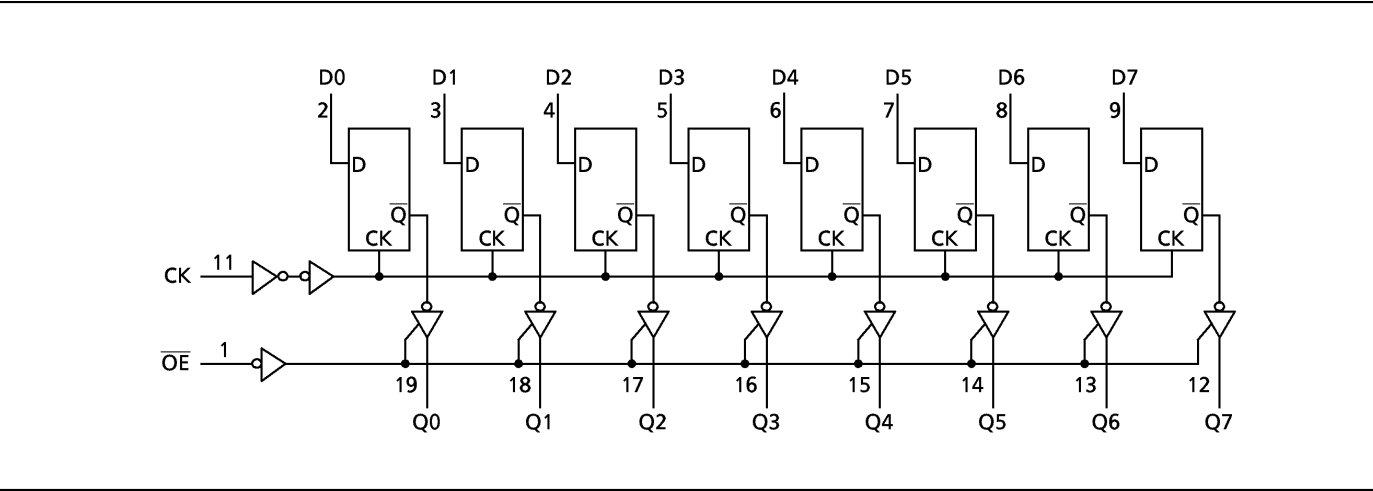
**PIN ASSIGNMENT****TRUTH TABLE**

INPUTS			OUTPUTS
$\overline{OE}$	CK	D	Q
H	X	X	Z
L		X	Q_n
L		L	L
L		H	H

X : Don't Care
Z : High Impedance
 Q_n : No Change

IEC LOGIC SYMBOL

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7.0$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC} /Ground Current	I_{CC}	± 200	mA
Power Dissipation	P_D	500 (DIP)*/ 180 (SOP/TSSOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	$^{\circ}C$

*500mW in the range of $T_a = -40^{\circ}C \sim 65^{\circ}C$. From $T_a = 65^{\circ}C$ to $85^{\circ}C$ a derating factor of $-10mW/^{\circ}C$ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~ V_{CC}	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	$-40 \sim 85$	$^{\circ}C$
Input Rise and Fall Time	dt/dV	0~ 100 ($V_{CC} = 3.3 \pm 0.3V$) 0~ 20 ($V_{CC} = 5 \pm 0.5V$)	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V _{IH}		2.0 3.0 5.5	1.50 2.10 3.85	— — —	— — —	1.50 2.10 3.85	— — —	V
Low - Level Input Voltage	V _{IL}		2.0 3.0 5.5	— — —	— — —	0.50 0.90 1.65	— — —	0.50 0.90 1.65	V
High - Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	V
			I _{OH} = -4mA	3.0	2.58	—	—	2.48	
			I _{OH} = -24mA	4.5	3.94	—	—	3.80	
Low - Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50μA	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	V
			I _{OL} = 12mA	3.0	—	—	0.36	—	
			I _{OL} = 24mA	4.5	—	—	0.36	—	
3 - State Output Off - State Current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	5.5	—	—	± 0.5	—	± 5.0	μA
Input Leakage Current	I _{IN}	V _{IN} = V _{CC} or GND	5.5	—	—	± 0.1	—	± 1.0	
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND	5.5	—	—	8.0	—	80.0	

* : This spec indicates the capability of driving 50Ω transmission lines.

One output should be tested at a time for a 10ms maximum duration.

TIMING REQUIREMENTS (Input t_r = t_f = 3ns)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		Ta = -40~85°C		UNIT
			V _{CC} (V)	LIMIT	LIMIT	LIMIT	
Minimum Pulse Width (CK)	t _{W(H)}		3.3 ± 0.3	7.0	7.0		ns
	t _{W(L)}		5.0 ± 0.5	5.0	5.0		
Minimum Set - up Time	t _s		3.3 ± 0.3	9.0	9.0		
			5.0 ± 0.5	4.5	4.5		
Minimum Hold Time	t _h		3.3 ± 0.3	1.0	1.0		
			5.0 ± 0.5	1.0	1.0		

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, $R_L = 500\Omega$, Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = − 40~85°C		UNIT
			V _{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK—Q)	t _{pLH}		3.3 ± 0.3	—	9.8	16.7	1.0	19.0	ns
	t _{pHL}		5.0 ± 0.5	—	6.1	9.2	1.0	10.5	
Output Enable Time	t _{pZL}		3.3 ± 0.3	—	9.2	15.8	1.0	18.0	
	t _{pZH}		5.0 ± 0.5	—	6.1	9.3	1.0	10.6	
Output Disable Time	t _{pLZ}		3.3 ± 0.3	—	6.6	11.0	1.0	12.5	MHz
	t _{pHZ}		5.0 ± 0.5	—	5.8	8.8	1.0	10.0	
Maximum Clock Frequency	f _{MAX}		3.3 ± 0.3 5.0 ± 0.5	50 95	100 160	— —	50 95	— —	
Input Capacitance	C _{IN}			—	5	10	—	10	pF
Output Capacitance	C _{OUT}			—	10	—	—	—	
Power Dissipation Capacitance	C _{PD} (1)			—	36	—	—	—	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

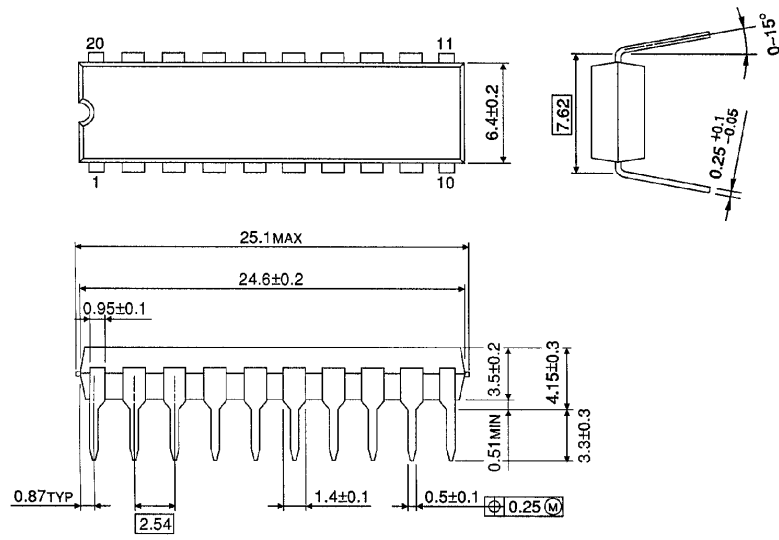
$$I_{\text{CC}}(\text{opr.}) = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{IN}} + I_{\text{CC}} / 8 \text{ (per F / F)}$$

And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation :

$$C_{\text{PD}}(\text{total}) = 26 + 10 \cdot n$$

DIP 20PIN PACKAGE DIMENSIONS (DIP20-P-300-2.54A)

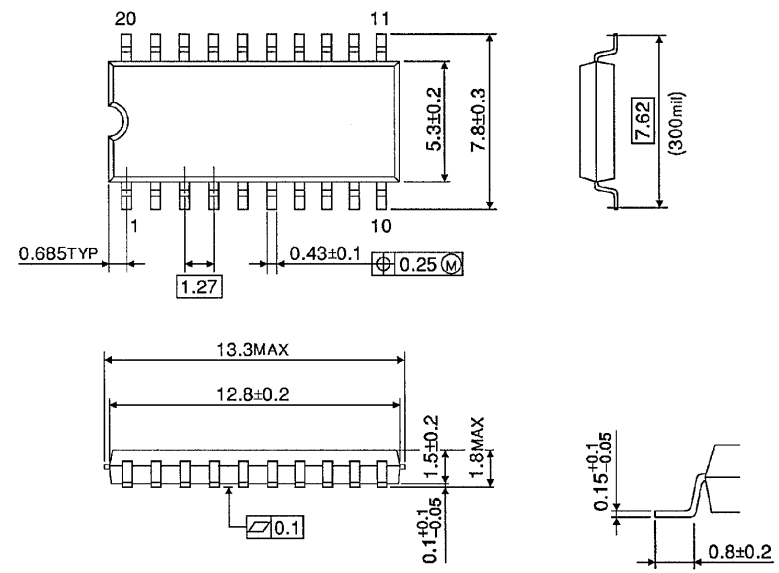
Unit in mm



Weight : 1.30g (Typ.)

SOP 20PIN (200mil BODY) PACKAGE DIMENSIONS (SOP20-P-300-1.27)

Unit in mm

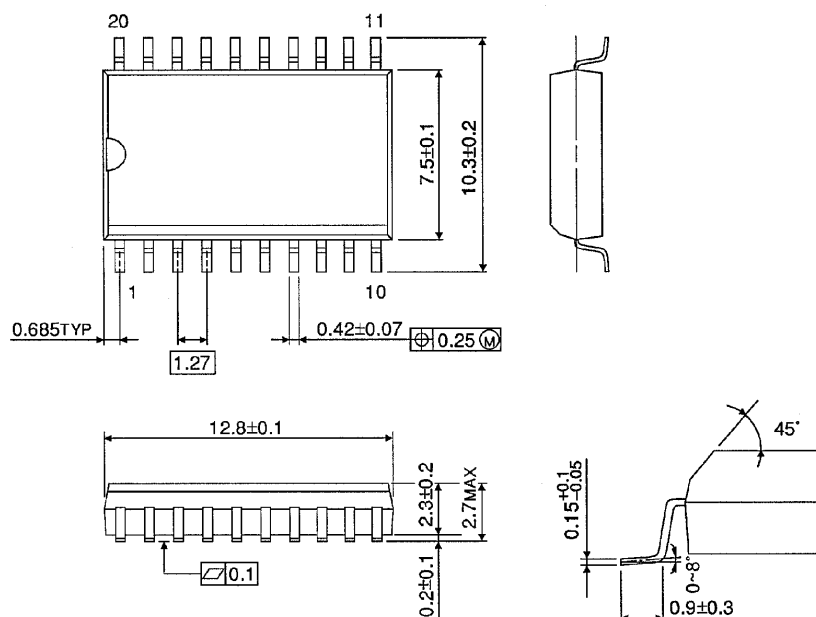


Weight : 0.22g (Typ.)

SOP 20PIN (300mil BODY) PACKAGE DIMENSIONS (SOL20-P-300-1.27)

Unit in mm

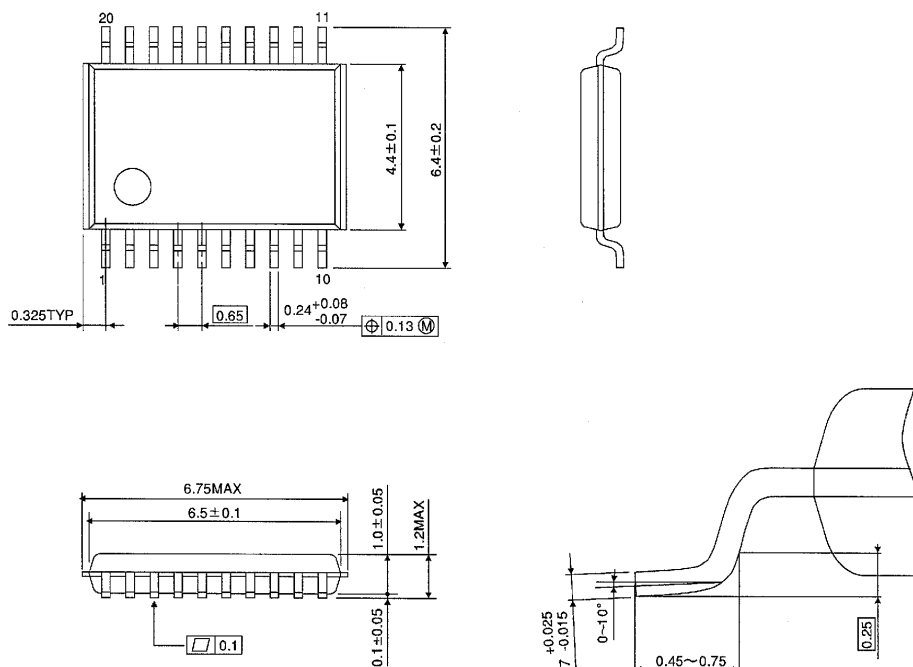
(Note) This package is not available in Japan.



Weight : 0.46g (Typ.)

TSSOP 20PIN PACKAGE DIMENSIONS (TSSOP20-P-0044-0.65)

Unit in mm



Weight : 0.08g (Typ.)

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