REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R146-92.	92-03-09	Monica L. Poelking
B	Add device types 05 and 06. Add case outlines X and Y. Editorial changes throughout.	96-06-26	Monica L. Poelking
C	Update boilerplate to MIL-PRF-38535 requirements. - CFS	06-06-15	Thomas M. Hess

REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C	C	C	C	C	C							
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27							

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED
Tim H. Noh

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Tim H. Noh

APPROVED BY
Don Cool

DRAWING APPROVAL DATE
91-09-11

REVISION LEVEL
C

MICROCIRCUIT, DIGITAL, 8-BIT CHMOS MICROCONTROLLER WITH 8K BYTES EPROM MEMORY, MONOLITHIC SILICON

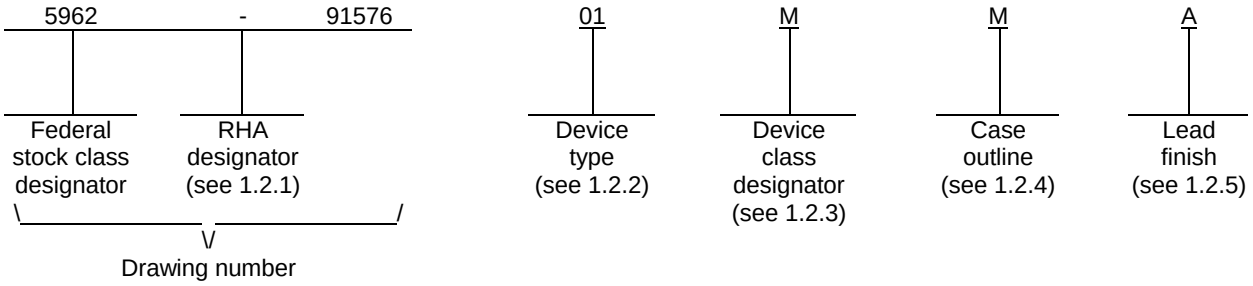
SIZE	CAGE CODE	
A	**67268**	**5962-91576**

SHEET 1 OF 27

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of high reliability (device classes Q and M), space application (device class V), and nontraditional performance environment (device class N). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN. For device class N, the user is cautioned to assure that the device is appropriate for the application environment.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes N, Q, and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	87C52	8-bit microcontroller with 8k-bytes EPROM memory (3.5 to 12 MHz)
02	87C52-16	8-bit microcontroller with 8k-bytes EPROM memory (3.5 to 16 MHz)
03	87C52	8-bit microcontroller with 8k-bytes of one time programmable EPROM memory (3.5 to 12 MHz)
04	87C52-16	8-bit microcontroller with 8k-bytes of one time programmable EPROM memory (3.5 to 16 MHz)
05	87C52	8-bit microcontroller with 8k-bytes of one time programmable EPROM memory (3.5 to 12 MHz)
06	87C52-16	8-bit microcontroller with 8k-bytes of one time programmable EPROM memory (3.5 to 16 MHz)

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
N	Certification and qualification to MIL-PRF-38535 with a nontraditional performance environment (encapsulated in plastic)
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835, JEDEC Publication 95, and as follows:

Outline letter	Descriptive designator	Terminals	Package style	Document
M	GQCC1-J44	44	"J" lead chip carrier 1/	MIL-STD-1835
Q	GDIP1-T40 or CDIP2-T40	40	Dual-in-line 1/	MIL-STD-1835
U	CQCC1-N44	44	Square leadless chip carrier 1/	MIL-STD-1835
X	MS-011-AC	40	Plastic dual-in-line	JEP 95
Y	MS-018-AC	44	Plastic "J" leaded chip carrier	JEP 95

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 2/

Storage temperature range ..... -65°C to +150°C
Voltage on EA/V_{PP} pin to V_{SS} range ..... 0 V dc to +13.0 V dc
Voltage on any pin to V_{SS} range ..... -0.5 V dc to +6.5 V dc
Input, output current on any two pins ..... ±10 mA
Maximum power dissipation (P_D) ..... 1.5 W
Maximum junction temperature (T_J) ..... +200°C
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case (θ_{JC}):
  Case outline X ..... 15°C/W
  Case outline Y ..... 14°c/W
  Case outlines M, Q, and U ..... See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) ..... +4.5 V dc to +5.5 V dc
Case operating temperature range (T_C):
  Devices 01 – 04 ..... -55°C to +125°C
  Devices 05 and 06 ..... -40°C to +85°C
Maximum low level input voltage:
  All inputs except EA ..... $0.2V_{CC}$ – 0.25 V dc
  EA ..... $0.2V_{CC}$ – 0.45 V dc
Minimum high level input voltage:
  All inputs except XTAL1, RESET ..... $0.2V_{CC}$ + 1.1 V dc
  XTAL1, RESET ..... $0.7V_{CC}$ + 0.2 V dc

1/ For device types 01 and 02, lid shall be transparent to permit ultraviolet light erasure.
2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ELECTRONICS INDUSTRIES ALLIANCE (EIA)

JEP 95 - Registered and Standard Outlines for Semiconductor Devices

(Copies of this document are available online at www.jedec.org/ or from the Electronics Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes N, Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes N, Q, and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes N, Q, and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes N, Q, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes N, Q, and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes N, Q, and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

3.11 Processing EPROM's. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.11.1 Erasure of EPROM's. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.5.

3.11.2 Programmability of EPROM's. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.6 and table III.

3.11.3 Verification of erasure of programmability of EPROM's. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device types	Limits		Unit
						Min	Max	
Input low voltage, (except $\overline{EA}$)	V_{IL}			1, 2, 3	All	-0.5 2/	$0.2V_{CC}$ – 0.25	V
Input low voltage to $\overline{EA}$	V_{IL1}					0 2/	$0.2V_{CC}$ – 0.45	V
Input high voltage, (except XTAL1, RESET)	V_{IH}					$0.2V_{CC}$ + 1.1	V_{CC} + 0.5 2/	V
Input high voltage, (XTAL1, RESET)	V_{IH1}					$0.7V_{CC}$ + 0.2	V_{CC} + 0.5 2/	V
Output low voltage, (Ports 1, 2, 3)	V_{OL}	I_{OL} = +1.6 mA 3/	V_{CC} = 4.5 V V_{IN} = V_{IL} max, V_{IH} min				0.45	V
Output low voltage, port 0, ALE, $\overline{PSEN}$	V_{OL1}	I_{OL} = +3.2 mA 3/					0.45	V
Output high voltage, (Ports 1, 2, 3)	V_{OH}	I_{OH} = -60 µA 4/				2.4		V
		I_{OH} = -25 µA 4/				$0.75V_{CC}$		
		I_{OH} = -10 µA				$0.9V_{CC}$		
Output high voltage, port 0 in external bus mode, ALE, $\overline{PSEN}$	V_{OH1}	I_{OH} = -800 µA				2.4		V
		I_{OH} = -300 µA				$0.75V_{CC}$		
		I_{OH} = -80 µA				$0.9V_{CC}$		
Logic 0 input current ports 1, 2, 3	I_{IL}	V_{IN} = 0.45 V					-75	µA
Logic 1 to 0 transition current, ports 1, 2, 3	I_{TL}	V_{CC} = 5.5 V 5/					-750	µA
Input leakage current, port 0	I_{LI}	$V_{IN} = V_{IH}$ min				0	10	µA
		$V_{IN} = V_{IL}$ max				0	-10	
Reset pull-down resistor	R_{RST}					50	300	kΩ
Pin capacitance	$C_{I/O}$	See 4.4.1.b		4	All		10	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Supply current	I_{CC1} 2/ 6/	Running at 12 MHz.	1, 2, 3	01, 03, 05		35	mA
		Idle at 12 MHz.				6	mA
		Power down.				75	µA
Supply current	I_{CC2} 6/	Running at 16 MHz.		02, 04, 06		39	mA
		Idle at 16 MHz.				7	mA
		Power down.				75	µA
Functional testing		V_{CC} = 4.5 V, 5.5 V See 4.4.1.d	7, 8	All			
External Program and Data Memory Characteristics							
Oscillator frequency	$1/t_{CLCL}$	See figure 3. 7/ 8/ 9/	9, 10, 11	01, 03, 05	3.5	12	MHz
				02, 04, 06	3.5	16	
ALE pulse width	t_{LHLL}			01, 03, 05	112		ns
				02, 04, 06	68		
				All	$2t_{CLCL}$ - 55		
Address valid to ALE low	t_{AVLL}			01, 03, 05	13		ns
				02, 04, 06	5		
				All	t_{CLCL} – 70 8/		
Address hold after ALE low	t_{LLAX}			01, 03, 05	33		ns
				02, 04, 06	12		
				All	t_{CLCL} – 50		
ALE low to valid instr. in	t_{LLIV}			01, 03, 05		218	ns
				02, 04, 06		132	
				All		$4t_{CLCL}$ - 115	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
ALE low to $\overline{\text{PSEN}}$ low	t_{LLPL}	See figure 3. 7/ 8/ 9/	9, 10, 11	01, 03, 05	28		ns
				02, 04, 06	7		
				All	t_{CLCL} - 55		
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}			01, 03, 05	190		ns
				02, 04, 06	125		
				All	$3t_{CLCL}$ - 60		
$\overline{\text{PSEN}}$ low to valid instr. in	t_{PLIV}			01, 03, 05		130	ns
				02, 04, 06		65	
				All		$3t_{CLCL}$ - 120	
Input instr. hold after $\overline{\text{PSEN}}$	t_{PXIX}			All	0		ns
Input instr. float after $\overline{\text{PSEN}}$	t_{PXIZ}			01, 03, 05		58	ns
				02, 04, 06		37	
				All		t_{CLCL} – 25	
Address to valid instr. in	t_{AVIV}			01, 03, 05		312	ns
				02, 04, 06		188	
				All		$5t_{CLCL}$ - 120	
$\overline{\text{PSEN}}$ low to address float	t_{PLAZ}			All		25	ns
$\overline{\text{RD}}$ pulse width	t_{RLRH}			01, 03, 05	400		ns
				02, 04, 06	270		
				All	$6t_{CLCL}$ - 100		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
$\overline{WR}$ pulse width	t_{WLWH}	See figure 3. 7/ 8/ 9/	9, 10, 11	01, 03, 05	400		ns
				02, 04, 06	270		
				All	$6t_{CLCL}$ - 100		
$\overline{RD}$ low to valid data in	t_{RLDV}			01, 03, 05		232	ns
				02, 04, 06		123	
				All		$5t_{CLCL}$ - 185	
Data hold after $\overline{RD}$	t_{RHDX}			All	0		ns
Data float after $\overline{RD}$	t_{RHDZ}			01, 03, 05		82	ns
				02, 04, 06		38	
				All		$2t_{CLCL}$ - 85	
ALE low to valid data in	t_{LLDV}			01, 03, 05		496	ns
				02, 04, 06		320	
				All		$8t_{CLCL}$ - 170	
Address to valid data in	t_{AVDV}			01, 03, 05		565	ns
				02, 04, 06		370	
				All		$9t_{CLCL}$ - 185	
ALE low to $\overline{RD}$ or $\overline{WR}$ low	t_{LLWL}			01, 03, 05	185	315	ns
				02, 04, 06	120	250	
				All	$3t_{CLCL}$ - 65	$3t_{CLCL}$ + 65	
Address to $\overline{RD}$ to $\overline{WR}$ low	t_{AVWL}			01, 03, 05	188		ns
				02, 04, 06	102		
				All	$4t_{CLCL}$ - 145		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Data valid to $\overline{WR}$ transition	t_{QVWX}	See figure 3. 7/ 8/ 9/	9, 10, 11	01, 03, 05	8		ns
				02, 04, 06	5		
				All	t_{CLCL} - 75		
Data hold after $\overline{WR}$	t_{WHQX}			01, 03, 05	18		ns
				02, 04, 06	5		
				All	t_{CLCL} - 65		
$\overline{RD}$ low to address float	t_{RLAZ}			All		0	ns
$\overline{RD}$ or $\overline{WR}$ high to ALE high	t_{WHLH}			01, 03, 05	18	148	ns
				02, 04, 06	5	127	
				All	t_{CLCL} – 65 9/	t_{CLCL} + 65	
Serial port clock cycle time	t_{XLXL}			01, 03, 05	1000		ns
				02, 04, 06	740		
				All	$12t_{CLCL}$		
Output data setup to clock rising edge	t_{QVXH}			01, 03, 05	700		ns
				02, 04, 06	484		
				All	$10t_{CLCL}$ - 133		
Output data hold after clock rising edge	t_{XHQX}			01, 03, 05	50		ns
				02, 04, 06	6		
				All	$2t_{CLCL}$ – 117		
Input data hold after clock rising edge	t_{XHDX}			All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Clock rising edge to input data valid	t_{XHDV}	See figure 3. 7/ 8/ 9/	9, 10, 11	01, 03, 05	700		ns
				02, 04, 06	484		
				All	$10t_{CLCL}$ - 133		
High time	t_{CHCX}			All	20		ns
Low time	t_{CLCX}			All	20		ns
Rise time	t_{CLCH}			All		20	ns
Fall time	t_{CHCL}			All		20	ns

1/ Unless otherwise specified, all testing to be performed using worst case test conditions. The operating temperature shall be as specified in 1.4.

2/ Guaranteed, if not tested, to the limits specified.

3/ Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL} of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and 2 pins when these pins when these pins make 1 to 0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE pin may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt trigger, or use an address latch with a Schmitt trigger strobe input. I_{OL} can exceed these conditions provided that no single output sinks more than 5 mA and no more than two outputs exceed the test conditions.

4/ Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the $0.9V_{CC}$ specification when the address bits are stabilizing.

5/ Pins of ports 1, 2, and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2 V.

6/ I_{CC} max at other frequencies is given by: Active mode: I_{CC} max = 0.94 x FREQ + 23.72.
Idle mode: I_{CC} max = 0.14 x FREQ + 4.32, where FREQ is the external oscillator frequency in MHz.
I_{CC} max is given in mA. See figure 4.

7/ All devices to be tested at 16 MHz only, but guaranteed across the specified operating frequency range. Devices not meeting the limits of the 16 MHz devices may be retested to be supplied at the slower 12 MHz speed grade.

8/ Parametric values are based on a 12 MHz oscillator for device types 01, 03, and 05, a 16 MHZ oscillator for device types 02, 04, and 06, and a variable oscillator for all devices.

9/ Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100 pF, load capacitance for all other outputs = 80 pF.

Device types:	All	
Case outlines:	Q, X	M, U, and Y
Terminal number	Terminal symbol	Terminal symbol
1	P1.0/T2	NC
2	P1.1/T2EX	T2/P1.0
3	P1.2	T2EX/P1.1
4	P1.3	P1.2
5	P1.4	P1.3
6	P1.5	P1.4
7	P1.6	P1.5
8	P1.7	P1.6
9	RST	P1.7
10	RXD/P3.0	RST
11	TXD/P3.1	RXD/P3.0
12	$\overline{\text{INT0}}$/P3.2	NC
13	$\overline{\text{INT1}}$/P3.3	TXD/P3.1
14	T0/P3.4	$\overline{\text{INT0}}$/P3.2
15	T1/P3.5	$\overline{\text{INT1}}$/P3.3
16	$\overline{\text{WR}}$/P3.6	T0/P3.4
17	$\overline{\text{RD}}$/P3.7	T1/P3.5
18	XTAL2	$\overline{\text{WR}}$/P3.6
19	XTAL1	$\overline{\text{RD}}$/P3.7
20	V_{SS}	XTAL2
21	P2.0/A8	XTAL1
22	P2.1/A9	V_{SS}
23	P2.2/A10	NC
24	P2.3/A11	P2.0/A8
25	P2.4/A12	P2.1/A9
26	P2.5/A13	P2.2/A10
27	P2.6/A14	P2.3/A11
28	P2.7/A15	P2.4/A12
29	$\overline{\text{PSEN}}$	P2.5/A13
30	ALE/$\overline{\text{PROG}}$	P2.6/A14
31	$\overline{\text{EA}}$/V_{PP}	P2.7/A15
32	P0.7/AD7	$\overline{\text{PSEN}}$
33	P0.6/AD6	ALE/$\overline{\text{PROG}}$
34	P0.5/AD5	NC
35	P0.4/AD4	$\overline{\text{EA}}$/V_{PP}
36	P0.3/AD3	P0.7/AD7
37	P0.2/AD2	P0.6/AD6
38	P0.1/AD1	P0.5/AD5
39	P0.0/AD0	P0.4/AD4
40	V_{DD}	P0.3/AD3
41	---	P0.2/AD2
42	---	P0.1/AD1
43	---	P0.0/AD0
44	---	V_{DD}

NC = No connection

FIGURE 1. Terminal connections.

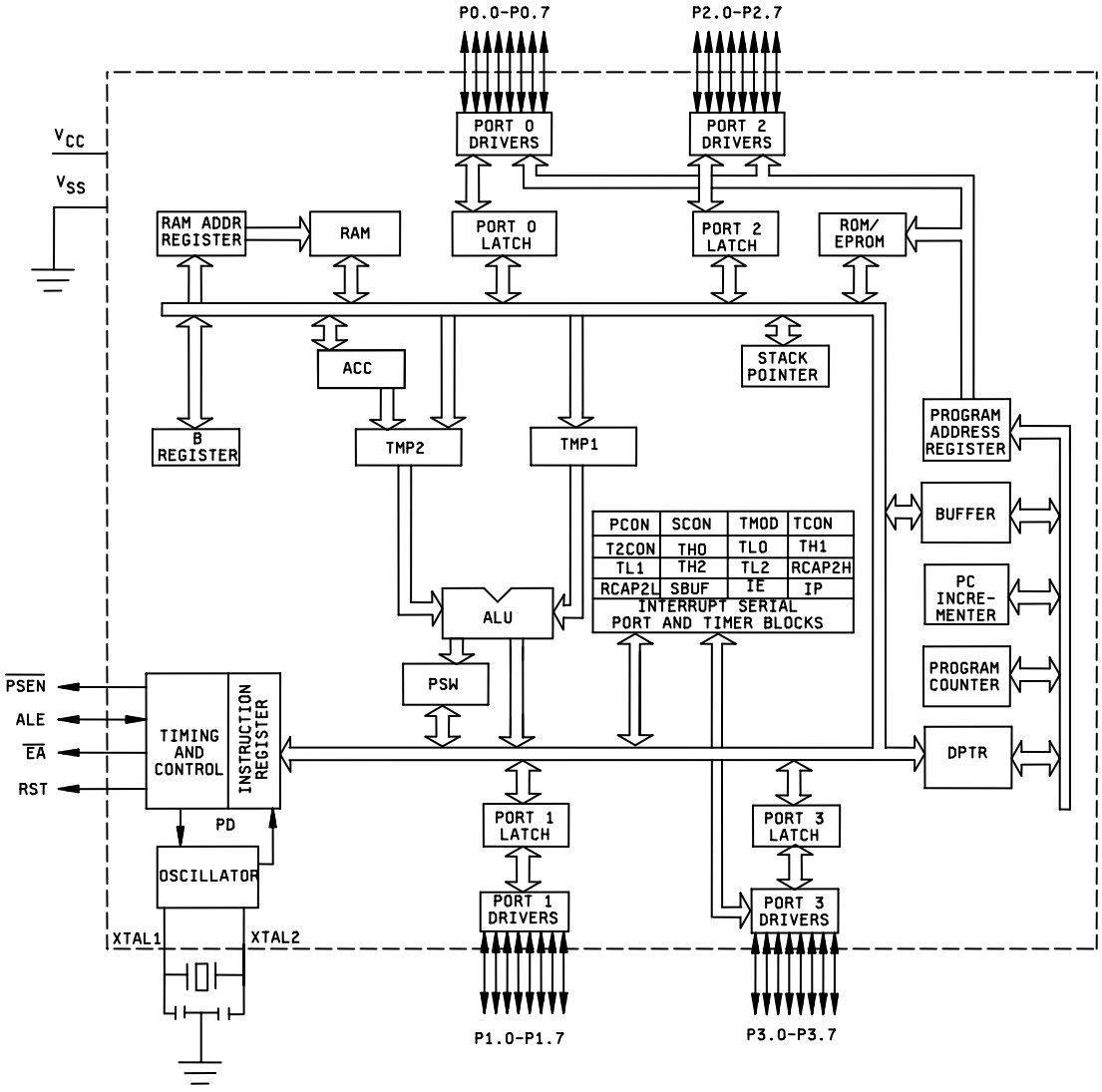
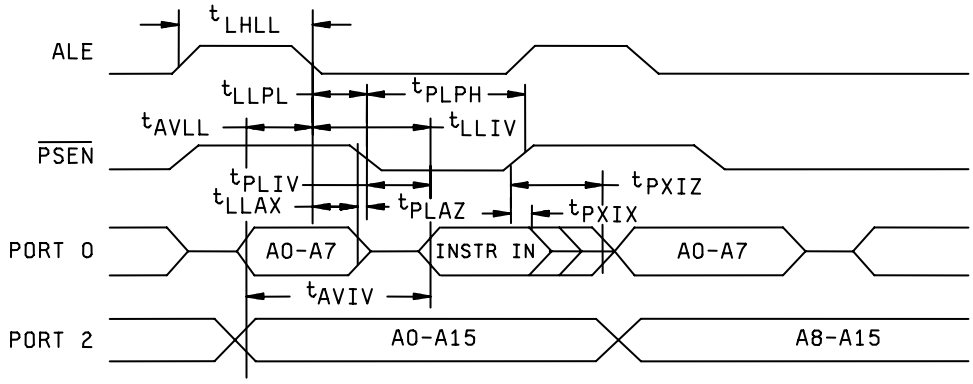
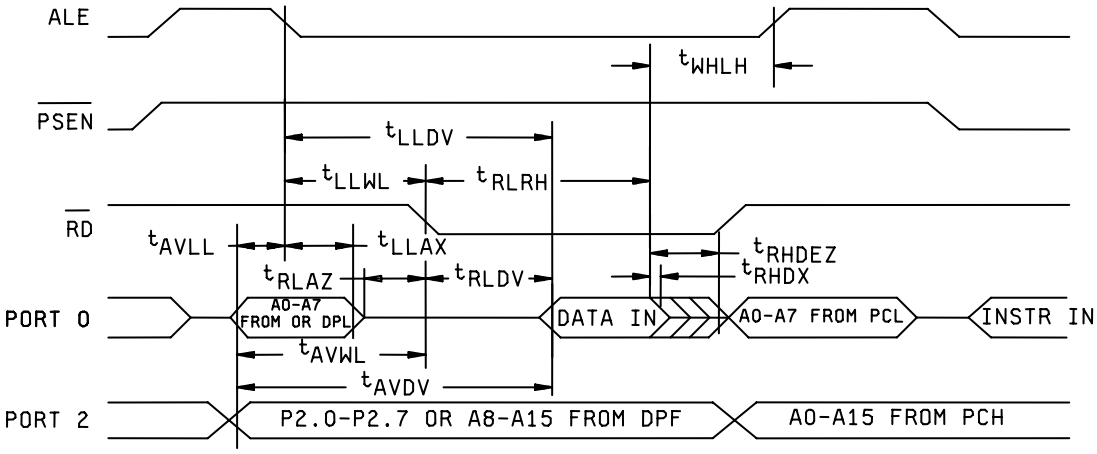


FIGURE 2. Block diagram.

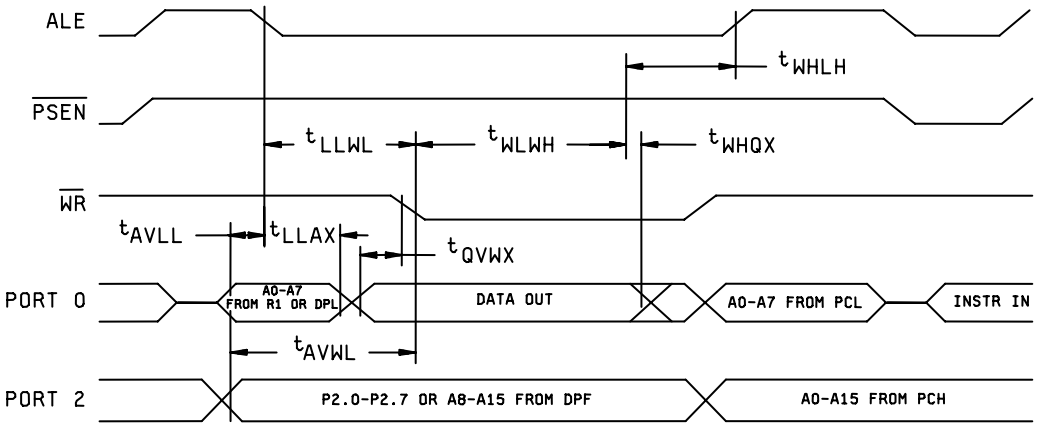


EXTERNAL PROGRAM MEMORY READ CYCLE

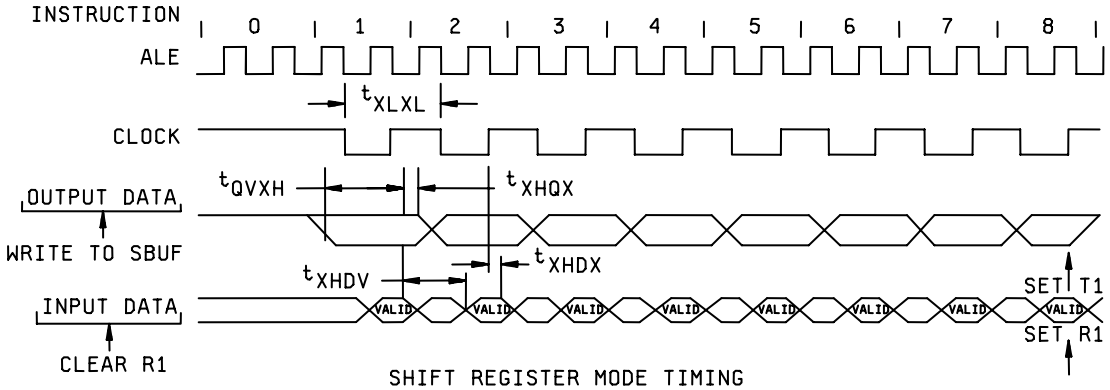


EXTERNAL DATA MEMORY READ CYCLE

FIGURE 3. Switching waveforms and test circuit.

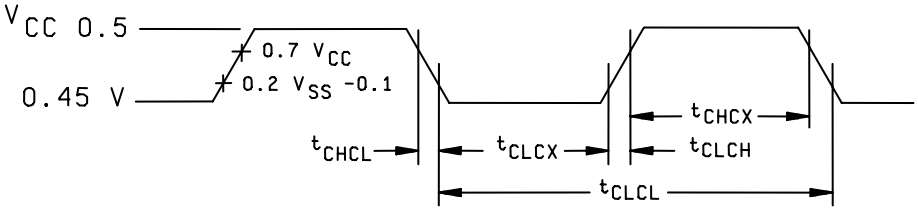


EXTERNAL DATA MEMORY WRITE CYCLE



SHIFT REGISTER MODE TIMING

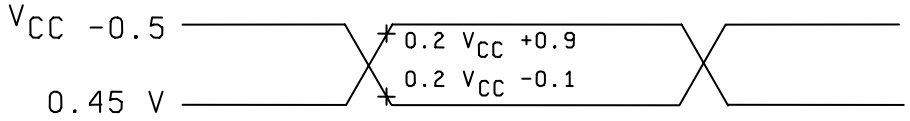
FIGURE 3. Switching waveforms and test circuit - Continued.



EXTERNAL CLOCK DRIVE

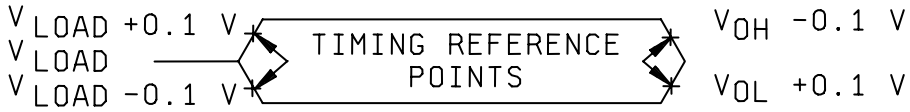
NOTE: AC: Testing

Input and output waveforms:



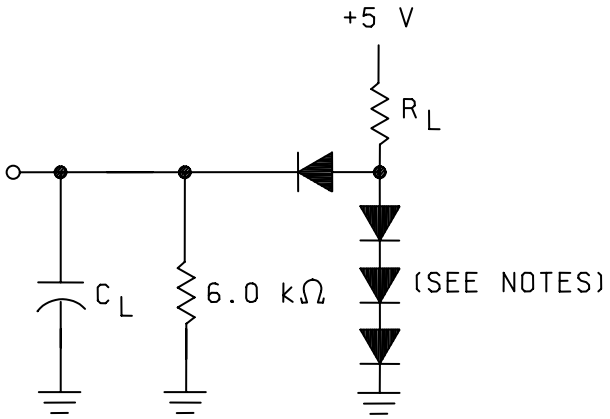
NOTE: AC inputs during testing are driven at V_{CC} – 0.5 V for a logic “1” and 0.45 V for a logic “0”. Timing measurements are made at V_{IH} minimum for a logic “1” and V_{IL} maximum for a logic “0”.

Float waveform:



NOTE: For timing purposes, a port pin ceases floating when a 100 mV change from load voltage occurs and begins floating when a 100 mV change from loaded V_{OH} or V_{OL} level occurs.
I_{OL} or $I_{OH} \geq \pm 20$ mA

FIGURE 3. Switching waveforms and test circuit - Continued.



Output	R_L	C_L
Port 0, ALE, $\overline{PSEN}$	1.2 kΩ	100 pF
All other outputs	2.4 kΩ	80 pF

NOTES:
1. All diodes are 1N914 or equivalent.
2. C_L includes tester and fixture capacitance.

FIGURE 3. Switching waveforms and test circuit - Continued.

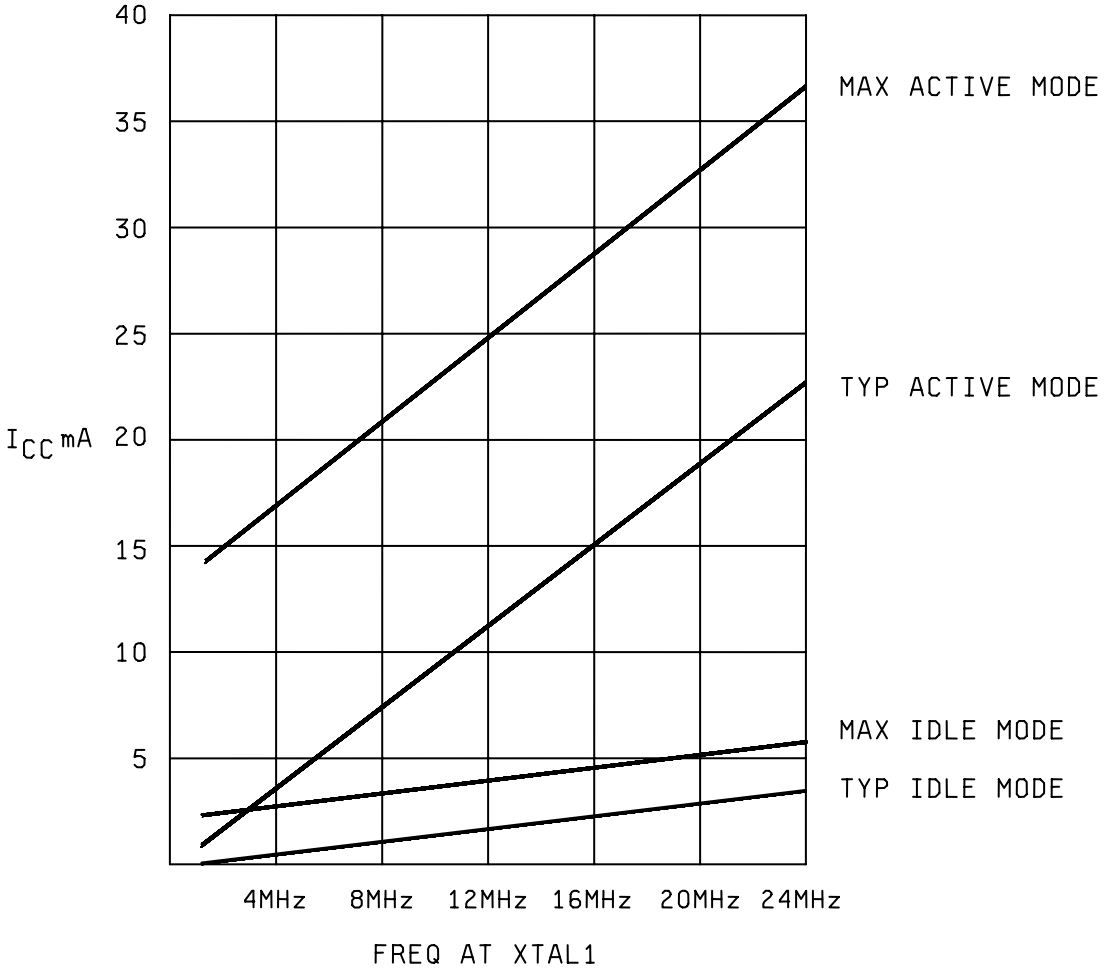


FIGURE 4. ICC versus frequency.

4. VERIFICATION

4.1 Sampling and inspection. For device classes N, Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes N, Q, and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps:

Margin test method A

(1) Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.11.2). The remaining cells shall provide a worst case speed pattern.

(2) Bake, unbiased for 72 hours at +140°C to screen for data retention lifetime.

(3) Perform a margin test using V_m = +5.9 V at +25°C using loose timing (i.e., $T_{ACC} > 1$ µs).

(4) Perform dynamic burn-in (see 4.2.1a).

(5) Margin at V_m = +5.9 V.

(6) Perform electrical tests (see 4.2).

(7) Erase (see 3.11.1), except devices submitted for groups A, B, C, and D testing.

(8) Verify erasure (see 3.11.3).

Margin test method B

(1) Program at 25°C, 100 percent of the bits.

(2) Bake, unbiased for 24 hours at +250°C.

(3) Perform margin test at V_m = +5.9 V.

(4) Erase (see 3.11.1).

(5) Perform interim electrical tests in accordance with table II.

(6) For device types 01 and 02, program 100 percent of the bits and verify (see 3.11.2).

(7) Perform burn-in (see 4.2.1a).

(8) One-hundred percent test at 25°C (group A, subgroups 1 and 7). V_m = 5.9 V with loose timing, apply PDA for device types 03, 04, 05, and 06, the virgin states of the device must be verified.

(9) Perform remaining final electrical subgroups and group A testing.

(10) For device types 01 and 02, erase, devices may be submitted for groups B, C, and D at this time.

(11) For device types 01 and 02, verify erasure (see 3.11.3).

(12) Steps 1 through 4 are performed at wafer level.

4.2.2 Additional criteria for device classes N, Q, and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes N, Q, and V. Qualification inspection for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes N, Q, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroup 4 ($C_{I/O}$) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of five devices with zero rejects shall be required.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes N, Q, and V, subgroups 7 and 8 shall include verifying the functionality of the device.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class M	Device class N	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	---	1, 7
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	2, 8a, 10	2, 8a, 10	2, 8a, 10	2, 8a, 10
Group D end-point electrical parameters (see 4.4)	2, 8a, 10	2, 8a, 10	2, 8a, 10	2, 8a, 10
Group E end-point electrical parameters (see 4.4)	2, 8a, 10	2, 8a, 10	2, 8a, 10	2, 8a, 10

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes N, Q, and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes N, Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

4.5 Erasing procedure. The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-s/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm^2 rating for 20 to 30 minutes, at a distance of about one inch, should be sufficient.

4.6 Programming procedures. The programming characteristics in table III and the following procedures shall be used for programming the device:

a. Connect the device in the electrical configuration (see figure 5) for programming. The waveforms of figure 6 and programming characteristics of table III shall apply.

b. Initially and after each erasure, all bits are in the high "H" state. Information is introduced by selectively programming "L" into the desired bit locations. A programmed "L" can be changed to an "H" by ultraviolet light erasure (see 4.5).

TABLE III. Programming and verification characteristics.

Parameter	Symbol	Conditions	Limits		Units
			Min	Max	
Programming supply voltage	V_{PP}	See figure 7. 1/	12.5	13.0	V
programming supply current	I_{PP}			50	mA
Oscillator frequency	t_{CLCL} 1/		4	6	MHz
Address setup to $\overline{PROG}$ low	t_{AVGL} 2/		$48t_{CLCL}$		ns
Address hold after $\overline{PROG}$	t_{GHAX} 2/		$48t_{CLCL}$		ns
Data setup to $\overline{PROG}$ low	t_{DVGL} 2/		$48t_{CLCL}$		ns
Data hold after $\overline{PROG}$	t_{GHDX} 2/		$48t_{CLCL}$		ns
P2.7 ($\overline{ENABLE}$) high to V_{PP}	t_{EHSH} 2/		$48t_{CLCL}$		ns
V_{PP} setup to $\overline{PROG}$ low	t_{SHGL} 2/		10		μs
V_{PP} hold after $\overline{PROG}$	t_{GHSL} 2/		10		μs
$\overline{PROG}$ width	t_{GLGH} 2/		90	110	μs
Address to data valid	t_{AVQV} 2/			$48t_{CLCL}$	ns
ENABLE low to data valid	t_{ELQV} 2/			$48t_{CLCL}$	ns
Data float after ENABLE	t_{EHQZ} 2/		0	$48t_{CLCL}$	ns
$\overline{PROG}$ high to $\overline{PROG}$ low	t_{GHGL} 2/		10		μs

1/ For programming specifications, T_C = 21°C to 27°C, V_{CC} = 5 V ±10 percent, V_{SS} = 0 V.
2/ Due to test equipment limitations, actual tested values may differ from those specified, but specified limits are guaranteed.

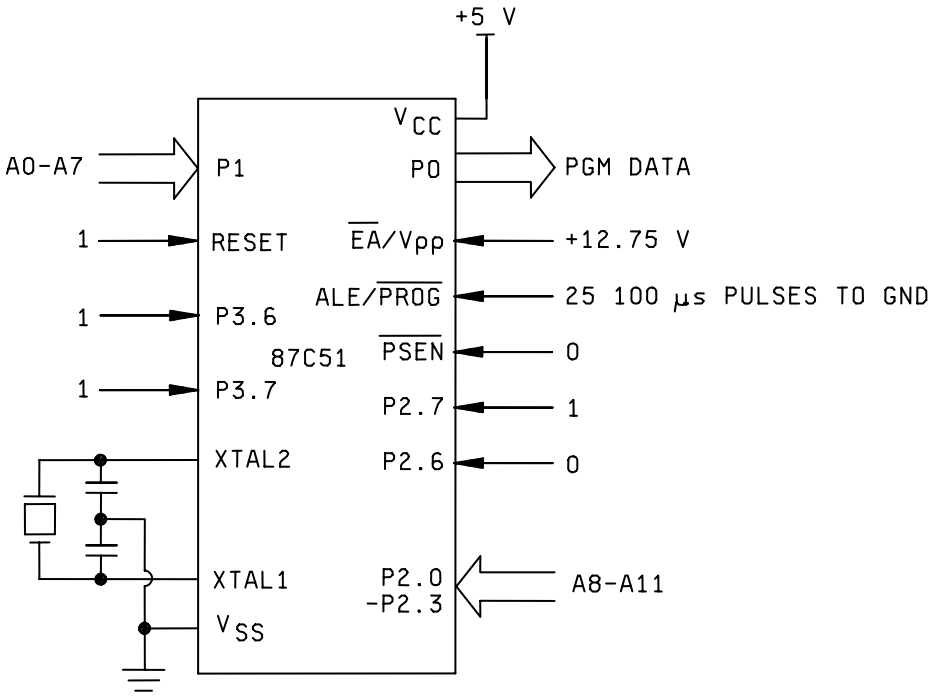


FIGURE 5. Programming configuration.

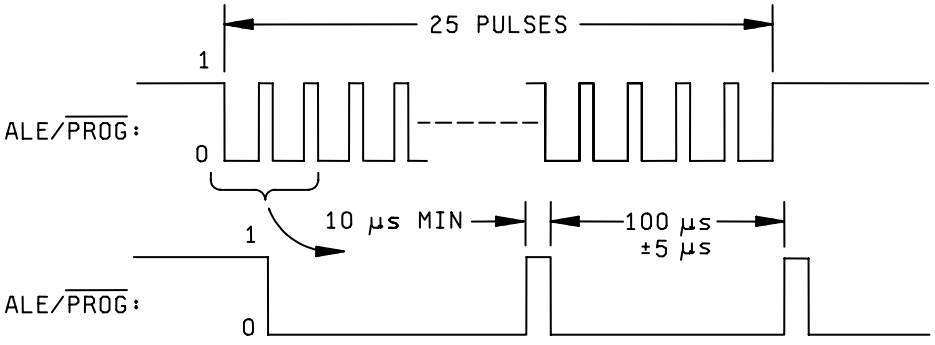
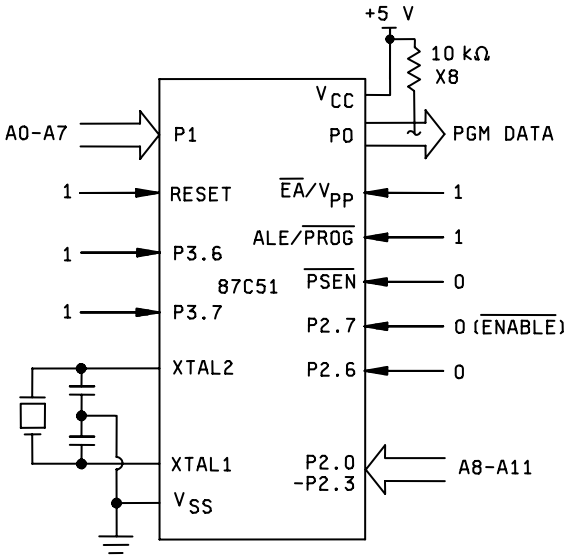


FIGURE 6. Programming waveforms.



EPROM PROGRAMMING AND VERIFICATION WAVEFORMS

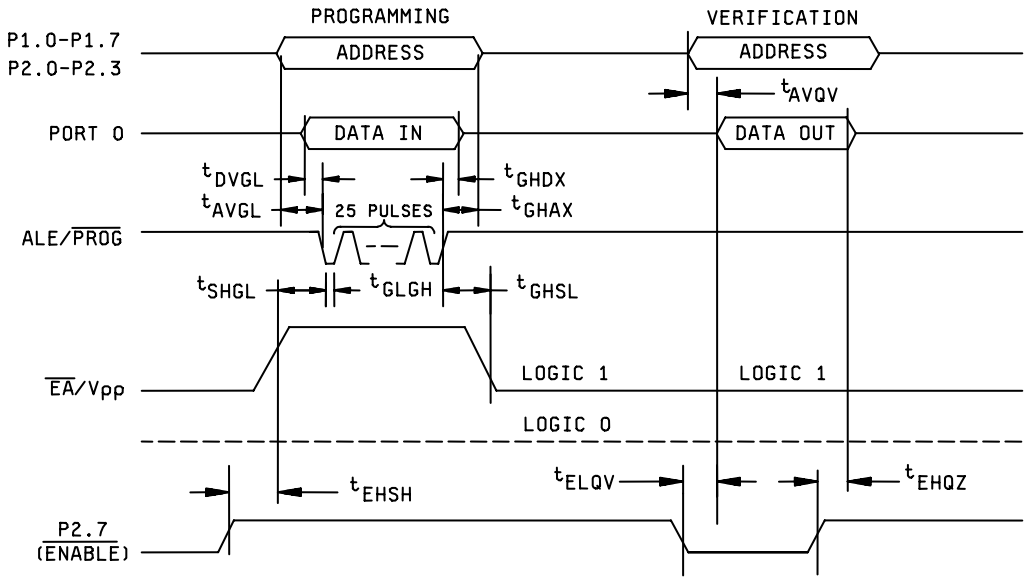


FIGURE 7. Programming verification.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331 and as follows in table IV.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes N, Q, and V. Sources of supply for device classes N, Q, and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

TABLE IV. Symbols, definitions, and functional descriptions.

Mnemonic	Type	Name and function
V_{SS}		Ground: O V reference.
V_{CC}		Power Supply: +5 V.
P0.0 – P0.7	I/O	Port 0: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification in the device. External pull-ups are required during program verification.
P1.0 – P1.7	I/O	Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Pins P1.0 and P1.1 also. Port 1 also receives the low-order address byte during program memory verification. Port 1 also serves alternate functions for timer 2:
	I	T2 (P1.0): Timer/counter 2 external count input.
	I	T2EX (P1.1): Timer/counter 2 trigger input.
P2.0 – P2.7	I/O	Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that uses 16-bit addresses (MOVX@DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that uses 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.
P3.0 – P3.7	I/O	Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 3 also serves the special features of the MCS-51 family, as listed below:
	I	RxD (P3.0): Serial input port
	O	TxD (P3.1): Serial output port
	I	$\overline{\text{INT0}}$ (P3.2): External interrupt 0
	I	$\overline{\text{INT1}}$ (P3.3): External interrupt 1
	I	T0 (P3.4): Timer 0 external input
	I	T1 (P3.5): Timer 1 external input
	O	$\overline{\text{WR}}$ (P3.6): External data memory write strobe
	O	$\overline{\text{RD}}$ (P3.7): External data memory read strobe

TABLE IV. Symbols, definitions, and functional descriptions - Continued.

Mnemonic	Type	Name and function
RST	I	RESET: A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC}.
ALE/$\overline{\text{PROG}}$	I/O	Address Latch Enable/Program Pulse: Output pulse for latching the low byte of the address during ac access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input ($\overline{\text{PROG}}$) during EPROM programming.
$\overline{\text{PSEN}}$	O	Program Store Enable: The read strobe to external program memory. When the device is executing code from the external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory.
$\overline{\text{EA}}/V_{PP}$	I	External Access Enable/Programming Supply Voltage: $\overline{\text{EA}}$ must be externally held low to enable the device to fetch from internal program memory locations 0000H to 1FFFH. If $\overline{\text{EA}}$ is held high, the device executes from internal program memory unless the program counter contains an address greater than 1FFFFH. The pin also receives the 12.75 V programming supply voltage (V_{PP}) during EPROM programming.
XTAL1	I	Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	O	Crystal 2: Output from the inverting oscillator amplifier.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-06-15

Approved sources of supply for SMD 5962-91576 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9157601MMA	0C7V7	87C52/BMA
5962-9157601MQA	0C7V7	87C52/BQA
5962-9157601MUA	3/	87C52/BUA
5962-9157602MMA	0C7V7	87C52-16/BMA
5962-9157602MQA	0C7V7	87C52-16/BQA
5962-9157602MUA	3/	87C52-16/BUA
5962-9157603MMA	0C7V7	87C52/BMA-OT
5962-9157603MQA	0C7V7	87C52/BQA-OT
5962-9157603MUA	3/	87C52/BUA-OT
5962-9157603NXA	3/	87C52/CN40A
5962-9157603NYA	3/	87C52/CA44A
5962-9157604MMA	0C7V7	87C52-16/BMA-OT
5962-9157604MQA	0C7V7	87C52-16/BQA-OT
5962-9157604MUA	3/	87C52-16/BUA-OT
5962-9157604NXA	3/	87C52-16/CN40A
5962-9157604NYA	3/	87C52-16/CA44A
5962-9157605NXA	3/	87C52/IN40A
5962-9157605NYA	3/	87C52/IA44A
5962-9157606NXA	3/	87C52-16/IN40A
5962-9157606NYA	3/	87C52-16/IA44A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.