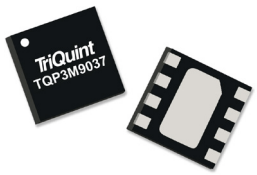
TQP3M9037

Ultra Low Noise, High Linearity LNA

Applications

- Repeaters
- Mobile Infrastructure
- LTE / WCDMA / CDMA / GSM
- General Purpose Wireless
- TDD or FDD systems

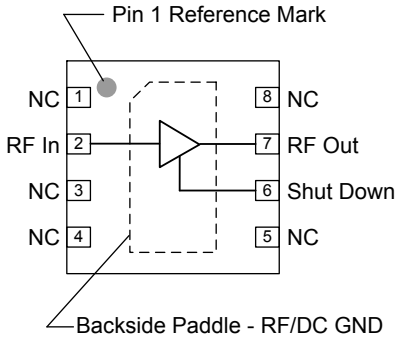


8-pin 2x2 mm DFN package

Product Features

- 1.5-2.7 GHz Operational Bandwidth
- Ultra low noise figure, 0.4 dB NF @ 1.95 GHz
- High gain, 20 dB Gain @ 1.95 GHz
- High linearity, +35 dBm Output IP3
- High input power ruggedness, 22 dBm CW
- Unconditionally stable
- Integrated on-chip matching, 50 ohm in/out
- Integrated active bias
- Integrated shutdown control pin
- +3V to +5V supply; does not require -Vgg
- Pin compatible with low-band TQP3M9036

Functional Block Diagram



General Description

The TQP3M9037 is a high-linearity, ultra-low noise gain block amplifier in a small 2x2 mm surface-mount package. At 1.95 GHz, the amplifier typically provides 20 dB gain, +35 dBm OIP3, and 0.4 dB noise figure while drawing 62 mA current from a 5V supply. This amplifier does not require a negative supply for operation and can be biased from a single positive supply ranging from 3.3 to 5 volts. The device is housed in a green/RoHS-compliant industry-standard 2x2 mm package.

The TQP3M9037 is internally matched using a high performance E-pHEMT process and only requires four external components for operation from a single positive supply: an external RF choke and blocking/bypass capacitors. This low noise amplifier contains an internal active bias to maintain high performance over temperature and integrates a shut-down biasing capability to allow for operation for TDD applications.

The TQP3M9037 covers the 1.5-2.7 GHz frequency band and is targeted for wireless infrastructure. It is pin compatible with the low-band, 0.4-1.5 GHz TQP3M9036.

Pin Configuration

Pin #	Symbol
1,3,4,5,8	No Connect or GND
2	RF In
6	Shut Down
7	RF Out
Backside Paddle	RF/DC GND

Ordering Information

Part No.	Description
TQP3M9037	Ultra low noise, High IP3 LNA
TQP3M9037-PCB	1.5-2.7 GHz Evaluation Board

Standard T/R size = 2500 pieces on a 7” reel.

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to 150°C
Supply Voltage (V_{DD})	+7 V
RF Input Power, CW, 50Ω,T = 25°C	+22 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage (V_{DD})	+3.3	5	5.25	V
T_{CASE}	-40		+85	°C
T_J (for >10^6 hours MTTF)			190	°C

Electrical specifications are measured at specified test conditions.
Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: +25°C, +5V Vsupply, 50 Ω system.

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		1500		2700	MHz
Test Frequency			1950		MHz
Gain		18.5	20.0	21.5	dB
Input Return Loss			10		dB
Output Return Loss			11		dB
Noise Figure			0.40	0.65	dB
Output P1dB			+20		dBm
Output IP3 (Note 1)	Pout=+5 dBm/tone, Δf=1 MHz	+32	+35		dBm
Power Shutdown Control (Pin 6)	On state	0		0.4	V
	Off state (Power down)	1.4		V_{DD}	V
Current, I_{DD} (Note 2)	On state	40	65	90	mA
	Off state (Power down)		3	4	mA
Shutdown pin current, I_{SD}	V_{PD} ≥ 1.4 V		140		µA
Thermal Resistance, θ_{jc}	channel to case			53.4	°C/W

Notes:
1. The typical performance value is preliminary. More production lots will be processed to establish final typical.
2. Current can be reduced by operating at a lower device voltage. (example: I_{dd} =50 mA at V_{dd} =4V)

Device Characterization Data

S-Parameter Data

Test conditions unless otherwise noted: V_{DD}=+5 V, I_{DD}=65 mA (typ.), Temp=+25°C, 50 Ohm system

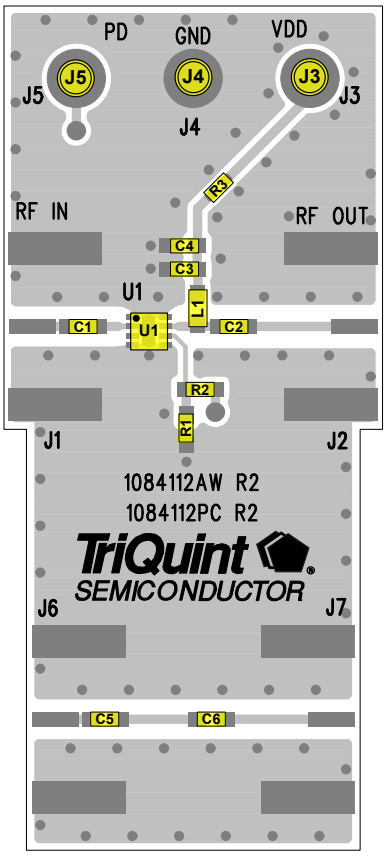
Freq (GHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
1.0	-9.6	-81.0	24.7	108.9	-30.5	16.3	-10.5	-19.3
1.1	-9.9	-85.6	24.2	104.2	-30.5	17.6	-10.2	-22.6
1.2	-10.2	-90.7	23.8	100.0	-30.5	18.8	-9.9	-25.3
1.3	-10.5	-95.1	23.3	96.0	-30.5	19.4	-9.6	-28.0
1.4	-10.8	-99.5	22.8	92.0	-30.5	20.0	-9.6	-31.2
1.5	-11.1	-103.1	22.4	88.4	-30.5	20.7	-9.6	-34.3
1.6	-11.7	-107.2	22.0	84.7	-30.5	21.1	-9.6	-36.3
1.7	-11.7	-110.8	21.6	81.4	-30.5	21.4	-9.4	-39.5
1.8	-12.0	-114.2	21.2	78.1	-30.5	21.5	-9.6	-42.1
1.9	-12.4	-117.7	20.8	74.8	-30.5	21.8	-9.6	-44.0
2.0	-12.8	-121.5	20.5	71.7	-30.5	21.6	-9.6	-46.5
2.1	-13.2	-126.0	20.2	68.5	-28.0	21.5	-9.6	-49.0
2.2	-13.6	-130.4	19.8	65.5	-28.0	21.3	-9.9	-50.8
2.3	-14.0	-135.3	19.6	62.5	-28.0	21.1	-9.9	-53.1
2.4	-14.0	-140.9	19.3	59.4	-28.0	20.4	-10.2	-56.9
2.5	-14.4	-146.7	19.0	56.4	-28.0	20.2	-10.5	-59.6
2.6	-14.4	-152.7	18.7	53.7	-28.0	19.3	-10.8	-62.4
2.7	-14.4	-159.2	18.4	50.7	-28.0	18.6	-11.1	-66.4
2.8	-14.4	-165.9	18.2	47.9	-28.0	18.2	-11.4	-70.0
2.9	-14.4	-172.3	18.0	45.0	-28.0	17.6	-11.7	-73.7

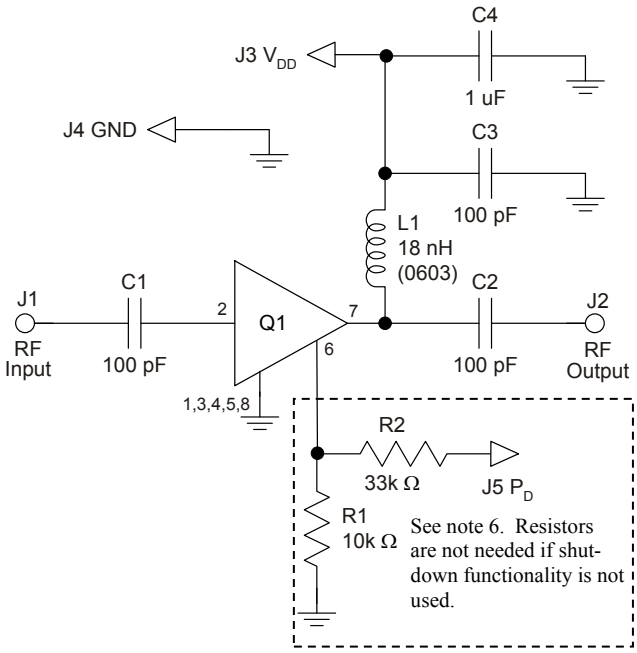
Noise Parameter Data

Test conditions unless otherwise noted: V_{DD}=+5 V, I_{DD}=65 mA (typ.), Temp=+25°C, 50 Ohm system

Freq (GHz)	NF_{min} (dB)	MagOpt (mag)	AngOpt (deg)	Rn (Ω)
1.6	0.288	0.222	67.1	0.048
1.7	0.246	0.346	62.9	0.047
1.8	0.293	0.114	66.2	0.060
1.9	0.250	0.511	42.9	0.037
2.0	0.268	0.147	67.9	0.048

Evaluation Board TQP3M9037-PCB





Notes:

1. See PC Board Layout for more information.
2. R3 (0 Ω jumper) is not shown on the schematic and may be replaced with copper trace in the target application layout.
3. All components are of 0402 size unless stated on the schematic.
4. C1, C2, and C3 are non-critical values. The reactive impedance should be as low as possible at the frequency of operation for optimal performance.
5. The L1 value is non-critical and needs to provide high reactive impedance at the frequency of operation.
6. R1 and R2 are optional and do not need to be loaded if the shut-down functionality is not needed; i.e. FDD applications. If R1 and R2 are not loaded, the LNA will operate in its standard "ON" state.
7. A through line is included on the evaluation board to de-embed the board losses.

Bill of Material

Reference Des.	Value	Description	Manuf.	Part Number
N/A	N/A	Printed Circuit Board	TriQuint	1084112
U1	n/a	Ultra Low Noise Amplifier	TriQuint	TQP3M9037
R1	10K Ω	Resistor, Chip, 0402, 5%, 1/16W	various	various
R2	33K Ω	Resistor, Chip, 0402, 5%, 1/16W	various	various
R3	0 Ω	Resistor, Chip, 0402, 5%, 1/16W	various	various
L1	18 nH	Inductor, 0603, 5%, Ceramic	various	various
C4	1.0 uF	Cap., Chip, 0402, 10%, 10V, X5R	various	various
C1, C2, C3, C5, C6	100 pF	Cap., Chip, 0402, 5%, 50V, NPO/COG	various	various
J3, J4, J5	n/a	Solder Turret	various	various

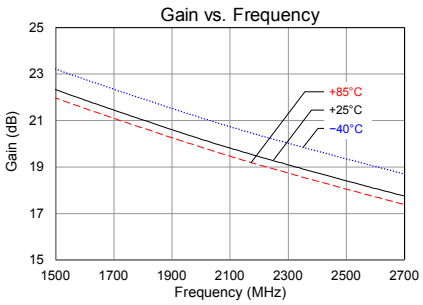
Typical Performance TQP3M9037-PCB

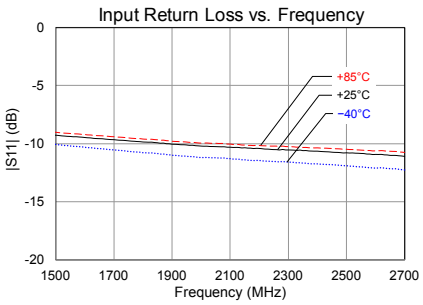
Test conditions unless otherwise noted: V_{DD}=+5 V, I_{DD}=65 mA (typ.), Temp=+25°C

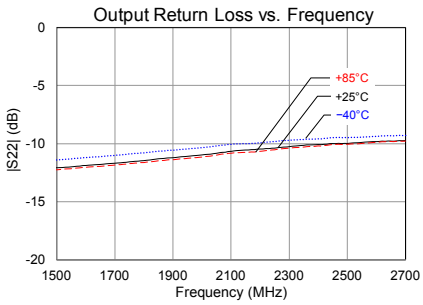
Parameter	Conditions	Typical Value		Units
Frequency		1950	2600	MHz
Gain		20.0	18.2	dB
Input Return Loss		10.6	11.5	dB
Output Return Loss		11.3	9.8	dB
Output P1dB		+20.0	+17.5	dBm
Output IP3	Pout= +5 dBm/tone, Δf=1 MHz	+35.0	+35.7	dBm
Noise figure		0.40	0.50	dB

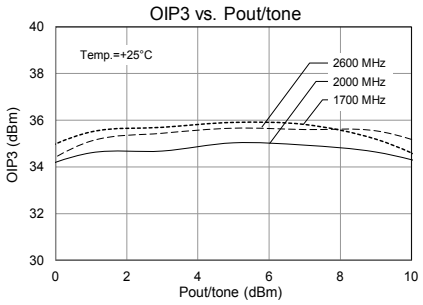
Notes:
1. Noise figure data shown in the table above is de-embedded from the eval board loss. The eval board loss is 0.09 dB at 1.9 GHz and 0.1 dB at 2.6 GHz.
2. For optimized return loss, see reference design on page 6.

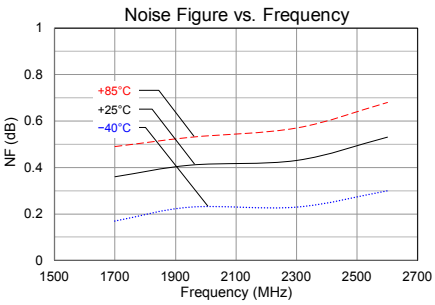
RF Performance Plots TQP3M9037-PCB

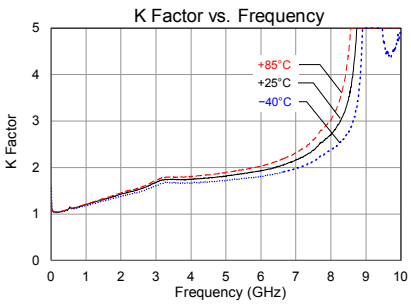




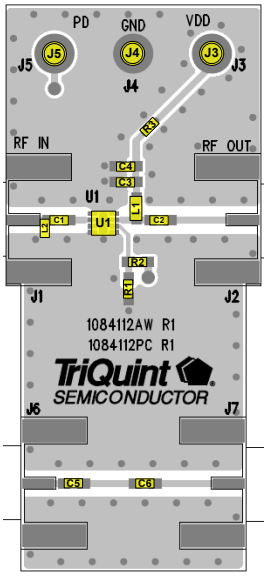


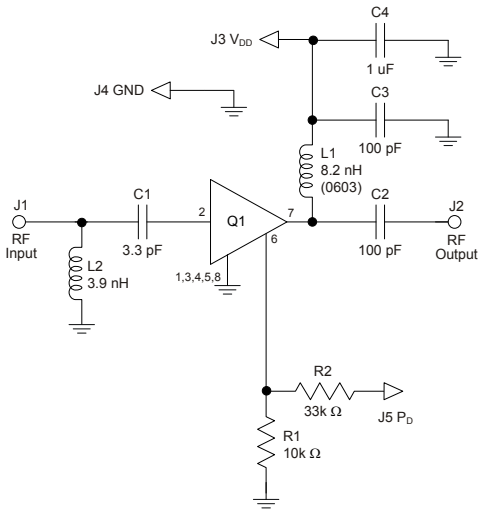






Reference Design – Optimized Return Loss





Notes:

1. See Evaluation Board PCB Information for material and stck-up.
2. R3 (0 Ω jumper) is not shown on the schematic and may be replaced with copper trace in the target application layout.
3. All components are of 0402 size unless stated on the schematic.
4. C2 and C3 are non-critical values. The reactive impedance should be as low as possible at the frequency of operation for optimal performance.
5. R1 and R2 are optional and do not need to be loaded if the shut-down functionality is not needed; i.e. FDD applications. If R1 and R2 are not loaded, the LNA will operate in its standard "ON" state.
6. A through line is included on the evaluation board to de-embed the board losses.

Bill of Material

Reference Des.	Value	Description	Manuf.	Part Number
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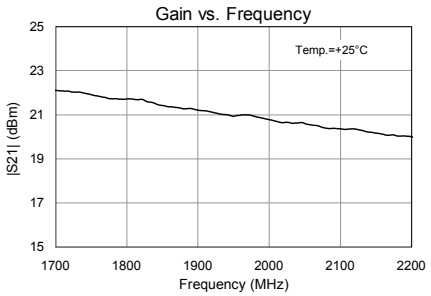
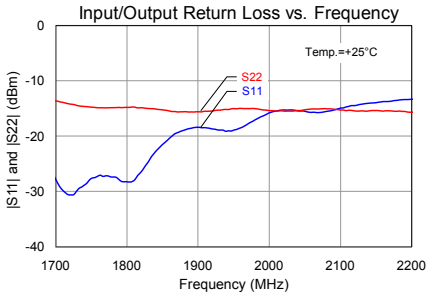
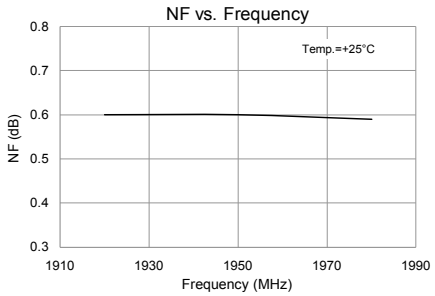
R2	33K Ω	Resistor, Chip, 0402, 5%, 1/16W	various	various
R3	0 Ω	Resistor, Chip, 0402, 5%, 1/16W	various	various
L1	8.2 nH	Inductor, 0603, 5%, Ceramic	various	various
L2	3.9 nH	Inductor, 0402, 5%, Ceramic	various	various
C1	3.3 pF	Cap., Chip, 0402, ±0.25 pF, 50V, NPO/COG	various	various
C4	1.0 uF	Cap., Chip, 0402, 10%, 10V, X5R	various	various
C2, C3, C5, C6	100 pF	Cap., Chip, 0402, 5%, 50V, NPO/COG	various	various
J3, J4, J5	n/a	Solder Turret	various	various

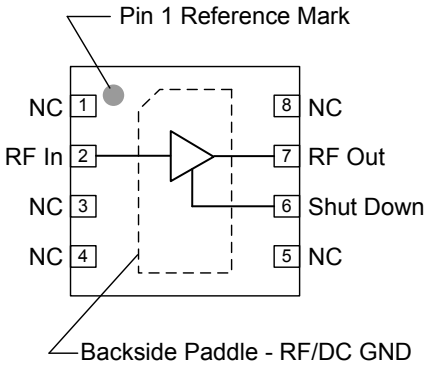
RF Performance Plots







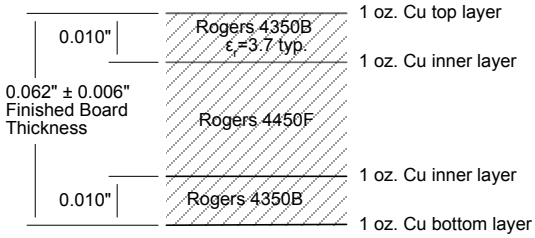
Pin Configuration and Description



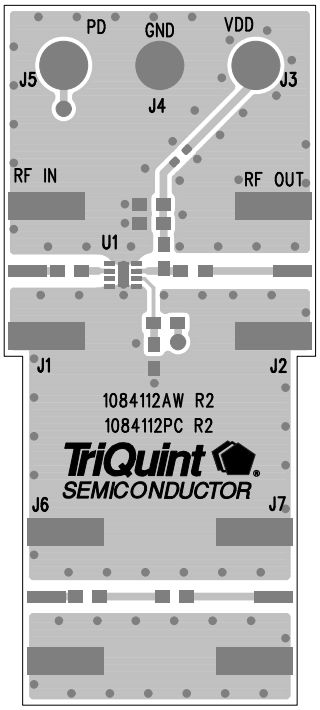
Pin	Symbol	Description
2	RF In	RF Input pin. A DC Block is required.
6	Shut Down	A high voltage turns off the device. If the pin is not connected or is less than 1V, then the device will operate under its normal operating condition.
7	RF Out / Bias	RF Output pin. DC bias will also need to be injected through a RF bias choke/inductor for operation.
1, 3, 4, 5, 8	NC	No electrical connection. Provide grounded land pads for PCB mounting integrity.
Backside Paddle	RF/DC GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance; see PCB Mounting Pattern for suggested footprint.

Evaluation Board PCB Information

PCB 1084112 Material and Stack-Up



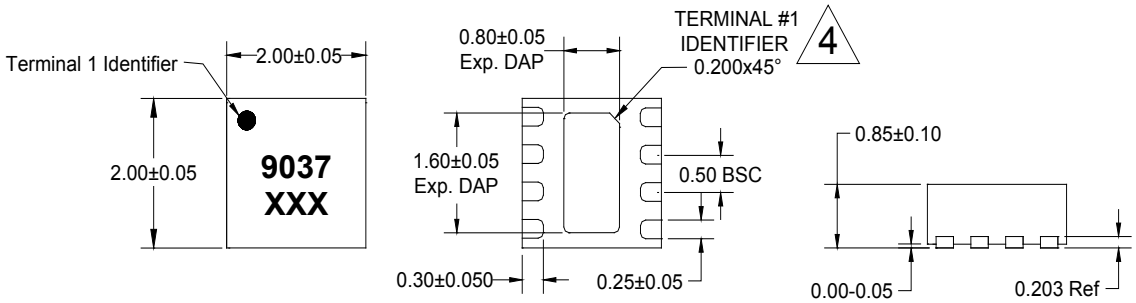
50 ohm input/output (I/O) line structure
Width = 0.020”
Gap = 0.032”



Mechanical Information

Package Marking and Dimensions

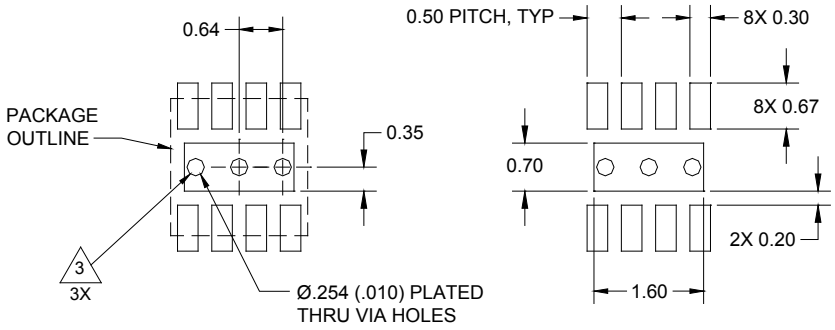
Marking: Part number – 9037
Lot Code –XXXX



NOTES:

1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-220, Issue E (Variation VGGC) for thermally enhanced plastic very thin fine pitch quad flat no lead package (QFN).
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



NOTES:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10”).
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating:	Class 1A
Value:	Passes ≥ 250 V to < 500 V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114

ESD Rating:	Class II
Value:	Passes 200 V to < 500 V
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22-C101

MSL Rating

MSL Rating:	Level 1
Test:	260°C convection reflow
Standard:	JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Package contact plating: NiPdAu

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Important Notice

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel:** +1.503.615.9000
Email: info-sales@tqs.com **Fax:** +1.503.615.8902

For technical questions and application information: **Email:** sjcapplications.engineering@tqs.com

Contact Information

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