DATA SHEET

TDA6106Q
Video output amplifier

Product specification
File under Integrated Circuits, IC02

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Philips Semiconductors

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Video output amplifier TDA6106Q

FEATURES

- No external heatsink required
- Black current measurement output for Automatic Black current Stabilization (ABS)
- Internal 2.5 V reference circuit
- Internal protection against positive appearing CRT flashover discharges
- Single supply voltage of 200 V
- Simple application with a variety of colour decoders
- Controlled switch-off behaviour.

GENERAL DESCRIPTION

The TDA6106Q is a monolithic video output amplifier with a 6 MHz bandwidth and is contained in a 9-lead plastic DIL-bent-SIL medium power package. The device uses high-voltage DMOS technology and is intended to drive the cathode of a CRT. To obtain maximum performance, the amplifier should be used with black current control.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA6106Q	DBS9MPF	plastic DIL-bent-SIL medium power package with fin; 9 leads	SOT111-1

BLOCK DIAGRAM

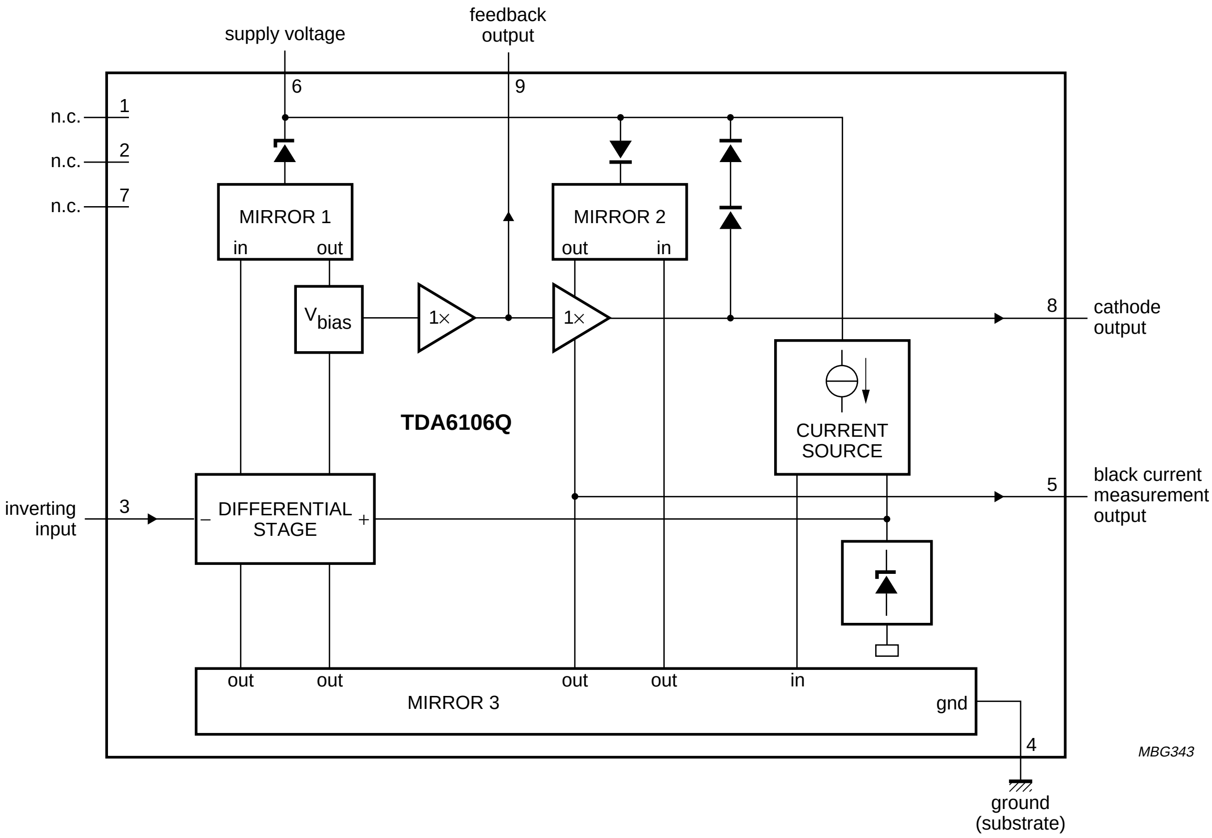


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
V_{in}	3	inverting input voltage
GND	4	ground, substrate
I_{om}	5	black current measurement output
V_{DD}	6	supply voltage
n.c.	7	not connected
V_{oc}	8	cathode output voltage
V_{of}	9	feedback output voltage

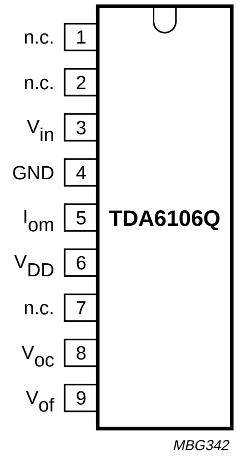


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); voltages with respect to pin 4 (ground) unless otherwise specified; currents specified as in Fig.1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		0	250	V
V_{in}	inverting input voltage		0	8	V
V_{om}	black current measurement output voltage		0	6	V
V_{oc}	cathode DC output voltage		0	V_{DD}	V
V_{of}	feedback output voltage		0	V_{DD}	V
$I_{oc(l)}$	low non-repetitive peak cathode output current	flashover discharge = 100 μC; note 1	0	5	A
$I_{oc(h)}$	high non-repetitive peak cathode output current	flashover discharge = 100 nC; note 2	0	10	A
P_{max}	maximum power dissipation		0	tbf	W
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		–20	+150	°C
V_{esd}	electrostatic discharge	note 3	–2000	+2000	V
		note 4	–300	+300	V

Notes

1. The cathode output is protected against peak currents (caused by positive voltage peaks during high-resistance flash) of 5 A maximum with a charge content of 100 μC.
2. The cathode output is also protected against peak currents (caused by positive voltage peaks during low-resistance flash) of 10 A maximum with a charge content of 100 nC.
3. Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
4. Machine model: equivalent to discharging a 200 pF capacitor through a 0 Ω resistor.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

QUALITY SPECIFICATION

Quality specification *"SNW-FQ-611 part E"* is applicable, except for ESD Human body model see Chapter "Limiting values", and can be found in the *"Quality reference handbook"* (ordering number 9397 750 00192).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER(1)	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	56	K/W
$R_{th\ j\text{-}c}$	thermal resistance from junction to case	12	K/W

Note

1. External heatsink not required.

CHARACTERISTICS

Operating range: T_{amb} = –20 to +65 °C; V_{DD} = 180 to 210 V (see note 1), V_{om} = 1.4 to 6 V.
Test conditions: T_{amb} = 25 °C; V_{DD} = 200 V; V_{om} = 4 V; C_L = 10 pF (C_L consists of parasitic and cathode capacitance); measured in test circuit of Fig.5; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DD}	quiescent voltage supply current	V_{ocDC} = 100 V	2.8	3.0	3.3	mA
I_{bias}	input bias current (pin 3)	V_{ocDC} = 100 V	0	–	20	μA
V_{int}	internal reference voltage input stage	V_{ocDC} = 100 V	–	2.5	–	V
$I_{om(os)}$	offset current of black current measurement output	I_{oc} = 0 μA; V_{in} = 1.5 to +3.5 V; V_{om} = 1.4 to 6 V	–10	0	+10	μA
ΔV_{Tint}	temperature drift of internal reference voltage input stage	V_{ocDC} = 100 V	–	0.5	–	mV/K
$\frac{\Delta I_{om}}{\Delta I_{oc}}$	linearity of current transfer	I_{oc} = –10 μA to 3 mA; V_{in} = 1.5 to +3.5 V; V_{om} = 1.4 to 6 V	0.9	1.0	1.1	
$I_{of(max)}$	maximum peak output current (pin 9)	V_{oc} = 20 V to V_{DD} –30 V	–	25	–	mA
$V_{oc(min)}$	minimum output voltage (pin 8)	V_{in} = 3.5 V	–	7	12	V
$V_{oc(max)}$	maximum output voltage (pin 8)	V_{in} = 1.5 V	V_{DD} – 14	V_{DD} – 10	–	V
GB	gain bandwidth product of open-loop gain $V_{os}/V_{i,\ dm}$	f = 500 kHz; V_{ocDC} = 100 V	–	0.52	–	GHz
BW_S	small signal bandwidth	V_{ocAC} = 60 V (p-p); V_{ocDC} = 100 V	5	6	–	MHz
BW_L	large signal bandwidth	V_{ocAC} = 100 V (p-p); V_{ocDC} = 100 V	4.7	5.7	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{pd}	cathode output propagation delay time 50% input to 50% output	V_{oc} = 50 to 150 V square wave; f < 1 MHz; t_{rin} = t_{fin} = 40 ns; see Figs 3 and 4	38	49	60	ns
t_r	cathode output rise time 10% output to 90% output	V_{oc} = 50 to 150 V square wave; f < 1 MHz; t_{fin} = 40 ns; see Fig.4	62	74	87	ns
t_f	cathode output fall time 90% output to 10% output	V_{oc} = 150 to 50 V square wave; f < 1 MHz; t_{rin} = 40 ns; see Fig.4	62	74	87	ns
t_s	settling time 50% input to (99% < output < 101%)	V_{oc} = 50 to 150 V square wave; f < 1 MHz; t_{rin} = t_{fin} = 40 ns; see Figs 3 and 4	–	–	350	ns
SR	slew rate between 50 and 150 V	V_{in} = 2 V (p-p) square wave; f < 1 MHz; t_{rin} = t_{fin} = 40 ns	–	1200	–	V/µs
O_V	cathode output voltage overshoot	V_{oc} = 50 to 150 V square wave; f < 1 MHz; t_{rin} = t_{fin} = 40 ns; see Figs 3 and 4	–	1	–	%
PSRR	power supply rejection ratio	f < 50 kHz; note 2	–	60	–	dB

Notes

1. The rating of supply voltage is 250 V, but because of flash the maximum operating range for supply voltage is 210 V.
2. PSSR: The ratio of the change in supply voltage to the change in input voltage when there is no change in output voltage.

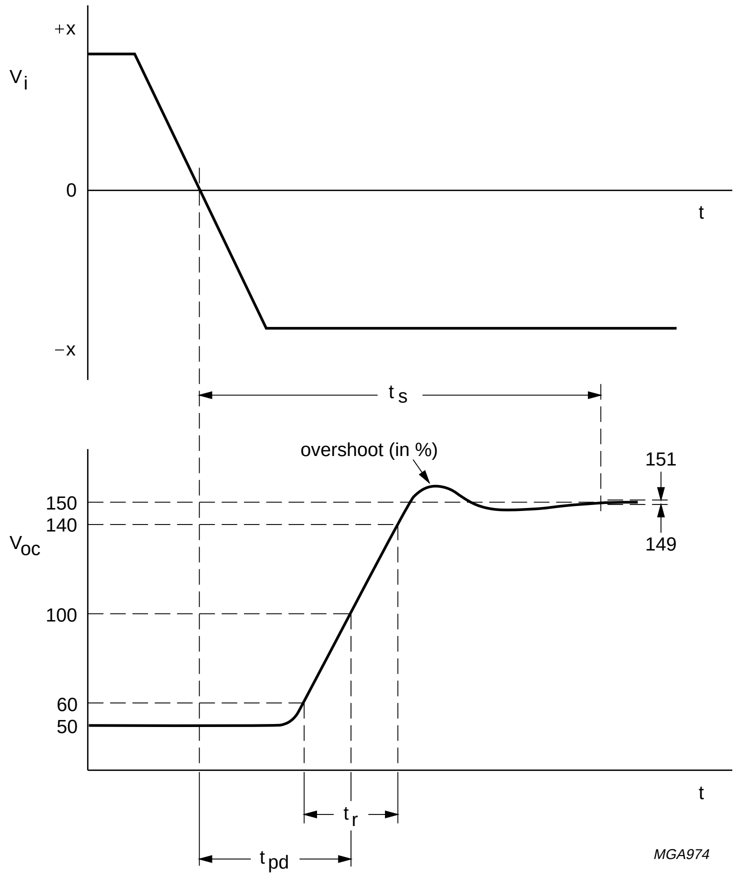


Fig.3 Output voltage (pin 8 rising edge) as a function of AC input signal.

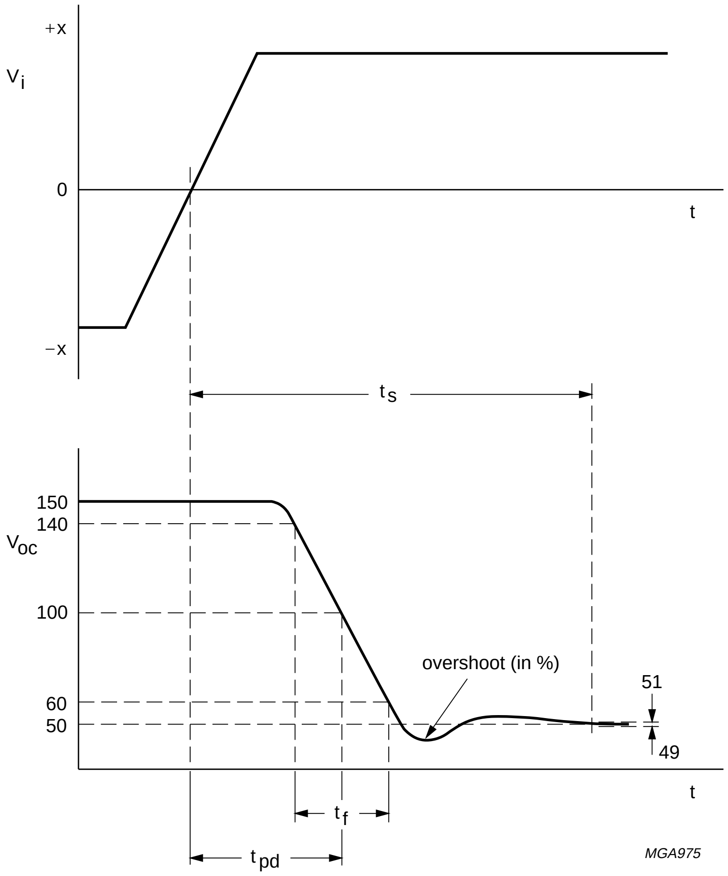


Fig.4 Output voltage (pin 8 falling edge) as a function of AC input signal.

Flashover protection

The TDA6106Q incorporates a protection diode against CRT flashover discharges that clamp the cathode output voltage to a maximum of $V_{DD} + V_{diode}$. To limit the diode current, an external 1.5 kΩ carbon high-voltage resistor in series with the cathode output and a 2 kV spark gap are needed (for this resistor-value, the CRT has to be connected to the main PCB). This addition produces an increase in the rise and fall times of approximately 7.5 ns and a decrease in the overshoot of approximately 1.3%.

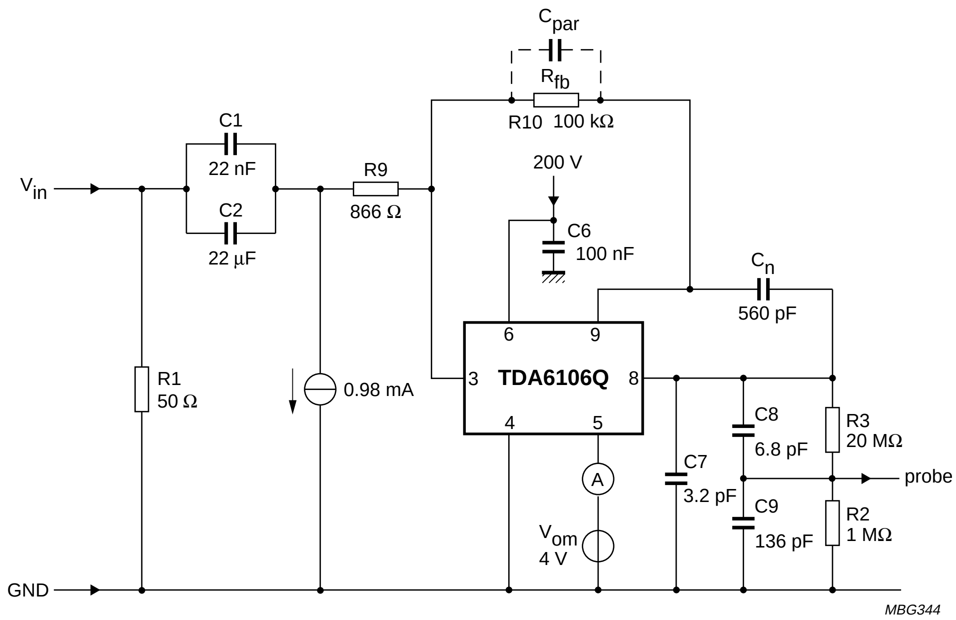
V_{DD} to GND must be decoupled:

1. With a capacitor larger than 20 nF with good HF behaviour (e.g. foil). This capacitor must be placed as close as possible to pins 6 and 4, but definitely within 5 mm.
2. With a capacitor larger than10 µF on the picture tube base print (shared by three output stages).

Switch-off behaviour

The output pins of the TDA6106Q are still under the control of the input pin for a supply voltage down to approximately 30 V.

TEST AND APPLICATION INFORMATION



C_{par} = 150 fF.

Fig.5 Test circuit with feedback factor $^1/_{116}$.

Dissipation

With respect to dissipation, distinction must be made between static dissipation (independent of frequency) and dynamic dissipation (proportional to frequency).

The static dissipation of the TDA6106Q is due to supply currents and load currents in the feedback network and CRT.

$$P_{stat} = V_{DD} \times I_{DD} + V_{oc} \times I_{oc} - V_{of} \times \left(\frac{V_{of}}{R_{fb}}\right)$$

Where:

R_{fb} = value of feedback resistor.

I_{oc} = DC value of cathode current.

The dynamic dissipation equals:

$$P_{dyn} = V_{DD} \times (C_L + C_{fb} + C_{int}) \times f \times V_{o(p-p)} \times b$$

Where:

C_L = load capacitance.

C_{fb} = feedback capacitance.

C_{int} = internal load capacitance (≈ 4 pF).

f = input frequency.

$V_{o(p-p)}$ = output voltage (peak-to-peak value).

b = non-blanking duty-cycle.

The IC must be mounted on the picture tube base print to minimize the load capacitance (C_L).

INTERNAL PIN CONFIGURATION

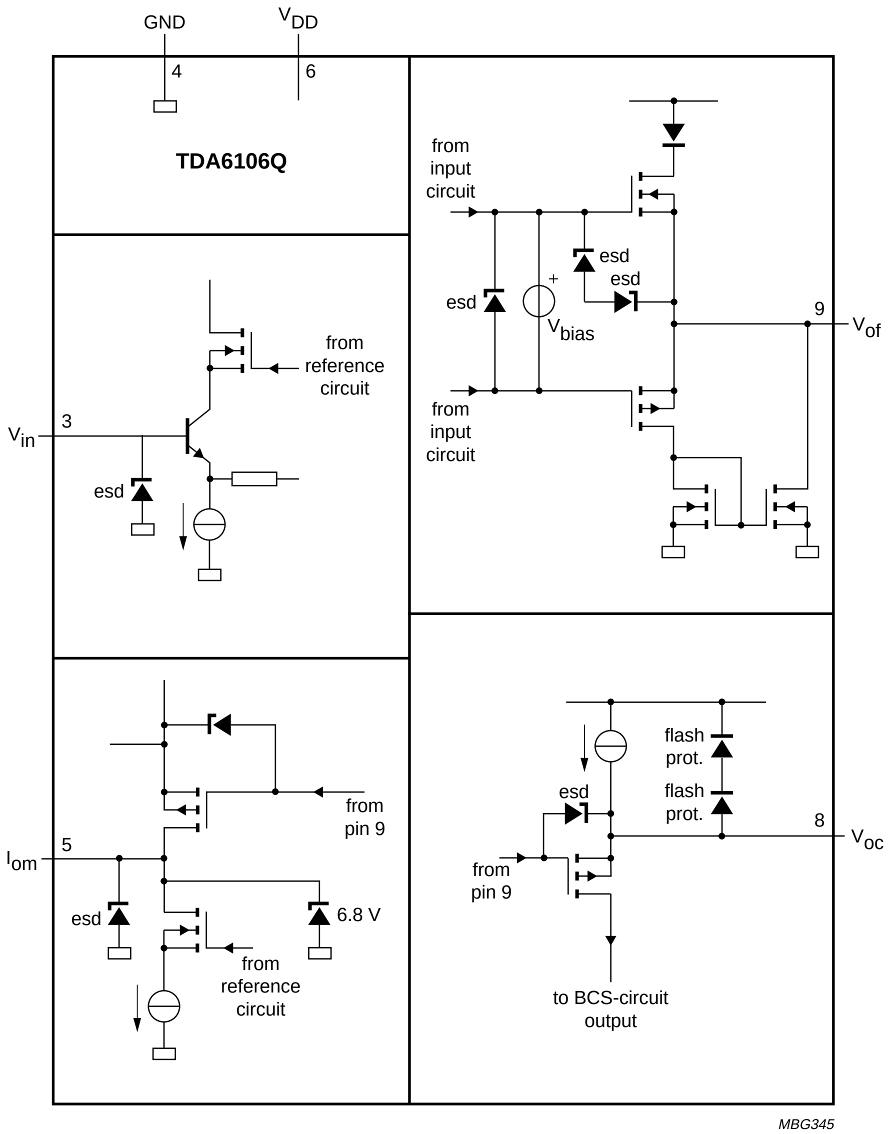
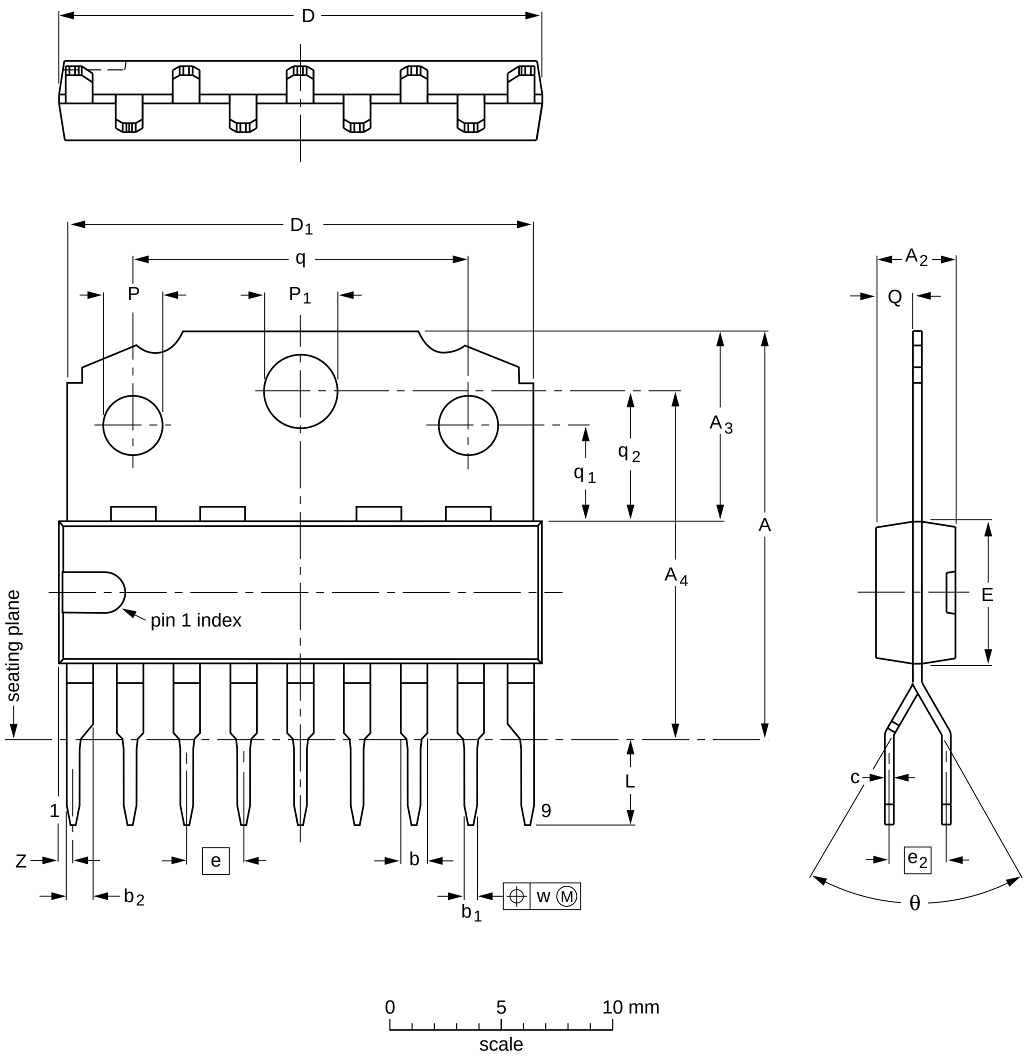


Fig.6 Internal pin configuration.

PACKAGE OUTLINE

DBS9MPF: plastic DIL-bent-SIL medium power package with fin; 9 leads **SOT111-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2 max.	A_3	A_4	b	b_1	b_2	c	D(1)	D_1	E(1)	e	e_2	L	P	P_1	Q	q	q_1	q_2	w	Z(1) max.	θ
mm	18.5 17.8	3.7	8.7 8.0	15.5 15.1	1.40 1.14	0.67 0.50	1.40 1.14	0.48 0.38	21.8 21.4	21.4 20.7	6.48 6.20	2.54	2.54	3.9 3.4	2.75 2.50	3.4 3.2	1.75 1.55	15.1 14.9	4.4 4.2	5.9 5.7	0.25	1.0	65° 55°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT111-1						~~92-11-17~~ 95-03-11

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *“IC Package Databook”* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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