

## 256 Kb (64K x 4) Static RAM

### Features

- **Fast access time: 12 ns, 15 ns, and 25 ns**
- **Wide voltage range: 5.0V  $\pm$  10% (4.5V to 5.5V)**
- **CMOS for optimum speed/power**
- **TTL-compatible inputs and outputs**
- **Available in 24 DIP, 24 SOJ, 28 DIP, and 28 SOJ**

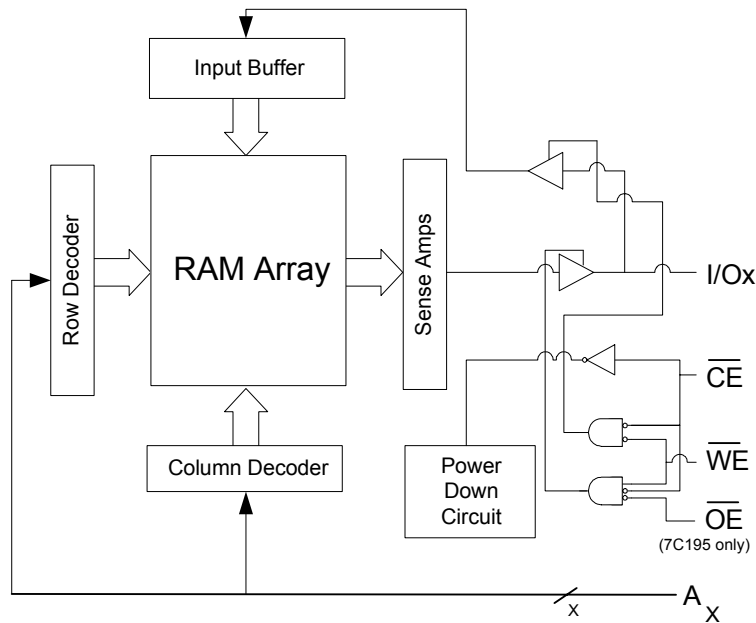
### General Description<sup>1</sup>

The CY7C194B-CY7C195B is a high-performance CMOS Asynchronous SRAM organized as 64K  $\times$  4 bits that supports an asynchronous memory interface. The device features an automatic power-down feature that significantly reduces power consumption when deselected. Output enable (OE) is supported only in CY7C195B.<sup>2</sup>

See the Truth Table in this data sheet for a complete description of read and write modes.

The CY7C194B-CY7C195B is available in 24 DIP, 24 SOJ, 28 DIP, and 28 SOJ package(s).

### Logic Block Diagram



### Product Portfolio

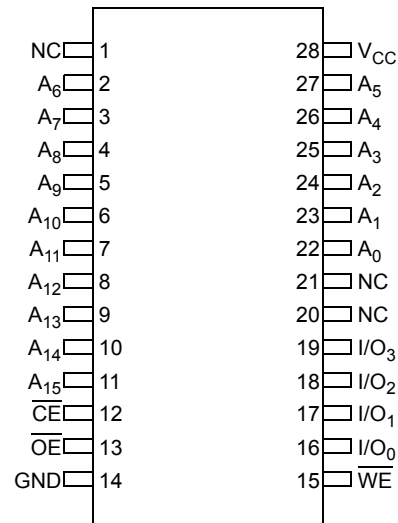
|                              | 12 ns | 15 ns | 25 ns | Unit |
|------------------------------|-------|-------|-------|------|
| Maximum Access Time          | 12    | 15    | 25    | ns   |
| Maximum Operating Current    | 90    | 80    | 80    | mA   |
| Maximum CMOS Standby Current | 10    | 10    | 10    | mA   |

### Notes:

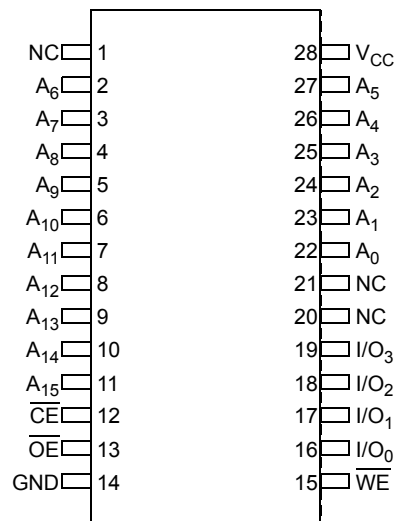
1. For best-practice recommendations, please refer to the Cypress application note *System Design Guidelines* on [www.cypress.com](http://www.cypress.com).
2. All OE-specific descriptions and parameters in this datasheet pertain to CY7C195 only.

# Pin Layout and Specifications

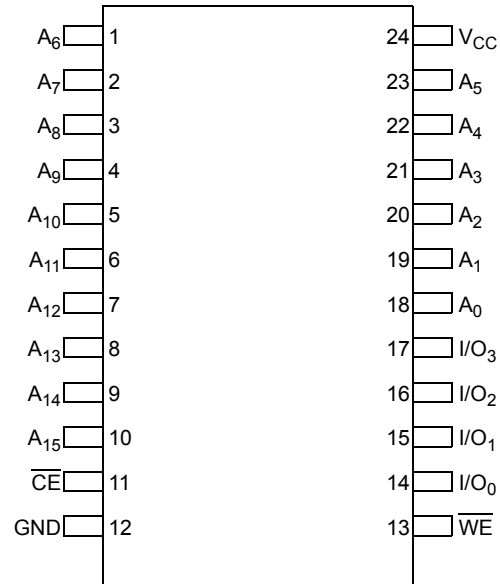
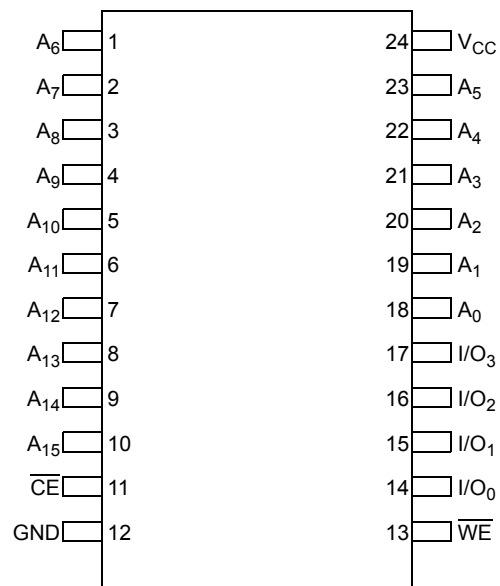
## CY7C195B 28 DIP (6.9 × 35.6 × 3.5 mm) – P21



## CY7C195B 28 SOJ (8 × 18 × 3.5 mm) – V21



**Pin Layout and Specifications** (continued)

**CY7C194B 24 SOJ (8 × 15 × 3.5 mm) – V13**

**CY7C194B 24 DIP (6.6 × 31.8 × 3.5 mm) – P13**


### Pin Description

| Pin              | Type            | Description                                                      | 28 DIP                                                             | 24 DIP                                                            | 24 SOJ                                                            | 28 SOJ                                                             |
|------------------|-----------------|------------------------------------------------------------------|--------------------------------------------------------------------|-------------------------------------------------------------------|-------------------------------------------------------------------|--------------------------------------------------------------------|
| A <sub>x</sub>   | Input           | <b>Address Inputs.</b>                                           | 2, 3, 4, 5, 6,<br>7, 8, 9, 10,<br>11, 22, 23,<br>24, 25, 26,<br>27 | 1, 2, 3, 4, 5,<br>6, 7, 8, 9,<br>10, 18, 19,<br>20, 21, 22,<br>23 | 1, 2, 3, 4, 5,<br>6, 7, 8, 9,<br>10, 18, 19,<br>20, 21, 22,<br>23 | 2, 3, 4, 5, 6,<br>7, 8, 9, 10,<br>11, 22, 23,<br>24, 25, 26,<br>27 |
| CE               | Control         | <b>Chip Enable.</b>                                              | 12                                                                 | 11                                                                | 11                                                                | 12                                                                 |
| I/O <sub>x</sub> | Input or Output | <b>Data Input/Outputs.</b>                                       | 16, 17, 18,<br>19                                                  | 14, 15, 16,<br>17                                                 | 14, 15, 16,<br>17                                                 | 16, 17, 18,<br>19                                                  |
| NC               | –               | <b>No Connect.</b> Pins are not internally connected to the die. | 1, 20, 21                                                          | –                                                                 | –                                                                 | 1, 20, 21                                                          |
| OE               | Control         | <b>Output Enable (CY7C195 only).</b>                             | 13                                                                 | –                                                                 | –                                                                 | 13                                                                 |
| V <sub>CC</sub>  | Supply          | <b>Power (5.0V).</b>                                             | 28                                                                 | 24                                                                | 24                                                                | 28                                                                 |
| WE               | Control         | <b>Write Enable.</b>                                             | 15                                                                 | 13                                                                | 13                                                                | 15                                                                 |

### CY7C195B Truth Table

| $\overline{\text{CE}}$ | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | I/O <sub>x</sub> | Mode                       | Power                       |
|------------------------|------------------------|------------------------|------------------|----------------------------|-----------------------------|
| H                      | X                      | X                      | High Z           | Deselect / Power-Down      | Standby ( $I_{\text{SB}}$ ) |
| L                      | L                      | H                      | Data Out         | Read                       | Active ( $I_{\text{CC}}$ )  |
| L                      | X                      | L                      | Data In          | Write                      | Active ( $I_{\text{CC}}$ )  |
| L                      | H                      | H                      | High Z           | Selected, outputs disabled | Active ( $I_{\text{CC}}$ )  |

### CY7C194B Truth Table

| $\overline{\text{CE}}$ | $\overline{\text{WE}}$ | Input/Output | Mode       | Power                       |
|------------------------|------------------------|--------------|------------|-----------------------------|
| H                      | X                      | High Z       | Power-Down | Standby ( $I_{\text{SB}}$ ) |
| L                      | H                      | Data Out     | Read       | Active ( $I_{\text{CC}}$ )  |
| L                      | L                      | Data In      | Write      | Active ( $I_{\text{CC}}$ )  |

**Maximum Ratings** (Above which the useful life may be impaired. For user guidelines, not tested.)

| Parameter        | Description                                                    | Value                          | Unit |
|------------------|----------------------------------------------------------------|--------------------------------|------|
| T <sub>STG</sub> | Storage Temperature                                            | –65 to +150                    | °C   |
| T <sub>AMB</sub> | Ambient Temperature with Power Applied (i.e. case temperature) | –55 to +125                    | °C   |
| V <sub>CC</sub>  | Core Supply Voltage Relative to V <sub>SS</sub>                | –0.5 to +7.0                   | V    |
| V <sub>CC</sub>  | DC Voltage Applied to any Pin Relative to V <sub>SS</sub>      | –0.5 to V <sub>CC</sub> + null | V    |
| I <sub>OUT</sub> | Output Short-Circuit Current                                   | 20                             | mA   |
| V <sub>ESD</sub> | Static Discharge Voltage (per MIL-STD-883, Method 3015)        | > 2001                         | V    |
| I <sub>LU</sub>  | Latch-up Current                                               | > 200                          | mA   |

## Operating Range

| Range      | Ambient Temperature (T <sub>A</sub> ) | Voltage Range (V <sub>CC</sub> ) |
|------------|---------------------------------------|----------------------------------|
| Commercial | 0°C to 70°C                           | 5.0V ± 10%                       |

## DC Electrical Characteristics<sup>3</sup>

| Parameter        | Description                                 | Condition                                                                                                                                    | 12 ns |                       | 15 ns |                       | 25 ns |                       | Unit |
|------------------|---------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|-------|-----------------------|-------|-----------------------|-------|-----------------------|------|
|                  |                                             |                                                                                                                                              | Min   | Max                   | Min   | Max                   | Min   | Max                   |      |
| V <sub>IH</sub>  | Input HIGH Voltage                          |                                                                                                                                              | 2.2   | V <sub>CC</sub> + 0.3 | 2.2   | V <sub>CC</sub> + 0.3 | 2.2   | V <sub>CC</sub> + 0.3 | V    |
| V <sub>IL</sub>  | Input LOW Voltage                           |                                                                                                                                              | –0.3  | 0.8                   | –0.3  | 0.8                   | –0.5  | 0.8                   | V    |
| V <sub>OH</sub>  | Output HIGH Voltage                         | V <sub>CC</sub> = Min., I <sub>OH</sub> = –4.0 ma                                                                                            | 2.4   | –                     | 2.4   | –                     | 2.4   | –                     | V    |
| V <sub>OL</sub>  | Output LOW Voltage                          | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 ma                                                                                             | –     | 0.4                   | –     | 0.4                   | –     | 0.4                   | V    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current    | V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = F <sub>MAX</sub> = 1 / t <sub>RC</sub>                                                  | –     | 90                    | –     | 80                    | –     | 80                    | mA   |
| I <sub>SB1</sub> | Automatic CE Power-down Current TTL Inputs  | V <sub>CC</sub> = Max., CE ≥ V <sub>IH</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = F <sub>MAX</sub> | –     | 30                    | –     | 30                    | –     | 30                    | mA   |
| I <sub>SB2</sub> | Automatic CE Power-down Current CMOS Inputs | V <sub>CC</sub> = Max., CE ≥ V <sub>CC</sub> – 0.3v, V <sub>IN</sub> > V <sub>CC</sub> – 0.3v or V <sub>IN</sub> ≤ 0.3, f = 0 Commercial     | –     | 10                    | –     | 10                    | –     | 10                    | mA   |
| I <sub>OZ</sub>  | Output Leakage Current                      | GND ≤ V <sub>i</sub> ≤ V <sub>CC</sub> , Output Disabled                                                                                     | –5    | +5                    | –5    | +5                    | –5    | +5                    | uA   |
| I <sub>IX</sub>  | Input Load Current                          | GND ≤ V <sub>i</sub> ≤ V <sub>CC</sub>                                                                                                       | –5    | +5                    | –5    | +5                    | –5    | +5                    | uA   |

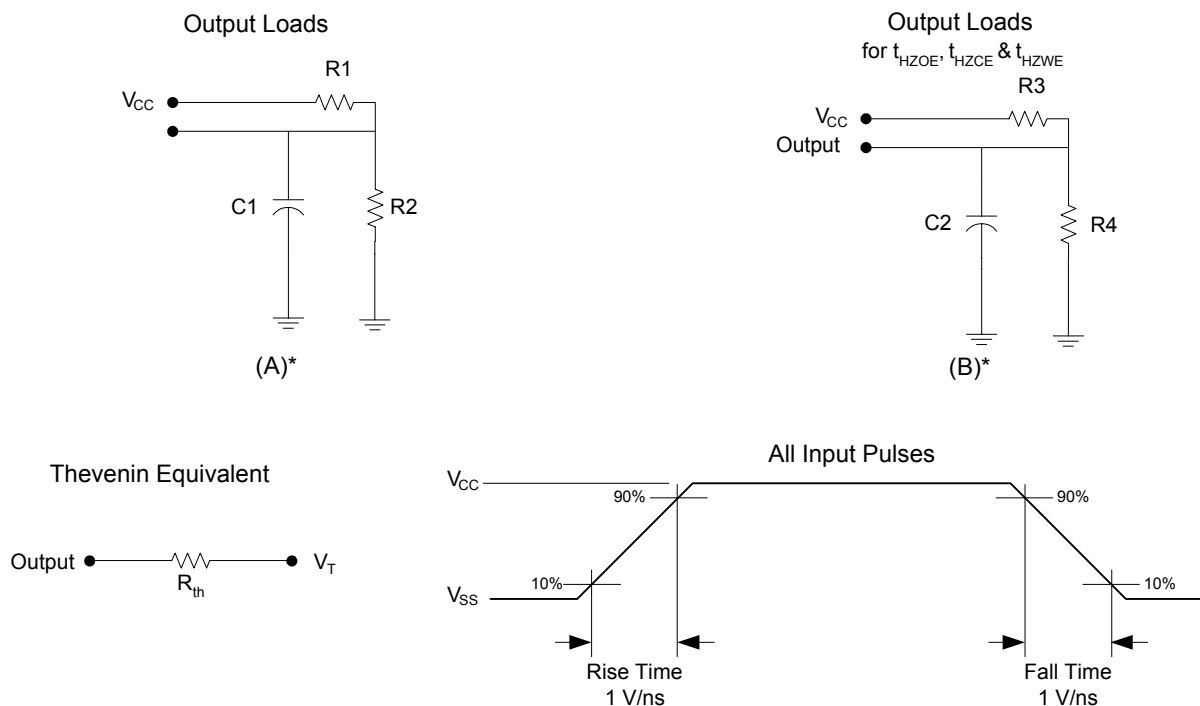
## Capacitance<sup>4</sup>

| Parameter        | Description        | Conditions                                               | Max            | Unit |
|------------------|--------------------|----------------------------------------------------------|----------------|------|
|                  |                    |                                                          | ALL - PACKAGES |      |
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V | 7              | pF   |
| C <sub>OUT</sub> | Output Capacitance |                                                          | 10             |      |

### Notes:

- V<sub>IL</sub> (min) = –2.0V for pulse durations of less than 20 ns.
- Tested initially and after any design or process change that may affect these parameters.

## AC Test Loads



\* including scope and jig capacitance

## AC Test Conditions

| Parameter       | Description       | Nom. | Unit     |
|-----------------|-------------------|------|----------|
| C1              | Capacitor 1       | 30   | pF       |
| C2              | Capacitor 2       | 5    |          |
| R1              | Resistor 1        | 480  | $\Omega$ |
| R2              | Resistor 2        | 255  |          |
| R3              | Resistor 3        | 480  |          |
| R4              | Resistor 4        | 255  |          |
| R <sub>TH</sub> | Resistor Thevenin | 167  |          |
| V <sub>TH</sub> | Voltage Thevenin  | 1.73 | V        |

## Thermal Resistance<sup>5</sup>

| Parameter     | Description                              | Conditions                                                                      | 28 SOJ | 24 SOJ | 28 DIP | 24 DIP | Unit                 |
|---------------|------------------------------------------|---------------------------------------------------------------------------------|--------|--------|--------|--------|----------------------|
| $\Theta_{JA}$ | Thermal Resistance (Junction to Ambient) | Still Air, soldered on a 3 x 4.5 square inches, two-layer printed circuit board | 69     | TBD    | TBD    | TBD    | $^{\circ}\text{C/W}$ |
| $\Theta_{JC}$ | Thermal Resistance (Junction to Case)    |                                                                                 | 29.84  | TBD    | TBD    | TBD    |                      |

### Notes:

5. Test Conditions assume a transition time of 3ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V

**AC Electrical Characteristics<sup>2 6 7 8</sup>**

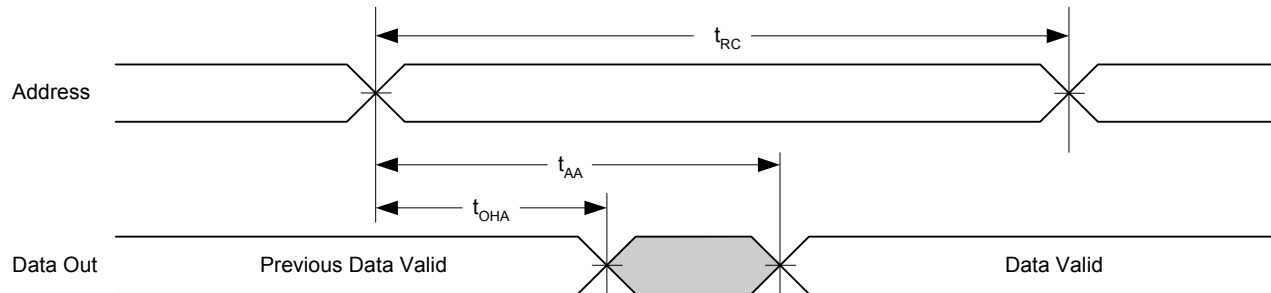
| Parameter  | Description                   | 12 ns |     | 15 ns |     | 25 ns |     | Unit |
|------------|-------------------------------|-------|-----|-------|-----|-------|-----|------|
|            |                               | Min   | Max | Min   | Max | Min   | Max |      |
| $t_{RC}$   | Read Cycle Time               | 12    | –   | 15    | –   | 25    | –   | ns   |
| $t_{AA}$   | Address to Data Valid         | –     | 12  | –     | 15  | –     | 25  | ns   |
| $t_{OHA}$  | Data Hold from Address Change | 3     | –   | 3     | –   | 3     | –   | ns   |
| $t_{ACE}$  | $\overline{CE}$ to Data Valid | –     | 12  | –     | 15  | –     | 25  | ns   |
| $t_{DOE}$  | OE to Data Valid              | –     | 6   | –     | 7   | –     | 10  | ns   |
| $t_{LZOE}$ | OE to Low Z                   | 0     | –   | 0     | –   | 0     | –   | ns   |
| $t_{HZOE}$ | $\overline{OE}$ to High Z     | –     | 5   | –     | 7   | –     | 10  | ns   |
| $t_{LZCE}$ | $\overline{CE}$ to Low Z      | 3     | –   | 3     | –   | 3     | –   | ns   |
| $t_{HZCE}$ | $\overline{CE}$ to High Z     | –     | 5   | –     | 7   | –     | 10  | ns   |
| $t_{PU}$   | $\overline{CE}$ to Power-up   | 0     | –   | 0     | –   | 0     | –   | ns   |
| $t_{PD}$   | $\overline{CE}$ to Power-down | –     | 12  | –     | 15  | –     | 25  | ns   |
| $t_{WC}$   | Write Cycle Time              | 12    | –   | 15    | –   | 25    | –   | ns   |
| $t_{SCE}$  | $\overline{CE}$ to Write End  | 9     | –   | 10    | –   | 18    | –   | ns   |
| $t_{AW}$   | Address Set-up to Write End   | 9     | –   | 10    | –   | 20    | –   | ns   |
| $t_{HA}$   | Address Hold from Write End   | 0     | –   | 0     | –   | 0     | –   | ns   |
| $t_{SA}$   | Address Set-up to Write Start | 0     | –   | 0     | –   | 0     | –   | ns   |
| $t_{PWE}$  | $\overline{WE}$ Pulse Width   | 8     | –   | 9     | –   | 18    | –   | ns   |
| $t_{SD}$   | Data Set-Up to Write End      | 7     | –   | 8     | –   | 10    | –   | ns   |
| $t_{HD}$   | Data Hold from Write End      | 0     | –   | 0     | –   | 0     | –   | ns   |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High Z | –     | 6   | –     | 7   | –     | 10  | ns   |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low Z | 3     | –   | 3     | –   | 3     | –   | ns   |

**Notes:**

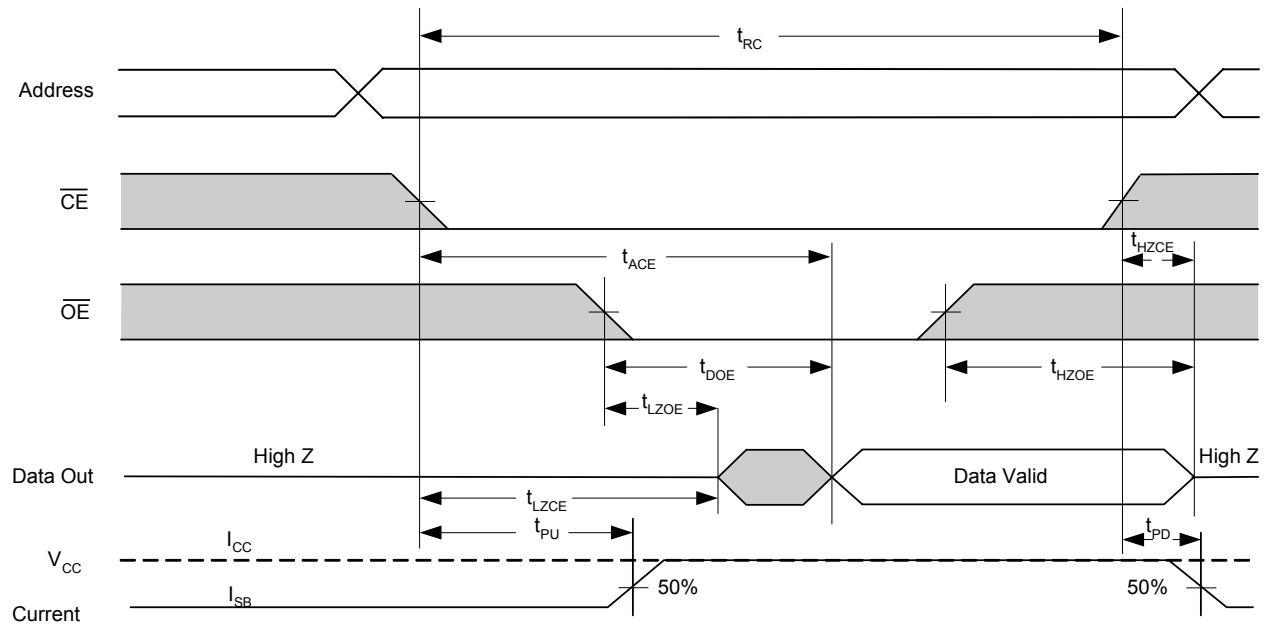
6. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
7. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
8.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZWE}$  are specified as in part (b) of the A/C Test Loads. Transitions are measured  $\pm 200$  mV from steady state voltage

## Timing Waveforms

### Read Cycle No. 1<sup>9 10</sup>

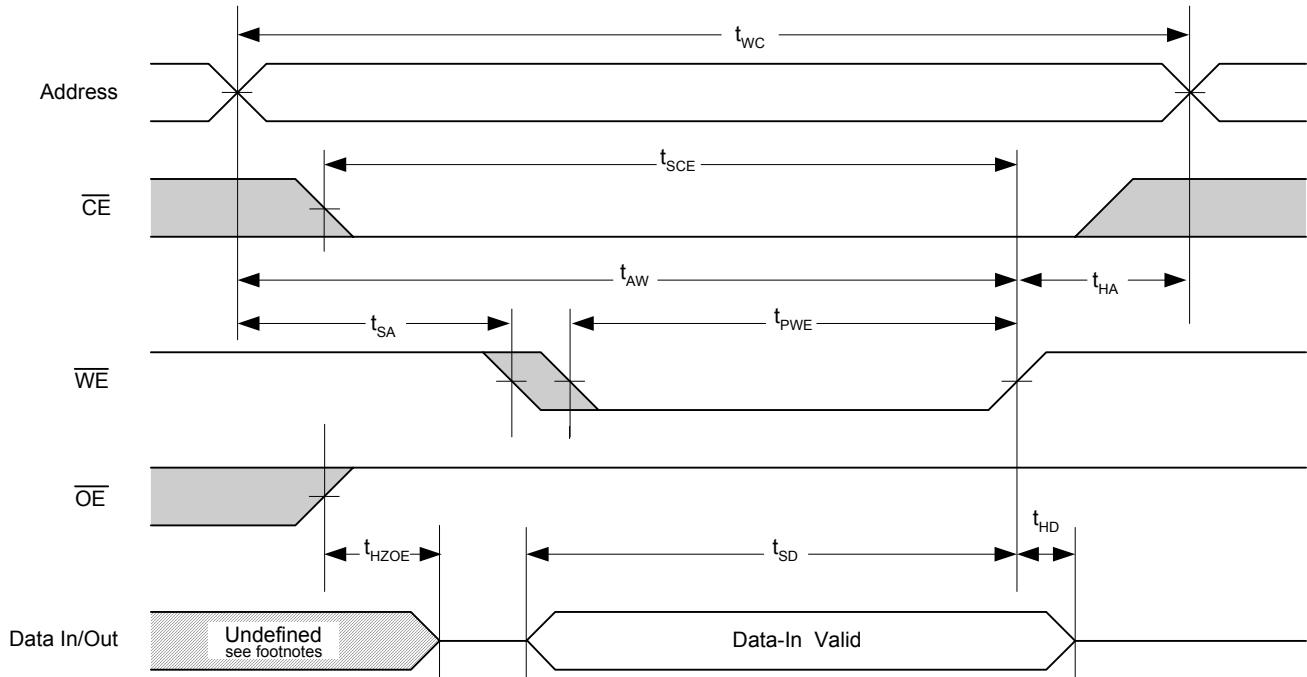
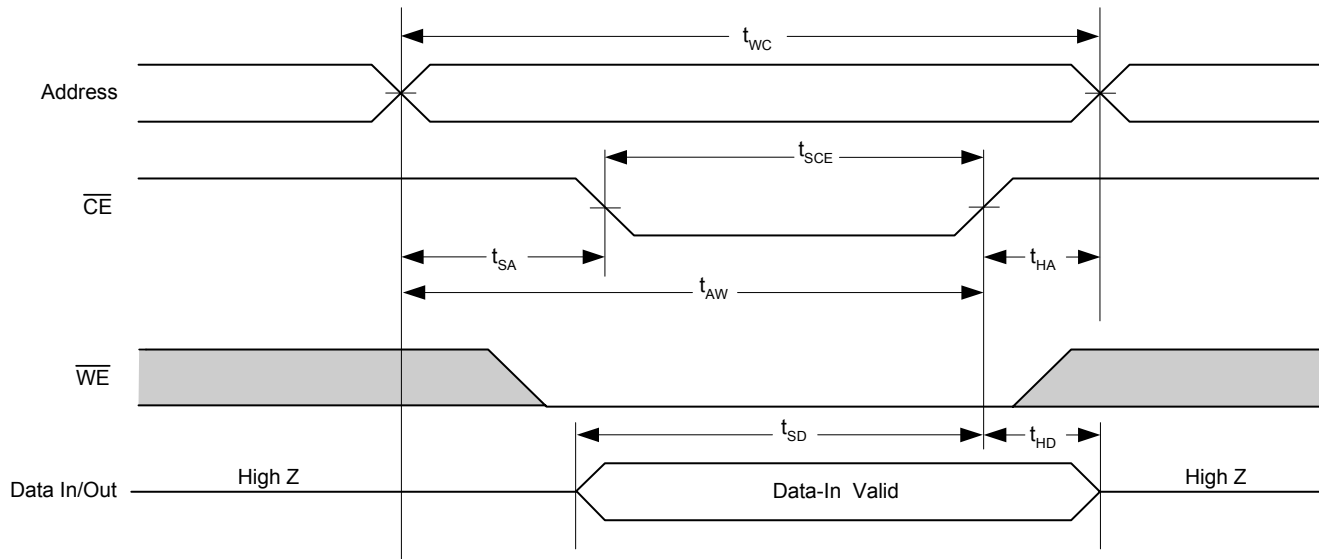


### Read Cycle No. 2<sup>2 11 12</sup>

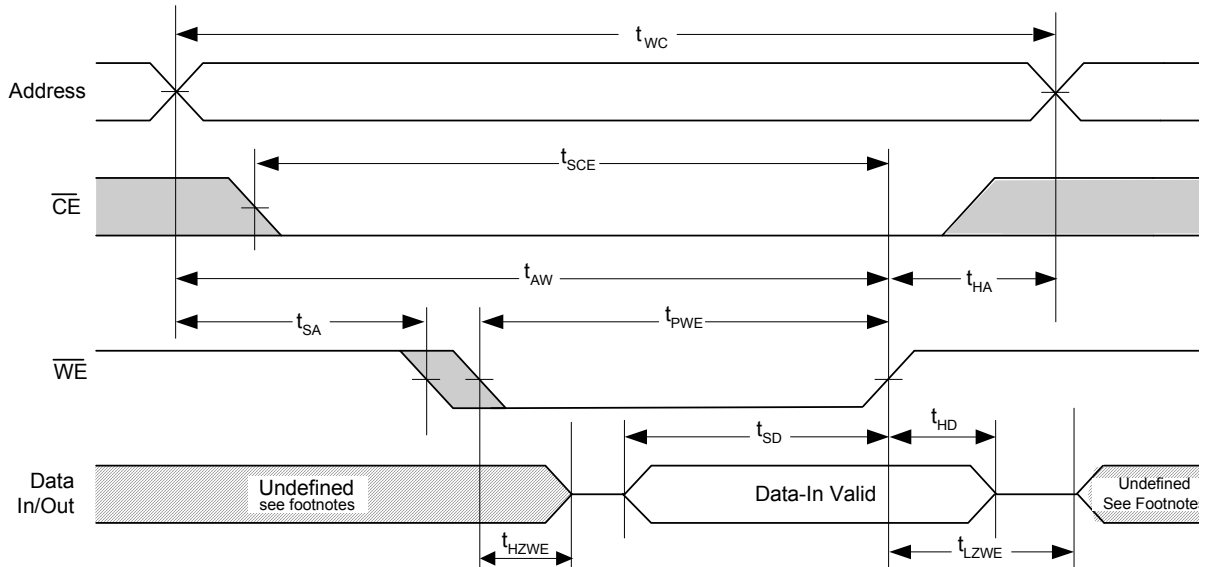


#### Notes:

9. Device is continuously selected.  $\overline{OE} = V_{IL} = \overline{CE}$ .
10.  $\overline{WE}$  is HIGH for Read Cycle.
11. This cycle is  $\overline{OE}$  Controlled and  $\overline{WE}$  is HIGH read cycle.
12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Write Cycle No. 1 ( $\overline{WE}$  Controlled) 2 13 14 15**

**Write Cycle No. 2 ( $\overline{CE}$  Controlled) 16 17 18**

**Notes:**

13. This cycle is  $\overline{WE}$  controlled,  $\overline{OE}$  is HIGH during write.
14. Data In/Out is high impedance if  $\overline{OE} = V_{IH}$ .
15. During this period the I/Os are in output state and input signals should not be applied.
16. This cycle is  $\overline{CE}$  controlled.
17. Data In/Out is high impedance if  $\overline{OE} = V_{IH}$ .
18. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.

**Write Cycle No. 3** ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  Low) <sup>2 19</sup>

**Ordering Information**

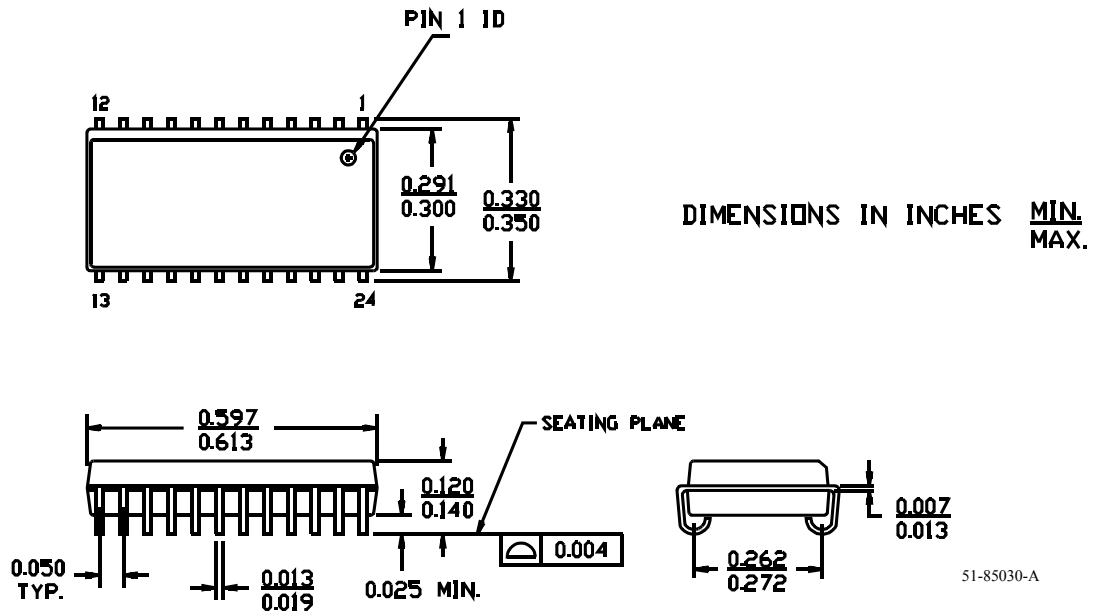
| Speed | Ordering Code | Package Name | Package Type                 | Power Option | Operating Range |
|-------|---------------|--------------|------------------------------|--------------|-----------------|
| 12 ns | CY7C195B-12VC | V21          | 28 SOJ (8 x 18 x 3.5 mm)     | Standard     | Commercial      |
| 15 ns | CY7C194B-15PC | P13          | 24 DIP (6.6 x 31.8 x 3.5 mm) | Standard     | Commercial      |
| 15 ns | CY7C194B-15VC | V13          | 24 SOJ (8 x 15 x 3.5 mm)     | Standard     | Commercial      |
| 15 ns | CY7C195B-15VC | V21          | 28 SOJ (8 x 18 x 3.5 mm)     | Standard     | Commercial      |
| 25 ns | CY7C194B-25VC | V13          | 24 SOJ (8 x 15 x 3.5 mm)     | Standard     | Commercial      |
| 25 ns | CY7C195B-25PC | P21          | 28 DIP (6.9 x 35.6 x 3.5 mm) | Standard     | Commercial      |

**Notes:**

19. The cycle is  $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  low. The minimum write cycle time is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

Package Diagram

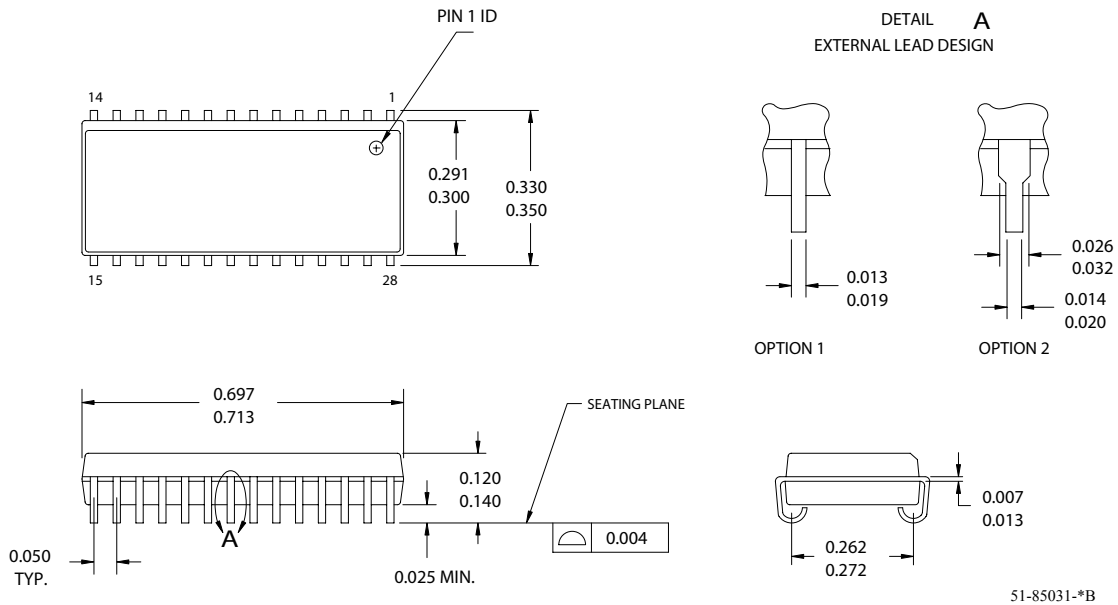
24-Lead (300-Mil) Molded SOJ V13



28-Lead (300-Mil) Molded SOJ V21

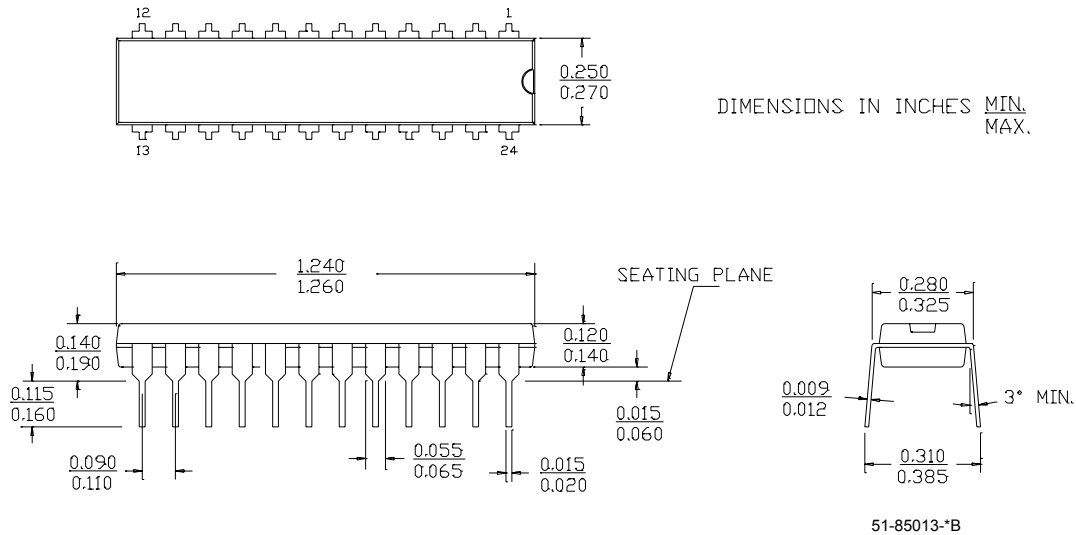
DIMENSIONS IN INCHES

MIN.  
MAX.

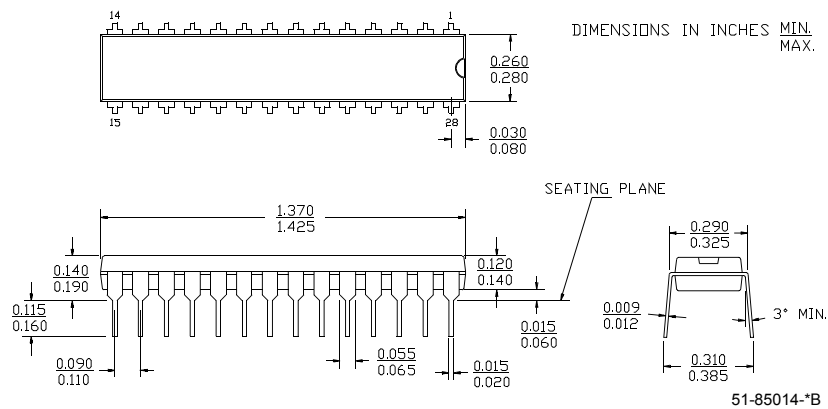


**Package Diagram (continued)**

**24-Lead (300-Mil) PDIP P13**



**28-Lead (300-Mil) Molded DIP P21**



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**Document History Page**

| Document Title: CY7C194B-CY7C195B 256 Kb (64K x 4) Static RAM<br>Document Number: 38-05409 |         |            |                 |                                                                                                                                                                                                                                                   |
|--------------------------------------------------------------------------------------------|---------|------------|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| REV.                                                                                       | ECN No. | Issue Date | Orig. of Change | Description of Change                                                                                                                                                                                                                             |
| **                                                                                         | 129234  | 09/16/03   | HGK             | New Data Sheet                                                                                                                                                                                                                                    |
| *A                                                                                         | 129786  | 09/18/03   | AJU             | Found typos in AC Electrical Characteristics table. Modified the following:<br>t <sub>SCE</sub> from 10, 12 and 20 to 9, 10 and 18;<br>t <sub>AW</sub> from 10, 12 and 20 to 9, 10 and 20;<br>t <sub>PWE</sub> from 10, 12 and 20 to 8, 9 and 18. |