

4-BIT BINARY RIPPLE COUNTER

FEATURES

- Various counting modes
- Asynchronous master reset
- Output capability: standard
- ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT93 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT93 are 4-bit binary ripple counters. The devices consist of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has a separate clock input ($\overline{CP}_0$ and $\overline{CP}_1$) to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q_n outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous master reset (MR_1 and MR_2) is provided which overrides both clocks and resets (clears) all flip-flops.

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a 4-bit ripple counter the output Q_0 must be connected externally to input $\overline{CP}_1$. The input count pulses are applied to clock input $\overline{CP}_0$. Simultaneous frequency divisions of 2, 4, 8 and 16 are performed at the Q_0 , Q_1 , Q_2 and Q_3 outputs as shown in the function table. As a 3-bit ripple counter the input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions of 2, 4 and 8 are available at the Q_1 , Q_2 and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

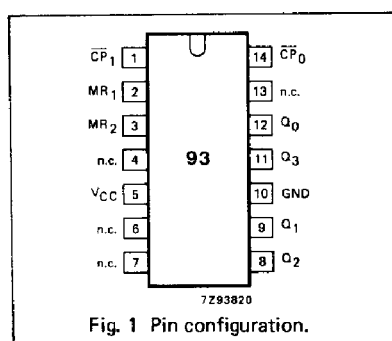


Fig. 1 Pin configuration.

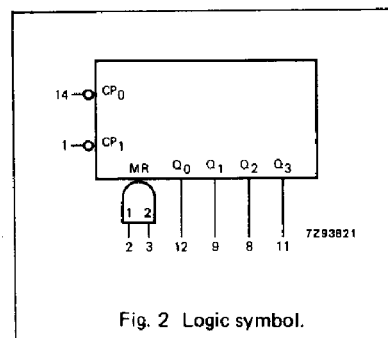


Fig. 2 Logic symbol.

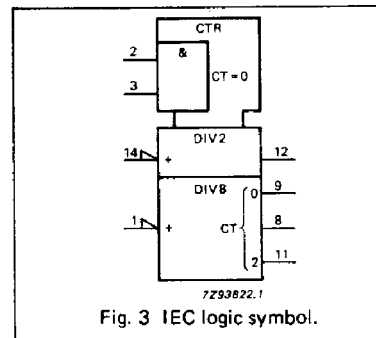


Fig. 3 IEC logic symbol.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}_0$ to Q_0	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	12	15	ns
f_{max}	maximum clock frequency		100	77	MHz
C_i	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	22	22	pF

$GND = 0 \text{ V}$; $T_{amb} = 25^\circ \text{C}$; $t_r = t_f = 6 \text{ ns}$

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

C_L = output load capacitance in pF

f_o = output frequency in MHz

V_{CC} = supply voltage in V

$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

2. For HC the condition is $V_i = GND$ to V_{CC}

For HCT the condition is $V_i = GND$ to $V_{CC} - 1.5 \text{ V}$

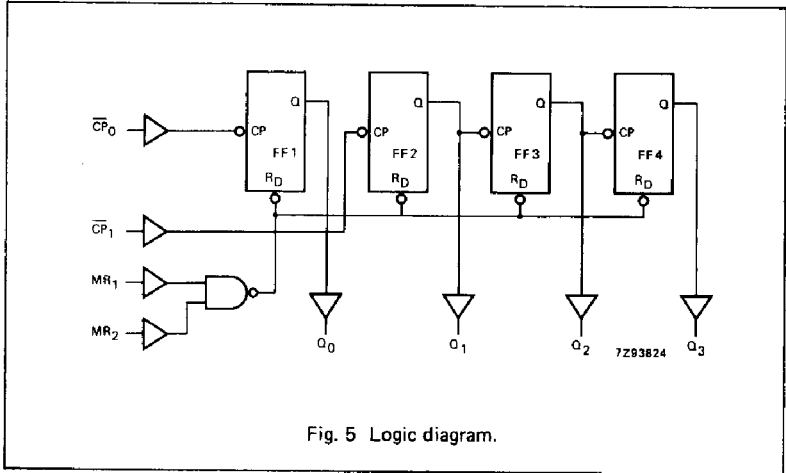
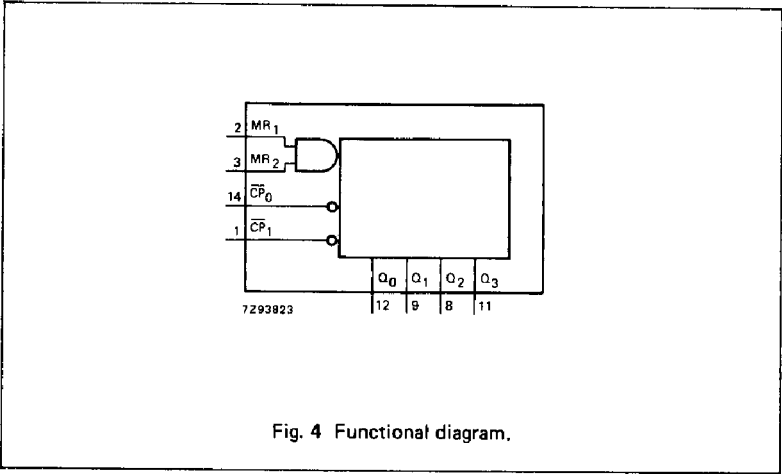
PACKAGE OUTLINES

14-lead DIL; plastic (SOT27)

14-lead mini pack; plastic (SO14; SOT108A)

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{CP}_1$	clock input 2nd, 3rd and 4th section (HIGH-to-LOW, edge-triggered)
2, 3	MR_1, MR_2	asynchronous master reset (active HIGH)
4, 6, 7, 13	n.c.	not connected
5	V_{CC}	positive supply voltage
10	GND	ground (0 V)
12, 9, 8, 11	Q_0 to Q_3	flip-flop outputs
14	$\overline{CP}_0$	clock input 1st section (HIGH-to-LOW, edge-triggered)



FUNCTION TABLE

COUNT	OUTPUTS			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

MODE SELECTION

RESET INPUTS		OUTPUTS			
MR ₁	MR ₂	Q ₀	Q ₁	Q ₂	Q ₃
H	H	L	L	L	L
L	H	count			
H	L				
L	L				

Note to function table
Output Q₀ connected to CP₁.
H = HIGH voltage level
L = LOW voltage level

DC CHARACTERISTICS FOR 74 HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

 I_{CC} category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS	
		74HC									V _{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} / t _{PLH}	propagation delay CP ₀ to Q ₀		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 6	
t _{PHL} / t _{PLH}	propagation delay CP ₁ to Q ₁		49 16 13	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig. 6	
t _{PHL} / t _{PLH}	propagation delay CP ₁ to Q ₂		61 22 18	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig. 6	
t _{PHL} / t _{PLH}	propagation delay CP ₁ to Q ₃		80 29 23	245 49 42		305 61 52		370 71 63	ns	2.0 4.5 6.0	Fig. 6	
t _{PHL}	propagation delay MR _n to Q _n		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 7	
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6	
t _{rem}	removal time MR _n to CP ₀ , CP ₁	50 10 9	8 3 2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 7	
t _W	pulse width CP ₀ , CP ₁	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6	
t _W	master reset pulse width MR _n	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7	
f _{max}	maximum clock pulse frequency CP ₀ , CP ₁	6.0 30 35	30 91 108		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{CP}_0, \overline{CP}_1$	0.60
MR_n	0.40

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V _{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay CP ₀ to Q ₀		18	34		43		51	ns	4.5	Fig. 6
t _{PHL} / t _{PLH}	propagation delay CP ₁ to Q ₁		18	34		43		51	ns	4.5	Fig. 6
t _{PHL} / t _{PLH}	propagation delay CP ₁ to Q ₂		24	46		58		69	ns	4.5	Fig. 6
t _{PHL} / t _{PLH}	propagation delay CP ₁ to Q ₃		30	58		73		87	ns	4.5	Fig. 6
t _{PHL}	propagation delay MR _n to Q _n		17	33		41		50	ns	4.5	Fig. 7
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6
t _{rem}	removal time MR _n to CP ₀ , CP ₁	10	3		13		15		ns	4.5	Fig. 7
t _W	pulse width CP ₀ , CP ₁	16	7		20		24		ns	4.5	Fig. 6
t _W	master reset pulse width MR _n	16	5		20		24		ns	4.5	Fig. 7
f _{max}	maximum clock pulse frequency CP ₀ , CP ₁	30	70		24		20		MHz	4.5	Fig. 6

AC WAVEFORMS

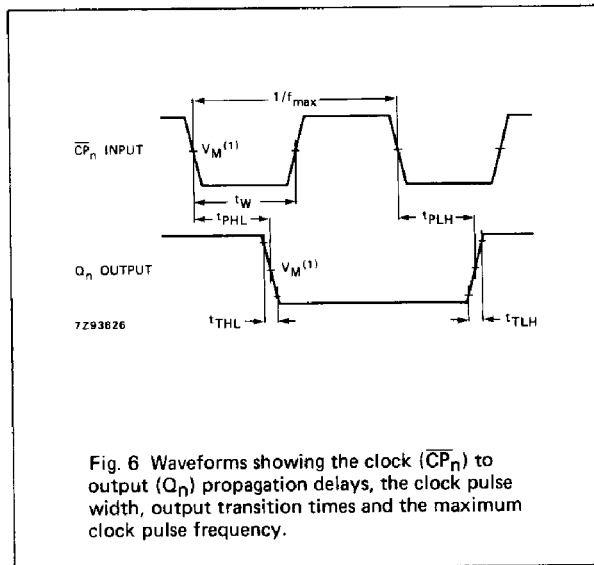


Fig. 6 Waveforms showing the clock ($\overline{CP}_n$) to output (Q_n) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.

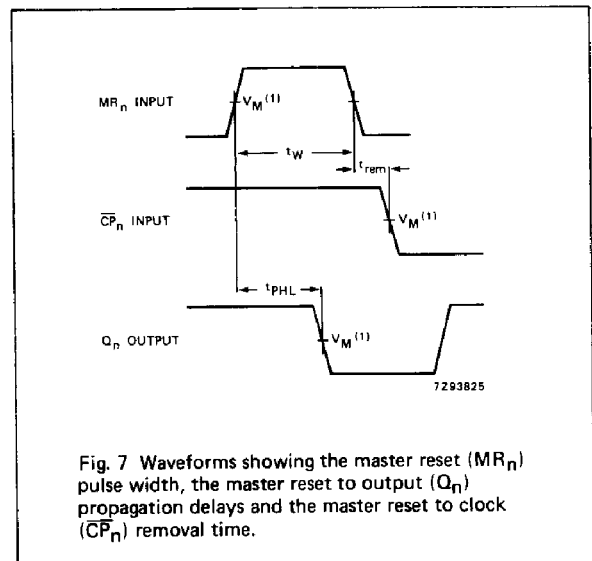


Fig. 7 Waveforms showing the master reset (MR_n) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock ($\overline{CP}_n$) removal time.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_L = \text{GND to } V_{CC}$.
HCT: $V_M = 1.3 \text{ V}$; $V_L = \text{GND to } 3 \text{ V}$.