



MC5494 • MC7494 MC9394 • MC8394

Add Suffix L for 16-pin ceramic dual in-line package (Case 620).

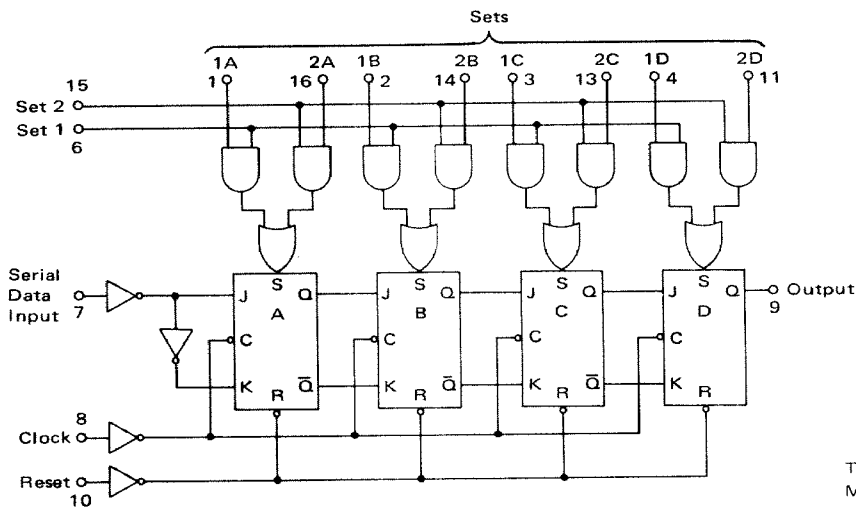
Suffix P for 16-pin plastic dual in-line package (Case 648) MC7494/MC8394 only.

This 4-bit register is designed for serial-out operation. Information can be accepted either serially or in parallel and then transferred to the slave-flip-flop on the positive edge of the clock.

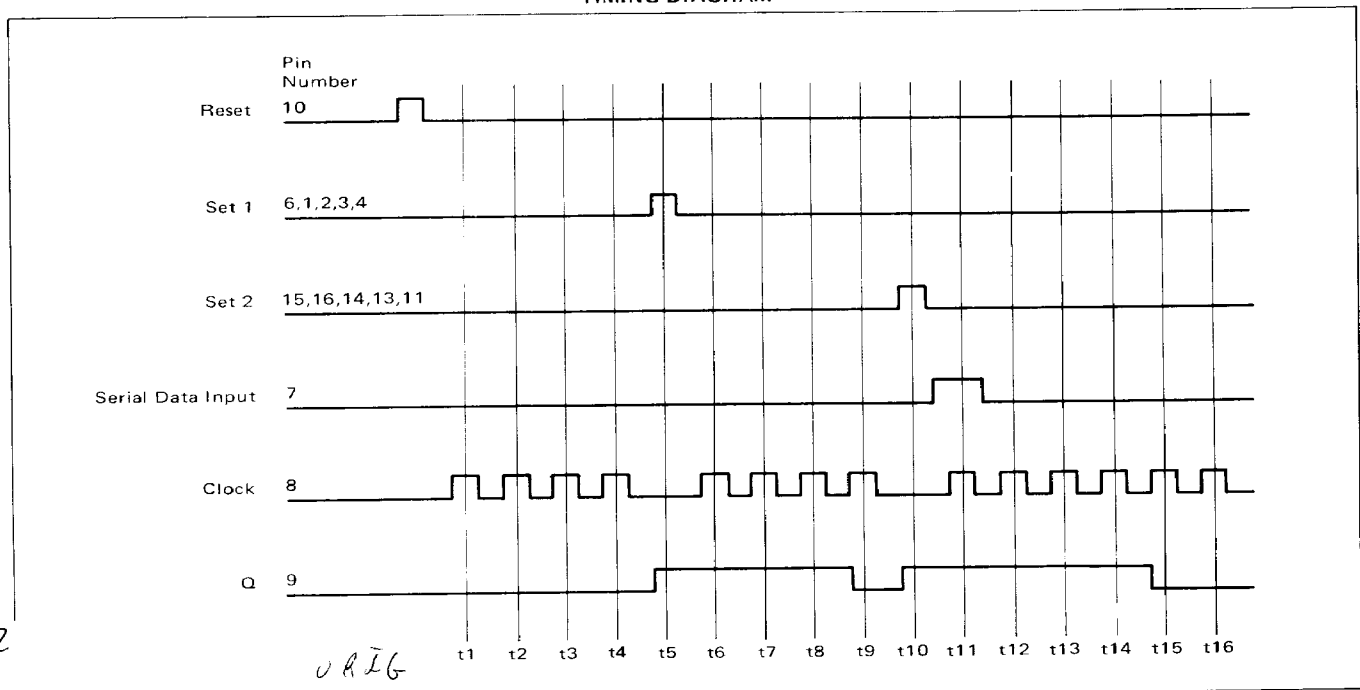
A "1" level on the reset line forces all flip-flops to the "0" state resetting the register and inhibiting operation. The flip-flop can also be forced to the "1" level by placing

the "1" levels on the necessary set inputs.

For serial-in operation, the information is entered through the serial-input and for parallel-in operation the flip-flops are set to the desired state by the proper use of the set and reset inputs. The reset input is independent of the clock, and the set inputs are independent of the clock and reset inputs.



TIMING DIAGRAM



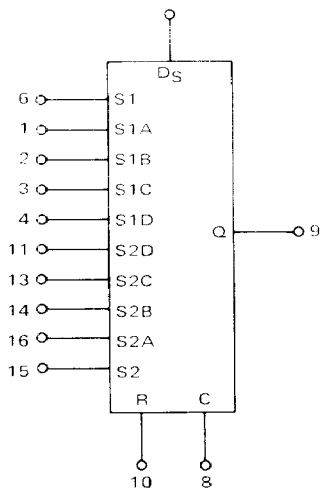
004480

4480

NOT

ELECTRICAL CHARACTERISTICS

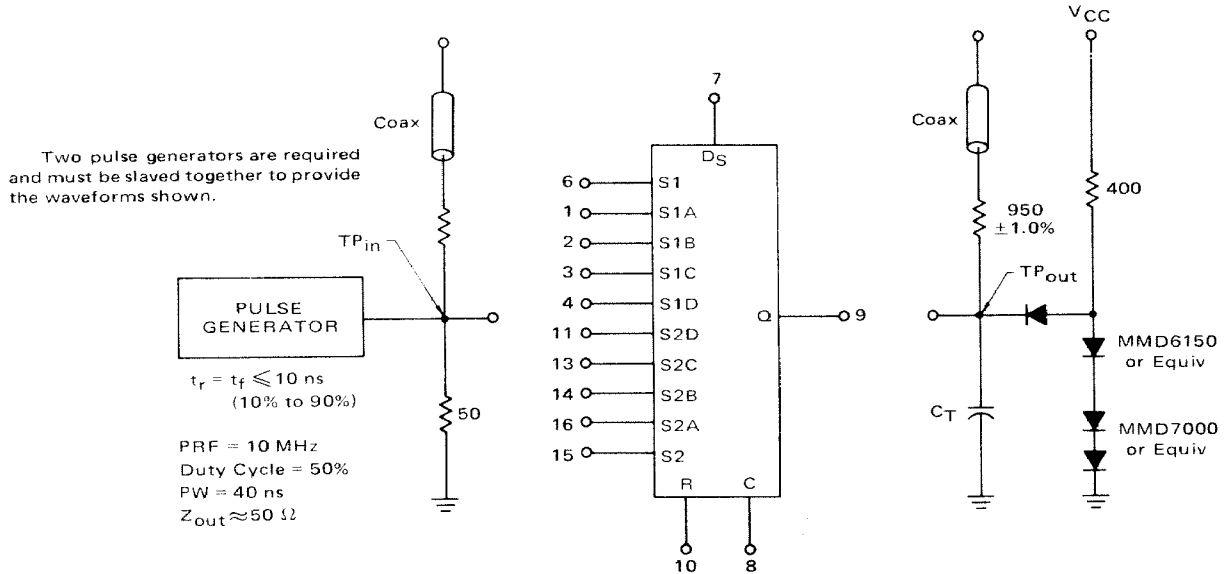
Test procedures are shown for only Set 1 and 1A inputs. The other inputs are tested in the same manner.



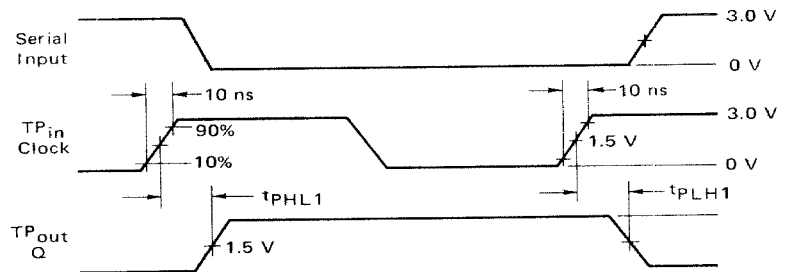
									TEST CURRENT/VOLTAGE (All Temperatures)										
									mA		Volts								
											I _{OL}	I _{OH}	V _{IL}	V _{IH}	V _{IHH}	V _{ILT}			V _{IHT}
									16	-0.4	0.4	2.4	5.5	0.8	2.0	4.5			5.5
									16	-0.4	0.4	2.4	5.5	0.8	2.0	4.75	5.25		
Characteristic	Symbol	Pin Under Test	MC5494/MC8394 Test Limits -55 to +125°C			MC7494/MC8394 Test Limits 0 to +75°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:								Gnd		
			Min	Max	Unit	Min	Max	Unit	I _{OL}	I _{OH}	V _{IL}	V _{IH}	V _{IHH}	V _{ILT}	V _{IHT}	V _{CCL}		V _{CCH}	
Input	Forward Current	1 6			mAdc mAdc		-1.6 -6.4	mAdc mAdc	-	-	1 6			-	-	6 1,2,3,4	5 5	12 12	
Leakage Current	I _{IH}	1 6	-	40 160	μAdc μAdc		40 160	μAdc μAdc			1 6		-	-	-	-	5 5	6,12 1,2,3,4,12	
	I _{IHH}	1 6	-	1.0 1.0	mAdc mAdc	-	1.0 1.0	mAdc mAdc	-	-	-	1 6	-	-	-	-	5 5	6,12 1,2,3,4,12	
Output	Output Voltage	V _{OL}	9	-	0.4	Vdc	-	0.4	Vdc	9	-	-	-	6,15	10	5	-	12	
		V _{OH}	9	2.4	-	Vdc	2.4	-	Vdc		9	-	-	-	4,6,11,15	5	-	12	
Short Circuit Current		I _{OS}	9	-20	-57	mAdc	-18	-57	mAdc			-	-	-	-	4,6,11,15	5	9,12	
Power Requirements (Total Device) Power Supply Drain		I _{CC} *	5	-	50	mAdc		58	mAdc							1,2,3, 7,8,11, 13,14,16	5	12	
Switching Parameters Clock to Q		f _{max}	8,9	10	-	MHz	10	-	MHz	Pulse In 7,8		Pulse Out 9		-	-	-	5	6,10*,12,15	
Propagation Delay Time Clock to Q		t _{PLH} ,t _{PHL}	9	-	40	ns	-	40	ns	7,8	9	-	-	-	-	-	5	6,12,10,15	
Set to Q		t _{PLH2}	9	-	35	ns	-	35	ns	6,10	9	-	-	-	-	1,2,3,4	5	12,15	
Reset to Q		t _{PHL2}	9	-	40	ns	-	40	ns	6,10	9	-	-	-	-	1,2,3,4	5	12,15	

* Momentarily hold Reset at 4.5 V, then ground and test.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



PROPAGATION DELAY – CLOCK TO OUTPUT



PROPAGATION DELAY – SET TO OUTPUT

