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Renesas Technology Corp. Customer Support Dept. April 1, 2003



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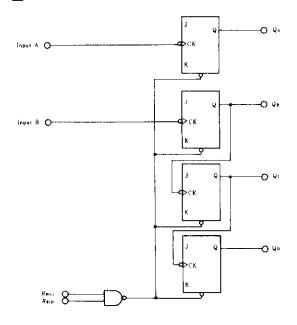
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The HD74LS93 contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and three-state binary counter for divide-by-eight. To use this maximum count length of this counter, the B input is connected to the  $\mathbf{Q}_{\mathbf{A}}$  output. The input count pulses are applied to input A and the outputs are described in the appropriate function table.

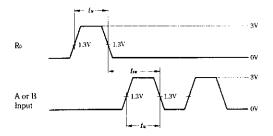
## **■BLOCK DIAGRAM**



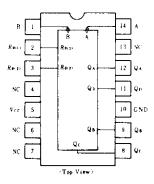
### **MRECOMMENDED OPERATING CONDITIONS**

Ite	n	Symbol	min	typ	max	Unit
Count	A input	,	0		32	2411
frequency	B input	frount	0	_	16	MHz
Pulse width	A input	tw	15			
	B input		30	-		l ns
	Reset inputs		15			
Setup time		ts u	25			ns

## **TIMING DEFINITION**



## **■PIN ARRANGEMENT**



## **MADSOLUTE MAXIMUM RATINGS**

Item Supply voltage		Symbol	Ratings	Unit V	
		Vec	7.0		
Input	R Inputs	17	7.0	V	
voltage	A, B Inputs	Vin	5.5	v	
Operating temperature range		Topt	-20~ +75		
Storage tem	perature range	Terk	65 + 150	°C	

## **TEUNCTION TABLE**

## ■ Reset/Count Function Table

Reset	Inputs		Out	puts	
R0m	R0(2)	Qυ	Qc	Qв	QA
Н	н	Ĺ	L	L	L
L	×		Со	unt	
×	I.		Со	unt	

### ●BCD Count Sequence (Notes 1)

		Out	puts	
Count.	Qυ	Qc	Qв	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	Н
2	L	L	н	I.
3	L	L	н	Н
4	L	Н	L	L
5	L	Н	L	Н
6	L	Н	Н	L
7	L	Н	Н	Н
8	Н	L	L	L
9	Н	L	L	Н
10	H	L	н	L
11	Н	L	Н	Н
12	Н	Н —	L	L
13	Н	Н	L	Н
14	Н	Н	Н	L
15	Н	Н	Н	н

Notes) 1. Output QA is connected to input B for BCD count.

2. H; high level, L; low level, X; irrelevant

## **ELECTRICAL CHARACTERISTICS** ( $Ta = -20 \sim +75$ °C)

Ite	m	Symbol	Symbol Test Conditions		min	typ*	max	Unit
		Vih			2.0			v
Input voltage		VIL			_		0.8	v
		Voн	$V_{CC} = 4.75V$ , $V_{IH} = 2V$ , $V_{IL} = 0.8$	/, I <sub>OH</sub> = −400µA	2.7	_		v
Output voltage			$V_{CC} = 4.75 \text{V},  V_{IH} = 2 \text{V},$	IoL = 4mA**		_	0.4	v
		Vol	$V_{IL}=0.8V$	10L=8mA** -			0.5	V
Any Reset					_	-	-0.4	
	A input	Iιι	$V_{CC} = 5.25 \text{V},  V_I = 0.4 \text{V}$			_	-2.4	mA
	B input					_	-1.6	
	Any Reset				-		20	
Input current	A input	Ĭıн	$V_{CC} = 5.25 \text{V},  V_i = 2.7 \text{V}$		-	<del>-</del>	40	μA
	B input				_	-	40	
	Any Reset		$V_{l} = 7 \text{ V}$		_	-	0.1	
	A input	Ī:	$V_{CC}=5.25V$	$V_l = 5.5 \text{V}$		_	0.2	mA
	B input			$V_I = 5.5 \text{V}$	-	_	0.2	
Short-circuit output current		los	Vcc=5.25V		- 20		-100	mA
Supply current	Supply current Icc*** Vcc=5.25V				9	15	mА	
Input clamp volts	ige	Vik	$V_{CC} = 4.75 \text{V}, I_{LN} = -18 \text{m}.$	4	-	_	-1.5	v

## **E**SWITCHING CHARACTERISTICS ( $V_{CC} = 5V$ , $T_a = 25^{\circ}C$ )

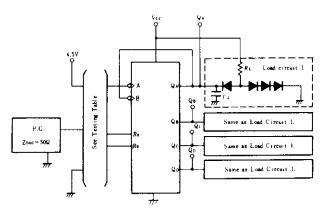
Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
		A	QA		32	42	_	MHz
Maximum count frequency	fmax	В	Qв		16		-	MITIZ
	tpl.H				_	10	16	ns
	tphl.	A	Q <sub>A</sub>	$C_L = 15 \mathrm{pF},  R_L = 2 \mathrm{k}\Omega$		12	18	
	tPLH	- A	Qυ		-	46	70	ns
	tphl				_	46	70	
	tPLH	В	Qв			10	16	ns
Propagation delay time	tphi.				_	14	21	
	tplH				_	21	32	
	tриL	В	<b>Q</b> c		- [	23	35	
	tplh				-	34	51	
	tphl	В	Q□		_	34	51	ns
	tphl .	Set-to-0	QA~QD		_	26	40	ns

 <sup>\*</sup> V<sub>CC</sub>=5V, Ta=25°C
 \*\* Q<sub>A</sub> output is tested at specified I<sub>OL</sub> plus the limit value of I<sub>IL</sub> for the B input. This permits driving the B input while maintaining full fan-out capability.

<sup>\*\*\*</sup>  $I_{CC}$  is measured with all outputs open, both R<sub>0</sub> inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

## **TESTING METHOD**

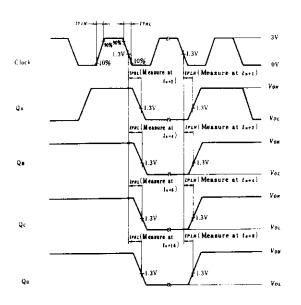
## 1) Test Circuit



Notes) 1.  $C_L$  includes probe and jig capacitance.

2. All diodes are 1S2074 (f).

## Waveform-1 fmax. tPLH, tPHL, (Clock→Q)



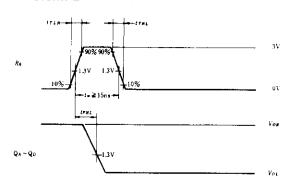
Notes) 1. Input pulse;  $t_{TLH} \le 15 \text{ ns}$ ,  $t_{THL} \le 5 \text{ ns}$ , PRR = 1 MHz, duty cycle=50% and: for  $f_{max}$ ,  $t_{TLH} = t_{THL} \le 2.5$  ns. 2.  $t_n$  is reference bit time when all outputs are low.

## 2) Testing Table

¥.	From input		Inputs			Outputs			
ltem	to output	Α	В	R₀	QA	Qв	Qc	Qυ	
	A →Q	IN	to QA	GND	Out	Out	Out	Out	
/mar	B →Q	4.5V	IN	GND		Out	Out	Out	
	A →Q <sub>A</sub>	IN	to Qa	GND	Out	_	_	_	
	A →Q <sub>D</sub>	IN	to QA	GND	_	-		Out	
PLH	B →Q <sub>B</sub>	4.5V	IN	GND		Out			
1PHL	B →Qc	4.5V	IN	GND	-		Out		
	$B \rightarrow Q_D$	4.5V	IN	GND	_	_	_	Out	
	R8→Q	IN*	to QA	IN	Out	Out	Out	Out	

<sup>\*</sup> For initialized.

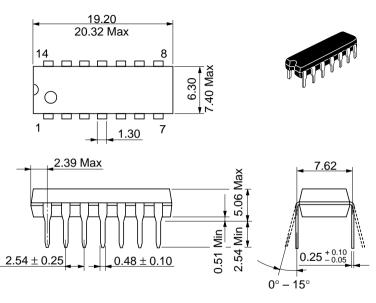
### Waveform-2 tPHL(Ro→Q)



Notes) 1.  $t_{TLH} \le 15$ ns,  $t_{THL} \le 5$ ns.

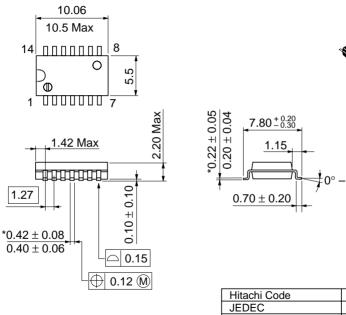
<sup>\*\*</sup> Measured with each input and unused inputs at 4.5V.

Unit: mm



Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g

Unit: mm



\*Dimension including the plating thickness
Base material dimension

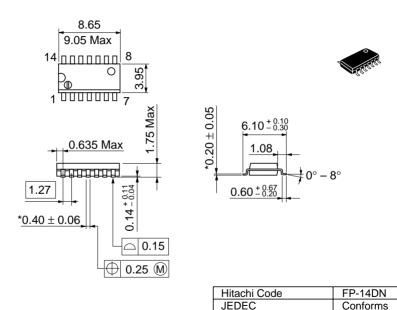
Hitachi Code FP-14DA

JEDEC —

EIAJ Conforms

Weight (reference value) 0.23 g

Unit: mm



EIAJ

Weight (reference value)

Conforms

0.13 g

\*Pd plating

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