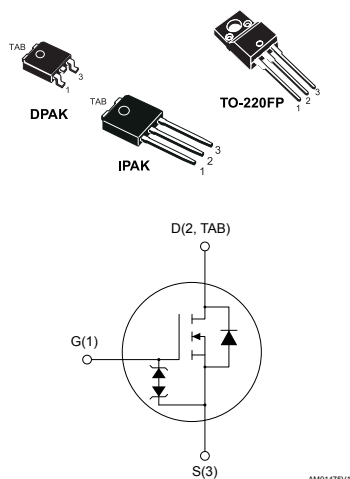


N-channel 620 V, 2.9 Ω typ., 2.2 A MDmesh™ K3 Power MOSFETs in DPAK, TO-220FP and IPAK packages



Features

Order code	V_{DS}	$R_{DS(on)max.}$	I_D	Package
STD2N62K3	620 V	3.6 Ω	2.2 A	DPAK
STF2N62K3				TO-220FP
STU2N62K3				IPAK

- 100% avalanche tested
- Extremely high dv/dt capability
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Applications

- Switching applications

Description

These MDmesh™ K3 Power MOSFETs are the result of improvements applied to STMicroelectronics' MDmesh™ technology, combined with a new optimized vertical structure. These devices boast an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering them suitable for the most demanding applications.

Product status link

[STD2N62K3](#)
[STF2N62K3](#)
[STU2N62K3](#)

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		DPAK	TO-220FP	IPAK	
V_{DS}	Drain-source voltage	620			V
V_{GS}	Gate-source voltage	± 30			V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	2.2	2.2 ⁽¹⁾	2.2	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	1	1 ⁽¹⁾	1	A
I_{DM} ⁽²⁾	Drain current (pulsed)	8.8			A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	45	20	45	W
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat-sink ($t = 1\text{ s}$, $T_C = 25\text{ }^{\circ}\text{C}$)	-	2500	-	V
dv/dt ⁽³⁾	Peak diode recovery voltage slope	12			V/ns
T_J	Operating junction temperature range	-55 to 150			$^{\circ}\text{C}$
T_{stg}	Storage temperature range				

1. Limited by maximum junction temperature.

2. Pulse width limited by safe operating area.

3. $I_{SD} \leq 2.2\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DSpeak} \leq V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value			Unit
		DPAK	TO-220FP	IPAK	
$R_{thj-case}$	Thermal resistance junction-case	2.78	6.25	2.78	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient		62.5	100	$^{\circ}\text{C}/\text{W}$
$R_{thj-pcb}$ ⁽¹⁾	Thermal resistance junction-pcb	50			$^{\circ}\text{C}/\text{W}$

1. When mounted on 1inch² FR-4 board, 2 oz Cu.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR} ⁽¹⁾	Avalanche current, repetitive or not-repetitive	2.2	A
E_{AS} ⁽²⁾	Single pulse avalanche energy	85	mJ

1. Pulse width limited by T_J max.

2. Starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$.

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0 V	620			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 620 V			1	μA
		V _{GS} = 0 V, V _{DS} = 620 V, T _C = 125 °C ⁽¹⁾			50	μA
I _{GSS}	Gate body leakage current	V _{DS} = 0 V, V _{GS} = ±20 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 50 μA	3	3.75	4.5	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 1.1 A		2.9	3.6	Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 50 V, f = 1 MHz, V _{GS} = 0 V	-	340	-	pF
C _{oss}	Output capacitance			26		
C _{rss}	Reverse transfer capacitance			4		
C _{o(tr)} ⁽¹⁾	Equivalent capacitance time related	V _{DS} = 0 to 496 V, V _{GS} = 0 V	-	17	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz open drain	-	5	-	Ω
Q _g	Total gate charge	V _{DD} = 496 V, I _D = 2.2 A, V _{GS} = 0 to 10 V (see Figure 17. Test circuit for gate charge behavior)	-	15	-	nC
Q _{gs}	Gate-source charge			3		
Q _{gd}	Gate-drain charge			9		

1. C_{o(tr)} is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 310 V, I _D = 1.1 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 16. Test circuit for resistive load switching times and Figure 21. Switching time waveform)	-	8	-	ns
t _r	Rise time			4.4		
t _{d(off)}	Turn-off delay time			21		
t _f	Fall time			22		

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{SD}	Source-drain current		-		2.2	A
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)				8.8	
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 2.2 A, V _{GS} = 0 V	-		1.6	V
t _{rr}	Reverse recovery time	I _{SD} = 2.2 A, di/dt = 100 A/μs	-	200		ns
Q _{rr}	Reverse recovery charge	V _{DD} = 60 V (see Figure 18. Test circuit for inductive load switching and diode recovery times)		0.9		μC
I _{RRM}	Reverse recovery current			9		A
t _{rr}	Reverse recovery time	I _{SD} = 2.2 A, di/dt = 100 A/μs	-	240		ns
Q _{rr}	Reverse recovery charge	V _{DD} = 60 V, T _j = 150 °C(see Figure 18. Test circuit for inductive load switching and diode recovery times)		1.15		μC
I _{RRM}	Reverse recovery current			10		A

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}$, $I_D = 0 \text{ A}$	± 30			V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics curves

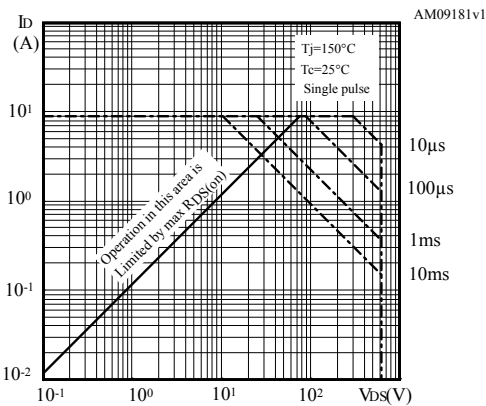
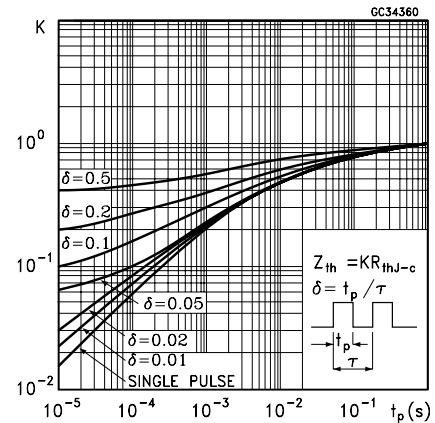
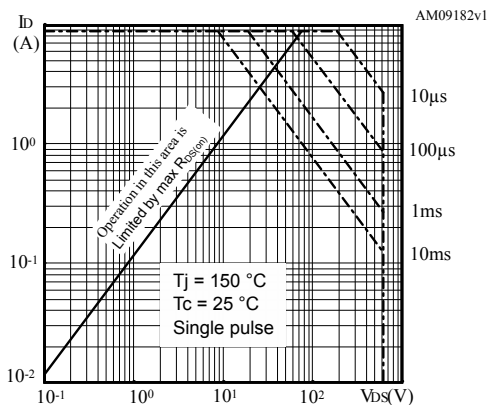
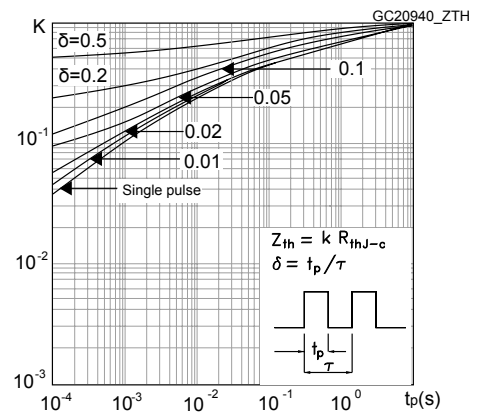
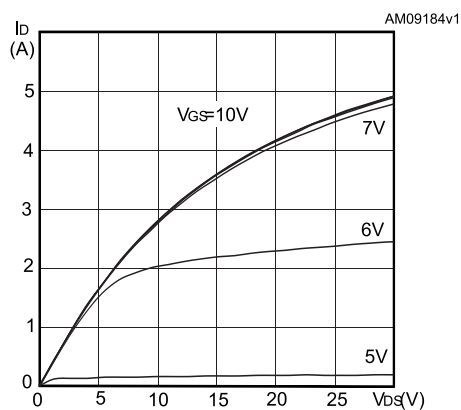
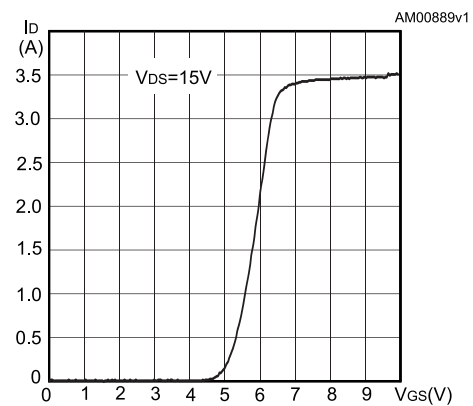
Figure 1. Safe operating area for DPAK and IPAK

Figure 2. Thermal impedance for DPAK and IPAK

Figure 3. Safe operating area for TO-220FP

Figure 4. Thermal impedance for TO-220FP

Figure 5. Output characteristics

Figure 6. Transfer characteristics


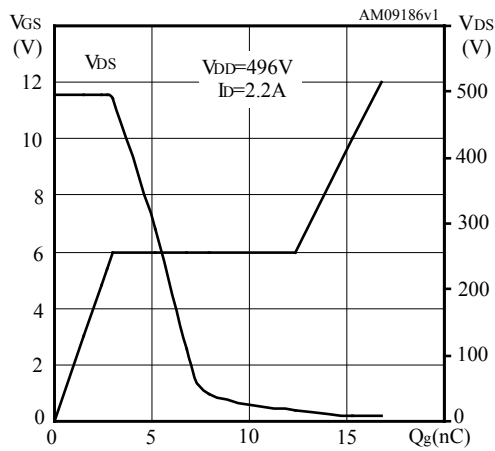
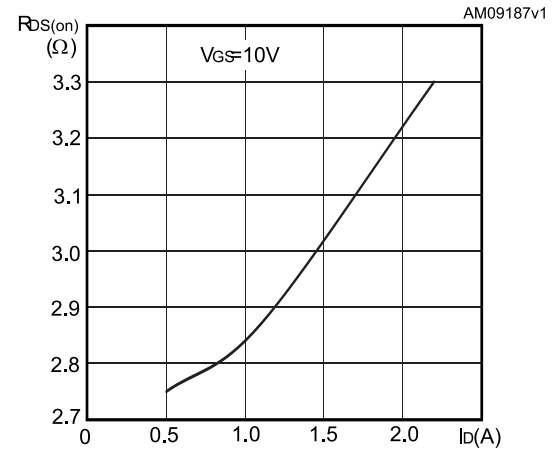
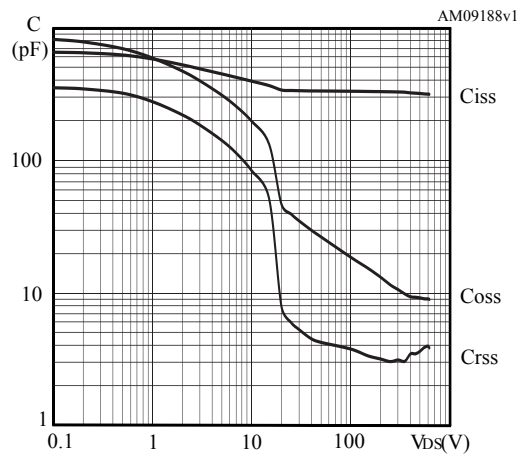
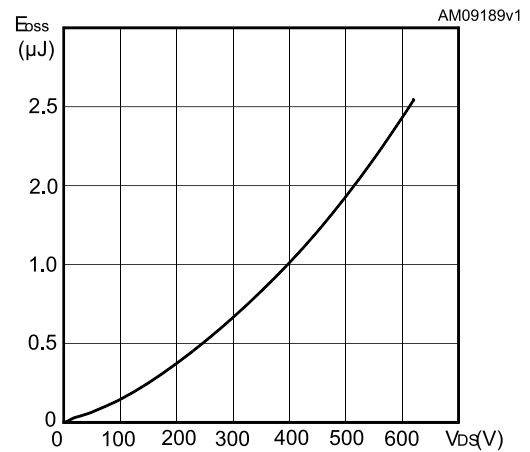
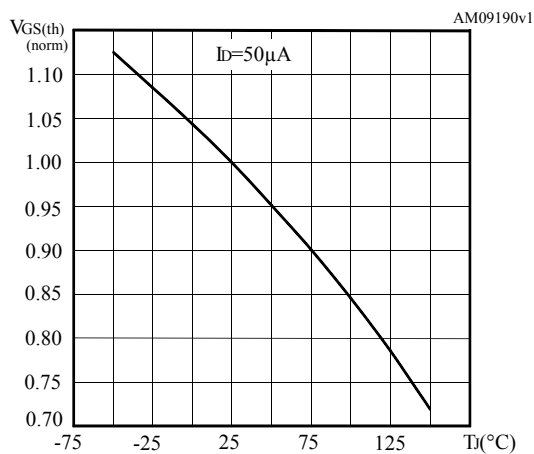
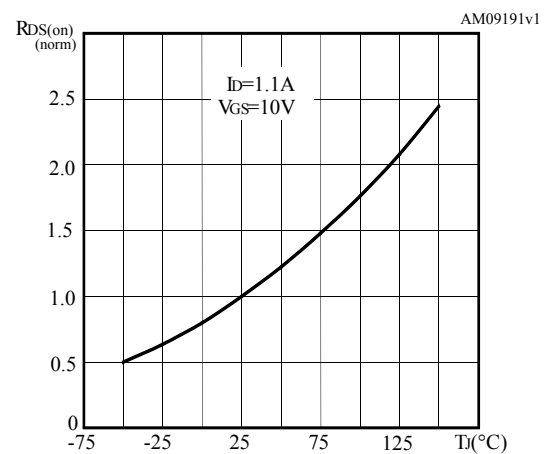
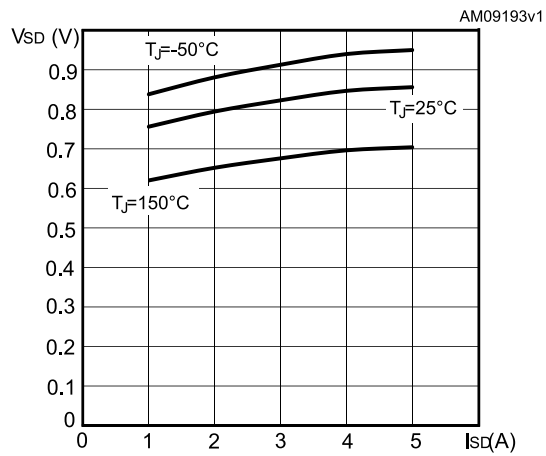
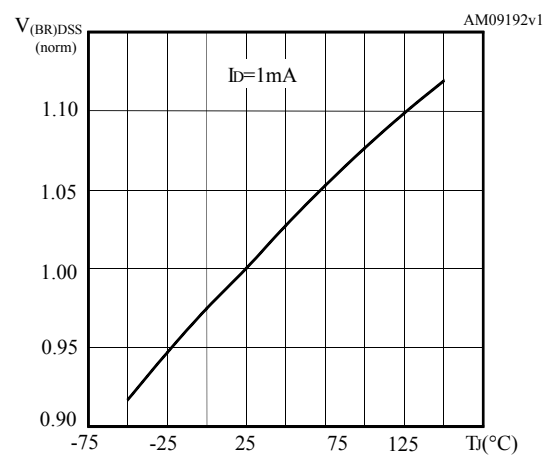
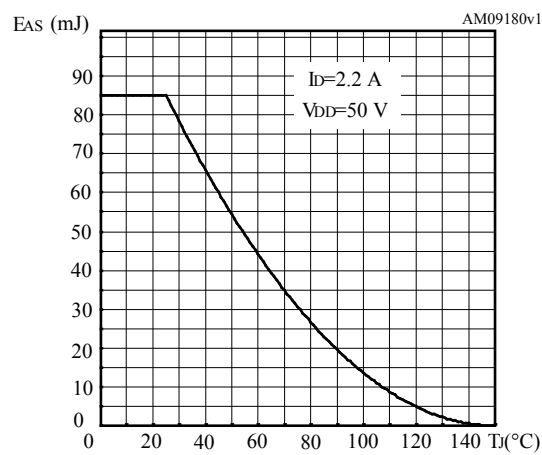
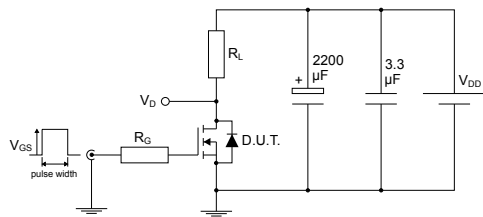
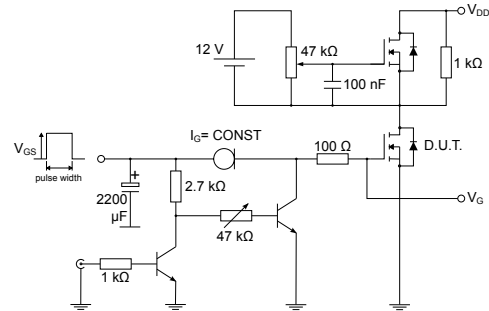
Figure 7. Gate charge vs gate-source voltage

Figure 8. Static drain-source on-resistance

Figure 9. Capacitance variations

Figure 10. Output capacitance stored energy

Figure 11. Normalized gate threshold voltage vs temperature

Figure 12. Normalized on-resistance vs temperature


Figure 13. Source-drain diode forward characteristics

Figure 14. Normalized $V_{(BR)DSS}$ vs temperature

Figure 15. Maximum avalanche energy vs starting T_J


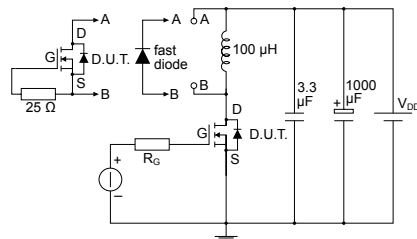
3 Test circuits

Figure 16. Test circuit for resistive load switching times


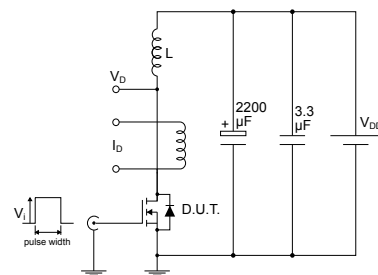
AM01468v1

Figure 17. Test circuit for gate charge behavior


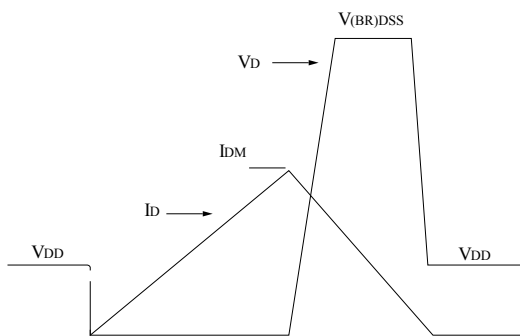
AM01469v1

Figure 18. Test circuit for inductive load switching and diode recovery times


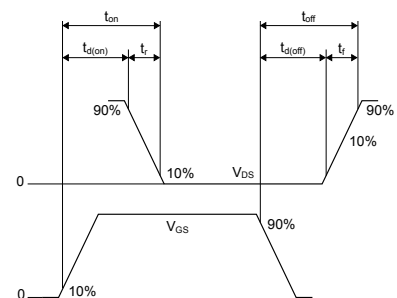
AM01470v1

Figure 19. Unclamped inductive load test circuit


AM01471v1

Figure 20. Unclamped inductive waveform


AM01472v1

Figure 21. Switching time waveform


AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A package information

Figure 22. DPAK (TO-252) type A package outline



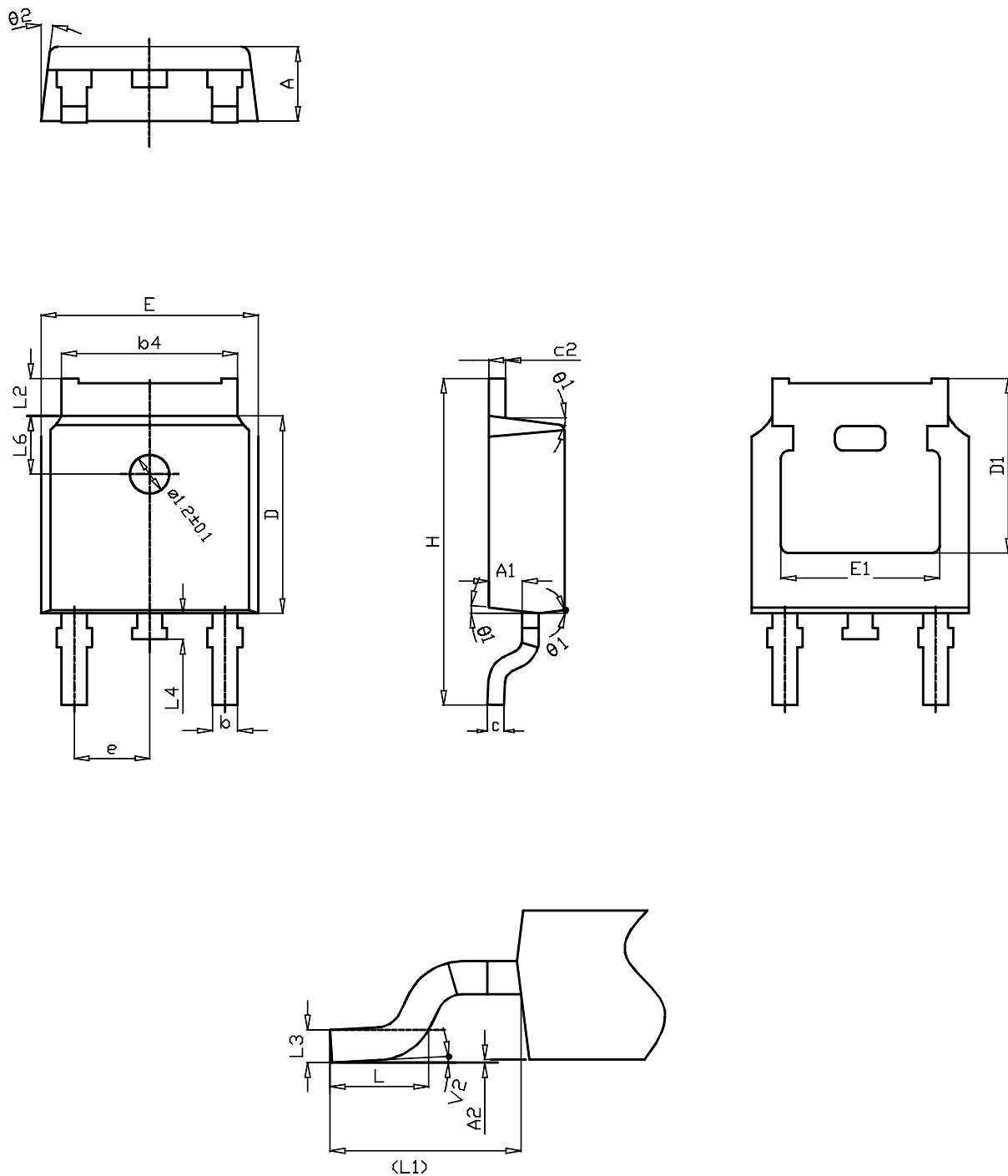
0068772_A_25

Table 9. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) type C package information

Figure 23. DPAK (TO-252) type C package outline



0068772_C_25

Table 10. DPAK (TO-252) type C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.25		
E	6.50	6.60	6.70
E1	4.70		
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.90		1.25
L3	0.51 BSC		
L4	0.60	0.80	1.00
L6	1.80 BSC		
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

4.3 DPAK (TO-252) type E package information

Figure 24. DPAK (TO-252) type E package outline

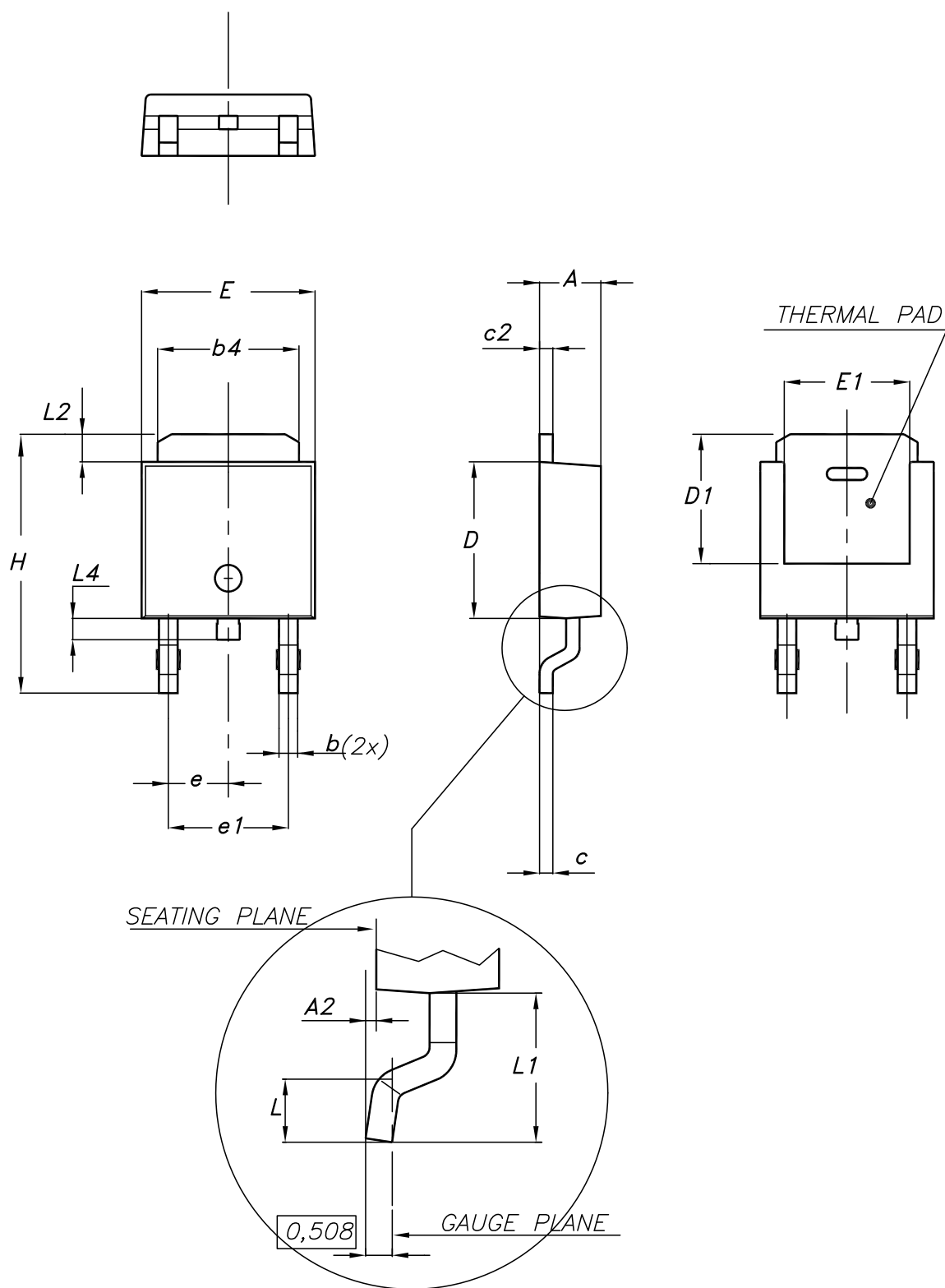


Table 11. DPAK (TO-252) type E mechanical data

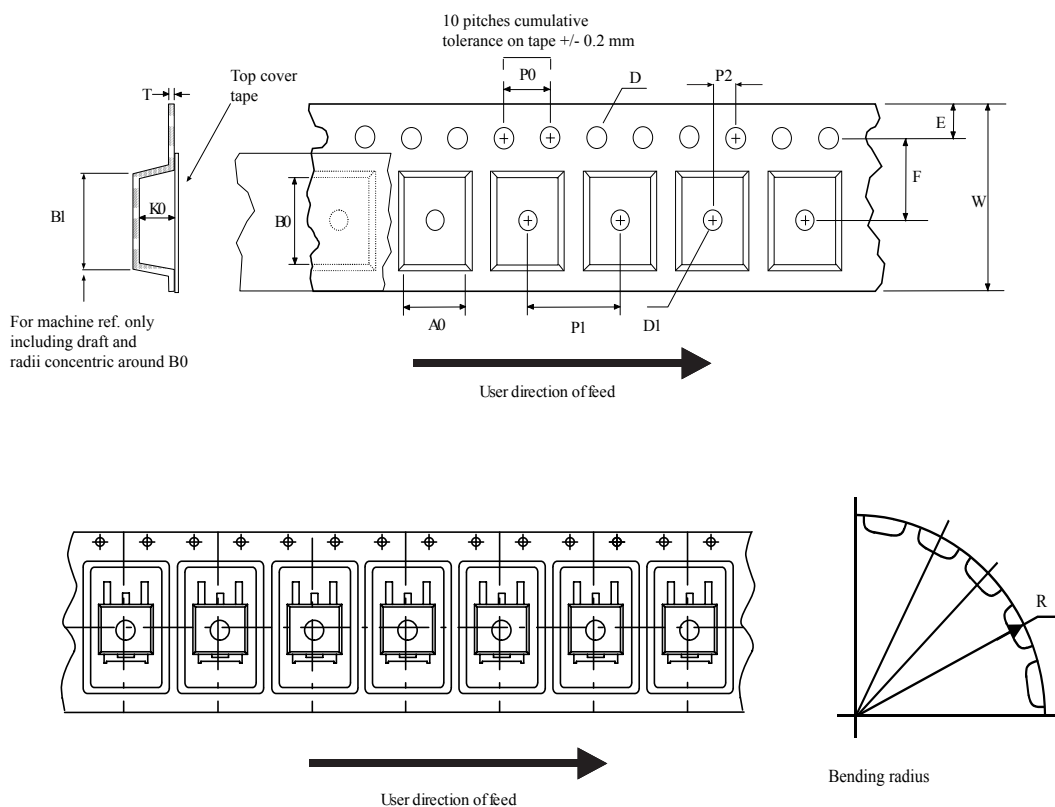
Dim.	mm		
	Min.	Typ.	Max.
A	2.18		2.39
A2			0.13
b	0.65		0.884
b4	4.95		5.46
c	0.46		0.61
c2	0.46		0.60
D	5.97		6.22
D1	5.21		
E	6.35		6.73
E1	4.32		
e		2.286	
e1		4.572	
H	9.94		10.34
L	1.50		1.78
L1		2.74	
L2	0.89		1.27
L4			1.02

Figure 25. DPAK (TO-252) recommended footprint (dimensions are in mm)


FP_0068772_25

4.4 DPAK (TO-252) packing information

Figure 26. DPAK (TO-252) tape outline



AM08852v1

Figure 27. DPAK (TO-252) reel outline

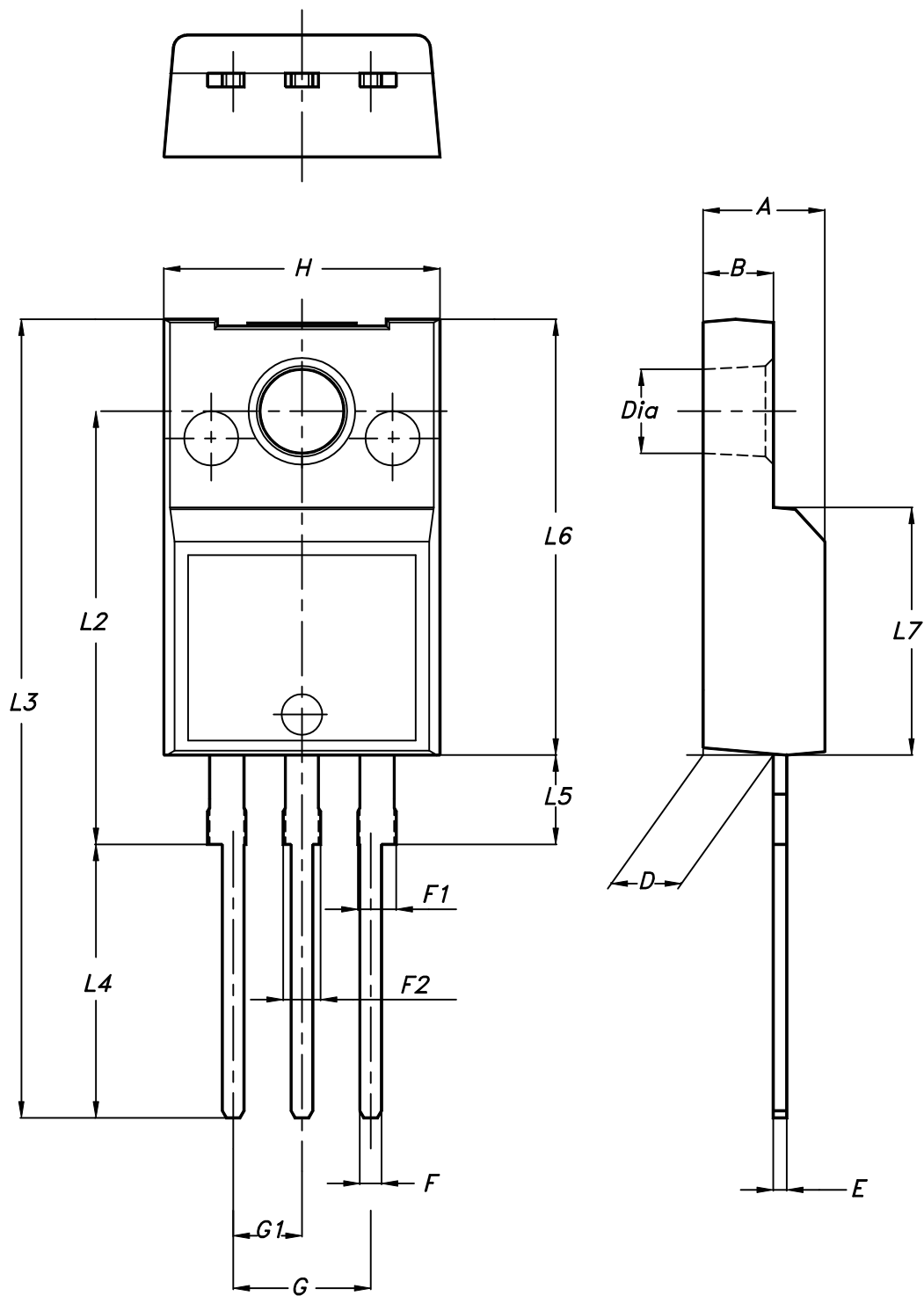

AM06038v1

Table 12. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

4.5 TO-220FP package information

Figure 28. TO-220FP package outline



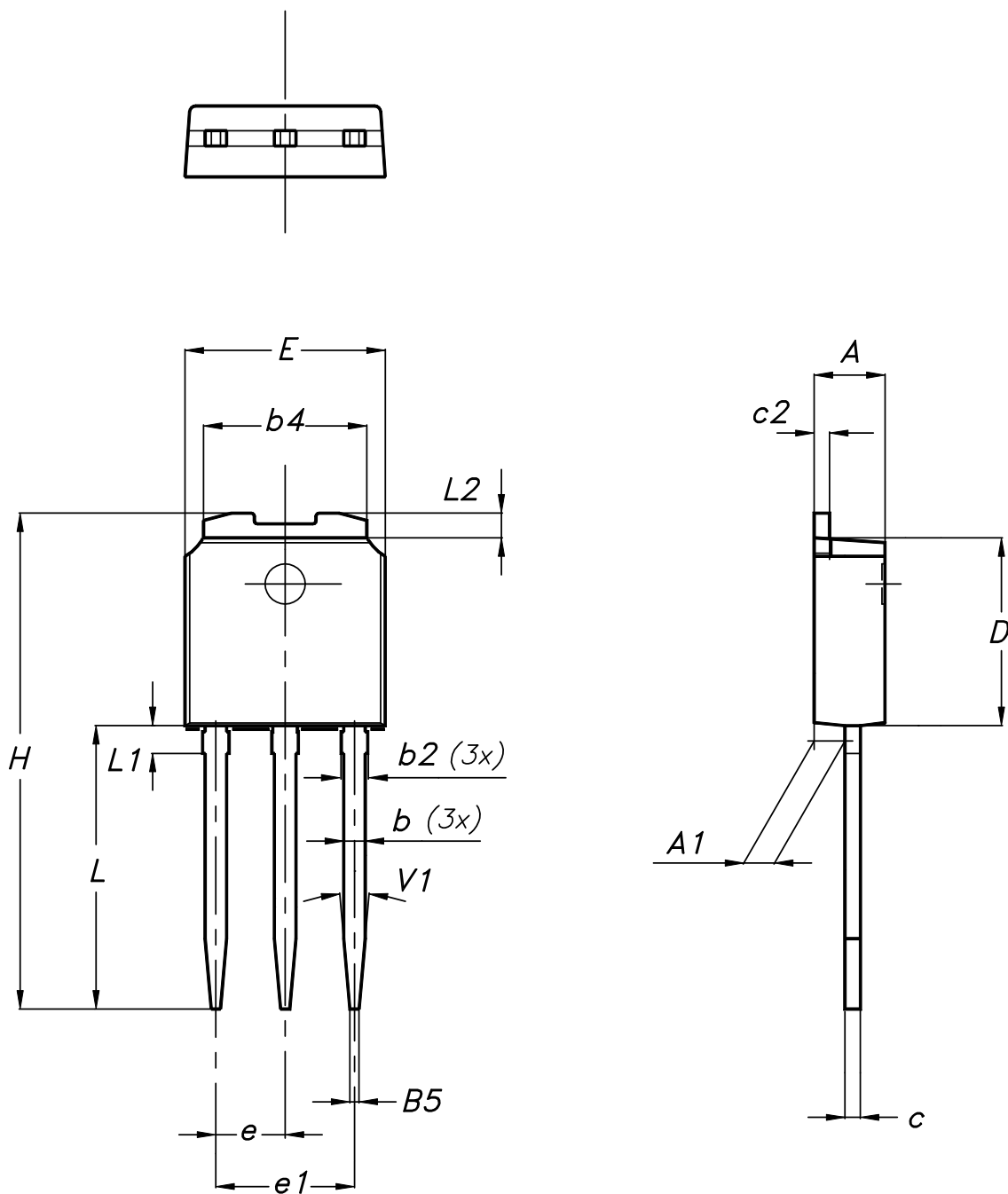
7012510_Rev_12_B

Table 13. TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

4.6 IPAK (TO-251) type A package information

Figure 29. IPAK (TO-251) type A package outline



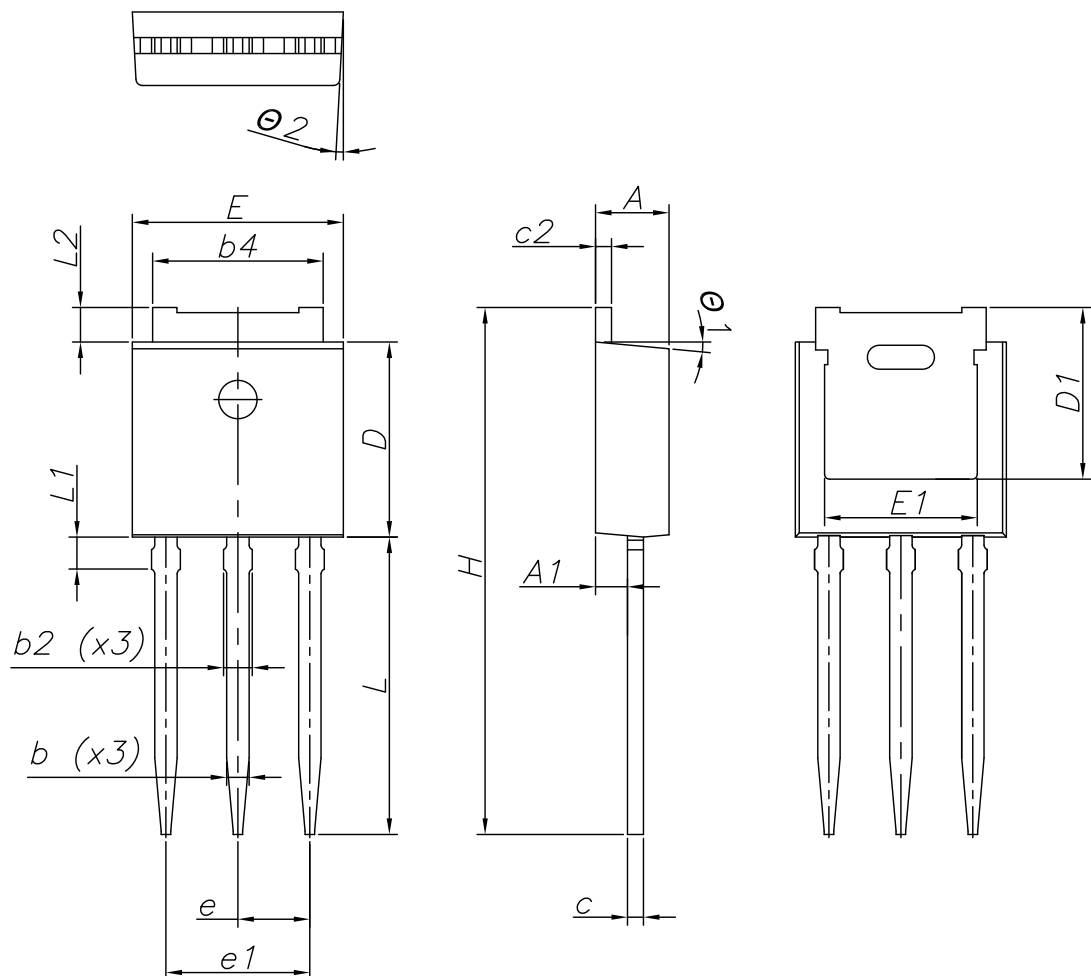
0068771_IK_typeA_rev14

Table 14. IPAK (TO-251) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

4.7 IPAK (TO-251) type C package information

Figure 30. IPAK (TO-251) type C package outline



0068771_IK_typeC_rev14

Table 15. IPAK (TO-251) type C package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.35
A1	0.90	1.00	1.10
b	0.66		0.79
b2			0.90
b4	5.23	5.33	5.43
c	0.46		0.59
c2	0.46		0.59
D	6.00	6.10	6.20
D1	5.20	5.37	5.55
E	6.50	6.60	6.70
E1	4.60	4.78	4.95
e	2.20	2.25	2.30
e1	4.40	4.50	4.60
H	16.18	16.48	16.78
L	9.00	9.30	9.60
L1	0.80	1.00	1.20
L2	0.90	1.08	1.25
θ1	3°	5°	7°
θ2	1°	3°	5°

5 Ordering information

Table 16. Order codes

Order code	Marking	Package	Packing
STD2N62K3	2N62K3	DPAK	Tape and reel
STF2N62K3		TO-220FP	Tube
STU2N62K3		IPAK	

Revision history

Table 17. Document revision history

Date	Version	Changes
31-May-2011	1	First release
20-Mar-2012	2	Added new package: D ² PAK – Table 1: Device summary, Section 4: Package mechanical data and Section 5: Packaging mechanical data have been modified. Minor text changes.
04-Jun-2018	3	The part numbers STB2N62K3 and STP2N62K3 have been moved to a separate datasheet. Removed maturity status indication from cover page. The document status is production data. Updated title and features in cover page. Updated Section 1 Electrical ratings , Section 2 Electrical characteristics , Section 2.1 Electrical characteristics curves and Section 4 Package information . Minor text changes.

Contents

1	Electrical ratings	2
2	Electrical characteristics.....	3
2.1	Electrical characteristics curves	5
3	Test circuits	8
4	Package information.....	9
4.1	DPAK (TO-252) type A package information	9
4.2	DPAK (TO-252) type C package information	11
4.3	DPAK (TO-252) type E package information	13
4.4	DPAK (TO-252) packing information.....	15
4.5	TO-220FP package information	17
4.6	IPAK (TO-251) type A package information	19
4.7	IPAK (TO-251) type C package information.....	21
5	Ordering information	24
	Revision history	25

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2018 STMicroelectronics – All rights reserved