



South Sea Semiconductor

SSD3030P

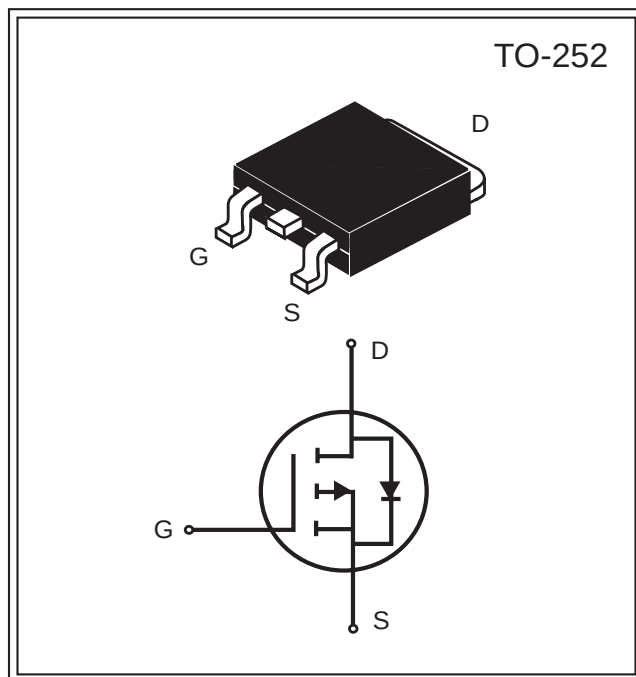
P-Channel Enhancement Mode MOSFET

Product Summary

V_{DS} (V)	I_D (A)	$R_{DS(ON)}$ (m Ω) Max
-30V	-30A	30 @ $V_{GS} = -10V$
		45 @ $V_{GS} = -4.5V$

FEATURES

- ◆ Super high dense cell design for low $R_{DS(ON)}$.
- ◆ Rugged and reliable.
- ◆ TO-252 package.



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous @ $T_J = 125^\circ\text{C}$	I_D	-30	A
-Pulsed ^b	I_{DM}	-60	A
Drain-Source Diode Forward Current ^a	I_S	-1.7	A
Maximum Power Dissipation ^a	P_D	50	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient ^a	$R_{\theta JA}$	50	

South Sea Semiconductor reserves the right to make changes to improve reliability or manufacturability without advance notice.

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**P-Channel Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ ^c	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V$, $I_D=-250\mu A$	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-24V$, $V_{GS}=0V$			-1	μA
Gate-Body Leakage	I_{GSS}	$V_{GS}=\pm 20V$, $V_{DS}=0V$			± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=-250\mu A$	-1	-1.5	-2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-10V$, $I_D=-20A$			30	m Ω
		$V_{GS}=-4.5V$, $I_D=-10A$			45	
On-State Drain Current	$I_{D(ON)}$	$V_{DS}=-5V$, $V_{GS}=-10V$	-40			A
Forward Transconductance	g_{FS}	$V_{DS}=-5V$, $I_D=-5.3A$	5			S
Input Capacitance	C_{ISS}	$V_{DS}=-15V$		800		pF
Output Capacitance	C_{OSS}	$V_{GS}=0V$		180		
Reverse Transfer Capacitance	C_{RSS}	$f=1.0MHz$		105		
Turn-On Delay Time	$t_{D(ON)}$	$V_{DD}=-15V$,		12.5		ns
Rise Time	t_r	$I_D=-1A$,		13.5		
Turn-Off Delay Time	$t_{D(OFF)}$	$V_{GEN}=-10V$,		84		
Fall Time	t_f	$R_{GEN}=6\Omega$,		39.5		
Total Gate Charge	Q_g	$V_{DS}=-15V$, $I_D=-5.3A$, $V_{GS}=-10V$		20		nC
		$V_{DS}=-15V$, $I_D=-5.3A$, $V_{GS}=-4.5V$		10.5		
Gate-Source Charge	Q_{gs}	$V_{DS}=-15V$, $I_D=-5.3A$,		2.4		
Gate-Drain Charge	Q_{gd}	$V_{GS}=-10V$		5		
Diode Forward Voltage	V_{SD}	$V_{GS}=0V$, $I_D=-1.7A$		-0.75	-1.2	V

Notes :

- Surface Mounted on FR4 Board, $t \leq 10$ sec.
- Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.