SA636

Low voltage high performance mixer FM IF system with high-speed RSSI

Rev. 6 — 5 December 2012 Product data sheet

1. General description

The SA636 is a low-voltage high performance monolithic FM IF system with high-speed RSSI incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic Received Signal Strength Indicator (RSSI), voltage regulator, wideband data output and fast RSSI op amps. The SA636 is available in 20-lead SSOP (Shrink Small Outline Package) and HVQFN20 (quad flat package).

The SA636 was designed for high bandwidth portable communication applications and will function down to 2.7 V. The RF section is similar to the famous SA605. The data output has a minimum bandwidth of 600 kHz. This is designed to demodulate wideband data. The RSSI output is amplified. The RSSI output has access to the feedback pin. This enables the designer to adjust the level of the outputs or add filtering.

SA636 incorporates a power-down mode which powers down the device when POWER_DOWN_CTRL pin is LOW. Power-down logic levels are CMOS and TTL compatible with high input impedance.

2. Features and benefits

- Wideband data output (600 kHz minimum)
- Fast RSSI rise and fall times
- Low power consumption: 6.5 mA typical at 3 V
- Mixer input to >500 MHz
- Mixer conversion power gain of 11 dB at 240 MHz
- Mixer noise figure of 12 dB at 240 MHz
- XTAL oscillator effective to 150 MHz (LC oscillator to 1 GHz local oscillator can be injected)
- 92 dB of IF amp/limiter gain
- 25 MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90 dB
- RSSI output internal op amp
- Internal op amps with rail-to-rail outputs
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.54 μV into 50 Ω matching network for 12 dB SINAD (Signal-to-Noise And Distortion ratio) for 1 kHz tone with RF at 240 MHz and IF at 10.7 MHz
- 10.7 MHz filter matching (330 Ω)
- Power-down mode (I_{CC} = 200 μA)

- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 Class II, Level B

3. Applications

- DECT (Digital European Cordless Telephone)
- Digital cordless telephones
- Digital cellular telephones
- Portable high performance communications receivers
- Single conversion VHF/UHF receivers
- FSK and ASK data receivers
- Wireless LANs

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
SA636BS	636B	HVQFN20	plastic thermal enhanced very thin quad flat package; no leads; 20 terminals; body 4 × 4 × 0.85 mm	SOT917-1
SA636DK/01	SA636DK	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

5. Block diagram

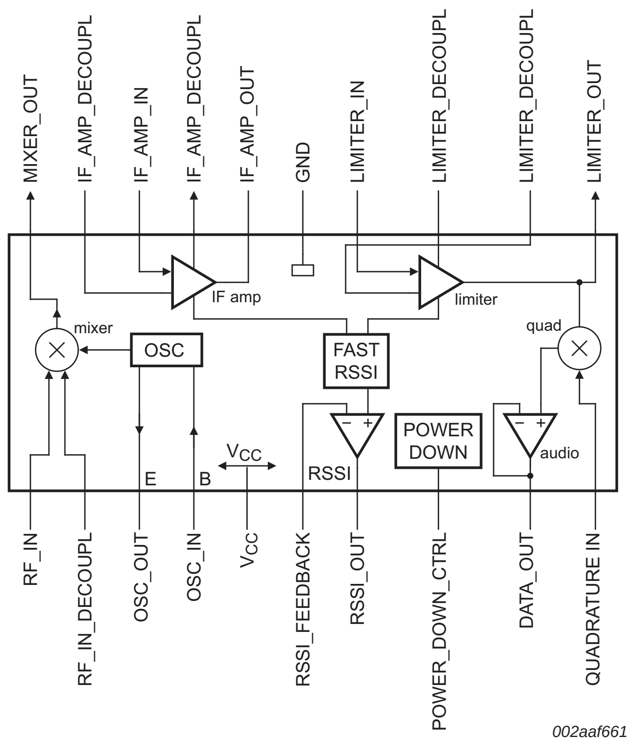


Fig 1. Block diagram of SA636

6. Pinning information

6.1 Pinning

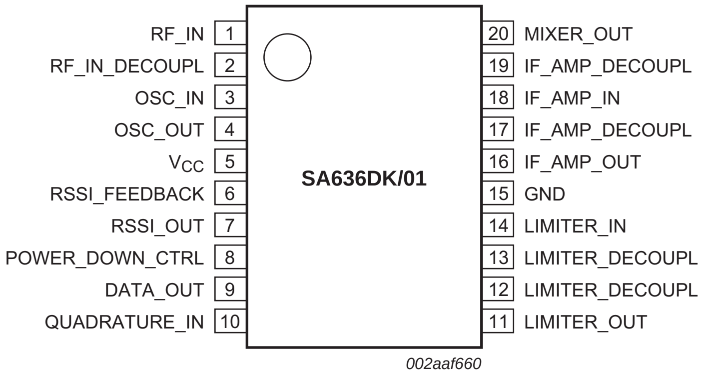
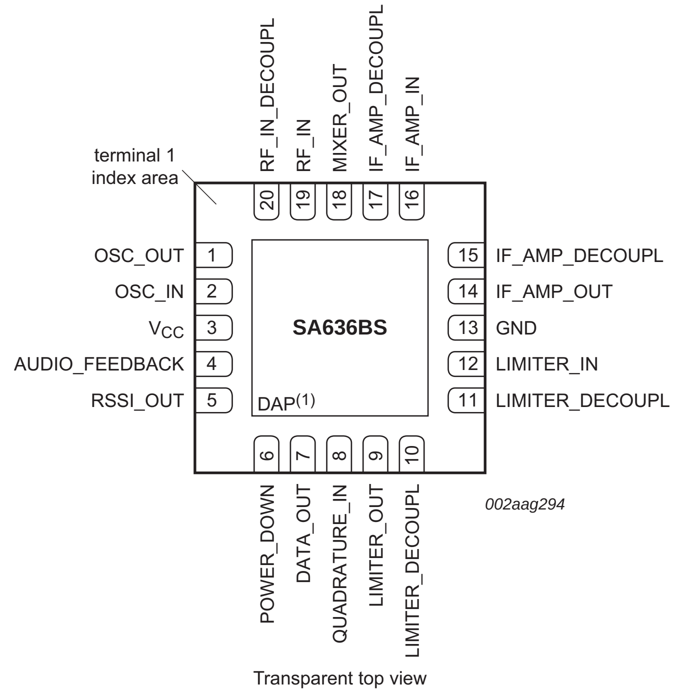


Fig 2. Pin configuration for SSOP20



(1) Die Attach Paddle (DAP).

Fig 3. Pin configuration for HVQFN20

6.2 Pin description

Table 2. Pin description

Symbol	Pin		Description
	SSOP20	HVQFN20	
RF_IN	1	19	RF input
RF_IN_DECOUPL	2	20	RF input decoupling pin
OSC_OUT	3	1	oscillator output (emitter)
OSC_IN	4	2	oscillator input (base)
V_{CC}	5	3	positive supply voltage
RSSI_FEEDBACK	6	4	RSSI amplifier negative feedback terminal
RSSI_OUT	7	5	RSSI output
POWER_DOWN_CTRL	8	6	power-down control; active HIGH
DATA_OUT	9	7	data output
QUADRATURE_IN	10	8	quadrature detector input terminal
LIMITER_OUT	11	9	limiter amplifier output
LIMITER_DECOUPL	12	10	limiter amplifier decoupling pin
LIMITER_DECOUPL	13	11	limiter amplifier decoupling pin
LIMITER_IN	14	12	limiter amplifier input
GND	15	13[1]	ground; negative supply
IF_AMP_OUT	16	14	IF amplifier output
IF_AMP_DECOUPL	17	15	IF amplifier decoupling pin
IF_AMP_IN	18	16	IF amplifier input
IF_AMP_DECOUPL	19	17	IF amplifier decoupling pin
MIXER_OUT	20	18	mixer output
-	-	DAP	exposed die attach paddle; connect to ground

[1] For the HVQFN20 package, the exposed die attach paddle must be connected to device ground pin 13 and the PCB ground plane. GND pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

7. Functional description

The SA636 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1 GHz. The bandwidth of the IF amplifier is about 40 MHz with 38 dB of gain from a 50 Ω source. The bandwidth of the limiter is about 28 MHz with about 54 dB of gain from a 50 Ω source. However, the gain/bandwidth distribution is optimized for 10.7 MHz, 330 Ω source applications. The overall system is well-suited to battery operation as well as high performance and high-quality products of all types such as cordless and cellular hand-held phones.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 14 dB, conversion gain of 11 dB, and input third-order intercept of −16 dBm. The oscillator will operate in excess of 1 GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100 MHz for crystal configurations. Butler oscillators are recommended for crystal configurations up to 150 MHz.

The output of the mixer is internally loaded with a 330 Ω resistor permitting direct connection to a 10.7 MHz ceramic filter for narrowband applications. The input resistance of the limiting IF amplifiers is also 330 Ω. With most 10.7 MHz ceramic filters and many crystal filters, no impedance matching network is necessary. For applications requiring wideband IF filtering, such as DECT, external LC filters are used (see Figure 15).

To achieve optimum linearity of the log signal strength indicator, there must be a 6 dBV insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 6 dBV insertion loss, a fixed or variable resistor can be added between the first IF output (IF_AMP_OUT) and the interstage network.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90 dB for operation at intermediate frequency at 10.7 MHz. Special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output (DATA_OUT) of the quadrature is a voltage output. This output is designed to handle a minimum bandwidth of 600 kHz. This is designed to demodulate wideband data, such as in DECT applications.

A Received Signal Strength Indicator (RSSI) completes the circuitry. The output range is greater than 90 dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPS or TACS cellular telephone, DECT and RCR-28 cordless telephone. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or second-order temperature compensation of the RSSI, if needed.

Remark: dBV = 20log V_O/V_I.

8. Internal circuitry

Table 3. Internal circuits for each pin

Pin numbers shown for SSOP20 package; HVQFN20 pins shown in parentheses in 'Pin' column.

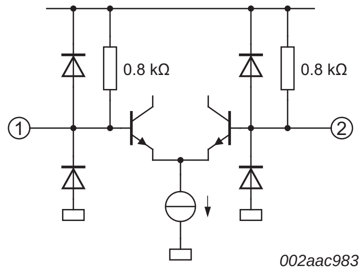
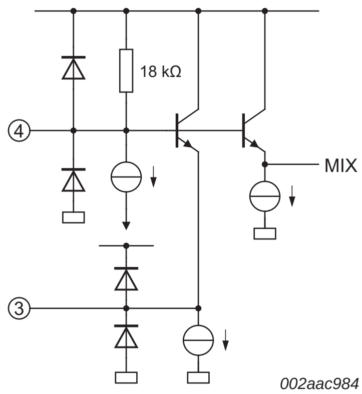
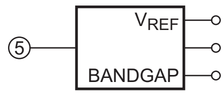
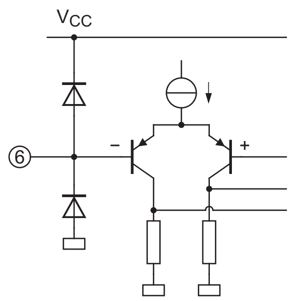
Symbol	Pin	DC V	Equivalent circuit
RF_IN	1 (19)	+1.07 V	 002aac983
RF_IN_DECOUPL	2 (20)	+1.07 V	
OSC_OUT	3 (1)	+1.57 V	 002aac984
OSC_IN	4 (2)	+2.32 V	
V_{CC}	5 (3)	+3.00 V	 002aac985
RSSI_FEEDBACK	6 (4)	+0.20 V	 002aac986

Table 3. Internal circuits for each pin *...continued*

Pin numbers shown for SSOP20 package; HVQFN20 pins shown in parentheses in 'Pin' column.

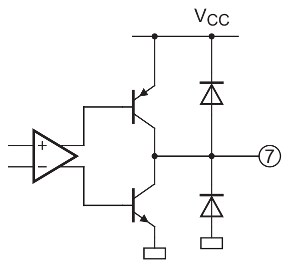
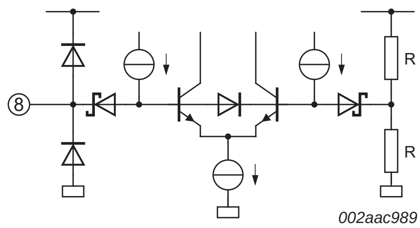
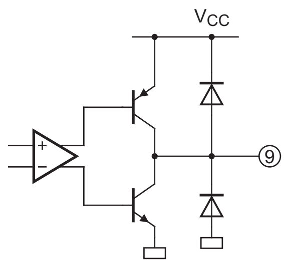
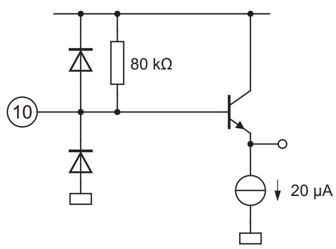
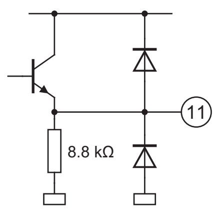
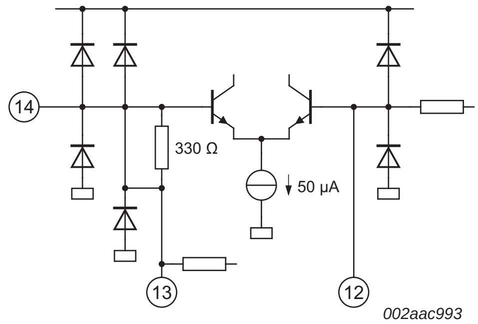
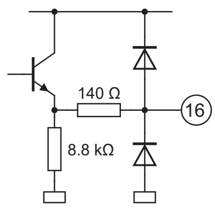
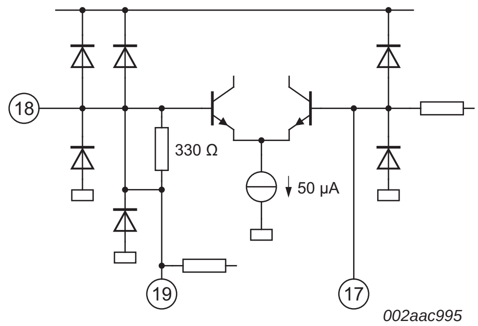
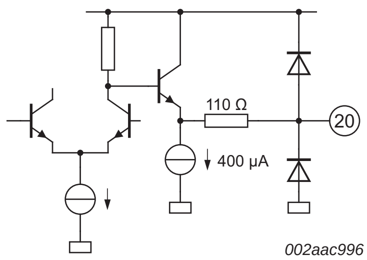
Symbol	Pin	DC V	Equivalent circuit
RSSI_OUT	7 (5)	+0.20 V	 *002aac988*
POWER_DOWN_CTRL	8 (6)	+2.75 V	 *002aac989*
DATA_OUT	9 (7)	+1.09 V	 *002aac990*
QUADRATURE_IN	10 (8)	+3.00 V	 *002aac991*
LIMITER_OUT	11 (9)	+1.35 V	 *002aac992*

Table 3. Internal circuits for each pin *...continued*

Pin numbers shown for SSOP20 package; HVQFN20 pins shown in parentheses in 'Pin' column.

Symbol	Pin	DC V	Equivalent circuit
LIMITER_DECOUPL	12 (10)	+1.23 V	
LIMITER_DECOUPL	13 (11)	+1.23 V	
LIMITER_IN	14 (12)	+1.23 V	
GND	15 (13)	0 V	-
IF_AMP_OUT	16 (14)	+1.22 V	
IF_AMP_DECOUPL	17 (15)	+1.22 V	
IF_AMP_IN	18 (16)	+1.22 V	
IF_AMP_DECOUPL	19 (17)	+1.22 V	
MIXER_OUT	20 (18)	+1.03 V	

9. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		0.3	7	V
V_n	voltage on any other pin		−0.3	V_{CC} + 0.3	V
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	ambient temperature	operating	−40	+85	°C

10. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Max	Unit
$Z_{th(j-a)}$	transient thermal impedance from junction to ambient	SA636DK/01 (SSOP20)	117	K/W
		SA636BS (HVQFN20)	40	K/W

11. Static characteristics

Table 6. Static characteristics
V_{CC} = 3 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.7	3.0	5.5	V
I_{CC}	supply current	DC current drain; POWER_DOWN_CTRL = HIGH	5.5	6.5	7.5	mA
I_I	input current	POWER_DOWN_CTRL = LOW	−10	-	+10	μA
		POWER_DOWN_CTRL = HIGH	−10	-	+10	μA
V_I	input voltage	POWER_DOWN_CTRL = LOW	0	-	0.3 × V_{CC}	V
		POWER_DOWN_CTRL = HIGH	0.7 × V_{CC}	-	V_{CC}	V
$I_{CC(stb)}$	standby supply current	POWER_DOWN_CTRL = LOW	-	0.2	0.5	mA
t_{ON}	power-up time	RSSI valid (10 % to 90 %)	-	10	-	μs
t_{OFF}	power-down time	RSSI invalid (90 % to 10 %)	-	5	-	μs

12. Dynamic characteristics

Table 7. Dynamic characteristics

T_{amb} = 25 °C; V_{CC} = +3 V, unless otherwise stated. RF frequency = 240.05 MHz + 14.5 dBV RF input step-up; IF frequency = 10.7 MHz; RF level = −45 dBm; FM modulation = 1 kHz with ±125 kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 19. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Mixer/oscillator section (external LO = 160 mV RMS value)						
f_i	input frequency		-	500	-	MHz
f_{osc}	oscillator frequency	external oscillator (buffer)	-	500	-	MHz
NF	noise figure	at 240 MHz	-	12	-	dB
$IP3_i$	input third-order intercept point	matched f1 = 240.05 MHz; f2 = 240.35 MHz	-	−16	-	dBm
$G_{p(conv)}$	conversion power gain	matched 14.5 dBV step-up	8	11	14	dB
$R_{i(RF)}$	RF input resistance	single-ended input	-	700	-	Ω
$C_{i(RF)}$	RF input capacitance		-	3.5	-	pF
$R_{o(mix)}$	mixer output resistance	MIXER_OUT pin	-	-	-	
IF section						
$G_{amp(IF)}$	IF amplifier gain	330 Ω load	-	38	-	dB
G_{lim}	limiter gain	330 Ω load	-	54	-	dB
$P_{i(IF)}$	IF input power	for −3 dB input limiting sensitivity; test at IF_AMP_IN pin	-	−105	-	dBm
α_{AM}	AM rejection	80 % AM 1 kHz	-	40	-	dB
$V_{o(RMS)}$	RMS output voltage	R_L = 100 kΩ	120	130	-	mV
B_{3dB}	3 dB bandwidth		600	700	-	kHz
SINAD	signal-to-noise-and-distortion ratio	RF level = −111 dBm	-	16	-	dB
THD	total harmonic distortion		-	−43	−38	dB
S/N	signal-to-noise ratio	no modulation for noise	-	60	-	dB
$V_{o(RSSI)}$	RSSI output voltage	IF with buffer				
		IF level = −118 dBm	-	0.2	0.5	V
		IF level = −68 dBm	0.3	0.6	1.0	V
		IF level = −10 dBm	0.9	1.3	1.8	V
$t_{r(o)}$	output rise time	IF RSSI output; 10 kHz pulse; no 10.7 MHz filter; no RSSI bypass capacitor; IF frequency = 10.7 MHz				
		RF level = −56 dBm	-	1.2	-	μs
		RF level = −28 dBm	-	1.1	-	μs
$t_{f(o)}$	output fall time	IF RSSI output; 10 kHz pulse; no 10.7 MHz filter; no RSSI bypass capacitor; IF frequency = 10.7 MHz				
		RF level = −56 dBm	-	2.0	-	μs
		RF level = −28 dBm	-	7.3	-	μs

Table 7. Dynamic characteristics *...continued*

T_{amb} = 25 °C; V_{CC} = +3 V, unless otherwise stated. RF frequency = 240.05 MHz + 14.5 dBV RF input step-up; IF frequency = 10.7 MHz; RF level = −45 dBm; FM modulation = 1 kHz with ±125 kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 19. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\alpha_{RSSI(range)}$	RSSI range		-	90	-	dB
$\Delta\alpha_{RSSI}$	RSSI variation		-	±1.5	-	dB
$Z_{i(IF)}$	IF input impedance		-	330	-	Ω
$Z_{o(IF)}$	IF output impedance		-	330	-	Ω
$Z_{i(lim)}$	limiter input impedance		-	330	-	Ω
$Z_{o(lim)}$	limiter output impedance		-	300	-	Ω
$V_{o(RMS)}$	RMS output voltage	limiter output level with no load	-	130	-	mV
RF/IF section (internal LO)						
$V_{o(RSSI)}$	RSSI output voltage	system; RF level = −10 dBm	-	1.4	-	V
SINAD	signal-to-noise-and-distortion ratio	system; RF level = −106 dBm	-	12	-	dB

13. Performance curves

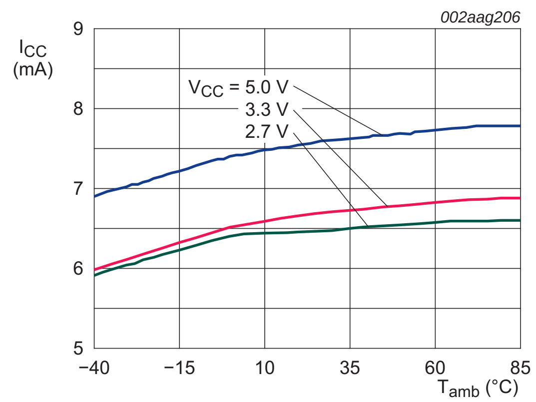


Fig 4. Supply current versus ambient temperature

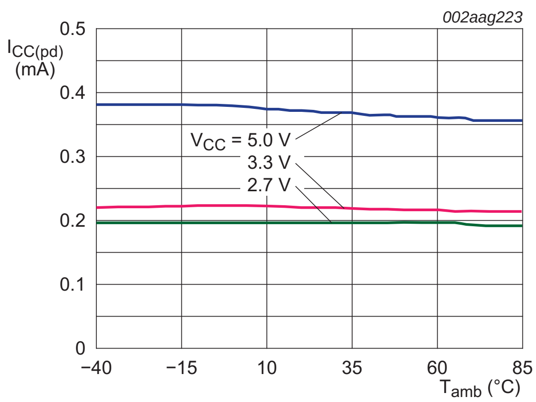
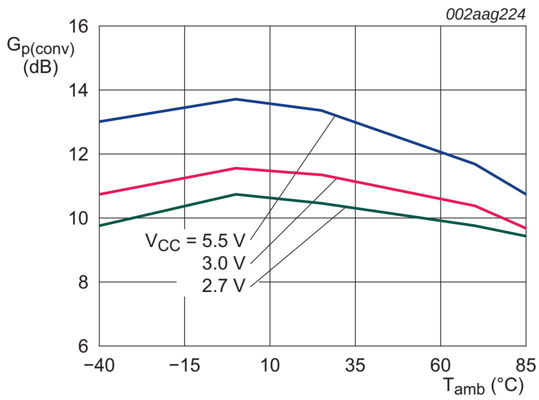
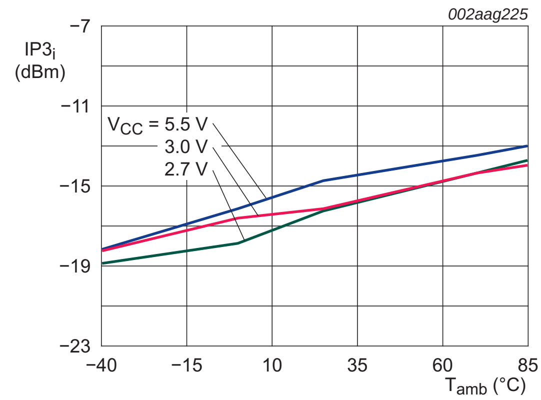


Fig 5. Power-down mode supply current versus ambient temperature



RF level = –45 dBm

Fig 6. Mixer conversion power gain versus ambient temperature



RF level = –45 dBm

Fig 7. Mixer input third-order intercept point at 240 MHz versus ambient temperature

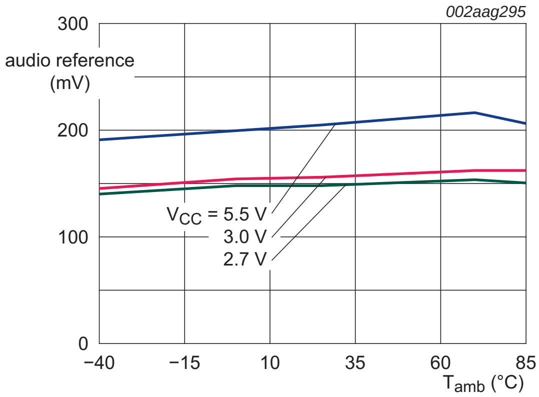
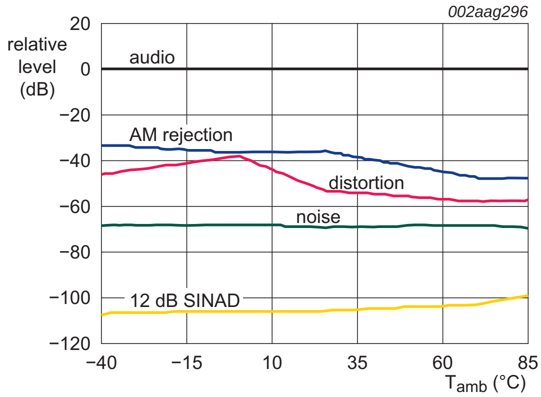


Fig 8. Audio reference level versus ambient temperature



V_{CC} = 3 V; RF = 240 MHz; level = –68 dBm;
deviation = 125 kHz

Fig 9. 12 dB SINAD and relative audio, THD, noise, and AM rejection versus ambient temperature

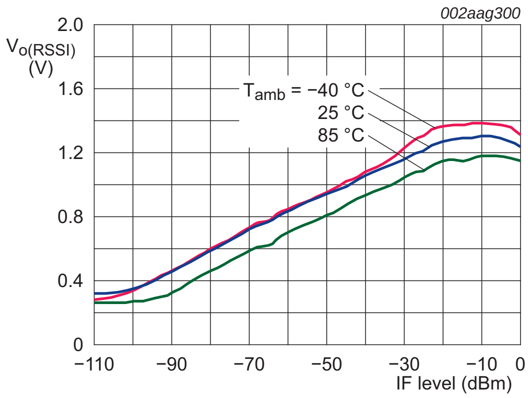


Fig 10. RSSI output voltage versus IF level

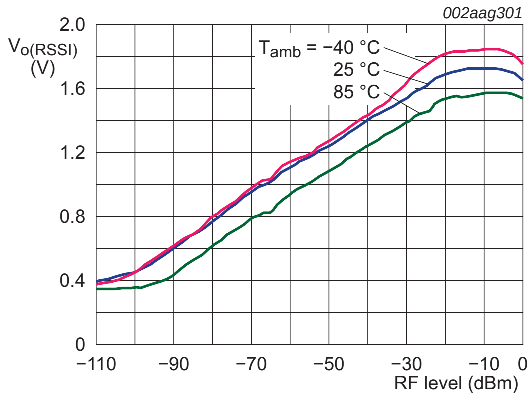


Fig 11. RSSI output voltage versus RF level

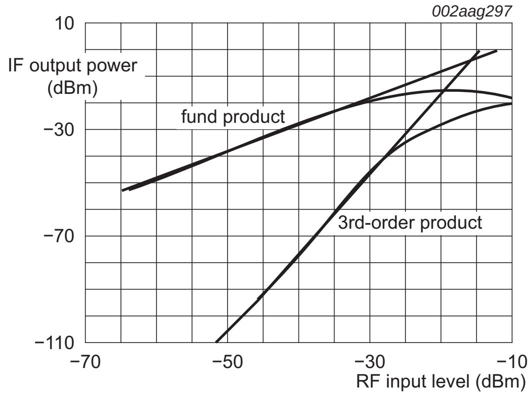
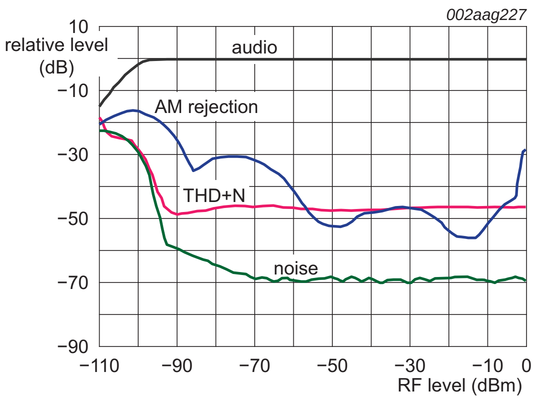
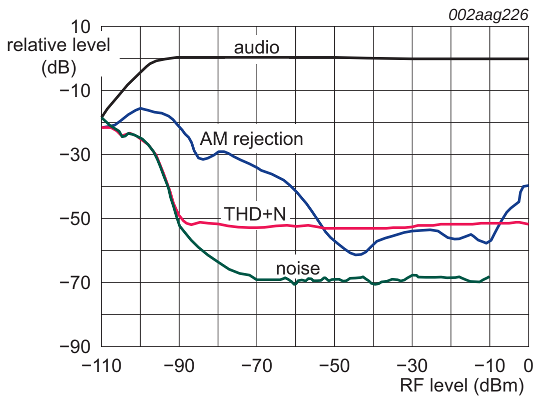


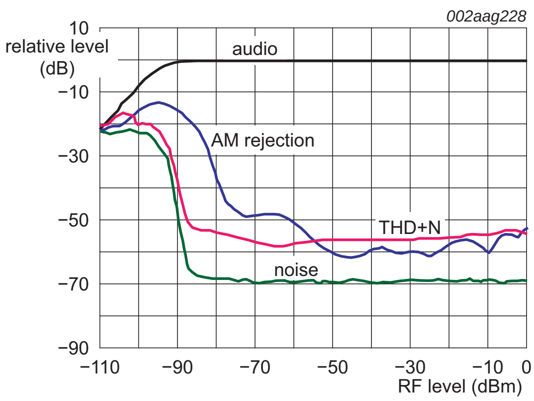
Fig 12. Mixer third-order intercept and compression



a. T_{amb} = −40 °C; $V_{o(aud)RMS}$ = 118 mV

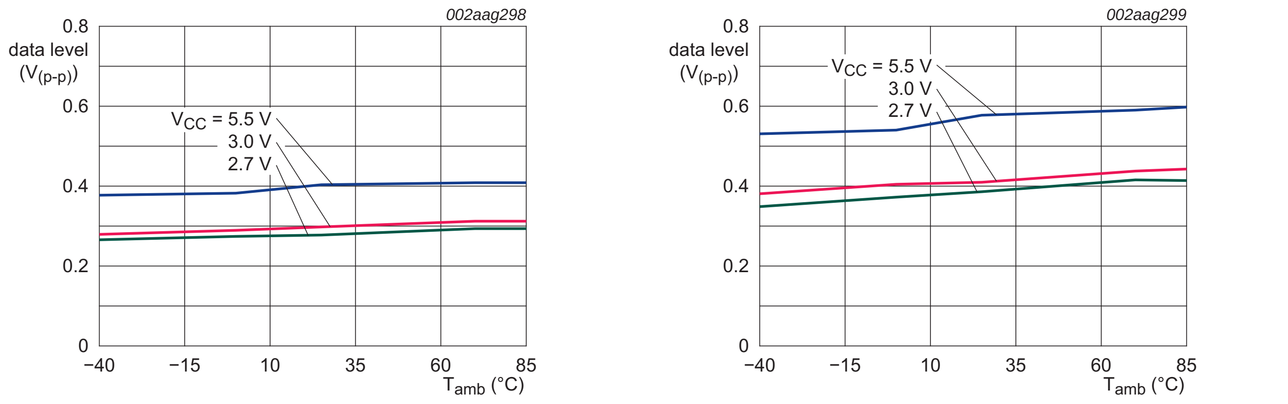


b. T_{amb} = 25 °C; $V_{o(aud)RMS}$ = 129 mV



c. T_{amb} = 85 °C; $V_{o(aud)RMS}$ = 131 mV

Fig 13. Relative level of audio, AM rejection, THD+N and noise versus RF level



a. 600 kHz data rate

b. 1 kHz data rate

IF = 9.85 MHz; deviation = 288 kHz; RF = –40 dBm

Fig 14. Data level versus ambient temperature

14. Application information

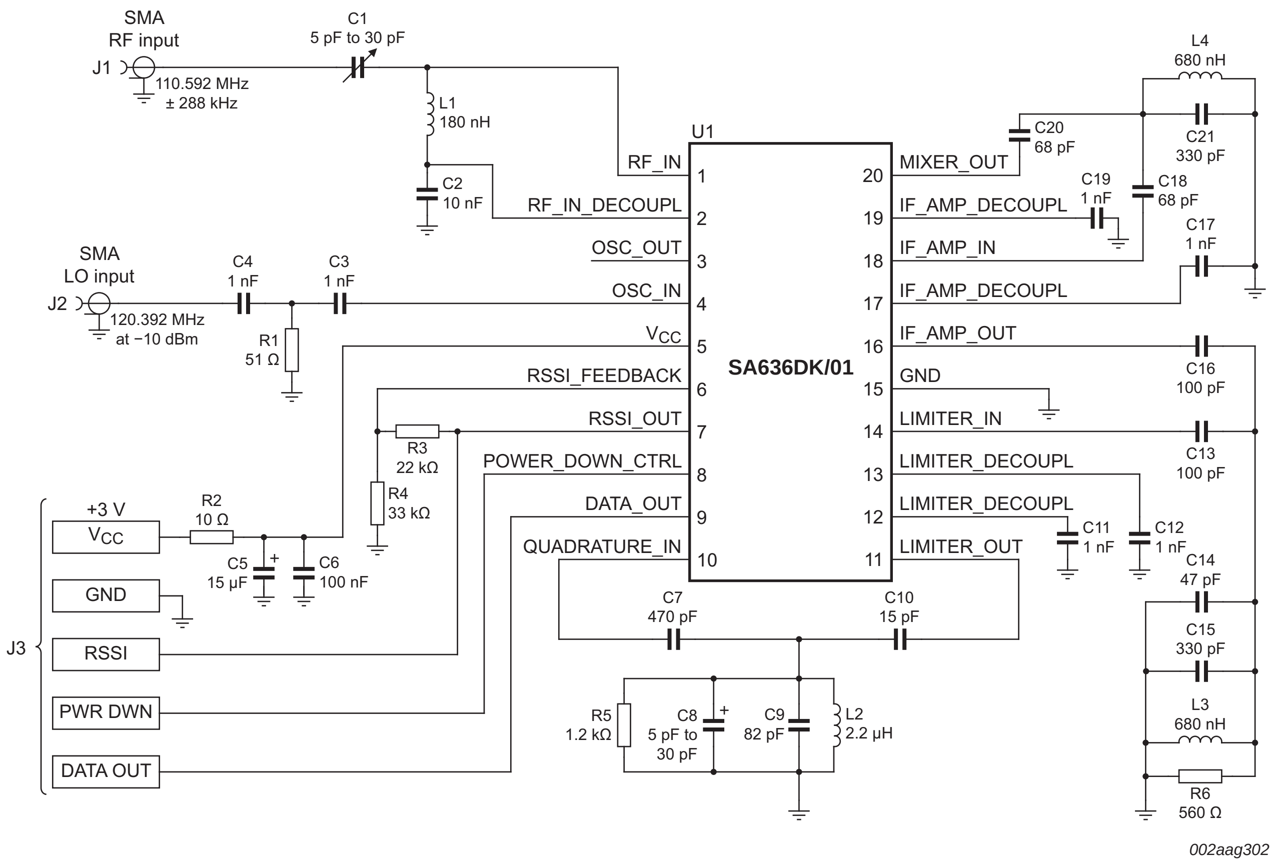
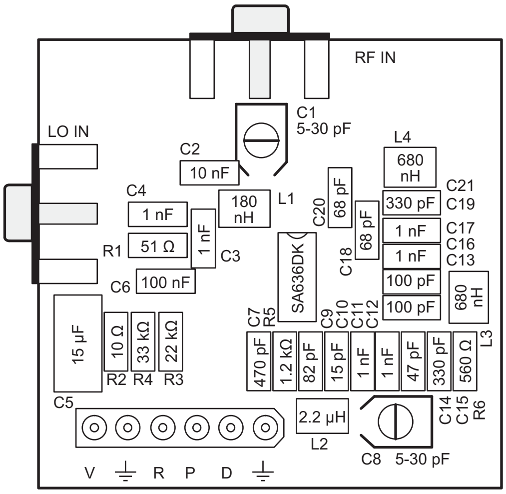


Fig 15. SA636 110.592 MHz (RF), 9.8 MHz (IF) DECT application circuit

Table 8. DECT application circuit electrical characteristics

RF frequency = 110.592 MHz; IF frequency = 9.8 MHz; RF level = –45 dBm; FM modulation = 100 kHz with ±288 kHz peak deviation.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Mixer/oscillator section (external LO = 160 mV RMS value)						
$G_{p(conv)}$	conversion power gain		-	13	-	dB
NF	noise figure	at 110 MHz	-	12	-	dB
$IP3_i$	input third-order intercept point	matched f1 = 110.592 MHz; f2 = 110.892 MHz	-	–15	-	dBm
$R_{i(RF)}$	RF input resistance		-	690	-	Ω
$C_{i(RF)}$	RF input capacitance		-	3.6	-	pF
IF section						
$G_{amp(IF)}$	IF amplifier gain	330 Ω load	-	38	-	dB
G_{lim}	limiter gain	330 Ω load	-	54	-	dB
$V_{o(RMS)}$	RMS output voltage	R_L = 3 kΩ	-	130	-	mV
B_{3dB}	3 dB bandwidth		-	700	-	kHz
RF/IF section (internal LO)						
$V_{o(RSSI)}$	RSSI output voltage	system; RF level = –10 dBm	-	1.4	-	V
S/N	signal-to-noise ratio	system; RF level = –83 dBm	-	10	-	dB



002aag362

a. Top silk screen

002aag363

b. Top view

002aag364

c. Bottom view

Remark: Not actual size.

Fig 16. SA636 demo board layout (SSOP20)

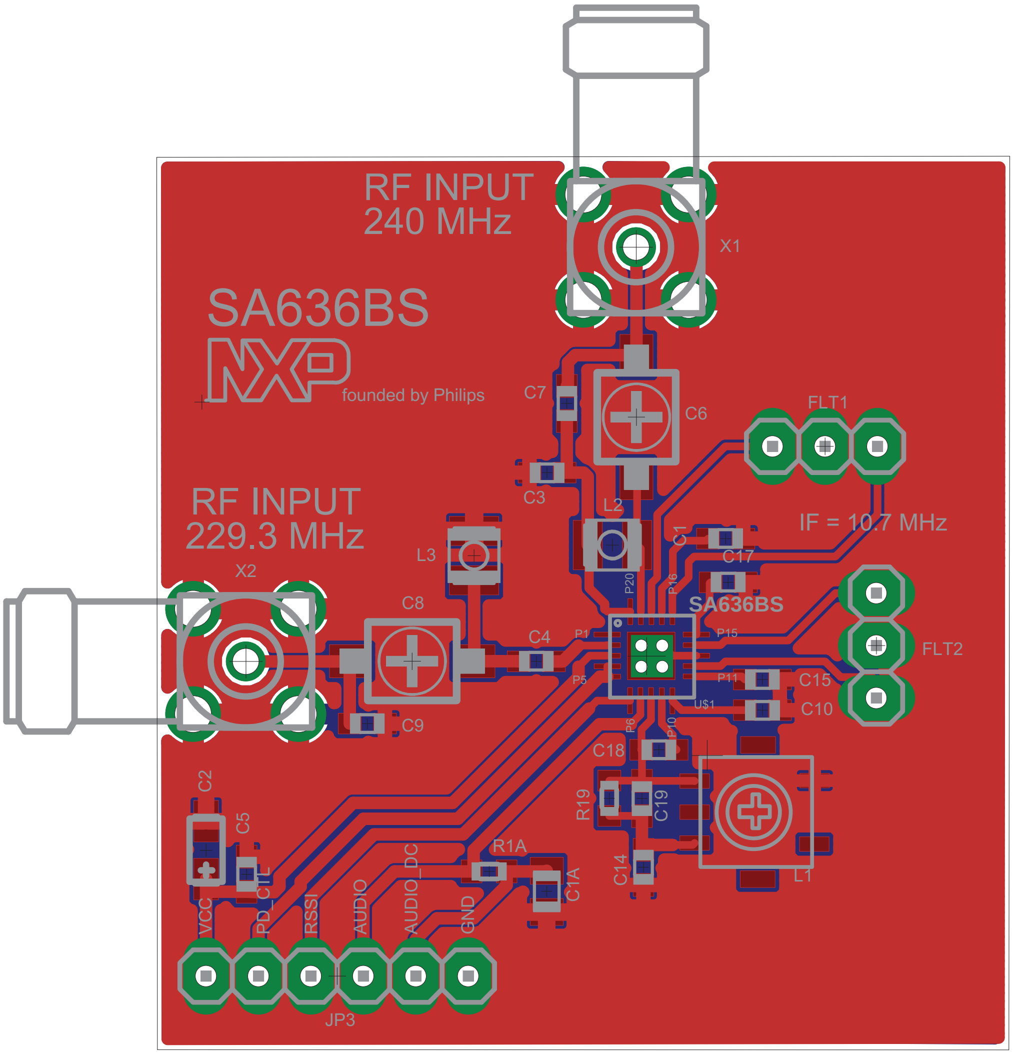


Fig 17. SA636BS demo board (HVQFN20)

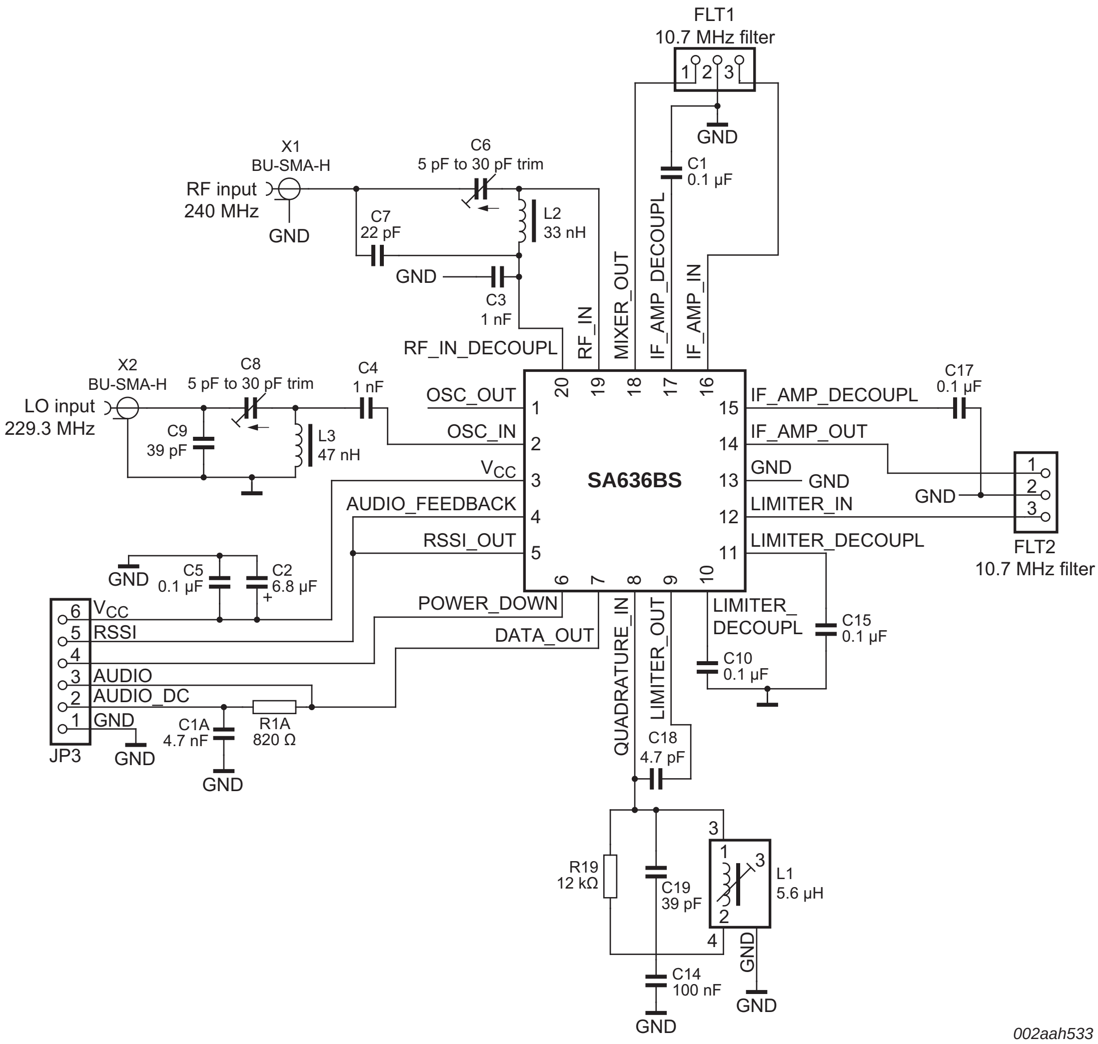
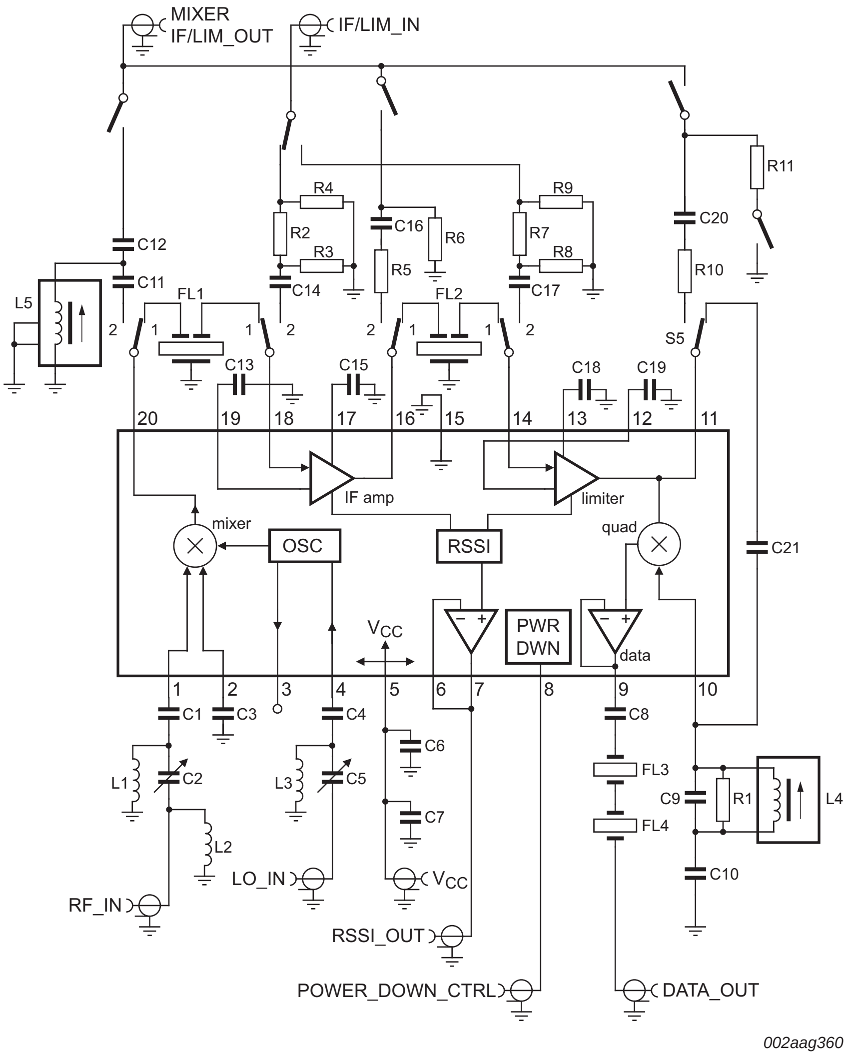


Fig 18. SA636BS schematic (HVQFN20)

15. Test information



The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.

All of the inductors, the quad tank, and their shield must be grounded. A 0.1 µF bypass capacitor on the supply pin improves sensitivity.

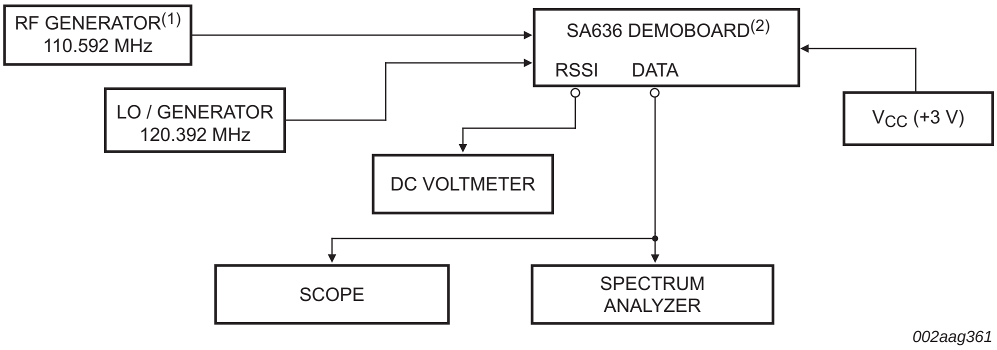
For the HVQFN20 package, the die attach paddle must be connected to the ground of PCB.

Fig 19. 240.05 MHz (RF) / 10.7 MHz (IF) test circuit

Table 9. Automatic test circuit component list

Component	Description
R1	7.5 kΩ resistor; select
R2, R7	6.49 kΩ resistor
R3, R8	347.8 Ω resistor
R4, R6, R9, R11	49.9 Ω resistor
R5, R10	1 kΩ resistor
R12, R14	60.4 Ω resistor
R13	249 Ω resistor
C1, C4	10 nF capacitor
C2	5.6 pF capacitor; select for input match
C3, C10, C11, C14, C16, C17, C20, C22	0.1 μF capacitor
C5	5 pF to 300 pF variable capacitor; Murata TZC3P300A 110R00
C6	100 pF capacitor
C7	15 μF, 20 V capacitor[1]
C8	1 μF capacitor
C9	39 pF capacitor; select
C10, C13, C15, C18, C19	1000 pF capacitor
C12	150 pF capacitor; select
C21	2.7 pF capacitor
L2	27 nH inductor[1]; Coilcraft 1008HT-27NT or Garret PM20-RO27; select for input match
L3	39 nH inductor; Coilcraft 1008HQ-39NX; select for input match
L4	5.6 μH variable, shielded inductor, 5 mm SMD; Toko 613BN-9056Z; select for input match
L5	1.27 μH to 2.25 μH variable shielded inductor; 5 mm SMD; select for mixer output match
FL1, FL2	10.7 MHz filter (Murata SFE10.7MA5-A)
FL3	‘C’ message weighted filter
FL4	active de-emphasis filter

[1] This value can be reduced when a battery is the power source.



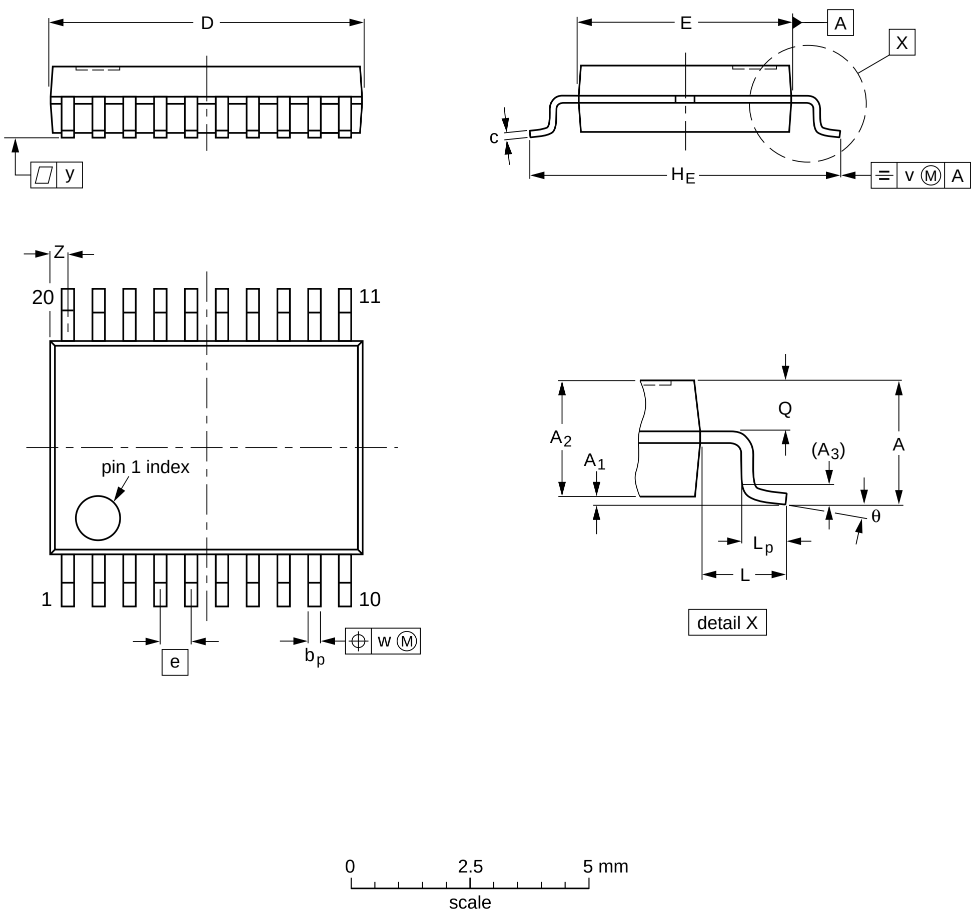
(1) Set your RF generator at 110.592 MHz; use a 100 kHz modulation frequency and a ±288 kHz deviation.

(2) The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500 mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.

Fig 20. Application circuit test setup

16. Package outline

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm **SOT266-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10° 0°

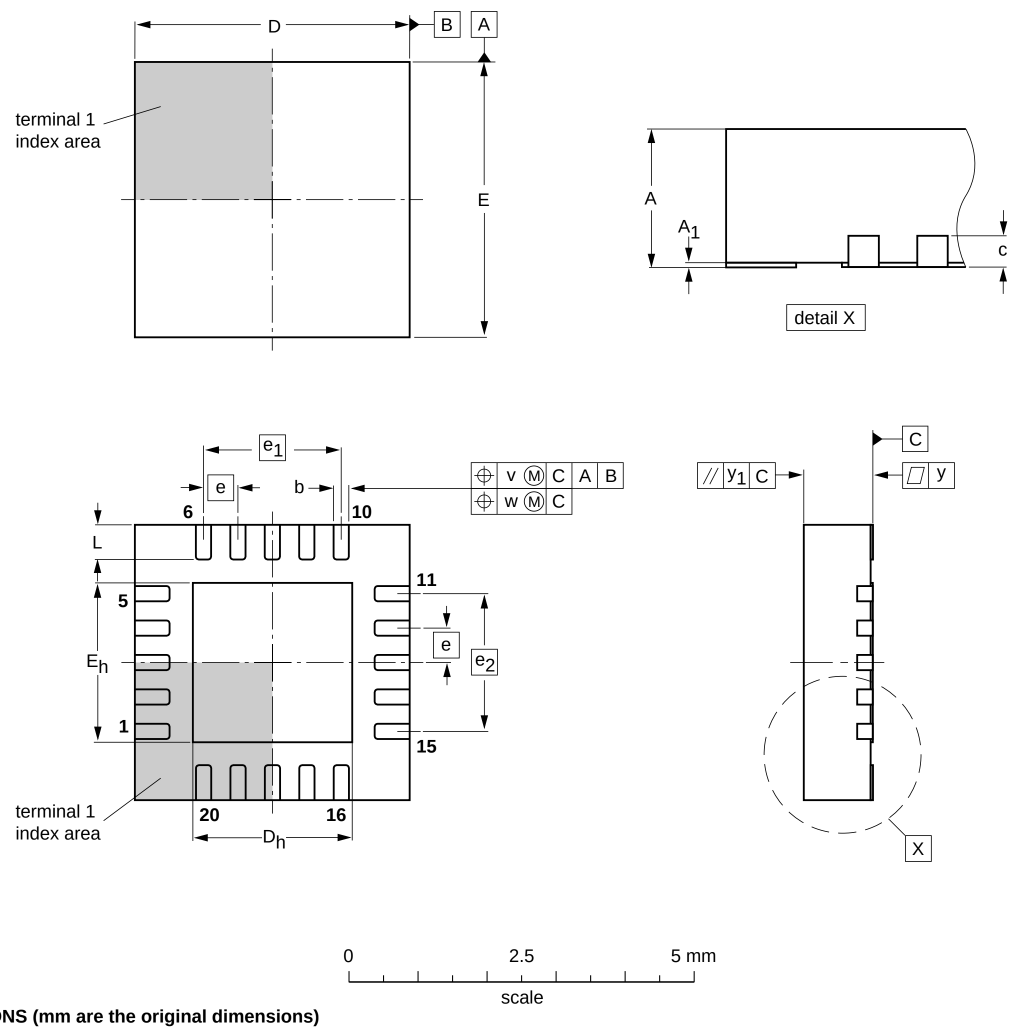
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT266-1		MO-152				~~99-12-27~~ 03-02-19

Fig 21. Package outline SOT266-1 (SSOP20)

HVQFN20: plastic thermal enhanced very thin quad flat package; no leads; 20 terminals; body 4 x 4 x 0.85 mm **SOT917-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.1 3.9	2.45 2.15	4.1 3.9	2.45 2.15	0.5	2	2	0.6 0.4	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT917 -1	- - -	MO-220	- - -			~~05-10-08~~ 05-10-31

Fig 22. Package outline SOT917-1 (HVQFN20)

17. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 23) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 10 and 11

Table 10. SnPb eutectic process (from J-STD-020C)

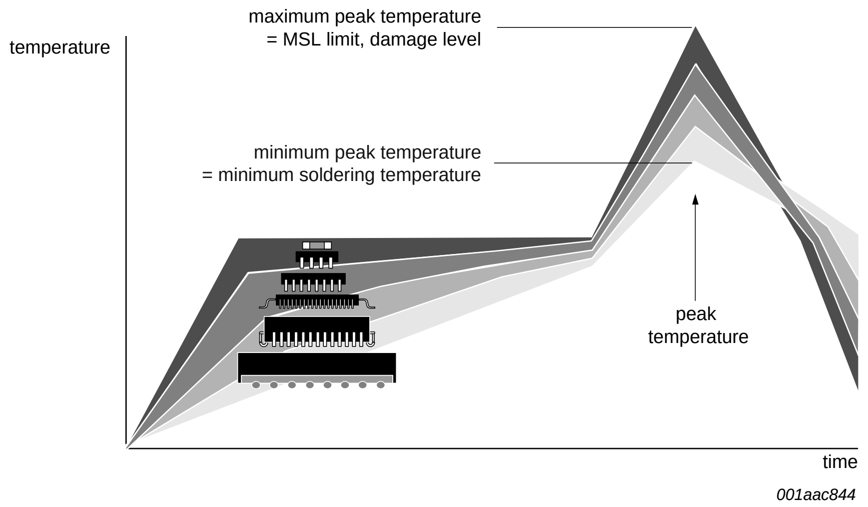
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 11. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 23.



MSL: Moisture Sensitivity Level

Fig 23. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

18. Abbreviations

Table 12. Abbreviations

Acronym	Description
AMPS	Advanced Mobile Phone System
ASK	Amplitude Shift Keying
BER	Bit Error Rate
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DECT	Digital European Cordless Telephone
ESD	ElectroStatic Discharge
FM	Frequency Modulation
FSK	Frequency Shift Keying
HBM	Human Body Model
IF	Intermediate Frequency
LAN	Local Area Network
LC	inductor-capacitor filter
RCR	Research and development Center for Radio systems
RF	Radio Frequency
RSSI	Received Signal Strength Indicator
SINAD	Signal-to-Noise And Distortion ratio
SMD	Surface Mount Device
TACS	Total Access Communication System

Table 12. Abbreviations *...continued*

Acronym	Description
TTL	Transistor-Transistor Logic
UHF	Ultra High Frequency
VHF	Very High Frequency

19. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SA636 v.6	20121205	Product data sheet	-	SA636 v.5
Modifications:	• Table 2 “Pin description”: – appended “connect to ground” to description of DAP (HVQFN20) – Table note [1]: first sentence is re-written • Figure 19 “240.05 MHz (RF) / 10.7 MHz (IF) test circuit”: added 3rd paragraph (just above figure title) • Added Figure 17 “SA636BS demo board (HVQFN20)” • Added Figure 18 “SA636BS schematic (HVQFN20)”			
SA636 v.5	20120724	Product data sheet	-	SA636 v.4
SA636 v.4	20110909	Product data sheet	-	SA636 v.3
SA636 v.3	20030801	Product data	ECN 853-1757 30101 dated 15 Jul 2003	SA636 v.2
SA636 v.2	19971107	Product data	ECN 853-1757 18664 dated 07 Nov 1997	SA636 v.1
SA636 v.1	19940616	Product specification	ECN 853-1757 13150 dated 07 Nov 1997	-

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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