- **Members of the Texas Instruments**
  ***Widebus*™ Family**

- **Inputs Are TTL-Voltage Compatible**

- **Provide Extra Data Width Necessary for Wider Address/Data Paths or Buses With Parity**

- **Flow-Through Architecture Optimizes PCB Layout**

- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**

- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings**

```
        54ACT16825 . . . DW PACKAGE
        74ACT16825 . . . DL PACKAGE
                 (TOP VIEW)

   1OE1 [  1      56  ] 1OE2
   1Y1  [  2      55  ] 1A1
   1Y2  [  3      54  ] 1A2
   GND  [  4      53  ] GND
   1Y3  [  5      52  ] 1A3
   1Y4  [  6      51  ] 1A4
   VCC  [  7      50  ] VCC
   1Y5  [  8      49  ] 1A5
   1Y6  [  9      48  ] 1A6
   1Y7  [ 10      47  ] 1A7
   GND  [ 11      46  ] GND
   1Y8  [ 12      45  ] 1A8
   1Y9  [ 13      44  ] 1A9
   GND  [ 14      43  ] GND
   GND  [ 15      42  ] GND
   2Y1  [ 16      41  ] 2A1
   2Y2  [ 17      40  ] 2A2
   GND  [ 18      39  ] GND
   2Y3  [ 19      38  ] 2A3
   2Y4  [ 20      37  ] 2A4
   2Y5  [ 21      36  ] 2A5
   VCC  [ 22      35  ] VCC
   2Y6  [ 23      34  ] 2A6
   2Y7  [ 24      33  ] 2A7
   GND  [ 25      32  ] GND
   2Y8  [ 26      31  ] 2A8
   2Y9  [ 27      30  ] 2A9
   2OE1 [ 28      29  ] 2OE2
```

description

The 'ACT16825 18-bit buffers/drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The 'ACT16825 can be used as two 9-bit buffers or one 18-bit buffer. They provide true data from A to Y.

The 3-state control gate is a 2-input NOR gate; therefore, if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all nine affected outputs are in the high-impedance state.

The 74ACT16825 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16825 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT16825 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 9-bit section)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

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Texas Instruments

54ACT16825, 74ACT16825
18-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS
SCAS155B – JANUARY 1991 – REVISED APRIL 1996

logic symbol†
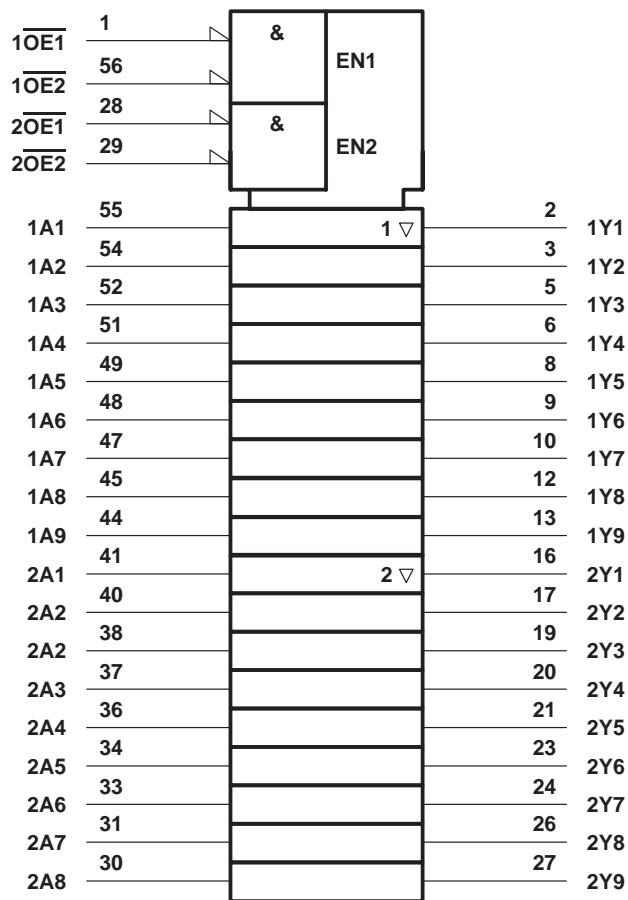
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

To Eight Other Channels   To Eight Other Channels
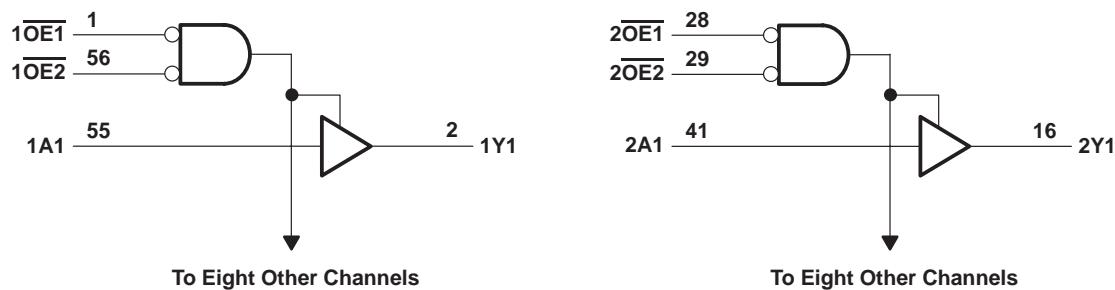
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) .... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) .... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) .... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±50 mA
Continuous current through V_{CC} or GND .... ±450 mA
Maximum package power dissipation at T_A = 55°C (in still air) (see Note 2): DL package .... 1.4 W
Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

		54ACT16825			74ACT16825			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			–24			–24	mA
I_{OL}	Low-level output current			24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	–55		125	–40		85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

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3

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	$T_A = 25°C$			54ACT16825		74ACT16825		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50\ \mu A$		4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
	$I_{OH} = -24\ mA$		4.5 V	3.94			3.8		3.8		
			5.5 V	4.94			4.8		4.8		
	$I_{OH} = -75\ mA^\dagger$		5.5 V				3.85		3.85		
V_{OL}	$I_{OL} = 50\ \mu A$		4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
	$I_{OL} = 24\ mA$		4.5 V			0.36		0.44		0.44	
			5.5 V			0.36		0.44		0.44	
	$I_{OL} = 75\ mA^\dagger$		5.5 V					1.65		1.65	
I_I	$V_I = V_{CC}$ or GND		5.5 V			±0.1		±1		±1	μA
I_{OZ}	$V_O = V_{CC}$ or GND		5.5 V			±0.5		±5		±5	μA
I_{CC}	$V_I = V_{CC}$ or GND,	$I_O = 0$	5.5 V			8		80		80	μA
$\Delta I_{CC}^\ddagger$	One input at 3.4 V, Other inputs at V_{CC} or GND		5.5 V			0.9		1		1	mA
C_i	$V_I = V_{CC}$ or GND		5 V		4						pF
C_o	$V_O = V_{CC}$ or GND		5 V		16						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\ V \pm 0.5\ V$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25°C$			54ACT16825		74ACT16825		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	4.1	7.5	9.3	4.1	10.5	4.1	10.5	ns
t_{PHL}			3.1	7.5	9.6	3.1	10.3	3.1	10.3	
t_{PZH}	$\overline{OE}$	Y	3.3	7.9	9.9	3.3	11	3.3	11	ns
t_{PZL}			4.1	9.5	12.1	4.1	13.2	4.1	13.2	
t_{PHZ}	$\overline{OE}$	Y	5.7	9	10.8	5.7	11.5	5.7	11.5	ns
t_{PLZ}			5.5	8.5	10	5.5	10.6	5.5	10.6	

operating characteristics, $V_{CC} = 5\ V$, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	$C_L = 50\ pF$, $f = 1\ MHz$	42	pF
		Outputs disabled		12	

![Texas Instruments logo]

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PARAMETER MEASUREMENT INFORMATION
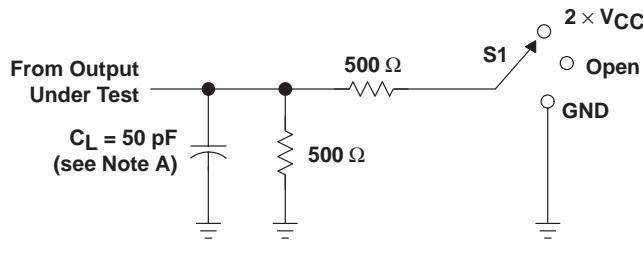
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

From Output Under Test

500 Ω   **S1** $2 \times V_{CC}$

○ Open

○ GND

C_L = 50 pF (see Note A)

500 Ω

LOAD CIRCUIT

Input   1.5 V   1.5 V   3 V / 0 V

t_{PLH} t_{PHL}

In-Phase Output   50% V_{CC} 50% V_{CC} V_{OH} / V_{OL}

t_{PHL} t_{PLH}

Out-of-Phase Output   50% V_{CC} 50% V_{CC} V_{OH} / V_{OL}

VOLTAGE WAVEFORMS

Output Control (low-level enabling)   1.5 V   1.5 V   3 V / 0 V

t_{PZL} t_{PLZ}

Output Waveform 1 S1 at $2 \times V_{CC}$ (see Note B)   50% V_{CC} 20% V_{CC} $\approx V_{CC}$ / V_{OL}

t_{PZH} t_{PHZ}

Output Waveform 2 S1 at GND (see Note B)   50% V_{CC} 80% V_{CC} V_{OH} / ≈ 0 V

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
      B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
      C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
      D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74ACT16825DL	Obsolete	Production	SSOP (DL) | 56	-	-	Call TI	Call TI	-40 to 85	ACT16825
74ACT16825DLR	Active	Production	SSOP (DL) | 56	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT16825
74ACT16825DLR.A	Active	Production	SSOP (DL) | 56	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT16825

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)
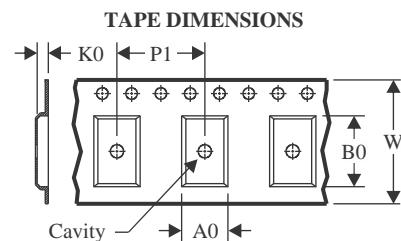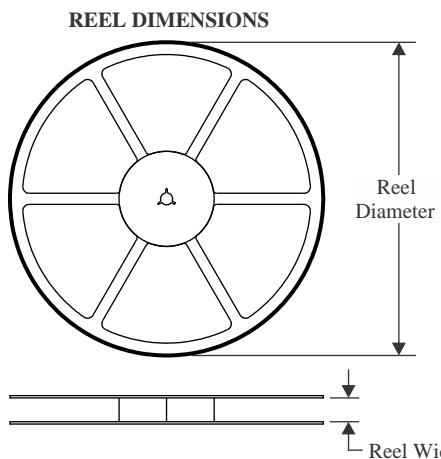
TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
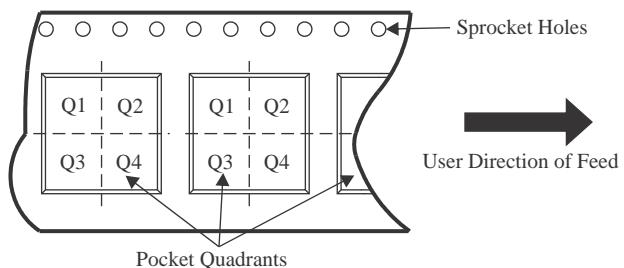
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74ACT16825DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS
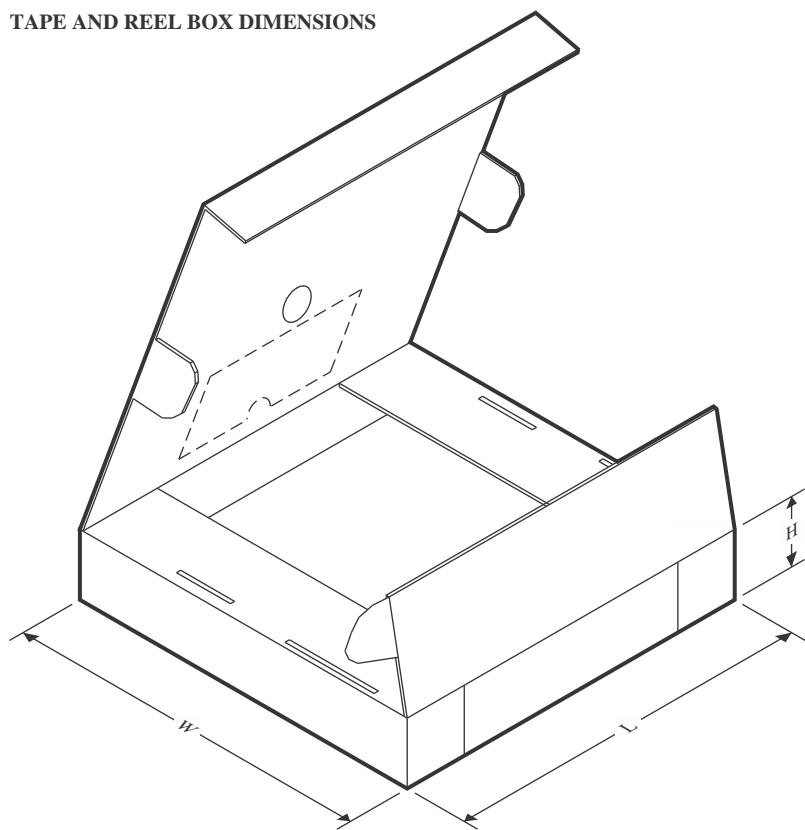
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74ACT16825DLR	SSOP	DL	56	1000	356.0	356.0	53.0

DL (R−PDSO−G56)   PLASTIC SMALL−OUTLINE PACKAGE

0.025 (0,635)

0.0135 (0,343)
0.008 (0,203)

⊕ 0.005 (0,13)Ⓜ

56   29

0.420 (10,67)
0.395 (10,03)

0.299 (7,59)
0.291 (7,39)

1   28

0.730 (18,54)
0.720 (18,29)

0.010 (0,25)
0.005 (0,13)

Gage Plane

0°−8°

0.010 (0,25)

0.040 (1,02)
0.020 (0,51)

0.110 (2,79) MAX

0.008 (0,20) MIN

Seating Plane

△ 0.004 (0,10)

4040048−4/F 05/13
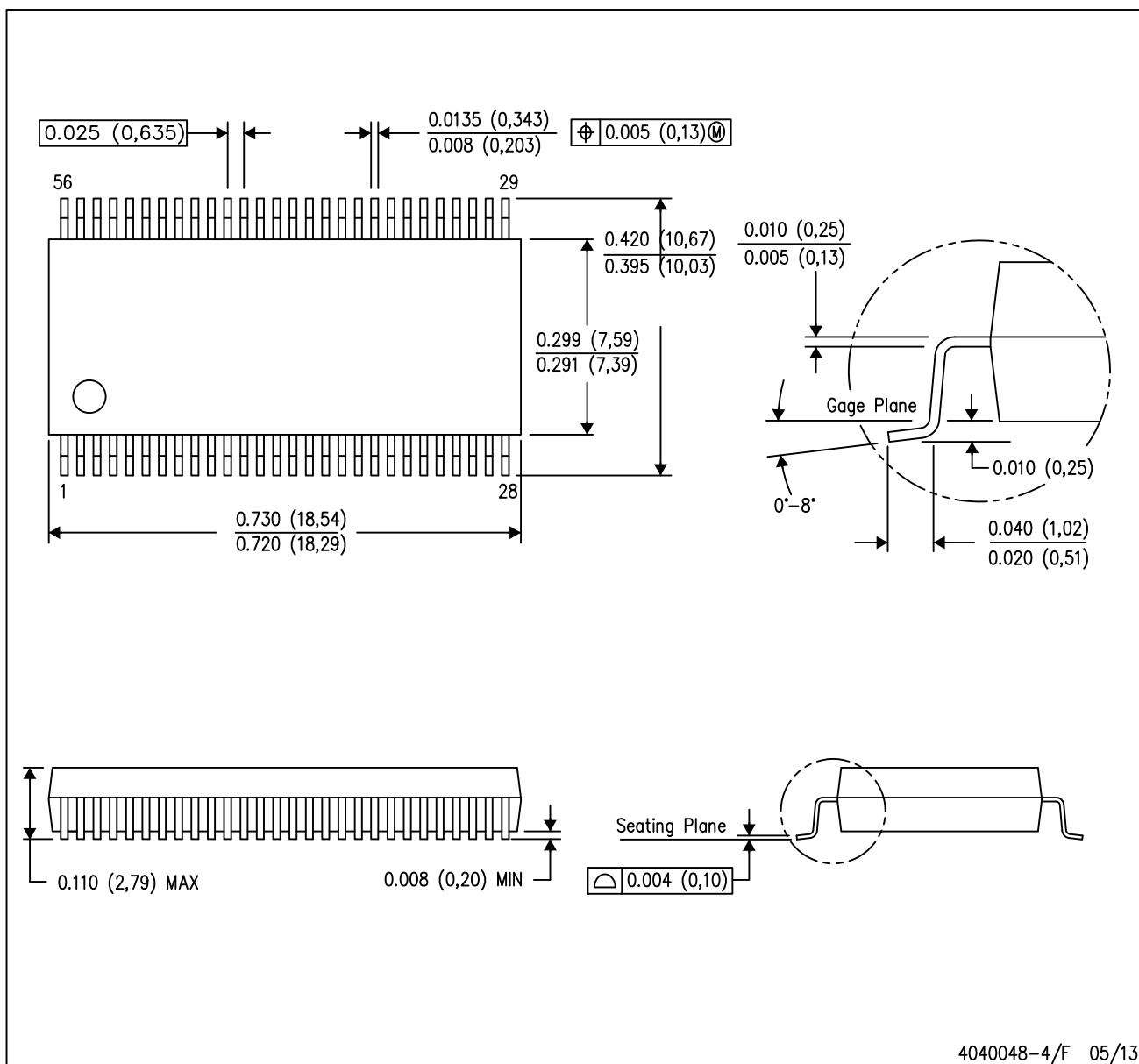
NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MO−118

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