

#### LOW EMI CLOCK GENERATOR

ICS180-52

### **Description**

The ICS180-52 generates a low EMI output clock from a clock or crystal input. The device uses IDT's proprietary mix of analog and digital Phase-Locked Loop (PLL) technology to spread the frequency spectrum of the output, thereby reducing the frequency amplitude peaks by several dB.

The ICS180-52 offers center spread selection of +/-0.625% and +/-1.875%. Refer to the MK1714-01/02 for the widest selection of input frequencies and multipliers.

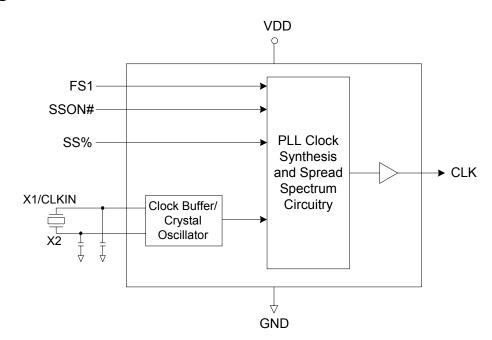
IDT offers a complete line of EMI reducing clock generators. Consult us when you need to remove crystals and oscillators from your board.

#### **Features**

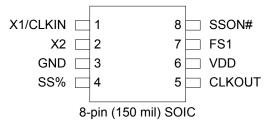
- Pin and function compatible to Cypress W180-52
- Packaged in 8-pin SOIC
- Provides a spread spectrum output clock
- Accepts a clock input and provides same frequency dithered output
- Input frequency of 8 to 15 MHz
- Peak reduction by 7dB 14dB typical on 3rd 19th odd harmonics
- Spread percentage selection for +/-0.625% and +/-1.875%
- Operating voltage of 3.3 V and 5 V
- Advanced, low-power CMOS process

NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01

### **Block Diagram**



## **Pin Assignment**



# **Spread Spectrum Select Table**

SS% (Pin 4)	Spread Direction	Spread Percentage (%)
0	Center	+/-0.625%
1	Center	+/1.875%

0 = connect to GND

1 = connect directly to VDD

Note: SS% pin has an internal pull-up resistor

## **Frequency Range Selection Table**

FS1 (Pin 7)	Frequency Range Selection (MHz)
0	8-10
1	10-15

## **Pin Descriptions**

Pin Number	Pin Name	Pin Type	Pin Description
1	X1/CLKIN	Input	Crystal or Clock Input.
2	X2	Output	Crystal output. Float for a clock input.
3	GND	Power	Connect to ground.
4	SS%	Input	Select pin for spread amount. See table above. Internal pull-up resistor.
5	CLKOUT	Output	Spread spectrum clock output per table above.
6	VDD	Power	Connect to 3.3 V or 5 V.
7	FS1	Input	Select pin for input frequency. See table above. Internal pull-up resistor.
8	SSON#	Input	Spread Spectrum Control. This pin enables spread spectrum when low. Internal pull-down resistor.

### **External Components**

The ICS180-52 requires a minimum number of external components for proper operation.

#### **Decoupling Capacitor**

A decoupling capacitor of 0.01µF must be connected between VDD and GND on pins 6 and 3, as close to these pins as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

#### **Series Termination Resistor**

When the PCB trace between the clock output and the load is over 1 inch, series termination should be used. To series terminate a  $50\Omega trace$  (a commonly used trace impedance) place a  $33\Omega resistor$  in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is  $20\Omega$ 

value of these capacitors is given by the following equation:

#### **PCB Layout Recommendations**

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

- 1) The  $0.01\mu F$  decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via.
- 2) To minimize EMI, the  $33\Omega$  series termination resistor (if needed) should be placed close to the clock output.
- 3) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the ICS180-52. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

### **Absolute Maximum Ratings**

Stresses above the ratings listed below can cause permanent damage to the ICS180-52. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

### **Recommended Operation Conditions**

Parameter	Min.	Тур.	Max.	Units
Ambient Operating Temperature	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+3.135		+5.5	V

### **DC Electrical Characteristics**

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Units
Operating Voltage	VDD		3.135		3.465	V
Supply Current	IDD	No load		18	32	mA
Input High Voltage	V <sub>IH</sub>		2.4			V
Input Low Voltage	V <sub>IL</sub>				0.8	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4 mA	VDD-0.4			V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -15 mA	2.4			V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 15 mA			0.4	V
Input Capacitance	C <sub>IN</sub>			5	7	pF
Output Impedance	Rout			25		ohms
Input Pull-up Resistor				500		ΚΩ
Power-up Time		First locked clock cycle after steady power			5	ms

Unless stated otherwise, **VDD = 5 V, ±10%**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Units
Operating Voltage	VDD		4.5	5	5.5	V
Supply Current	IDD	No load		30	50	mA
Input High Voltage	V <sub>IH</sub>		0.7VDD			V
Input Low Voltage	V <sub>IL</sub>				0.15VDD	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -24 mA	2.4			V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 24 mA			0.4	V
Output Impedance	Rout			20		ohms
Input Capacitance	C <sub>IN</sub>			5	7	pF
Input Pull-up Resistor				500		ΚΩ
Power-up Time		First locked clock cycle after steady power			5	ms

#### **AC Electrical Characteristics**

Unless stated otherwise, **VDD = 3.3 V±5% or 5 V±10%**, Ambient Temperature 0 to  $+70^{\circ}$  C, C<sub>L</sub>=15 pf

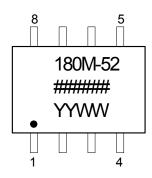
Parameter	Symbol	Conditions	Min.	Тур.	Max.	Units
Input/Output Clock Frequency			8		15	MHz
Input Clock Duty Cycle		Time above VDD/2	40		60	%
Output Clock Duty Cycle		Note 1	40	50	60	%
Output Rise Time	t <sub>OR</sub>	0.8 to 2.4 V, note 1		2	5	ns
Output Fall Time	t <sub>OF</sub>	2.4 to 0.8 V, note 1		2	5	ns
Jitter		Cycle-to-cycle		250	300	ps

Note 1: Measured with 15 pF load

#### **Thermal Characteristics**

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Units
Thermal Resistance Junction to	$\theta_{JA}$	Still air		150		° C/W
Ambient	$\theta_{JA}$	1 m/s air flow		140		° C/W
	$\theta_{JA}$	3 m/s air flow		120		° C/W
Thermal Resistance Junction to Case	$\theta_{JC}$			40		° C/W

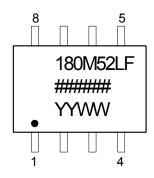
## **Marking Diagram**



#### Notes:

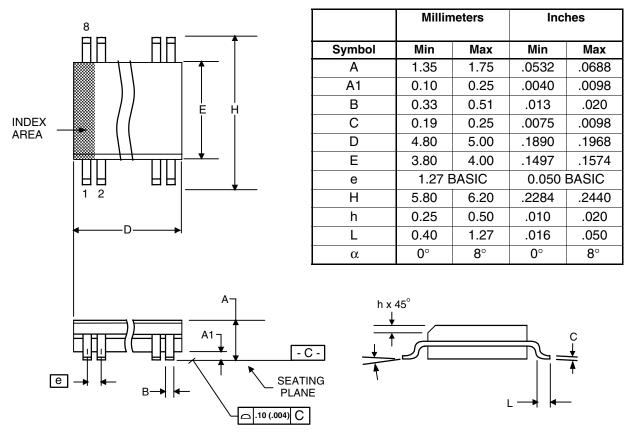
- 1. ##### is the lot number.
- 2. YYWW is the last two digits of the year and week that the part was assembled.
- 3. "LF" denotes Pb (lead) free package.
- 4. Bottom marking: country of origin.

# Marking Diagram (Pb free)



### Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



# **Ordering Information**

Part / Order Number	Marking	Shipping packaging	Package	Temperature
180M-52*		Tubes	8-pin SOIC	0 to +70° C
180M-52T*		Tape and Reel	8-pin SOIC	0 to +70° C
180M-52LF	see page 5	Tubes	8-pin SOIC	0 to +70° C
180M-52LFT		Tape and Reel	8-pin SOIC	0 to +70° C

\*NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01

"LF" denotes Pb free packaging.

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