

2N4391, 2N4392, 2N4393

N-Channel Silicon Junction Field-Effect Transistor

- Low On Resistance Analog Switches
- Choppers
- Commutators

Absolute maximum ratings at $T_A = 25^\circ\text{C}$

Reverse Gate Source & Reverse Gate Drain Voltage

– 40 V

Continuous Forward Gate Current

50 mA

Continuous Device Power Dissipation

1.8 W

Power Derating

12 mW/°C

At 25°C free air temperature
Static Electrical Characteristics

		2N4391		2N4392		2N4393		Process NJ132		
		Min	Max	Min	Max	Min	Max	Unit	Test Conditions	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 40		– 40		– 40		V	$I_G = -1\mu\text{A}$, $V_{DS} = \emptyset\text{V}$	
Gate Reverse Current	I_{GSS}		– 100		– 100		– 100	pA	$V_{GS} = -20\text{V}$, $V_{DS} = \emptyset\text{V}$	
			– 200		– 200		– 200	nA	$V_{GS} = -20\text{V}$, $V_{DS} = \emptyset\text{V}$	$T_A = 150^\circ\text{C}$
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 4	– 10	– 2	– 5	– 0.5	– 3	V	$V_{DS} = -20\text{V}$, $I_D = 1\text{nA}$	
Gate Source Forward Voltage	$V_{GS(F)}$		1		1		1	V	$I_G = 1\text{mA}$, $V_{DS} = \emptyset\text{V}$	
Drain Saturation Current (Pulsed)	I_{DSS}	50	150	25	75	5	30	mA	$V_{DS} = 20\text{V}$, $V_{GS} = \emptyset\text{V}$	
Drain Cutoff Current	$I_{D(OFF)}$						100	pA	$V_{DS} = 20\text{V}$, $V_{GS} = -5\text{V}$	
							200	nA	$V_{DS} = 20\text{V}$, $V_{GS} = -5\text{V}$	$T_A = 150^\circ\text{C}$
					100			pA	$V_{DS} = 20\text{V}$, $V_{GS} = -7\text{V}$	
					200			nA	$V_{DS} = 20\text{V}$, $V_{GS} = -7\text{V}$	$T_A = 150^\circ\text{C}$
			100					pA	$V_{DS} = 20\text{V}$, $V_{GS} = -12\text{V}$	
			200					nA	$V_{DS} = 20\text{V}$, $V_{GS} = -12\text{V}$	$T_A = 150^\circ\text{C}$
Drain Source ON Voltage	$V_{DS(ON)}$						0.4	V	$V_{GS} = \emptyset\text{V}$, $I_D = 3\text{mA}$	
					0.4			V	$V_{GS} = \emptyset\text{V}$, $I_D = 6\text{mA}$	
			0.4					V	$V_{GS} = \emptyset\text{V}$, $I_D = 12\text{mA}$	
Static Drain Source ON Resistance	$r_{DS(ON)}$		30		60		100	Ω	$V_{GS} = \emptyset\text{V}$, $I_D = 1\text{mA}$	

Dynamic Electrical Characteristics

Drain Source ON Resistance	$r_{ds(on)}$		30		60		100	Ω	$V_{GS} = \emptyset\text{V}$, $I_D = \emptyset\text{A}$	$f = 1\text{kHz}$
Common Source Input Capacitance	C_{iss}		14		14		14	pF	$V_{DS} = 20\text{V}$, $V_{GS} = \emptyset\text{V}$	$f = 1\text{kHz}$
Common Source Reverse Transfer Capacitance	C_{rss}						3.5	pF	$V_{DS} = \emptyset\text{V}$, $V_{GS} = -5\text{V}$	$f = 1\text{kHz}$
					3.5			pF	$V_{DS} = \emptyset\text{V}$, $V_{GS} = -7\text{V}$	$f = 1\text{kHz}$
			3.5					pF	$V_{DS} = \emptyset\text{V}$, $V_{GS} = -12\text{V}$	$f = 1\text{kHz}$

Switching Characteristics

Turn ON Delay Time	$t_{d(on)}$		15		15		15	ns	$V_{DD} = 10\text{V}$, $V_{GS(ON)} = \emptyset\text{V}$ 2N4391 2N4392 2N4393 $I_{D(ON)}$ 12 6 3 mA $V_{GS(OFF)}$ – 12 – 7 – 5 V	
Rise Time	t_r		5		5		5	ns		
Turn OFF Delay Time	$t_{d(off)}$		20		35		50	ns		
Fall Time	t_f		15		20		30	ns		

TO-18 Package

See Section G for Outline Dimensions

Pin Configuration

1 Source, 2 Drain, 3 Gate & Case

Surface Mount

SMP4391, SMP4392, SMP4393



InterFET Corporation

1000 N. Shiloh Road, Garland, TX 75042

(972) 487-1287 FAX (972) 276-3375