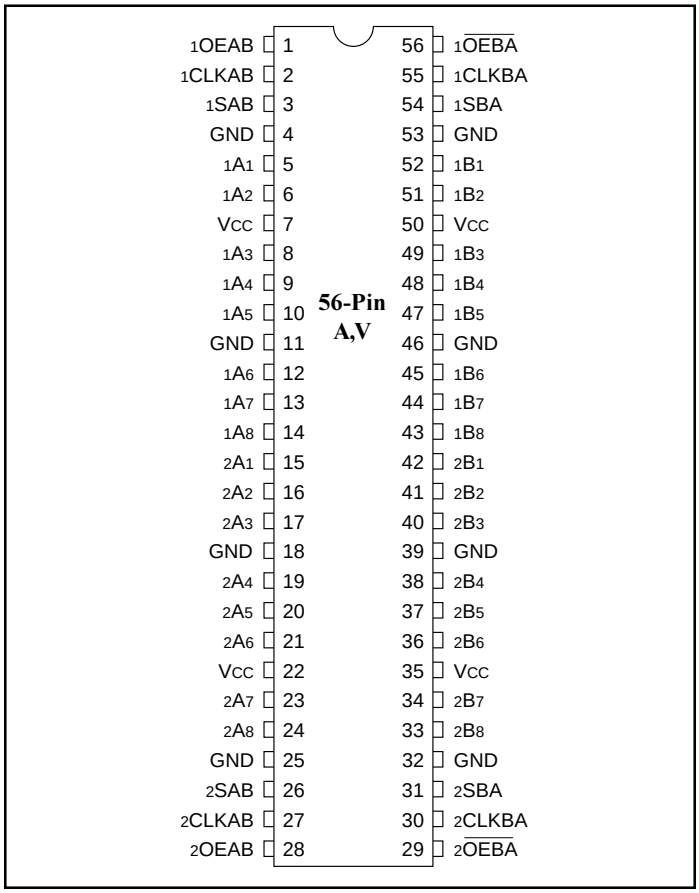
PI74ALVCH16652

16-Bit Bus Transceiver and Register with 3-State Outputs

Product Features

- PI74ALVCH16652 is designed for low voltage operation
- V_{CC} = 2.3V to 3.6V
- Hysteresis on all inputs
- Typical V_{OLP} (Output Ground Bounce)
  < 0.8V at V_{CC} = 3.3V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
  > 2.0V at V_{CC} = 3.3V, T_A = 25°C
- Bus Hold retains last active bus state during 3-State, eliminating the need for external pullup resistors
- Industrial operation at –40°C to +85°C
- Packages available:
  – 56-pin 240 mil wide plastic TSSOP (A)
  – 56-pin 300 mil wide plastic SSOP (V)

Product Pin Configuration



Product Description

Pericom Semiconductor's PI74ALVCH series of logic circuits are produced in the Company's advanced 0.5 micron CMOS technology, achieving industry leading speed.

The PI74ALVCH16652 is a 16-bit bus transceiver and register designed for low 2.3V to 3.6V Vcc operation. It consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

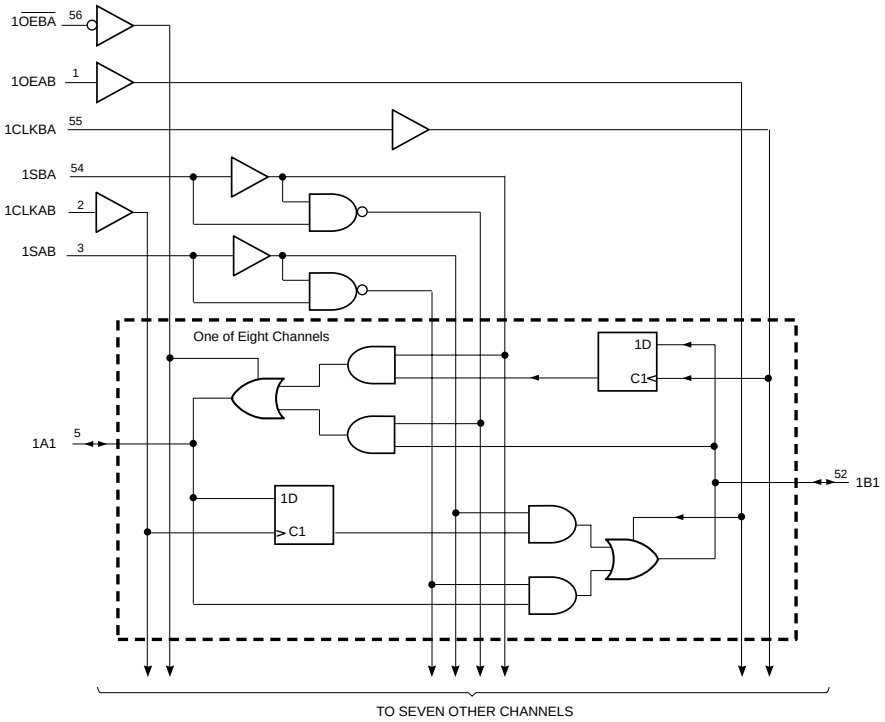
Complementary Output Enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select Control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. Circuitry used for Select Control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data.

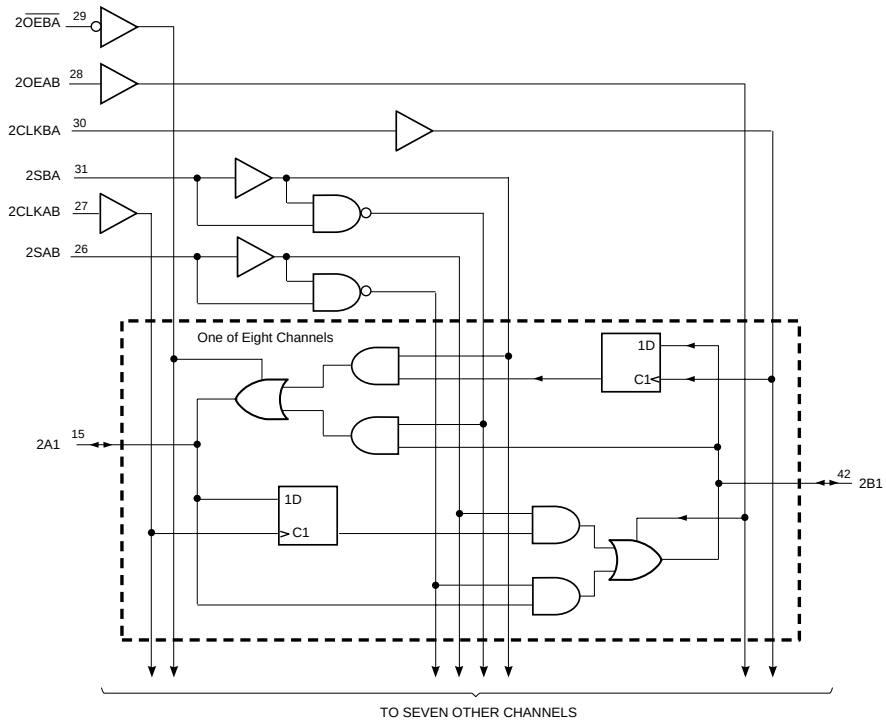
Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the levels on the Select Control or Output Enable inputs. When SAB and SBA are in the real-time transfer mode, it also is possible to store data without using the internal D-type flip-lops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are in the high-impedance state, each set of bus lines remains at its last level configuration.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{\text{OEBA}}$ should be tied to Vcc through a pull-up resistor and OEAB should be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sinking current sourcing capability of the driver.

Logic Block Diagrams





Product Pin Description

Pin Name	Description
OEAB	Output Enable Inputs (Active HIGH)
$\overline{OEBA}$	Output Enable Inputs (Active LOW)
xCLKAB, xCLKBA	Clock Pulse Inputs
xSAB, xSBA	Select Control Inputs
xAx	Data Register A Inputs, Data Register B Outputs
xBx	Data Register B Inputs, Data Register A Outputs
GND	Ground
VCC	Power

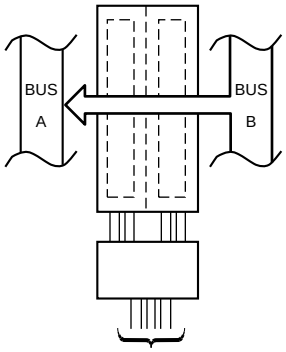
Truth Table(1)

Inputs						Data I/O*		Operation or Function
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1 - A8	B1 - B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified**	Store A, hold B
H	H	↑	↑	X**	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified**	Input	Hold A, store B
L	L	↑	↑	X	X**	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus & stored B data to A bus

Notes:

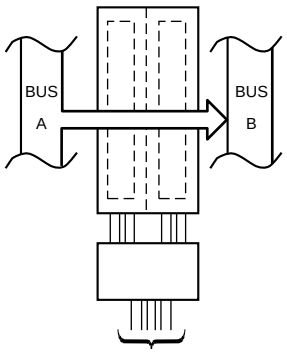
1. H = High Voltage Level, X = Don't Care,
   L = Low Voltage Level, ↑ = LOW-to-HIGH Transition
   * The data output functions may be enabled or disabled by a varietyof level combinations at the $\overline{OEAB}$ or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
   ** Select control = L; clocks can occur simultaneously. Select control = H; to load both registers, clocks must be staggered.

REAL-TIME TRANSFER
BUS B TO A



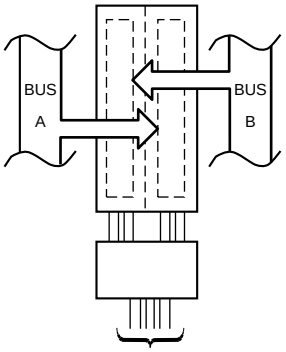
OEAB	$\overline{\text{OEBA}}$	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS A TO B



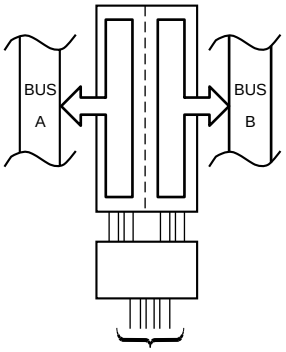
OEAB	$\overline{\text{OEBA}}$	xCLKAB	xCLKBA	xSAB	xSBA
H	H	X	X	L	X

STORAGE FROM
A AND/OR B



OEAB	$\overline{\text{OEBA}}$	xCLKAB	xCLKBA	xSAB	xSBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

TRANSFER STORED
DATA TO A AND/OR B



OEAB	$\overline{\text{OEBA}}$	xCLKAB	xCLKBA	xSAB	xSBA
H	L	H or L	H or L	H	X

Note:
1. Cannot transfer data to A bus and B bus simultaneously.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C
Ambient Temperature with Power Applied ..... –40°C to +85°C
Input Voltage Range, V_{IN} ..... –0.5V to V_{CC}+0.5V
Output Voltage Range, V_{OUT} ..... –0.5V to V_{CC}+0.5V
DC Input Voltage ..... –0.5V to +5.0V
DC Output Current 100mA
Power Dissipation 1.0W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 3.3V ±10%)

Parameters	Description	Test Conditions[1]	Min.	Typ.[2]	Max.	Units
V_{CC}	Supply Voltage		2.3		3.6	V
V_{IH}[3]	Input HIGH Voltage	V_{CC} = 2.3V to 2.7V	1.7			
		V_{CC} = 2.7V to 3.6V	2.0			
V_{IL}[3]	Input LOW Voltage	V_{CC} = 2.3V to 2.7V			0.7	
		V_{CC} = 2.7V to 3.6V			0.8	
V_{IN}[3]	Input Voltage		0		V_{CC}	
V_{OUT}[3]	Output Voltage		0		V_{CC}	
V_{OH}	Output HIGH Voltage	I_{OH} = -100µA, V_{CC} = Min. to Max.	V_{CC} –0.2			
		V_{IH} = 1.7V, I_{OH} = –6mA, V_{CC} = 2.3V	2.0			
		V_{IH} = 1.7V, I_{OH} = –12mA, V_{CC} = 2.3V	1.7			
		V_{IH} = 2.0V, I_{OH} = –12mA, V_{CC} = 2.7V	2.2			
		V_{IH} = 2.0V, I_{OH} = –12mA, V_{CC} = 3.0V	2.4			
		V_{IH} = 2.0V, I_{OH} = –24mA, V_{CC} = 3.0V	2.0			
V_{OL}	Output LOW Voltage	I_{OL} = 100µA, V_{IL} = Min. to Max.			0.2	
		V_{IL} = 0.7V, I_{OL} = 6mA, V_{CC} = 2.3V			0.4	
		V_{IL} = 0.7V, I_{OL} = 12mA, V_{CC} = 2.3V			0.7	
		V_{IL} = 0.8V, I_{OL} = 12mA, V_{CC} = 2.7V			0.4	
		V_{IL} = 0.8V, I_{OL} = 24mA, V_{CC} = 3.0V			0.55	
I_{OH}[3]	Output HIGH Current	V_{CC} = 2.3V			-12	mA
		V_{CC} = 2.7V			-12	
		V_{CC} = 3.0V			-24	
I_{OL}[3]	Output LOW Current	V_{CC} = 2.3V			12	
		V_{CC} = 2.7V			12	
		V_{CC} = 3.0V			24	

DC Electrical Characteristics-Continued (Over the Operating Range, $T_A = -40°C$ to $+85°C$, $V_{CC} = 3.3V \pm 10\%$)

Parameters	Description	Test Conditions[1]	Min.	Typ.[2]	Max.	Units
I_{IN}	Input Current	$V_{IN} = V_{CC}$ or GND, $V_{CC} = 3.6V$			±5	
I_{IN} (HOLD)	Input Hold Current	$V_{IN} = 0.7V$, $V_{CC} = 2.3V$	45			
		$V_{IN} = 1.7V$, $V_{CC} = 2.3V$	–45			
		$V_{IN} = 0.8V$, $V_{CC} = 3.0V$	75			
		$V_{IN} = 2.0V$, $V_{CC} = 3.0V$	–75			
		$V_{IN} = 0$ to $3.6V$, $V_{CC} = 3.6V$			±500	µA
I_{OZ}	Output Current (3-State Outputs)	$V_{OUT} = V_{CC}$ or GND, $V_{CC} = 3.6V$			±10	
I_{CC}	Supply Current	$V_{CC} = 3.6V$, $I_{OUT} = 0µA$, $V_{IN} =$ GND or V_{CC}			40	
ΔI_{CC}	Supply Current per Input @ TTL HIGH	$V_{CC} = 3.0V$ to $3.6V$, One Input at V_{CC} - 0.6V, Other Inputs at V_{CC} or GND			750	
C_I	Control Inputs	$V_{IN} = V_{CC}$ or GND, $V_{CC} = 3.3V$		3.5		pF
C_{IO}	A or B Ports	$V_O = V_{CC}$ or GND, $V_{CC} = 3.3V$		8.5		

Notes:
1. For Max or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 3.3V$, +25°C ambient and maximum loading.
3. Unused Control Inputs must be held HIGH or LOW to prevent them from floating.

Timing Requirements over Operating Range

Parameters	Description		Conditions	$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 2.7V$		$V_{CC} = 3.3V \pm 0.3V$		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
f_{CLOCK}	Clock Frequency		$C_L = 50pF$, $R_L = 500\Omega$	0	150	0	150	0	150	MHz
t_W	Pulse Duration	CLKAB or CLKBA HIGH or LOW						2.5		ns
t_{SU}	Setup Time	A before CLKAB↑ or B before CLKBA↑						0.9		
t_H	Hold Time	A after CLKAB↑ or B after CLKBA↑						0.9		

Note:
1. Unused control inputs must be held HIGH or LOW to prevent them from floating.

Switching Characteristics over Operating Range[1]

Parameters	From (INPUT)	To (OUTPUT)	Conditions	V_{CC} = 2.7V		V_{CC} = 3.3V ± 0.3V		Units
				Min.	Max.	Min.[2]	Max.	
f_{MAX}			C_L = 50pF R_L = 500Ω	150		150		MHz
t_{PD}	A or B	B or A			5.7	1.4	5.2	ns
	CLKAB or CLKBA	A or B			7.3	2.4	6.6	
	SAB or SBA	B to A			7.4	1.9	6.7	
t_{EN}	$\overline{OE}$ or OE	A or B			5.0	1.6	4.5	
t_{DIS}	$\overline{OE}$ or OE	A or B			5.3	1.2	4.8	
	Description							
$\Delta t/\Delta v$[3]	Input transition Rise or Fall			0	10	0	10	ns/V

Notes:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

Operating Characteristics, T_A = 25°C

Parameter		Test Conditions	V_{CC} = 2.5V ± 0.2V	V_{CC} = 3.3V ± 0.3V	Units
			Typical		
C_{PD} Power Dissipation Capacitance	Outputs Enabled	C_L = 50pF f = 10 MHz			pF
	Outputs Disabled				