M5M467405/465405DJ,DTP -5,-6,-5S,-6S
M5M467805/465805DJ,DTP -5,-6,-5S,-6S
M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

PRELIMINARY **Some of contents are subject to change without notice.**

DESCRIPTION

The M5M467405/465405DJ,DTP is a 16777216-word by 4-bit, M5M467805/465805DJ,DTP is a 8388608-word by 8-bit, and M5M465165DJ,DTP is a 4194304-word by 16-bit dynamic RAMs, fabricated with the high performance CMOS process, and are suitable for large-capacity memory systems with high speed and low power dissipation.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M467405DXX-5,5S M5M467805DXX-5,5S	50	13	25	13	84	300
M5M467405DXX-6,6S M5M467805DXX-6,6S	60	15	30	15	104	250
M5M465405DXX-5,5S M5M465805DXX-5,5S	50	13	25	13	84	390
M5M465405DXX-6,6S M5M465805DXX-6,6S	60	15	30	15	104	325

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M465165DXX-5,5S	50	13	25	13	84	420
M5M465165DXX-6,6S	60	15	30	15	104	390

XX=J,TP

- Standard 32 pin SOJ, 32 pin TSOP (M5M467405Dxx/M5M465405Dxx/M5M467805Dxx/M5M465805Dxx)
  Standard 50 pin SOJ, 50 pin TSOP (M5M465165Dxx)
- Single 3.3 ± 0.3V supply
- Low stand-by power dissipation
  1.8mW (Max) - - - - - - - - - - - - - LVCMOS input level
- Low operating power dissipation
  M5M467405Dxx-5,5S / M5M467805Dxx-5,5S - - - - - - - - - - - - 360.0mW (Max)
  M5M467405Dxx-6,6S / M5M467805Dxx-6,6S - - - - - - - - - - - - 324.0mW (Max)
  M5M465405Dxx-5,5S / M5M465805Dxx-5,5S - - - - - - - - - - - - 468.0mW (Max)
  M5M465405Dxx-6,6S / M5M465805Dxx-6,6S - - - - - - - - - - - - 432.0mW (Max)
  M5M465165Dxx-5,5S - 504.0mW (Max)
  M5M465165Dxx-6,6S - 468.0mW (Max)
- Self refresh capability*
  Self refresh current - - - - - - - - - - - - - 400µA (Max)
- EDO mode , Read-modify-write, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode , $\overline{OE}$ and $\overline{W}$ to control output buffer impedance
- All inputs, outputs LVTTL compatible and low capacitance

*:Applicable to self refresh version(M5M467405/465405/467805/465805/465165DJ,DTP-5S,-6S:option) only

ADDRESS

Part No.	Row Add.	Col. Add.	Refresh	Refresh Cycle	
				Normal	S-version
M5M467405Dxx	A0-A12	A0-A10	$\overline{RAS}$ Only Ref,Normal R/W	8192/64ms	8192/128ms
			CBR Ref,Hidden Ref	4096/64ms	4096/128ms
M5M465405Dxx	A0-A11	A0-A11	$\overline{RAS}$ Only Ref,Normal R/W CBR Ref,Hidden Ref	4096/64ms	4096/128ms
M5M467805Dxx	A0-A12	A0-A9	$\overline{RAS}$ Only Ref,Normal R/W	8192/64ms	8192/128ms
			CBR Ref,Hidden Ref	4096/64ms	4096/128ms
M5M465805Dxx	A0-A11	A0-A10	$\overline{RAS}$ Only Ref,Normal R/W CBR Ref,Hidden Ref	4096/64ms	4096/128ms
M5M465165Dxx	A0-A11	A0-A9	$\overline{RAS}$ Only Ref,Normal R/W CBR Ref,Hidden Ref	4096/64ms	4096/128ms

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

M5M467405/465405DJ,DTP -5,-6,-5S,-6S
M5M467805/465805DJ,DTP -5,-6,-5S,-6S
M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

PIN DESCRIPTION

M5M467405Dxx / M5M465405Dxx

Pin Name	Function
A_0-A_{12}	Address Inputs
DQ1-DQ4	Data Inputs / Outputs
$\overline{RAS}$	Row Address Strobe Input
$\overline{CAS}$	Column Address Strobe Input
$\overline{W}$	Write Control Input
$\overline{OE}$	Output Enable Input
Vcc	Power Supply (+3.3V)
Vss	Ground (0V)
NC	No Connection

M5M467805Dxx / M5M465805Dxx

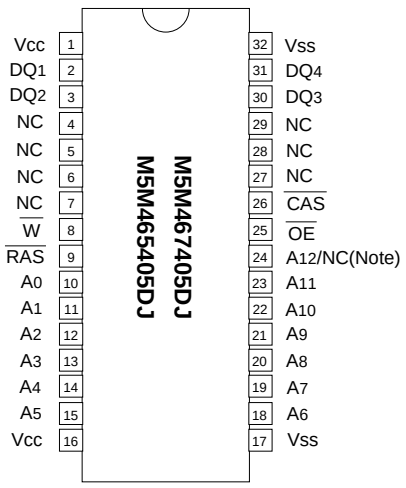
Pin Name	Function
A_0-A_{12}	Address Inputs
DQ1-DQ8	Data Inputs / Outputs
$\overline{RAS}$	Row Address Strobe Input
$\overline{CAS}$	Column Address Strobe Input
$\overline{W}$	Write Control Input
$\overline{OE}$	Output Enable Input
Vcc	Power Supply (+3.3V)
Vss	Ground (0V)
NC	No Connection

M5M465165Dxx

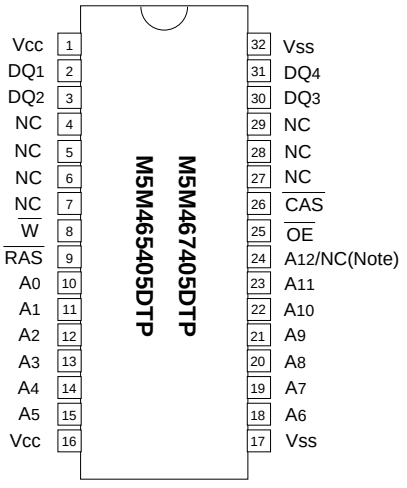
Pin Name	Function
A_0-A_{11}	Address Inputs
DQ1-DQ16	Data Inputs / Outputs
$\overline{RAS}$	Row Address Strobe Input
$\overline{UCAS}$	Upper byte control Column Address Strobe Input
$\overline{LCAS}$	Lower byte control Column Address Strobe Input
$\overline{W}$	Write Control Input
$\overline{OE}$	Output Enable Input
Vcc	Power Supply (+3.3V)
Vss	Ground (0V)
NC	No Connection

XX=J, TP

M5M467400/465400DJ, DTP PIN CONFIGURATION (TOP VIEW)



Outline 32P0N (400mil SOJ)



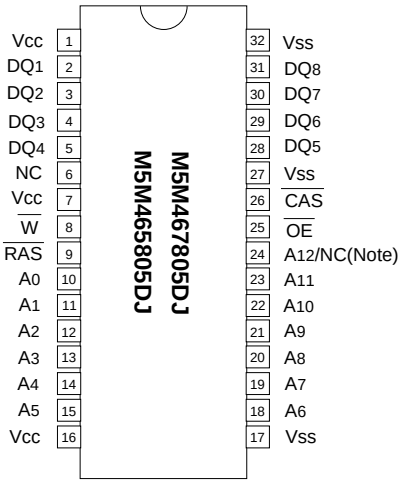
Outline 32P3N (400mil TSOP Normal Bend)

Note : A12...M5M467405Dxx, NC...M5M465405Dxx
NC : NO CONNECTION

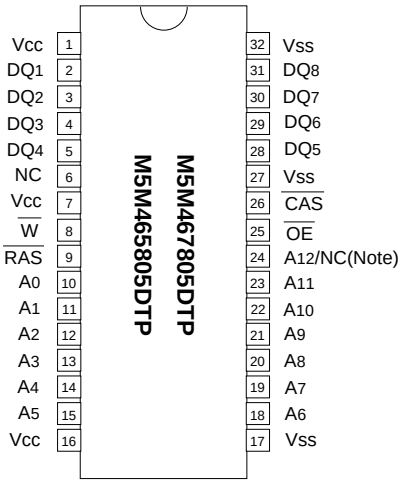
M5M467405/465405DJ,DTP -5,-6,-5S,-6S
M5M467805/465805DJ,DTP -5,-6,-5S,-6S
M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

M5M467805/465805DJ, DTP PIN CONFIGURATION (TOP VIEW)



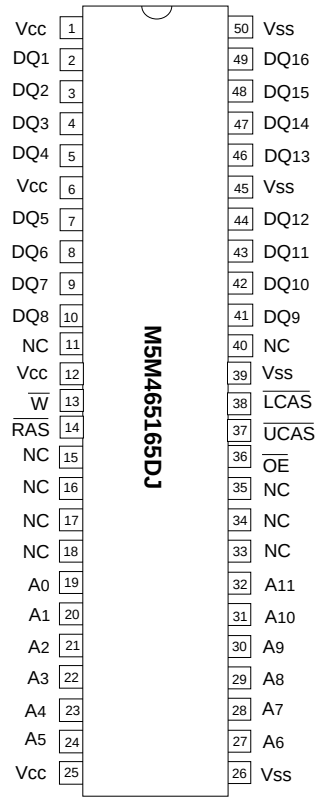
Outline 32P0N (400mil SOJ)



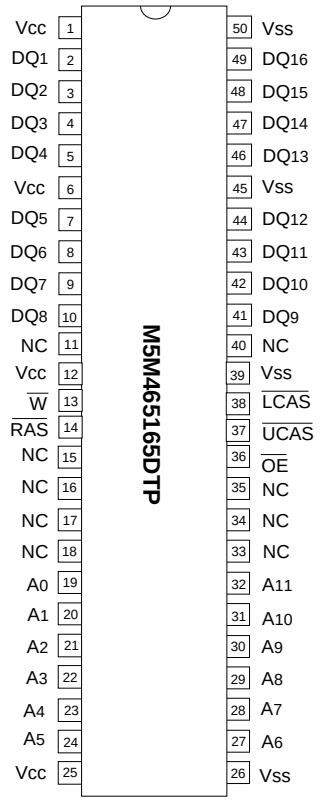
Outline 32P3N (400mil TSOP Normal Bend)

Note : A12...M5M467800Dxx, NC...M5M465800Dxx
NC : NO CONNECTION

M5M465165DJ, DTP PIN CONFIGURATION (TOP VIEW)



Outline 50P0G (400mil SOJ)



Outline 50P3G (400mil TSOP Normal Bend)

NC : NO CONNECTION

M5M467405/465405DJ,DTP -5,-6,-5S,-6S
M5M467805/465805DJ,DTP -5,-6,-5S,-6S
M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

FUNCTION

The M5M467405(805)/465405(805,165)DJ, DTP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., EDO mode, $\overline{CAS}$ before $\overline{RAS}$ refresh, and delayed-write.
The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

M5M467405Dxx / M5M465405Dxx / M5M467805Dxx / M5M465805Dxx

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	NO	EDO mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	NO	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	NO	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	NO	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	OPN	YES	
Hidden refresh	ACT	ACT	NAC	ACT	DNC	DNC	OPN	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

M5M465165Dxx

Operation	Inputs							Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	DQ1~DQ8	DQ9~DQ16		
Lower byte read	ACT	ACT	NAC	NAC	ACT	APD	APD	VLD	OPN	NO	EDO mode identical
Upper byte read	ACT	NAC	ACT	NAC	ACT	APD	APD	OPN	VLD	NO	
Word read	ACT	ACT	ACT	NAC	ACT	APD	APD	VLD	VLD	NO	
Lower byte write	ACT	ACT	NAC	ACT	NAC	APD	APD	DIN	DNC	NO	
Upper byte write	ACT	NAC	ACT	ACT	NAC	APD	APD	DNC	DIN	NO	
Word write	ACT	ACT	ACT	ACT	NAC	APD	APD	DIN	DIN	NO	
$\overline{RAS}$-only refresh	ACT	NAC	NAC	DNC	DNC	APD	DNC	OPN	OPN	YES	
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DNC	DNC	VLD	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	ACT	DNC	DNC	DNC	DNC	OPN	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : Invalid, APD : applied, OPN : open

M5M467405/465405DJ,DTP -5,-6,-5S,-6S
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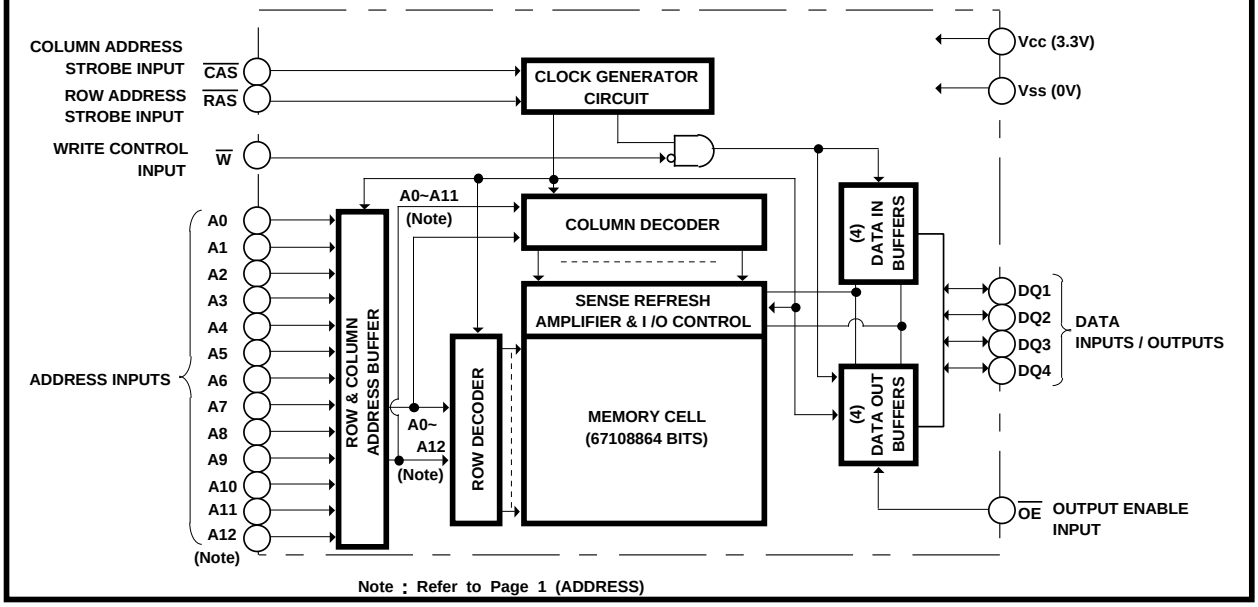
EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

M5M467405Dxx / M5M465405Dxx

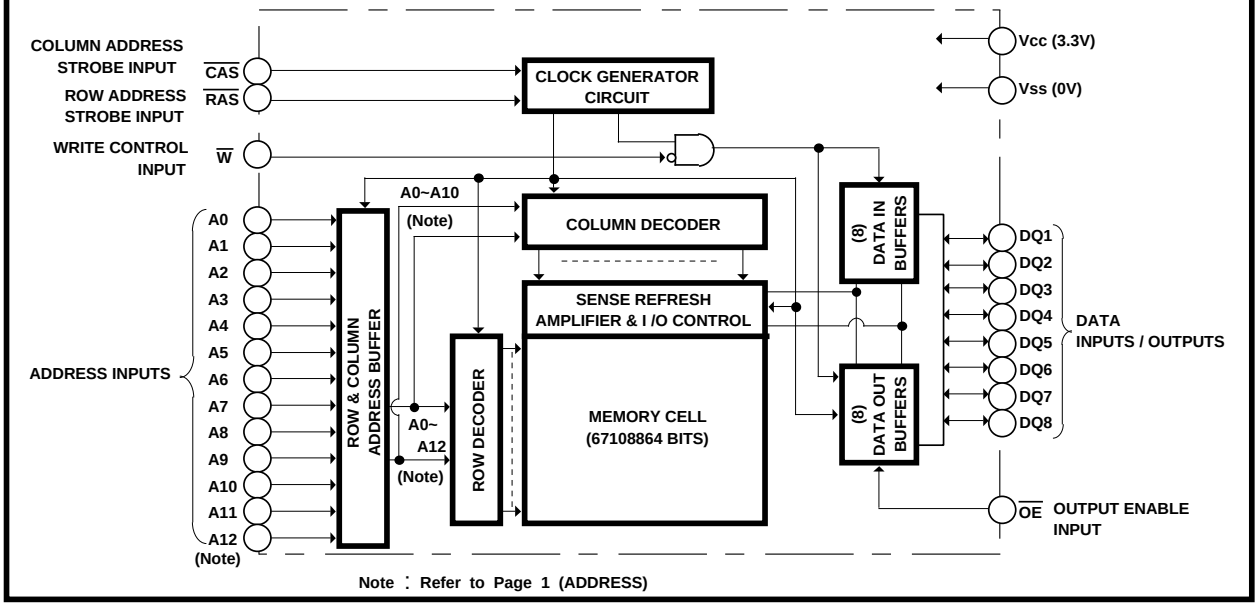
BLOCK DIAGRAM



Note : Refer to Page 1 (ADDRESS)

M5M467805Dxx / M5M465805Dxx

BLOCK DIAGRAM



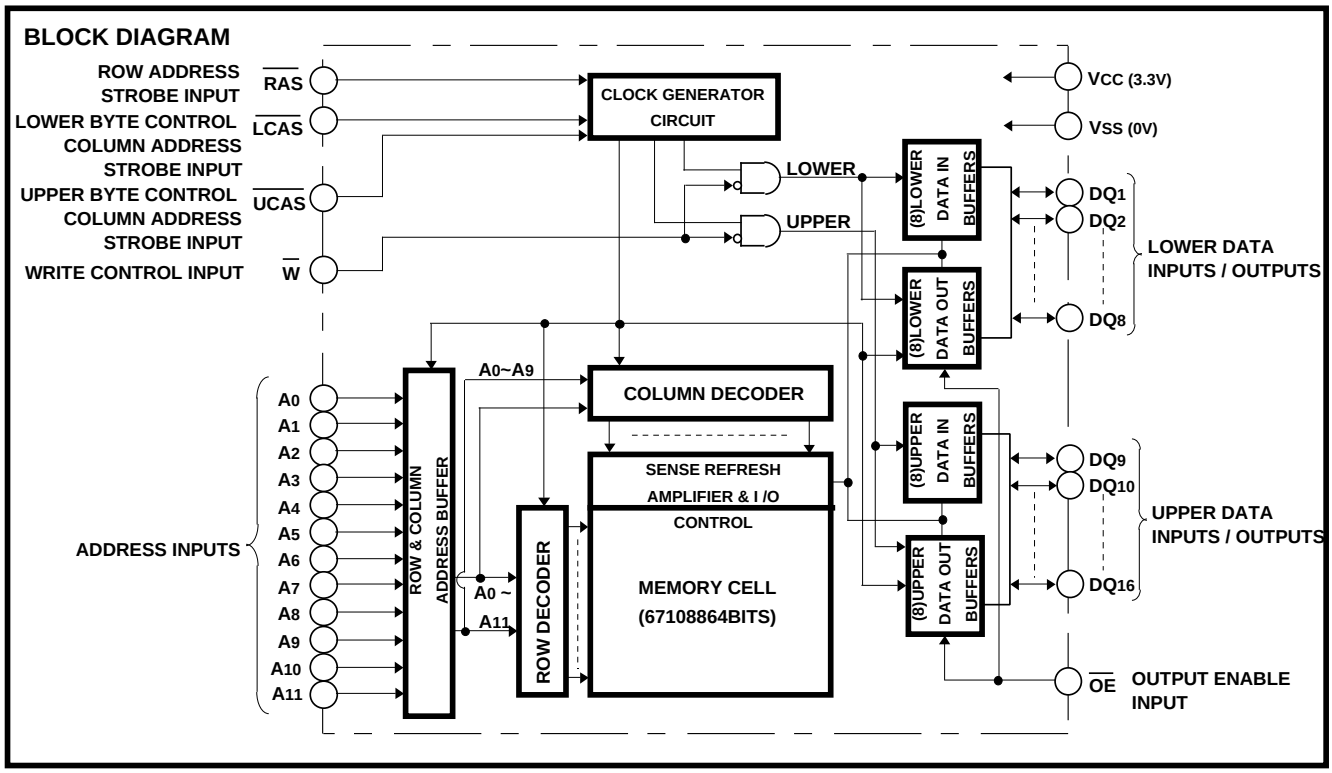
Note : Refer to Page 1 (ADDRESS)

M5M467405/465405DJ,DTP -5,-6,-5S,-6S
M5M467805/465805DJ,DTP -5,-6,-5S,-6S
M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

M5M465165Dxx

BLOCK DIAGRAM



M5M467405/465405DJ,DTP -5,-6,-5S,-6S
M5M467805/465805DJ,DTP -5,-6,-5S,-6S
M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	-0.5 ~ 4.6	V
VI	Input voltage		-0.5 ~ 4.6	V
V0	Output voltage		-0.5 ~ 4.6	V
I0	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0 ~ 70	°C
Tstg	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0 ~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	3.0	3.3	3.6	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.0		Vcc+0.3	V
V_{IL}	Low-level input voltage, all inputs	-0.3		0.8	V

Note 1 : All voltage values are with respect to Vss.

ELECTRICAL CHARACTERISTICS (Ta=0 ~70°C, Vcc=3.3 ± 0.3V, Vss=0V, unless otherwise noted) (Note 2)
[M5M467405D / M5M467805D]

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-2mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V ≤ V_{OUT} ≤ Vcc	-10		10	µA
I_I	Input current		0V≤VIN ≤ Vcc+0.3V, Other input pins=0V	-10		10	µA
I_{CC1} (AV)	Average supply current from Vcc operating (Note 3,4,5)	M5M467405D-5,5S M5M467805D-5,5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			100	mA
		M5M467405D-6,6S M5M467805D-6,6S				90	
I_{CC2} (AV)	Average supply current from Vcc stand-by (Note 6)	M5M467405D-5,5S -6,6S M5M467805D-5,5S -6,6S	$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			1	mA
		M5M467405D-5,6 M5M467805D-5,6	$\overline{RAS}$= $\overline{CAS}$ ≥Vcc -0.2V,output open			0.5	
		M5M467405D-5S,6S M5M467805D-5S,6S				0.3	
I_{CC4} (AV)	Average supply current from Vcc EDO-Mode (Note 3,4,5)	M5M467405D-5,5S M5M467805D-5,5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{HPC}=min. output open			100	mA
		M5M467405D-6,6S M5M467805D-6,6S				90	
I_{CC6} (AV)	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3,5)	M5M467405D-5,5S M5M467805D-5,5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			130	mA
		M5M467405D-6,6S M5M467805D-6,6S				120	

Note 2: Current flowing into an IC is positive, out is negative.
3: Icc1 (AV) , Icc4 (AV) and Icc6 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: Icc1 (AV) and Icc4 (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column Address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{CAS}$=V_{IH}.

M5M467405/465405DJ,DTP -5,-6,-5S,-6S
M5M467805/465805DJ,DTP -5,-6,-5S,-6S
M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
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EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

ELECTRICAL CHARACTERISTICS (Ta=0～70°C, Vcc=3.3± 0.3V, Vss=0V, unless otherwise noted) (Note 2)

[M5M465405D / M5M465805D]

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-2mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V ≤ V_{OUT} ≤ Vcc	-10		10	μA
I_I	Input current		0V≤V_{IN} ≤ Vcc+0.3V, Other input pins=0V	-10		10	μA
I_{CC1} (AV)	Average supply current from Vcc operating (Note 3,4,5)	M5M465405D-5,5S M5M465805D-5,5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			130	mA
		M5M465405D-6,6S M5M465805D-6,6S				120	
I_{CC2} (AV)	Average supply current from Vcc stand-by (Note 6)	M5M465405D-5,5S -6,6S M5M465805D-5,5S -6,6S	$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			1	mA
		M5M465405D-5,6 M5M465805D-5,6	$\overline{RAS}$= $\overline{CAS}$ ≥Vcc -0.2V,output open			0.5	
		M5M465405D-5S,6S M5M465805D-5S,6S				0.3	
I_{CC4} (AV)	Average supply current from Vcc EDO-Mode (Note 3,4,5)	M5M465405D-5,5S M5M465805D-5,5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{HPC}=min. output open			100	mA
		M5M465405D-6,6S M5M465805D-6,6S				90	
I_{CC6} (AV)	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3,5)	M5M465405D-5,5S M5M465805D-5,5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			130	mA
		M5M465405D-6,6S M5M465805D-6,6S				120	

[M5M465165D]

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-2mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≤ V_{OUT} ≤Vcc	-10		10	μA
I_I	Input current		0V ≤ V_{IN} ≤ Vcc+0.3V, Other input pins=0V	-10		10	μA
I_{CC1} (AV)	Average supply current from Vcc operating (Note 3,4,5)	M5M465165D-5,5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			140	mA
		M5M465165D-6,6S				130	
I_{CC2} (AV)	Average supply current from Vcc stand-by (Note 6)	M5M465165D-5,5S -6,6S	$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			1	mA
		M5M465165D-5,6	$\overline{RAS}$= $\overline{CAS}$ ≥Vcc -0.2V, output open			0.5	
		M5M465165D-5S,6S				0.3	
I_{CC4} (AV)	Average supply current from Vcc EDO-Mode (Note 3,4,5)	M5M465165D-5,5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{HPC}=min. output open			120	mA
		M5M465165D-6,6S				110	
I_{CC6} (AV)	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3,5)	M5M465165D-5,5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			140	mA
		M5M465165D-6,6S				130	

M5M467405/465405DJ,DTP -5,-6,-5S,-6S
M5M467805/465805DJ,DTP -5,-6,-5S,-6S
M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

CAPACITANCE (Ta=0～ 70°C, Vcc=3.3 ± 0.3V, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance,address inputs	V_I=Vss f=1MHz Vi=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				7	pF

SWITCHING CHARACTERISTICS (Ta=0 ~ 70°C, Vcc=3.3 ± 0.3V, Vss=0V, unless otherwise noted , see notes 6,14,15)

Symbol	Parameter		Limits				Unit
			M5M46X405D-5,5S M5M46X805D-5,5S M5M465165D-5,5S		M5M46X405D-6,6S M5M46X805D-6,6S M5M465165D-6,6S		
			Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7,8)		13		15	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7,9)		50		60	ns
t_{AA}	Column address access time	(Note 7,10)		25		30	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7,11)		28		33	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 7)		13		15	ns
t_{OHC}	Output hold time from $\overline{CAS}$		5		5		ns
t_{OHR}	Output hold time from $\overline{RAS}$	(Note 13)	5		5		ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 12)		13		15	ns
t_{WEZ}	Output disable time after $\overline{W}$ high	(Note 12)		13		15	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12,13)		13		15	ns
t_{REZ}	Output disable time after $\overline{RAS}$ high	(Note 12,13)		13		15	ns

Note 6: An initial pause of 500μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause. And any eight initialization cycles are required after prolonged periods (greater than 64 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to VOH=2.4V(IOH=-2mA) / VOL=0.4V(IOL=2mA) loads and 100pF. The reference levels for measuring of output signals are VOH=2.0V and VOL=0.8V.

8: Assumes that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$ and $t_{CP} \geq t_{CP(max)}$.

9: Assumes that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10: Assumes that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$.

11: Assumes that $t_{CP} \leq t_{CP(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

12: $t_{OEZ(max)}$, $t_{WEZ(max)}$, $t_{OFF(max)}$ and $t_{REZ(max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leq \pm 10$ μA) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

13: Output is disabled after both $\overline{RAS}$ and $\overline{CAS}$ go to high.

M5M467405/465405DJ,DTP -5,-6,-5S,-6S
M5M467805/465805DJ,DTP -5,-6,-5S,-6S
M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and EDO Mode Cycles)

(Ta=0 ~ 70°C, Vcc=3.3 ±0.3V, Vss=0V, unless otherwise noted See notes 14,15)

Symbol	Parameter	Limits				Unit
		M5M46X405D-5,5S M5M46X805D-5,5S M5M465165D-5,5S		M5M46X405D-6,6S M5M46X805D-6,6S M5M465165D-6,6S		
		Min	Max	Min	Max	
t_{REF}	Refresh cycle time		64		64	ms
t_{REF}	Refresh cycle time (S-version only)		128		128	ms
t_{RP}	$\overline{RAS}$ high pulse width	30		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (Note16)	14	37	14	45	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width	8		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low (Note17)	10	25	12	30	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low	0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low (Note18)	0	10	0	13	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low	8		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low	8		10		ns
t_{DZC}	Delay time, data to $\overline{CAS}$ low (Note19)	0		0		ns
t_{DZO}	Delay time, data to $\overline{OE}$ low (Note19)	0		0		ns
t_{RDD}	Delay time, $\overline{RAS}$ high to data (Note20)	13		15		ns
t_{CDD}	Delay time, $\overline{CAS}$ high to data (Note20)	13		15		ns
t_{ODD}	Delay time, $\overline{OE}$ high to data (Note20)	13		15		ns
t_{WED}	Delay time, $\overline{W}$ low to data (Note20)	13		15		ns
t_T	Transition time (Note21)	1	50	1	50	ns

Note 14: The timing requirements are assumed t_T =2ns.
15: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.
16: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled exclusively by t_{CAC} or t_{AA}.
17: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$, access time is controlled exclusively by t_{AA}.
18: $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}.
19: Either t_{DZC} or t_{DZO} must be satisfied.
20: Either t_{RDD} or t_{CDD} or t_{ODD} or t_{WED} must be satisfied.
21: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter	Limits				Unit
		M5M46X405D-5,5S M5M46X805D-5,5S M5M465165D-5,5S		M5M46X405D-6,6S M5M46X805D-6,6S M5M465165D-6,6S		
		Min	Max	Min	Max	
t_{RC}	Read cycle time	84		104		ns
t_{RAS}	$\overline{RAS}$ low pulse width	50	10000	60	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	8	10000	10	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	35		40		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		ns
t_{RCS}	Read Setup time before $\overline{CAS}$ low	0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (Note 22)	0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (Note 22)	0		0		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time	25		30		ns
t_{CAL}	Column address to $\overline{CAS}$ hold time	13		18		ns
t_{ORH}	$\overline{RAS}$ hold time after $\overline{OE}$ low	13		15		ns
t_{OCH}	$\overline{CAS}$ hold time after $\overline{OE}$ low	13		15		ns

Note 22: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits				Unit
		M5M46X405D-5,5S M5M46X805D-5,5S M5M465165D-5,5S		M5M46X405D-6,6S M5M46X805D-6,6S M5M465165D-6,6S		
		Min	Max	Min	Max	
t_{WC}	Write cycle time	84		104		ns
t_{RAS}	$\overline{RAS}$ low pulse width	50	10000	60	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	8	10000	10	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	35		40		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low (Note 24)	0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	8		10		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	8		10		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	8		10		ns
t_{WP}	Write pulse width	8		10		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	8		10		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits				Unit
		M5M46X405D-5,5S M5M46X805D-5,5S M5M465165D-5,5S		M5M46X405D-6,6S M5M46X805D-6,6S M5M465165D-6,6S		
		Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time (Note23)	109		133		ns
t_{RAS}	$\overline{RAS}$ low pulse width	75	10000	89	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	38	10000	44	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	70		82		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	38		44		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note24)	28		32		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note24)	65		77		ns
t_{AWD}	Delay time, address to $\overline{W}$ low (Note24)	40		47		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low	13		15		ns

Note 23: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+4t_T$.

24: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ and $t_{CPWD} \geq t_{CPWD(min)}$ (for EDO mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) is satisfied, the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

M5M467405/465405DJ,DTP -5,-6,-5S,-6S
M5M467805/465805DJ,DTP -5,-6,-5S,-6S
M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

EDO Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle, Read Write Mix Cycle, Hi-Z control by $\overline{OE}$ or $\overline{W}$) (Note 25)

Symbol	Parameter	Limits				Unit
		M5M46X405D-5,5S M5M46X805D-5,5S M5M465165D-5,5S		M5M46X405D-6,6S M5M46X805D-6,6S M5M465165D-6,6S		
		Min	Max	Min	Max	
t_{HPC}	EDO mode read/write cycle time	20		25		ns
t_{HPRWC}	EDO Mode read write / read modify write cycle time	55		66		ns
t_{DOH}	Output hold time from $\overline{CAS}$ low	5		5		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle (Note26)	65	100000	77	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note27)	8	13	10	16	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	28		33		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note24)	43		50		ns
t_{CHOL}	Hold time to maintain the data Hi-Z until CAS access	7		7		ns
t_{OEPE}	$\overline{OE}$ Pulse Width (Hi-Z control)	7		7		ns
t_{WPE}	$\overline{W}$ Pulse Width (Hi-Z control)	7		7		ns
t_{HCWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low after read	28		32		ns
t_{HAWD}	Delay time, Address to $\overline{W}$ low after read	40		47		ns
t_{HPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low after read	43		50		ns
t_{HCOD}	Delay time, $\overline{CAS}$ low to $\overline{OE}$ high after read	13		15		ns
t_{HAOD}	Delay time, Address to $\overline{OE}$ high after read	25		30		ns
t_{HPOD}	Delay time, $\overline{CAS}$ precharge to $\overline{OE}$ high after read	28		33		ns

Note 25: All previously specified timing requirements and switching characteristics are applicable to their respective EDO mode cycle.
26: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
27: $t_{CP(max)}$ is specified as a reference point only. If $t_{CP} \geq t_{CP(max)}$, access time is controlled exclusively by tCAC.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 28)

Symbol	Parameter	Limits				Unit
		M5M46X405D-5,5S M5M46X805D-5,5S M5M465165D-5,5S		M5M46X405D-6,6S M5M46X805D-6,6S M5M465165D-6,6S		
		Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		ns

Note 28: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

M5M467405/465405DJ,DTP -5,-6,-5S,-6S
M5M467805/465805DJ,DTP -5,-6,-5S,-6S
M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S / -6S . The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70°C, Vcc=3.3V ± 0.3V, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits Min	Limits Typ	Limits Max	Unit
$I_{CC8\ (AV)}$	Average supply current from Vcc Extended - Refresh cycle (note 5,6)	M5M46X405D-5S,6S M5M46X805D-5S,6S M5M465165D-5S,6S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling input high level ≧ Vcc-0.2V input low level ≦ 0.2V output = OPEN , tRC = 31.25µs tRAS = tRAS(min) ~ 300ns			500	µA
$I_{CC9\ (AV)}$	Average supply current from Vcc Self - Refresh cycle (note 6)	M5M46X405D-5S,6S M5M46X805D-5S,6S M5M465165D-5S,6S	$\overline{RAS}$ = $\overline{CAS}$ ≦ 0.2V output = OPEN			400	µA

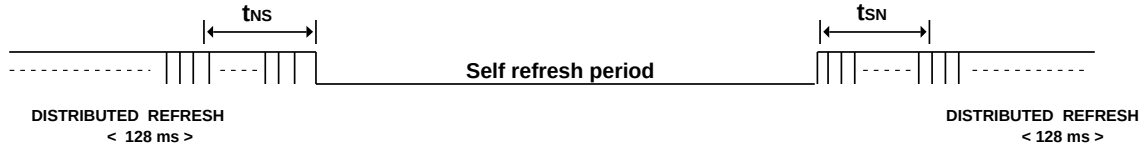
TIMING REQUIREMENTS (Ta=0 ~ 70°C, Vcc=3.3V ± 0.3V, Vss=0V, unless otherwise noted See notes 14,15)

Symbol	Parameter	Limits M5M46X405D-5S M5M46X805D-5S M5M465165D-5S Min	Limits Max	Limits M5M46X405D-6S M5M46X805D-6S M5M465165D-6S Min	Limits Max	Unit
t_{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		µs
t_{RPS}	Self Refresh $\overline{RAS}$ high precharge time	84		104		ns
t_{CHS}	Self Refresh $\overline{CAS}$ hold time	- 50		- 50		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

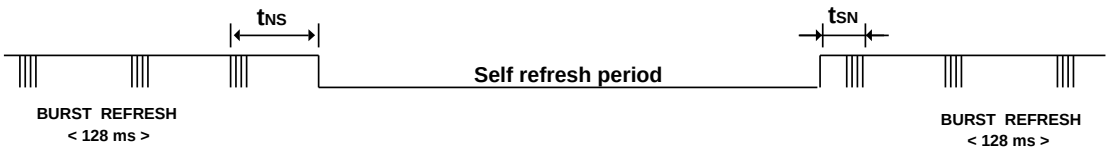
(1) In case of CBR distributed refresh

The last / first full refresh cycles must be made within tNS / tSN before / after self refresh , on the condition of tNS ≦ 128 ms and tSN ≦ 128 ms.



(2) In case of burst refresh

The last / first full refresh cycles must be made within tNS / tSN before / after self refresh , on the condition of tNS ≦ 16 ms and tSN ≦ 16 ms.



M5M467405/465405DJ,DTP -5,-6,-5S,-6S
M5M467805/465805DJ,DTP -5,-6,-5S,-6S
M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
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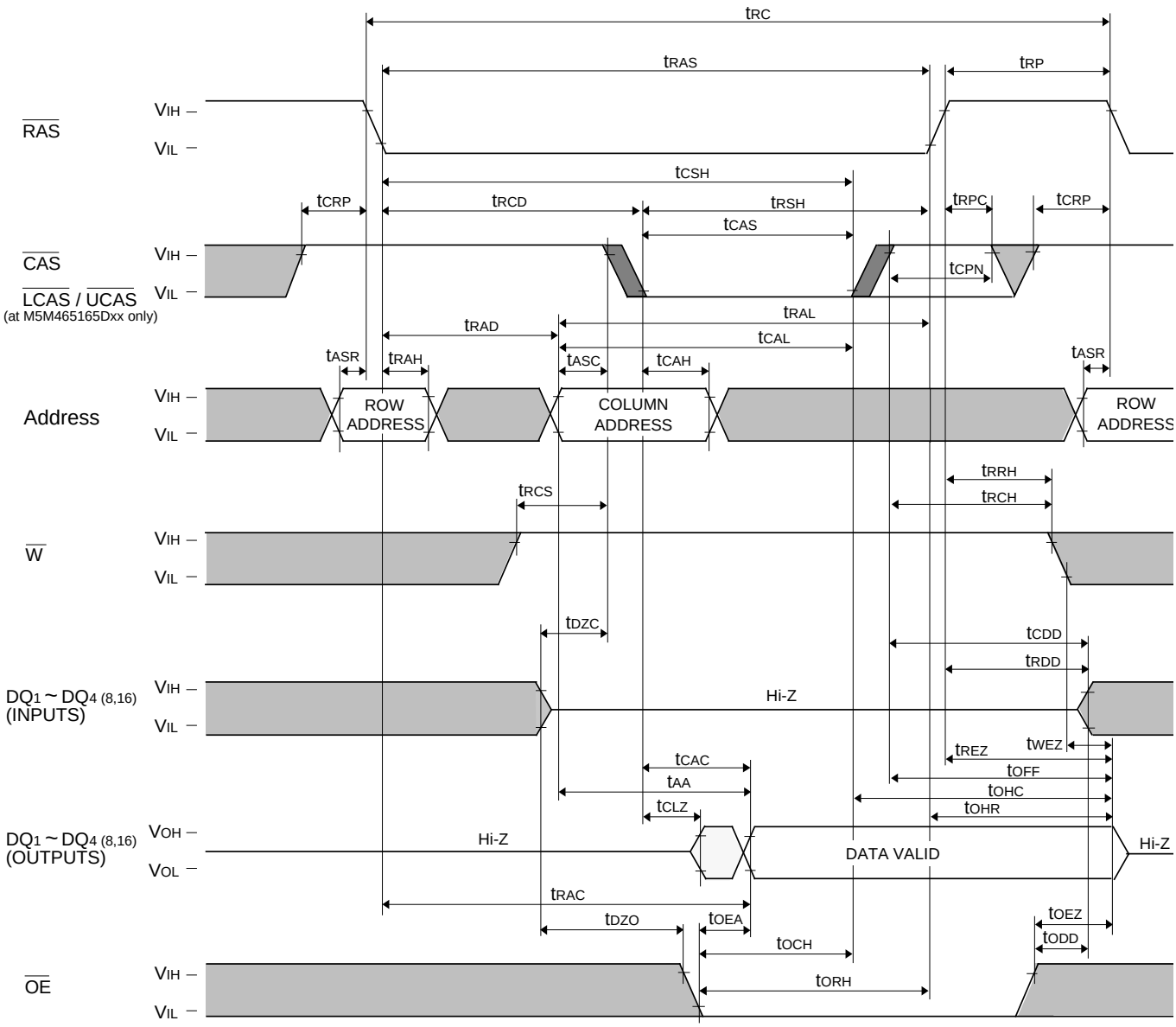
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

Timing Diagrams (Note 29)

Read Cycle



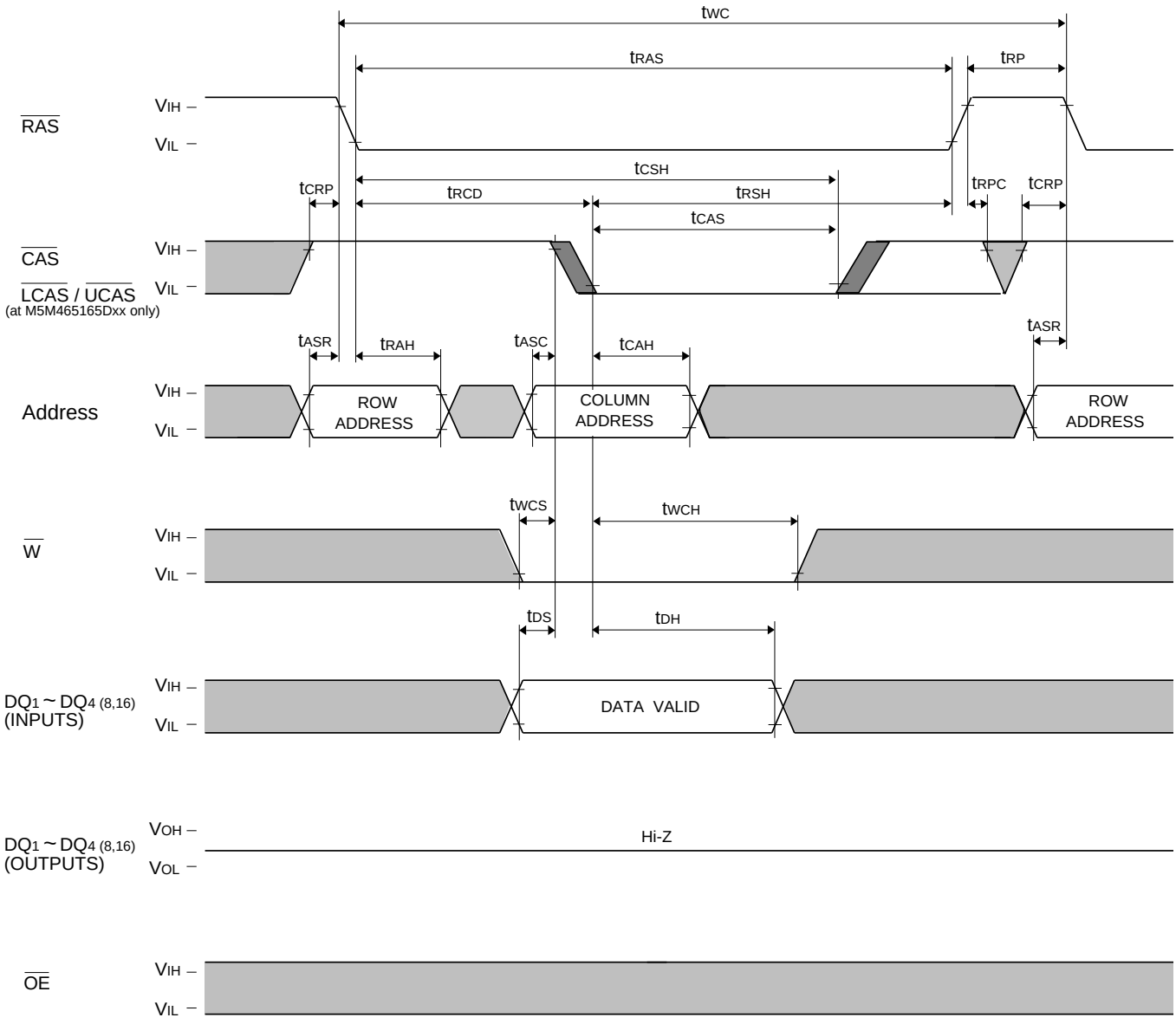
Note 29:

Indicates the don't care input.
$V_{IH}(min) \leq V_{IN} \leq V_{IH}(max)$ or $V_{IL}(min) \leq V_{IN} \leq V_{IL}(max)$

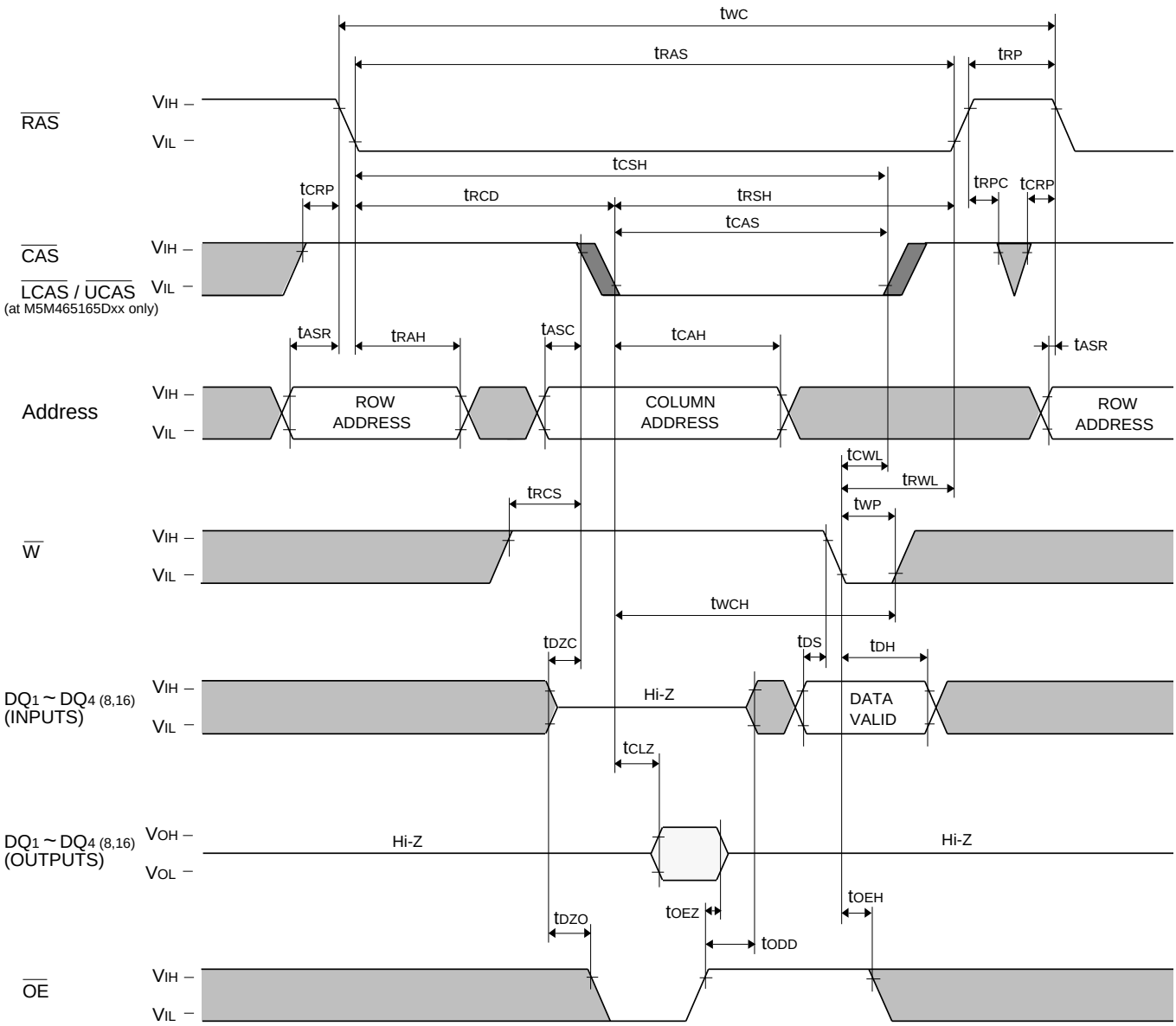
Indicates the invalid output.

Indicates the skew of the two inputs. (at M5M465165Dxx only)

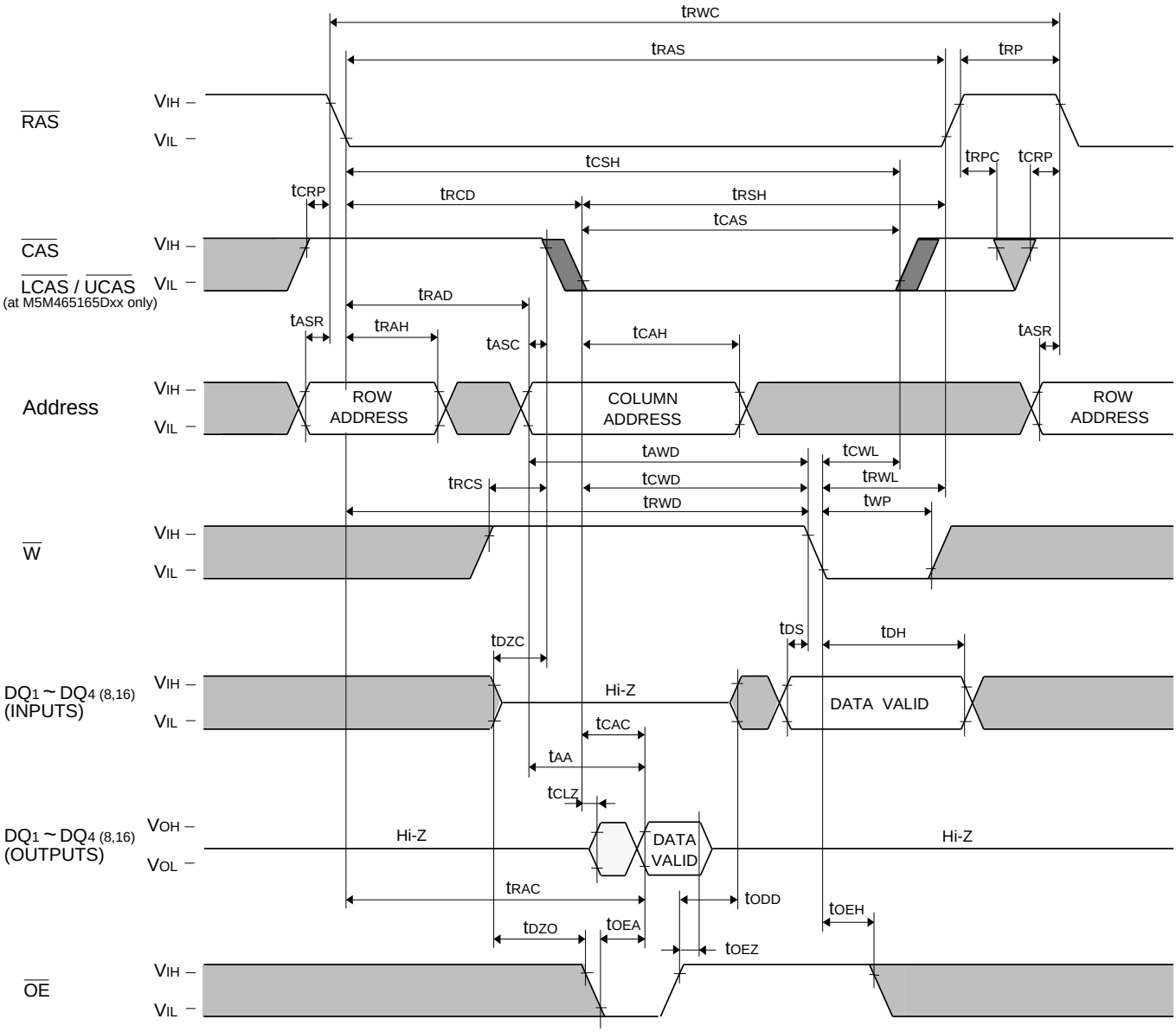
Write Cycle (Early Write)



Write Cycle (Delayed Write)



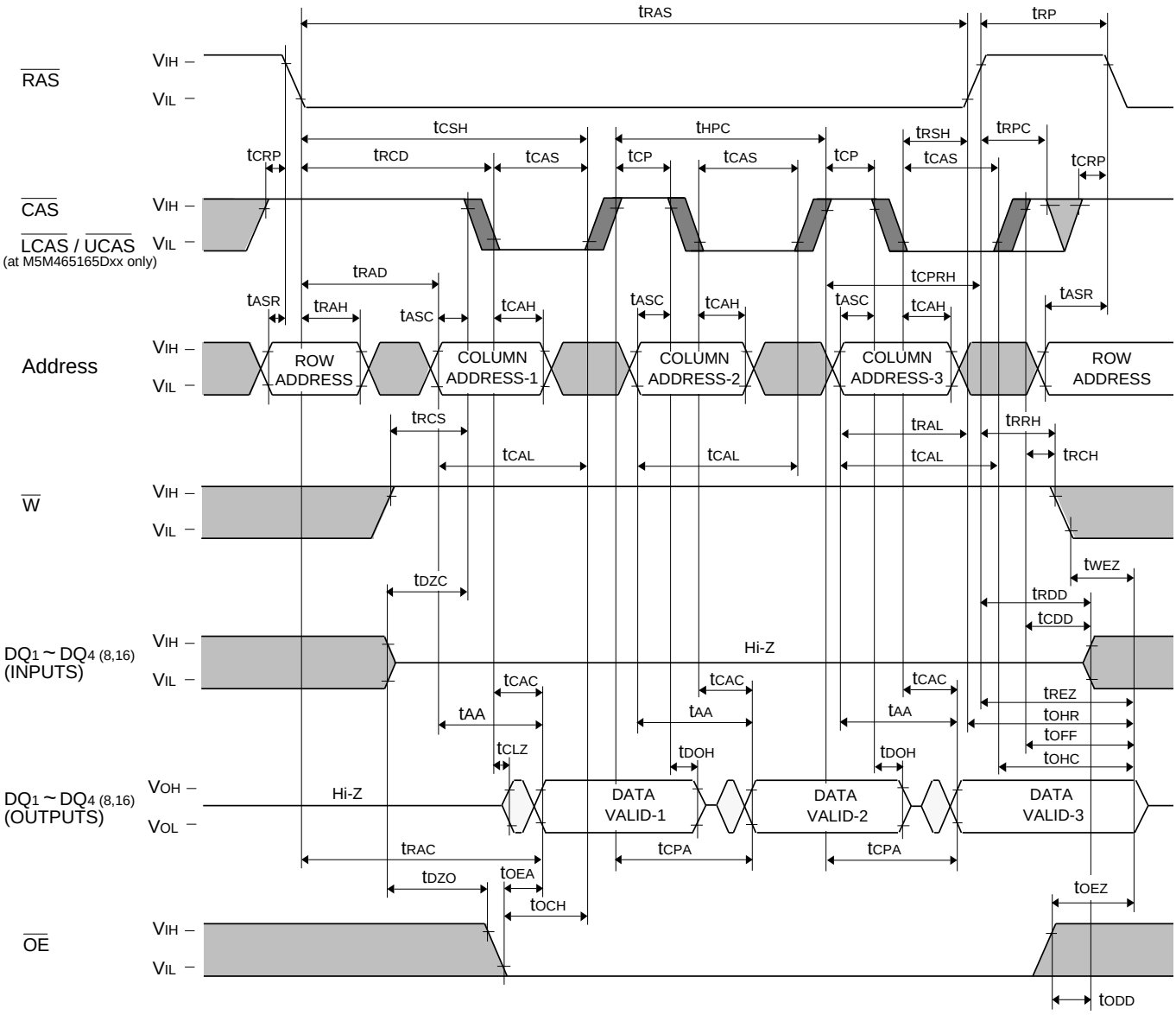
Read-Write, Read-Modify-Write Cycle



M5M467405/465405DJ,DTP -5,-6,-5S,-6S
M5M467805/465805DJ,DTP -5,-6,-5S,-6S
M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

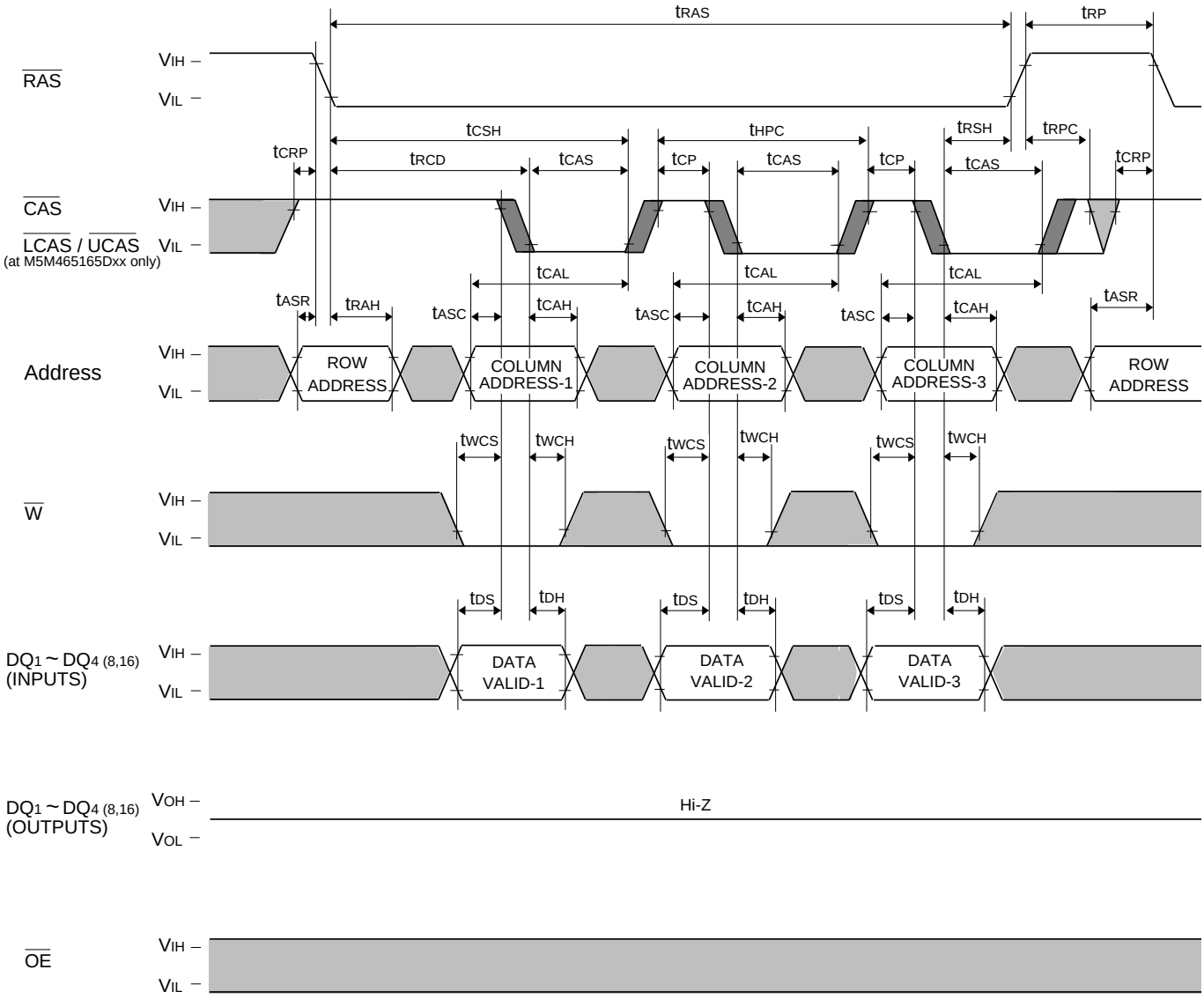
EDO Mode Read Cycle



M5M467405/465405DJ,DTP -5,-6,-5S,-6S
M5M467805/465805DJ,DTP -5,-6,-5S,-6S
M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

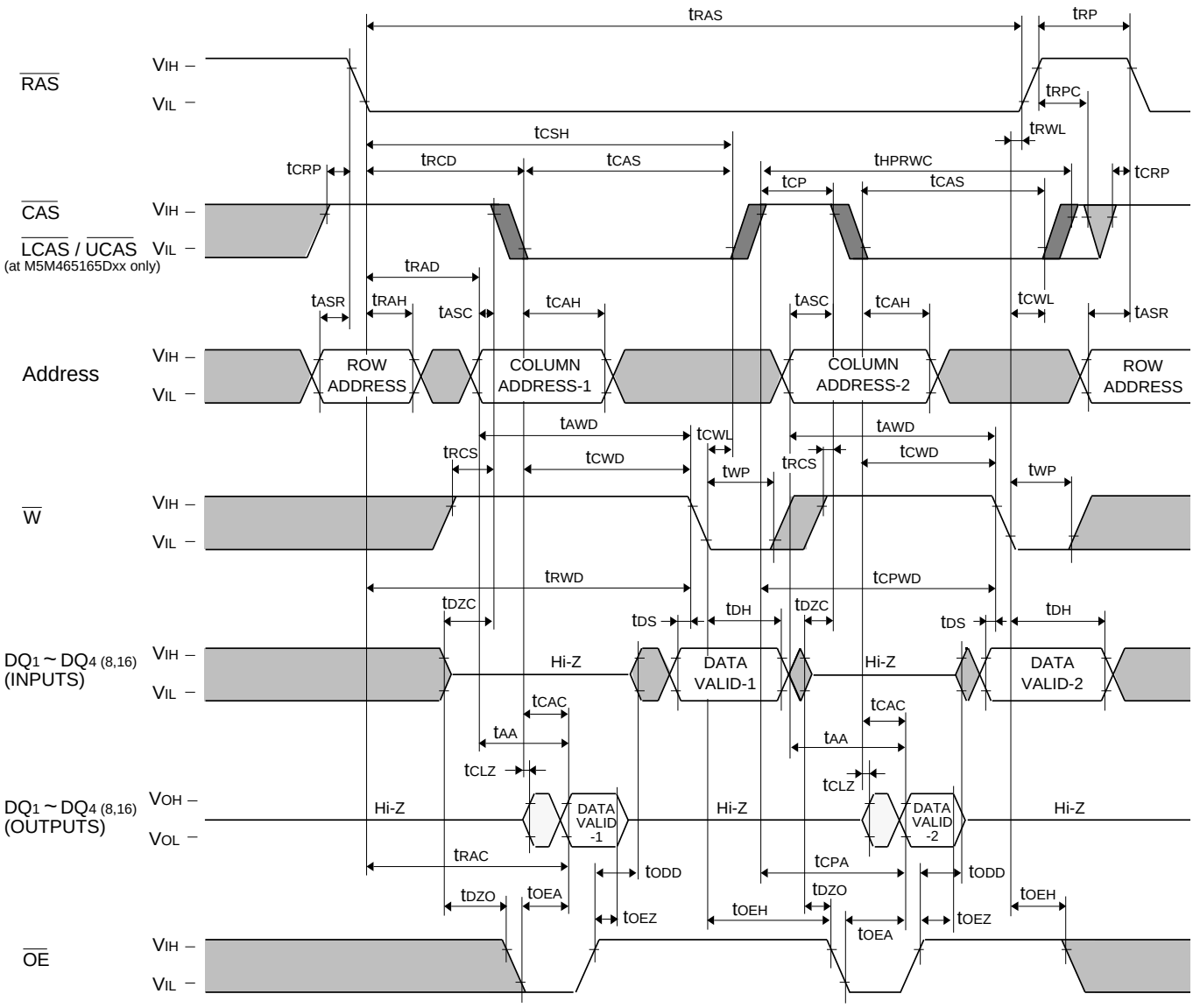
EDO Mode Write Cycle (Early Write)



M5M467405/465405DJ,DTP -5,-6,-5S,-6S
M5M467805/465805DJ,DTP -5,-6,-5S,-6S
M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

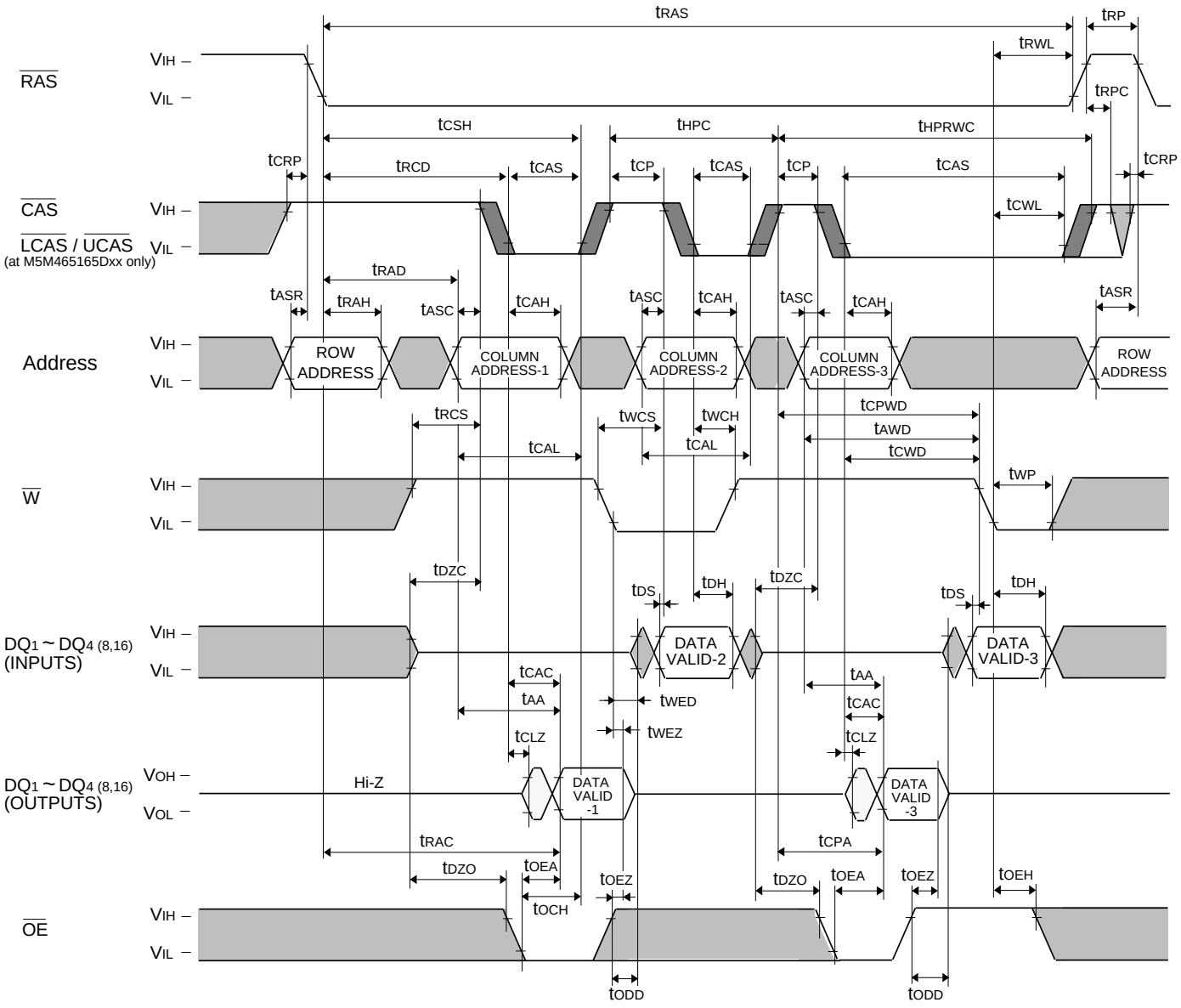
EDO Mode Read-Write, Read-Modify-Write Cycle



M5M467405/465405DJ,DTP -5,-6,-5S,-6S
M5M467805/465805DJ,DTP -5,-6,-5S,-6S
M5M465165DJ,DTP -5,-6,-5S,-6S

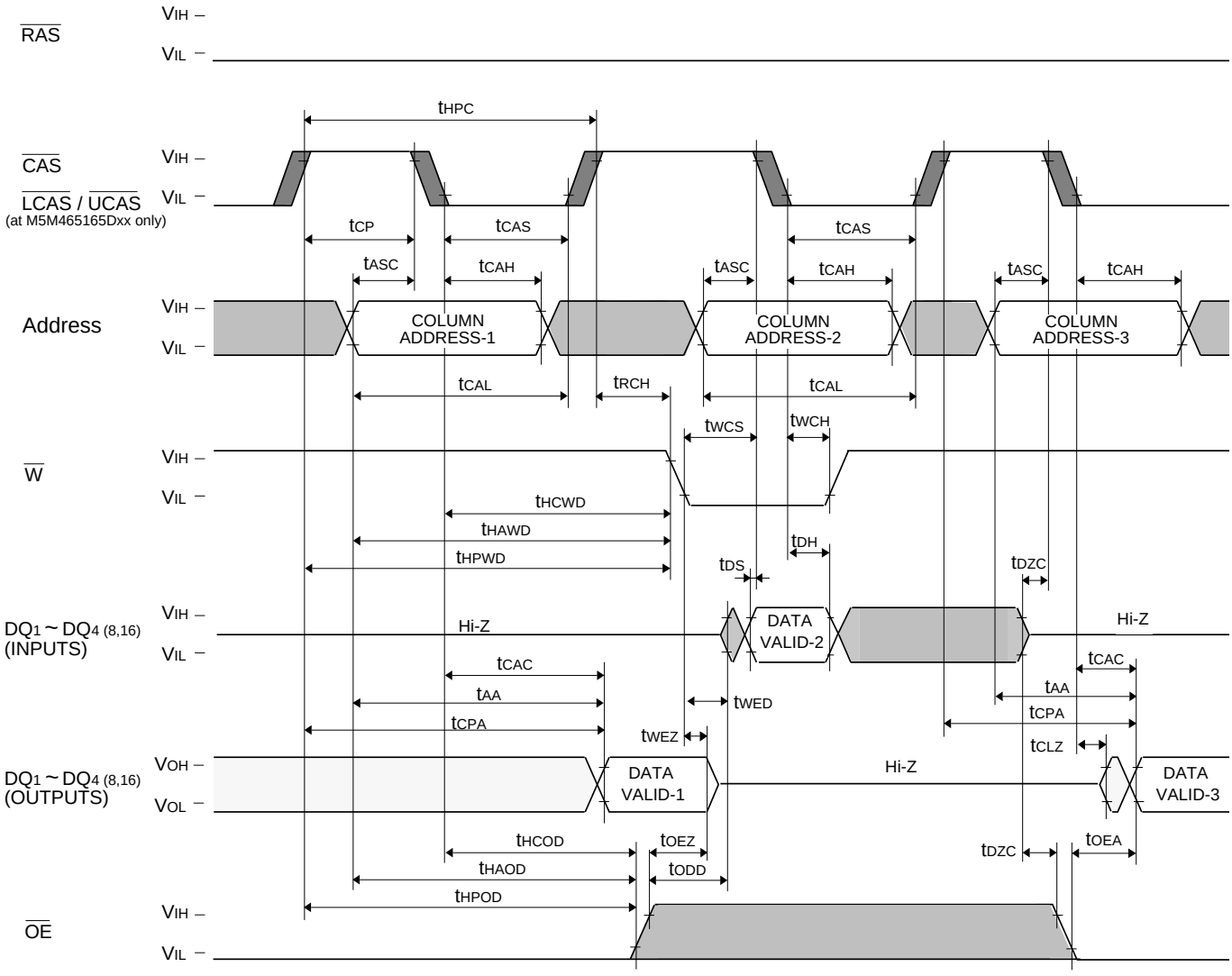
EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

EDO Mode Mix Cycle (1) (Note 30)



Note 30: $\overline{OE}$=L; $\overline{W}$ Hi-Z control
$\overline{OE}$=H; $\overline{OE}$ Hi-Z control

EDO Mode Mix Cycle (2) (Note 30)

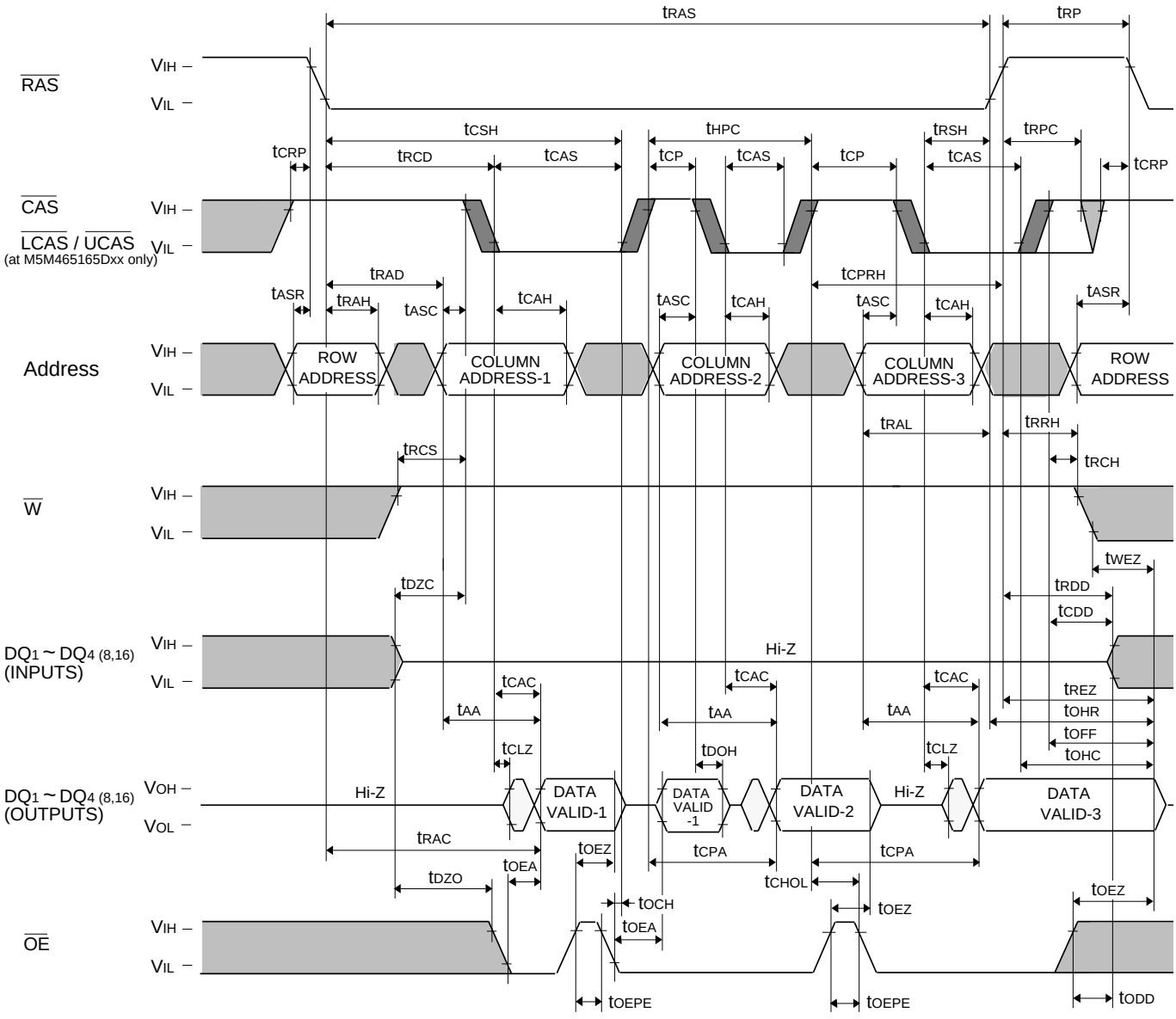


Note 30: $\overline{OE}$=L; $\overline{W}$ Hi-Z control
$\overline{OE}$=H; $\overline{OE}$ Hi-Z control

M5M467405/465405DJ,DTP -5,-6,-5S,-6S
M5M467805/465805DJ,DTP -5,-6,-5S,-6S
M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

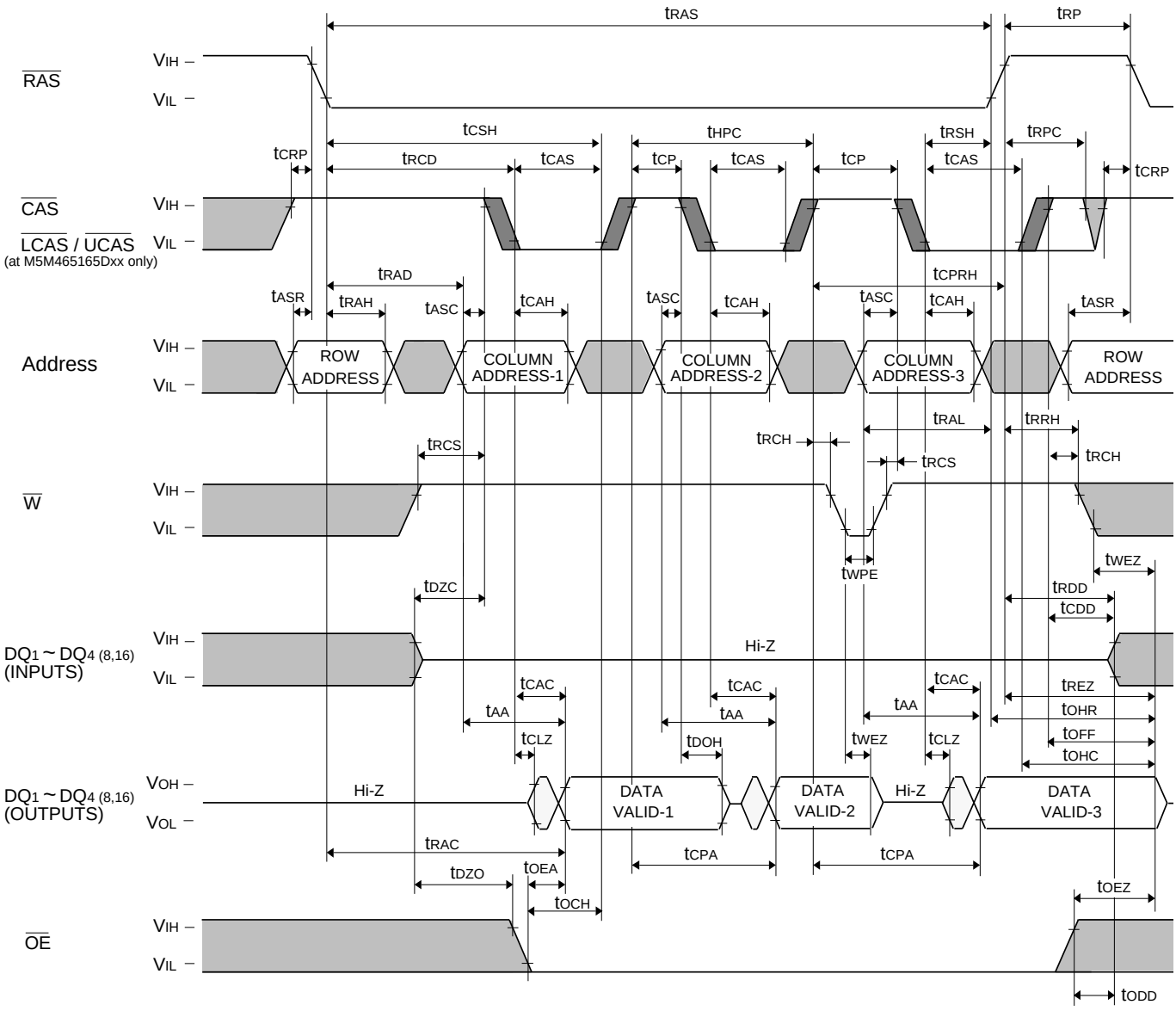
EDO Mode Read Cycle (Hi-Z control by $\overline{OE}$)



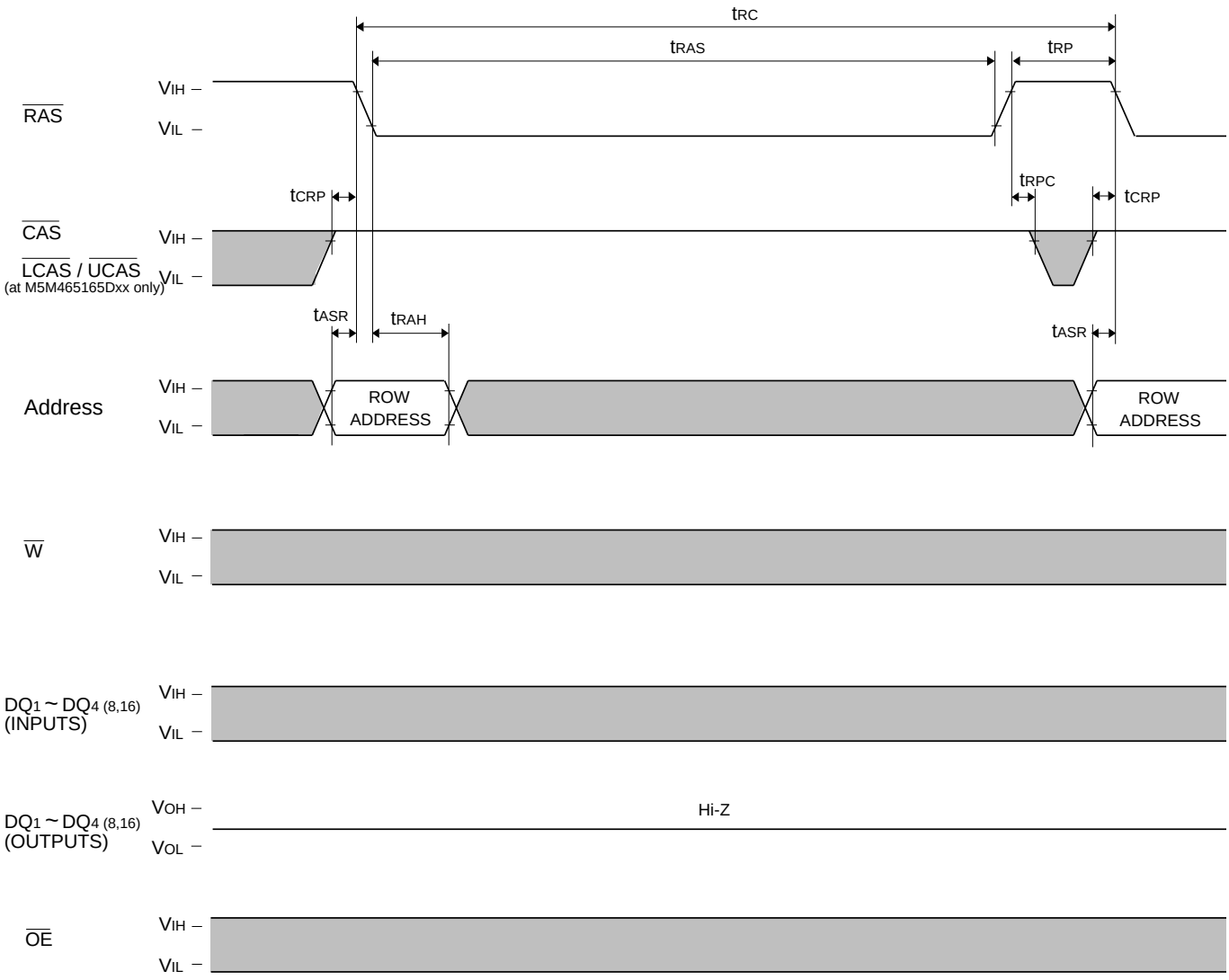
M5M467405/465405DJ,DTP -5,-6,-5S,-6S
M5M467805/465805DJ,DTP -5,-6,-5S,-6S
M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

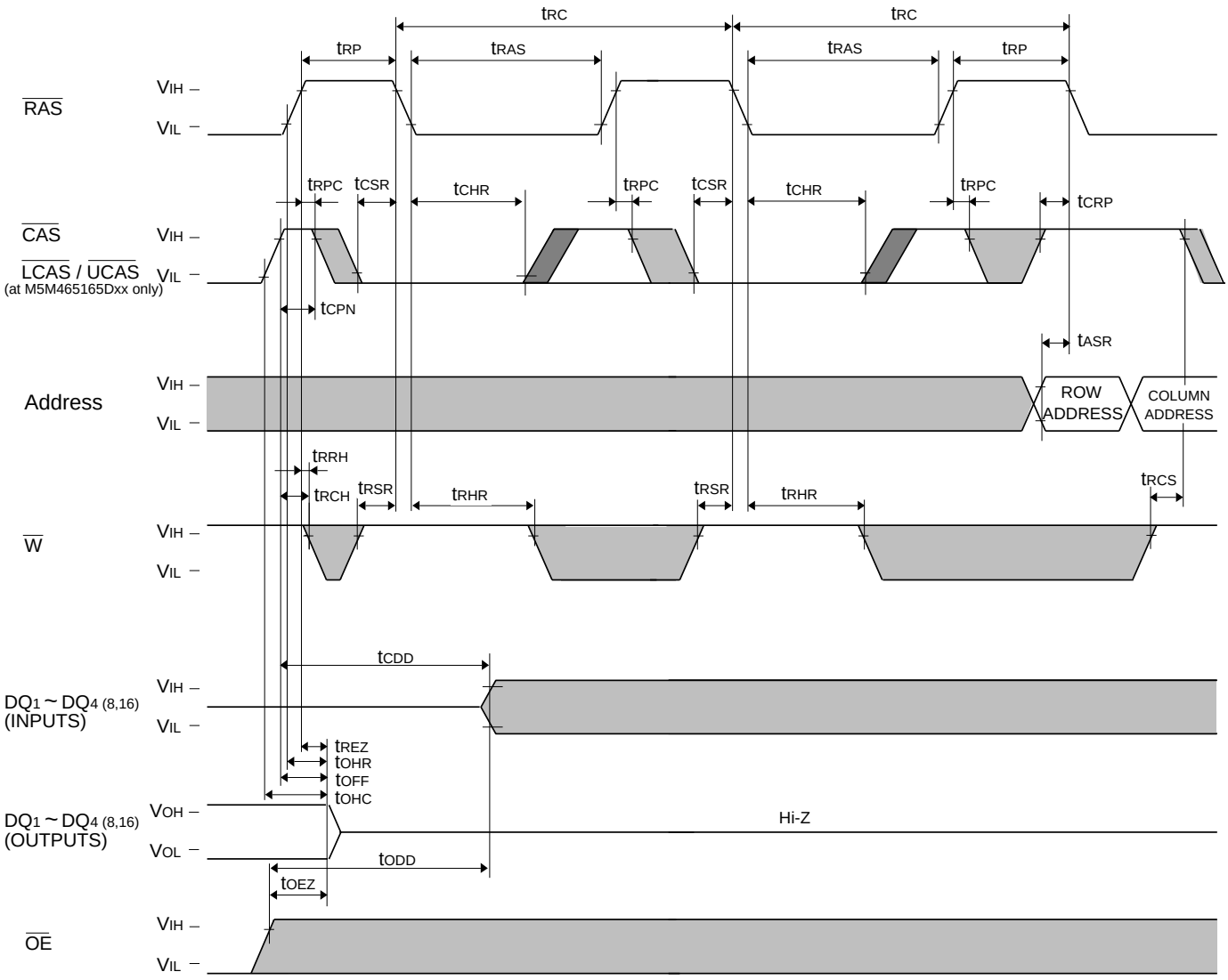
EDO Mode Read Cycle (Hi-Z control by $\overline{W}$)



$\overline{\text{RAS}}$-only Refresh Cycle



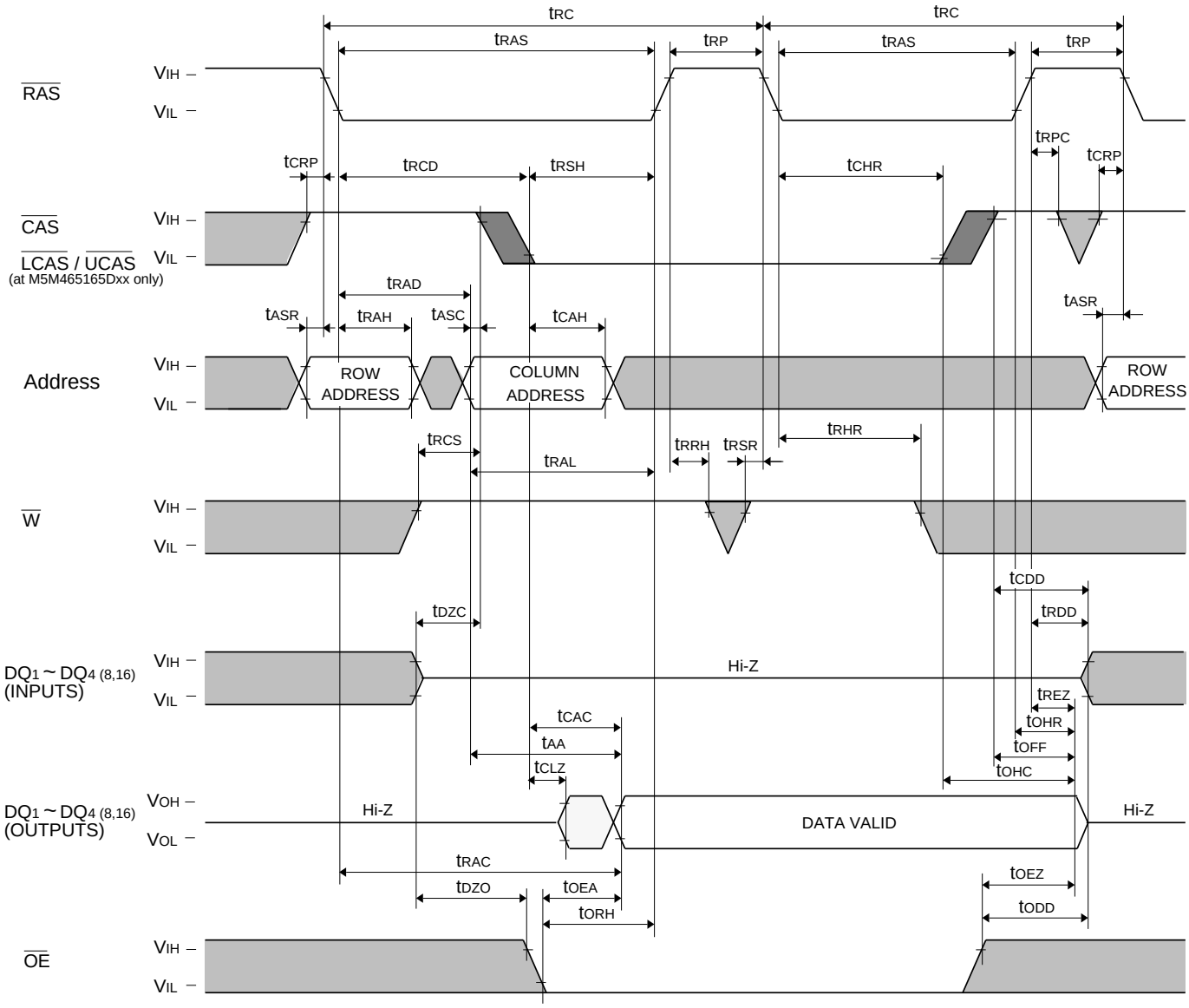
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle



M5M467405/465405DJ,DTP -5,-6,-5S,-6S
M5M467805/465805DJ,DTP -5,-6,-5S,-6S
M5M465165DJ,DTP -5,-6,-5S,-6S

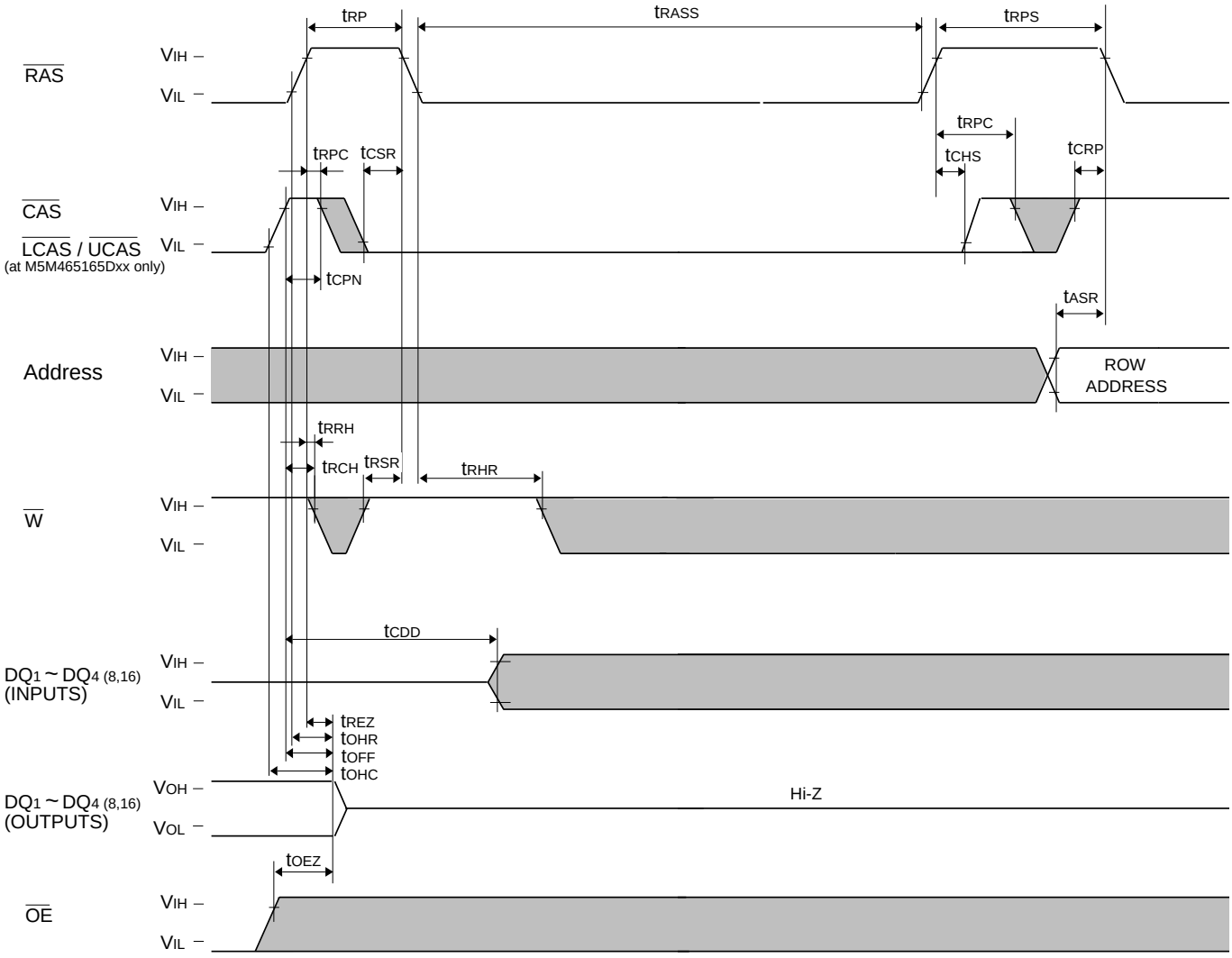
EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

Hidden Refresh Cycle (Read) (Note 31)



Note 31: Early write, delayed write, read write, or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

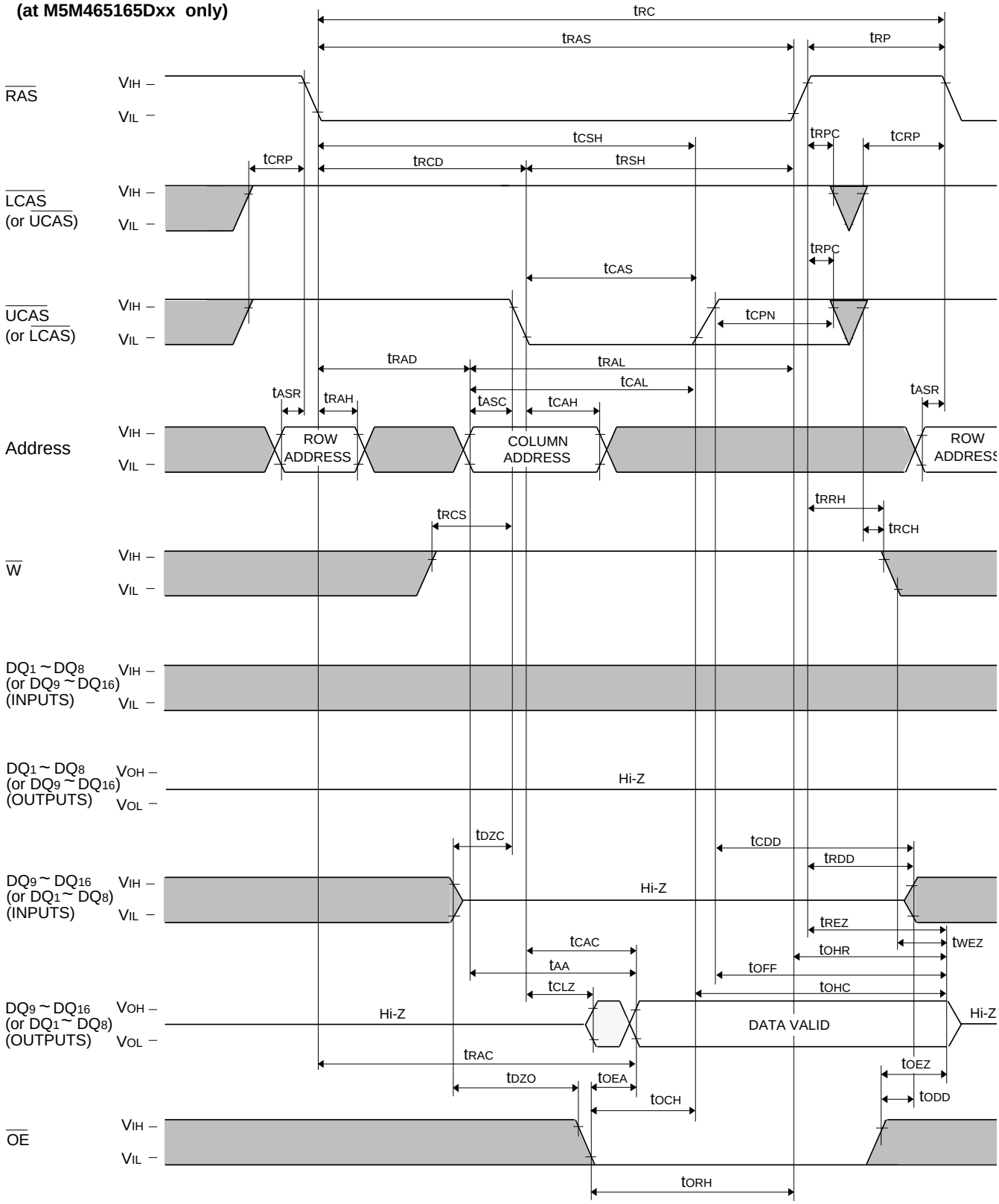
Self Refresh Cycle



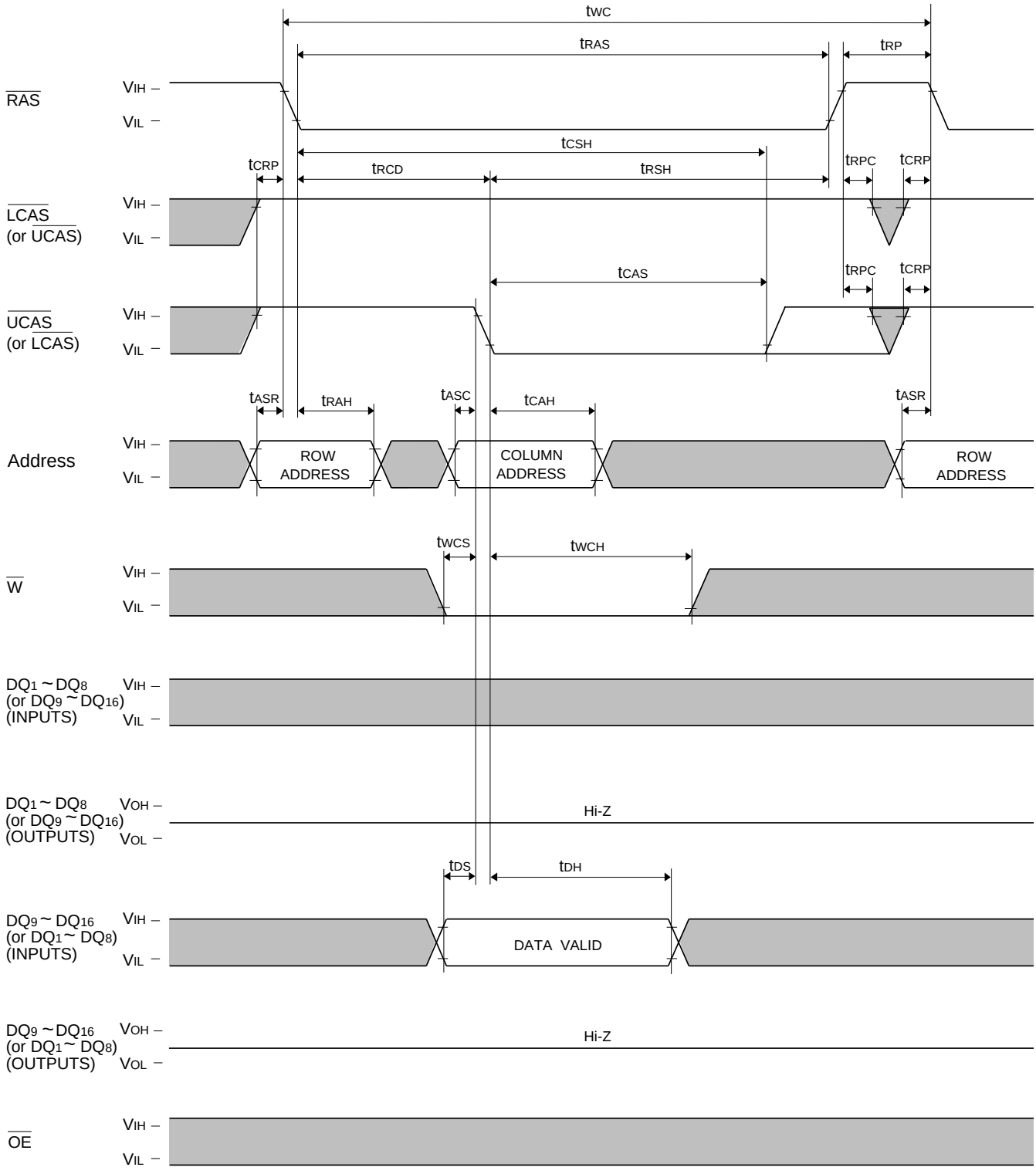
M5M467405/465405DJ,DTP -5,-6,-5S,-6S
M5M467805/465805DJ,DTP -5,-6,-5S,-6S
M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

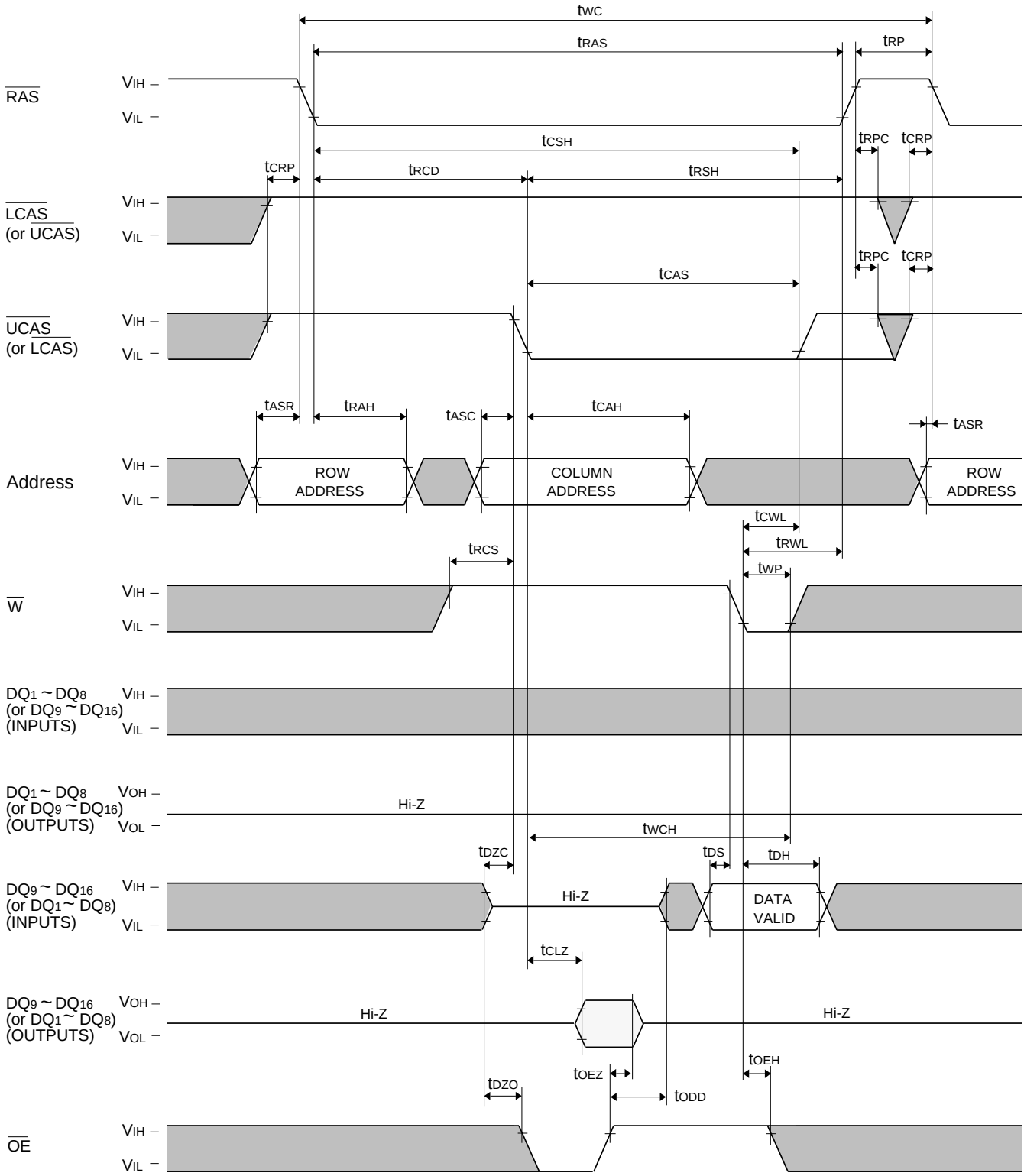
Upper / (Lower) Byte Read Cycle
(at M5M465165Dxx only)



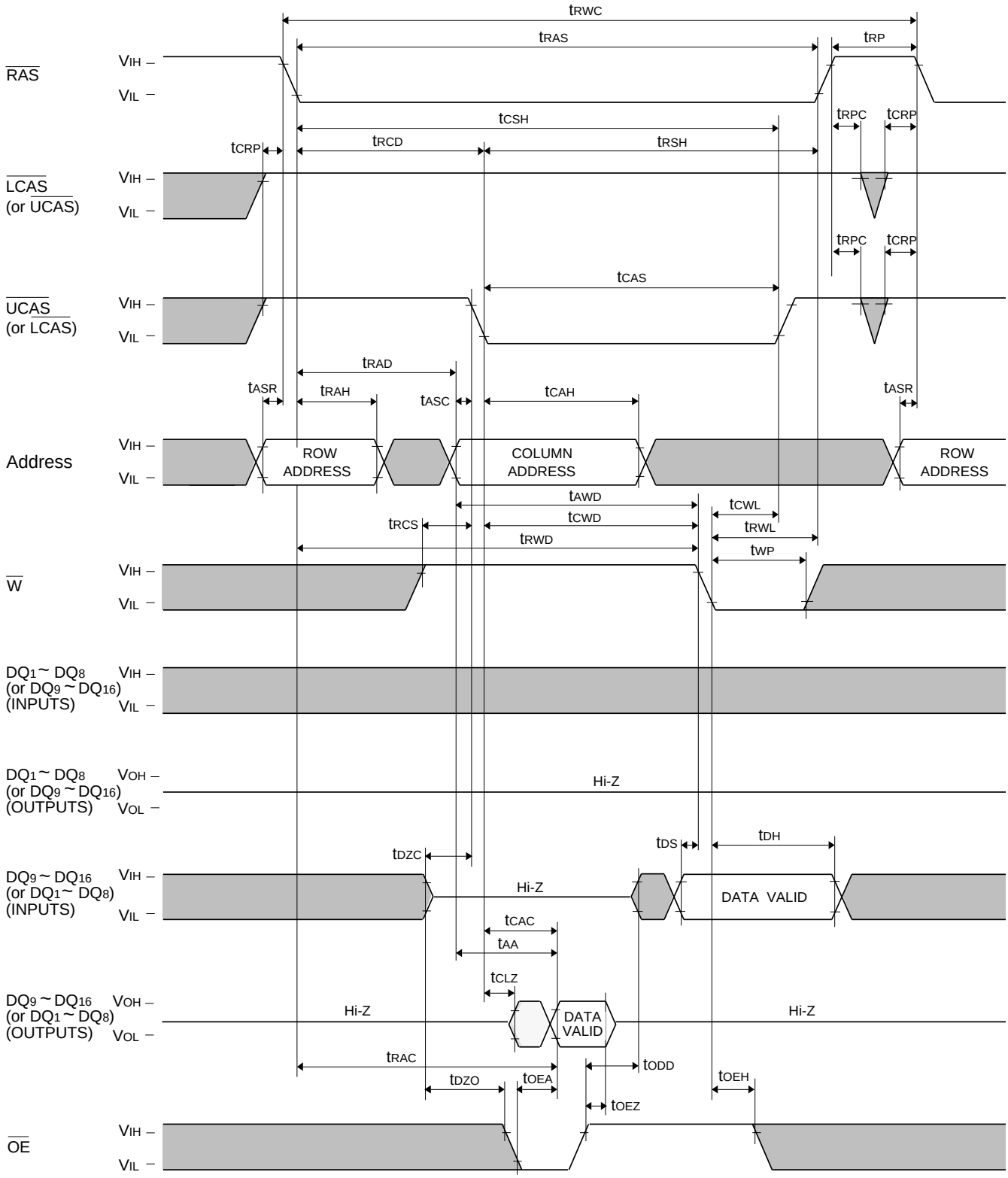
Upper / (Lower) Byte Write Cycle (Early Write)
(at M5M465165Dxx only)



Upper / (Lower) Byte Write Cycle (Delayed Write)
(at M5M465165Dxx only)



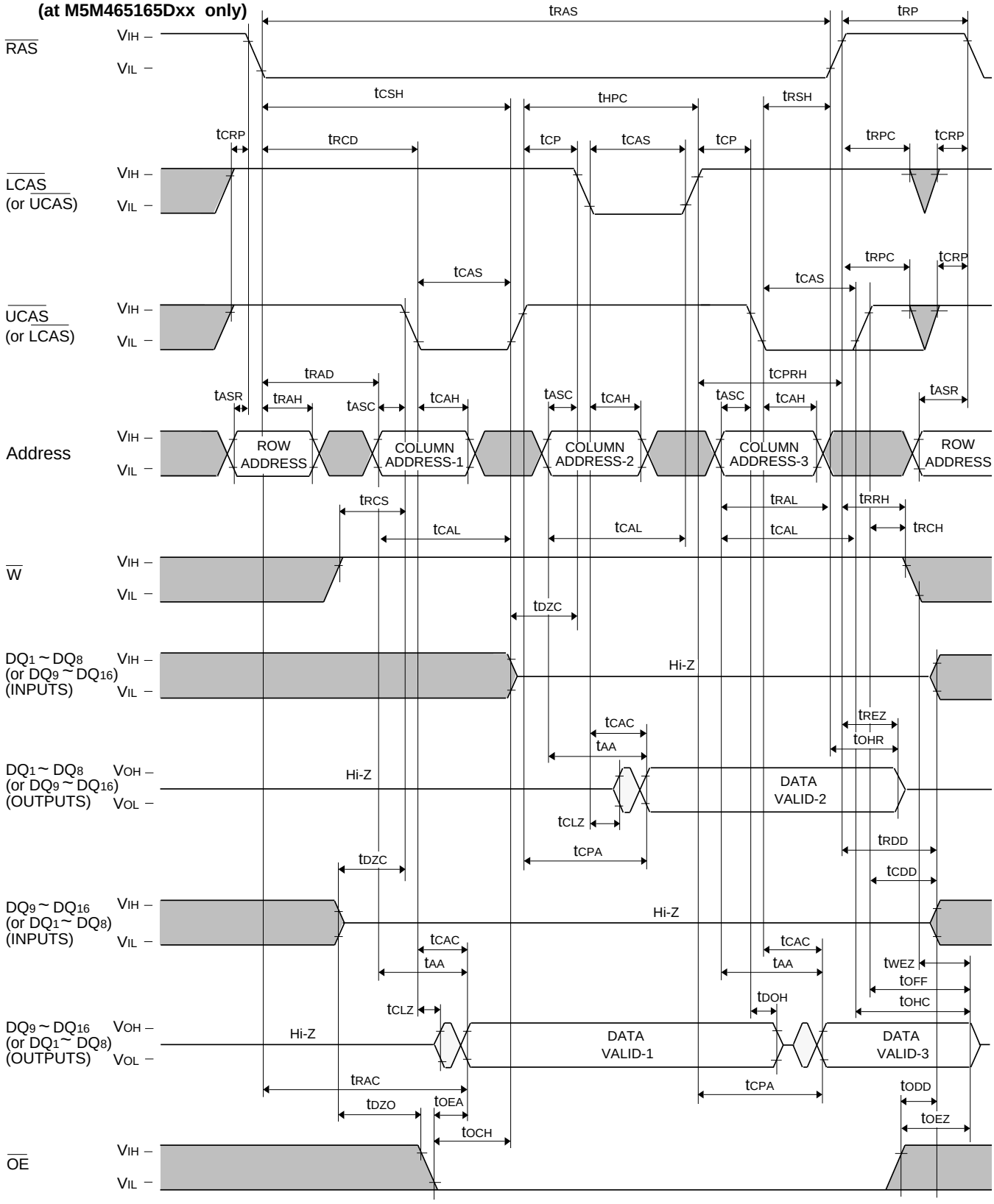
Upper / (Lower) Byte Read-Write, Upper / (Lower) Byte Read-Modify-Write Cycle.
(at M5M465165Dxx only)



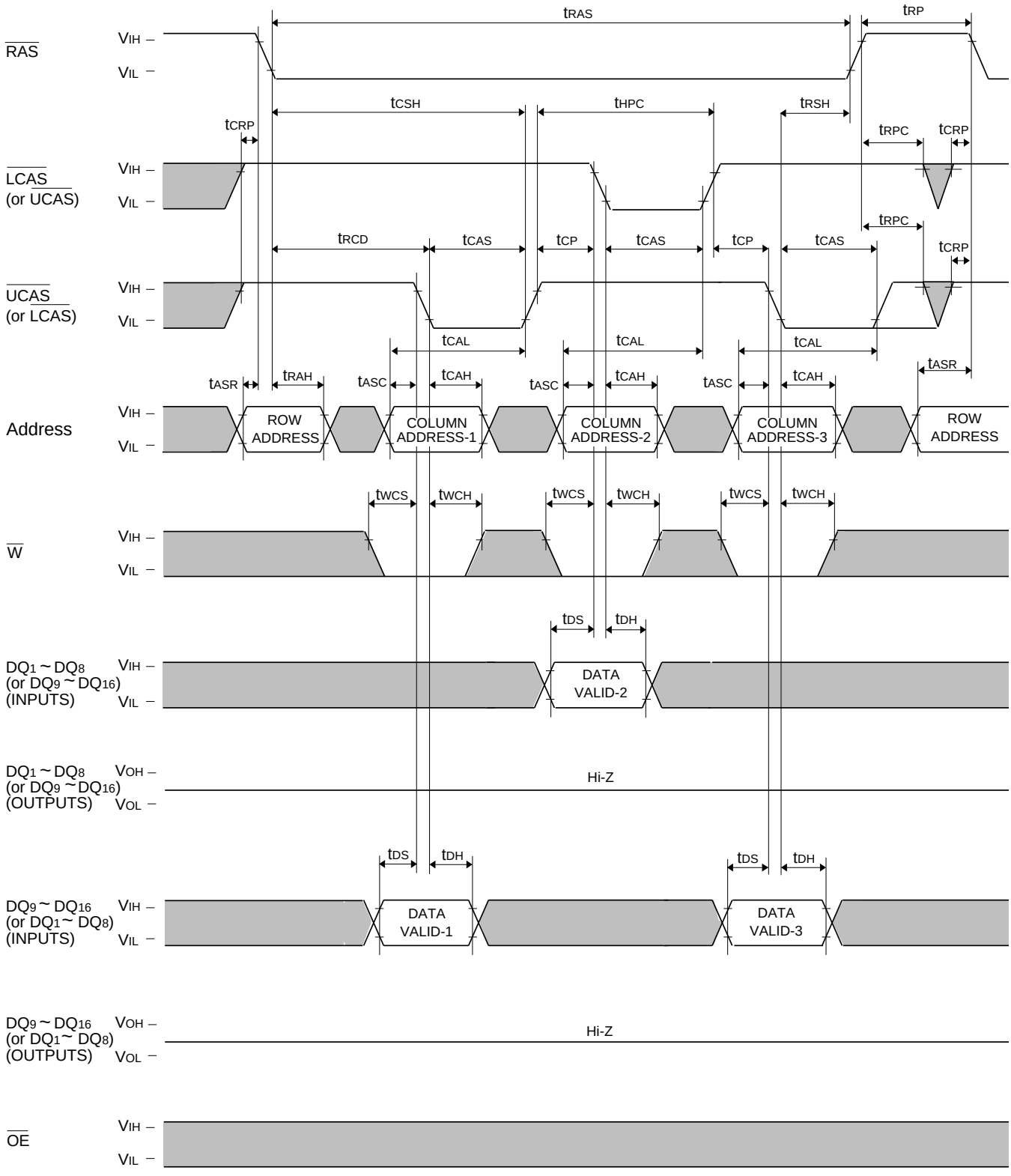
M5M467405/465405DJ,DTP -5,-6,-5S,-6S
M5M467805/465805DJ,DTP -5,-6,-5S,-6S
M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

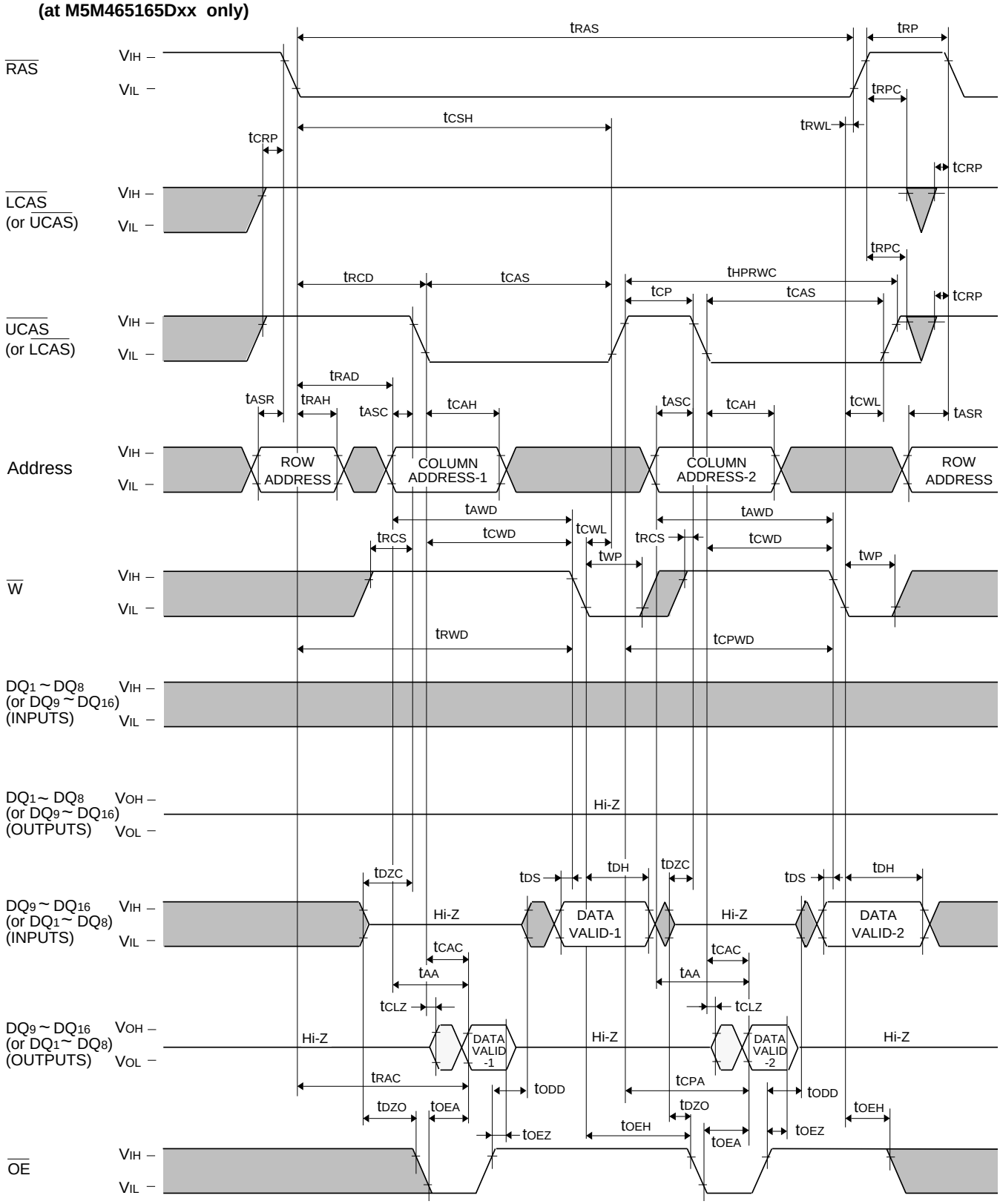
EDO Mode Byte Read Cycle
(at M5M465165Dxx only)



EDO Mode Byte Write Cycle (Early Write)
(at M5M465165Dxx only)



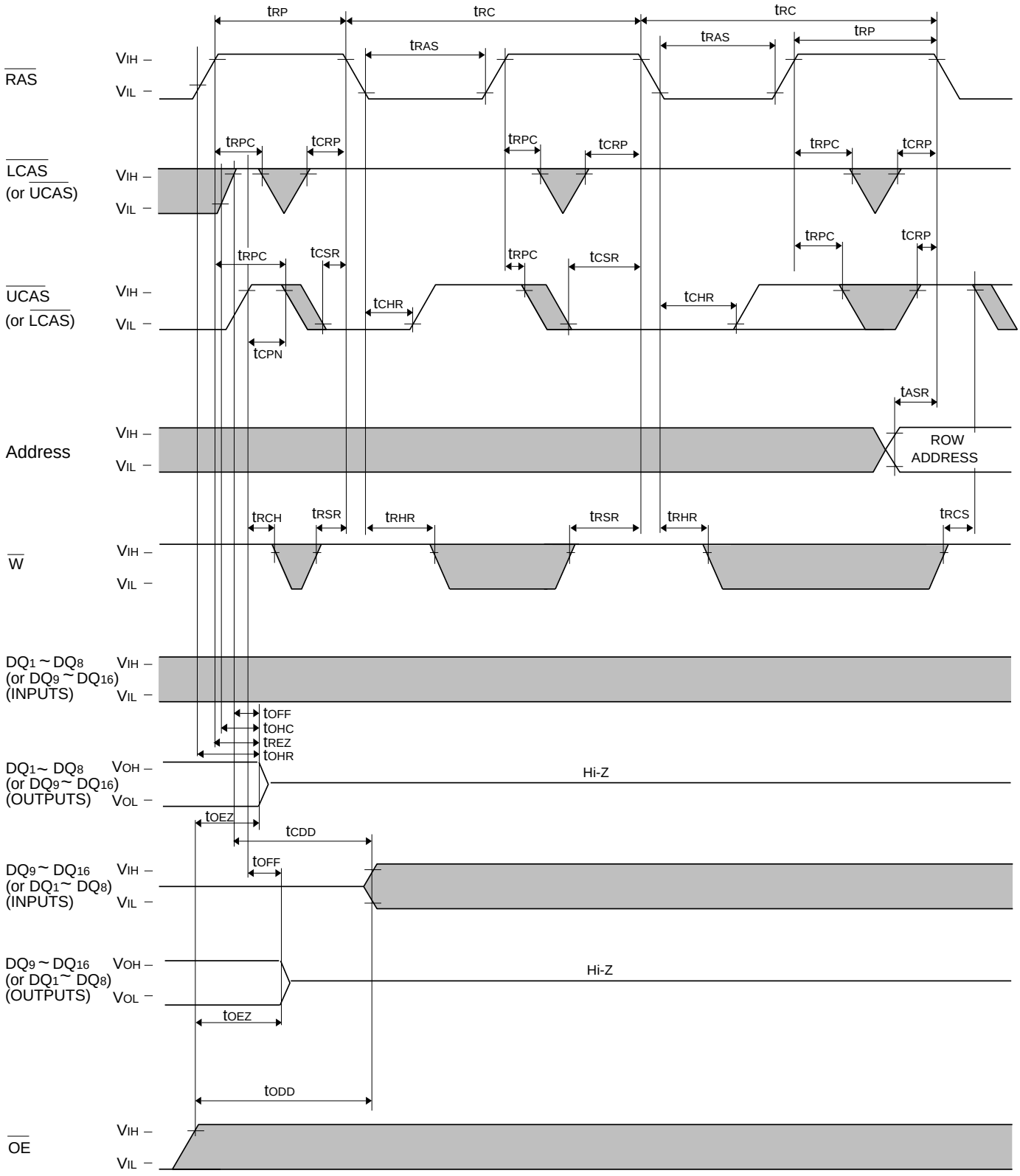
EDO Mode Upper/(Lower) Byte Read-Write, Upper/(Lower) Byte Read-Modify-Write Cycle (at M5M465165Dxx only)



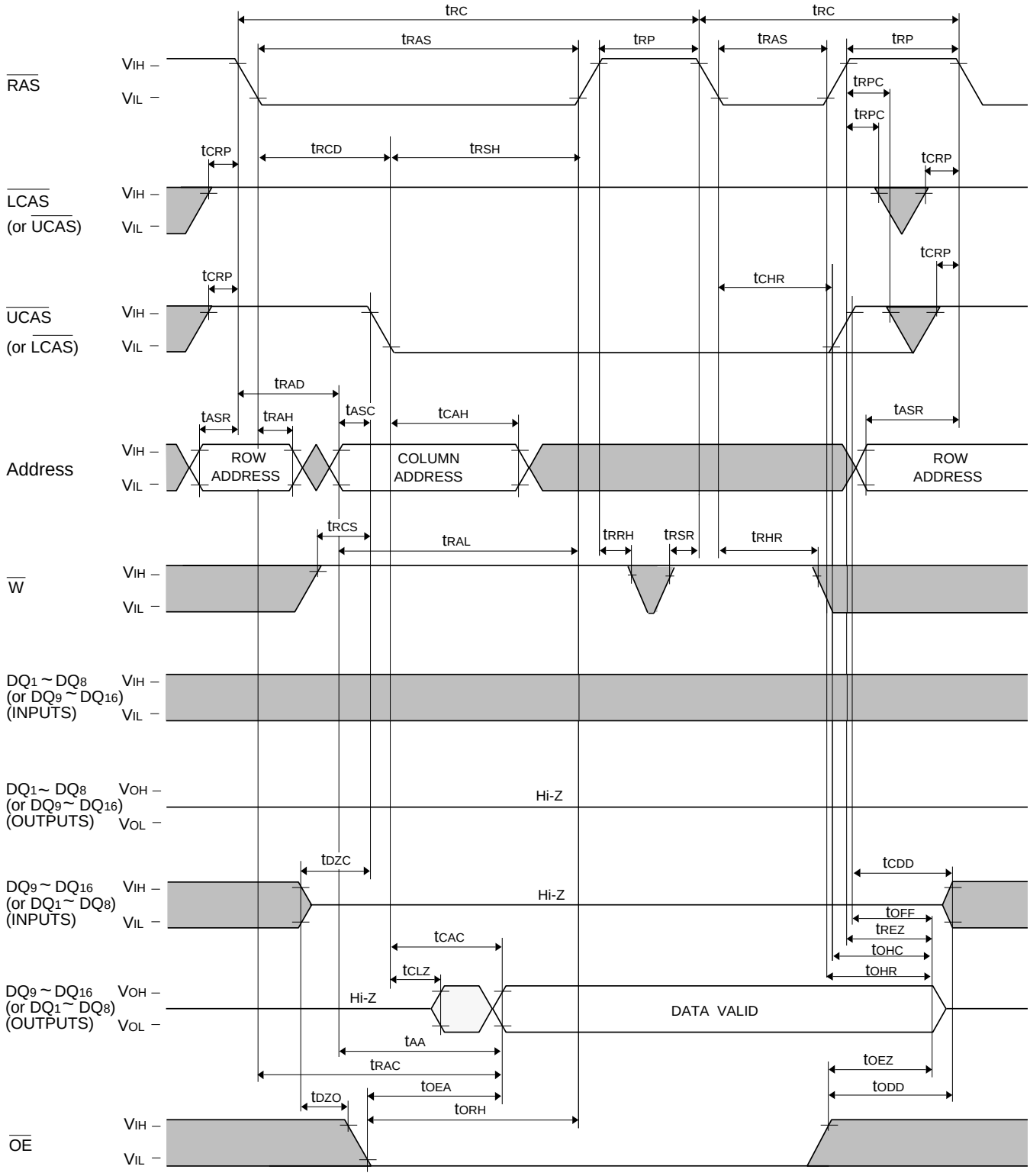
M5M467405/465405DJ,DTP -5,-6,-5S,-6S
M5M467805/465805DJ,DTP -5,-6,-5S,-6S
M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

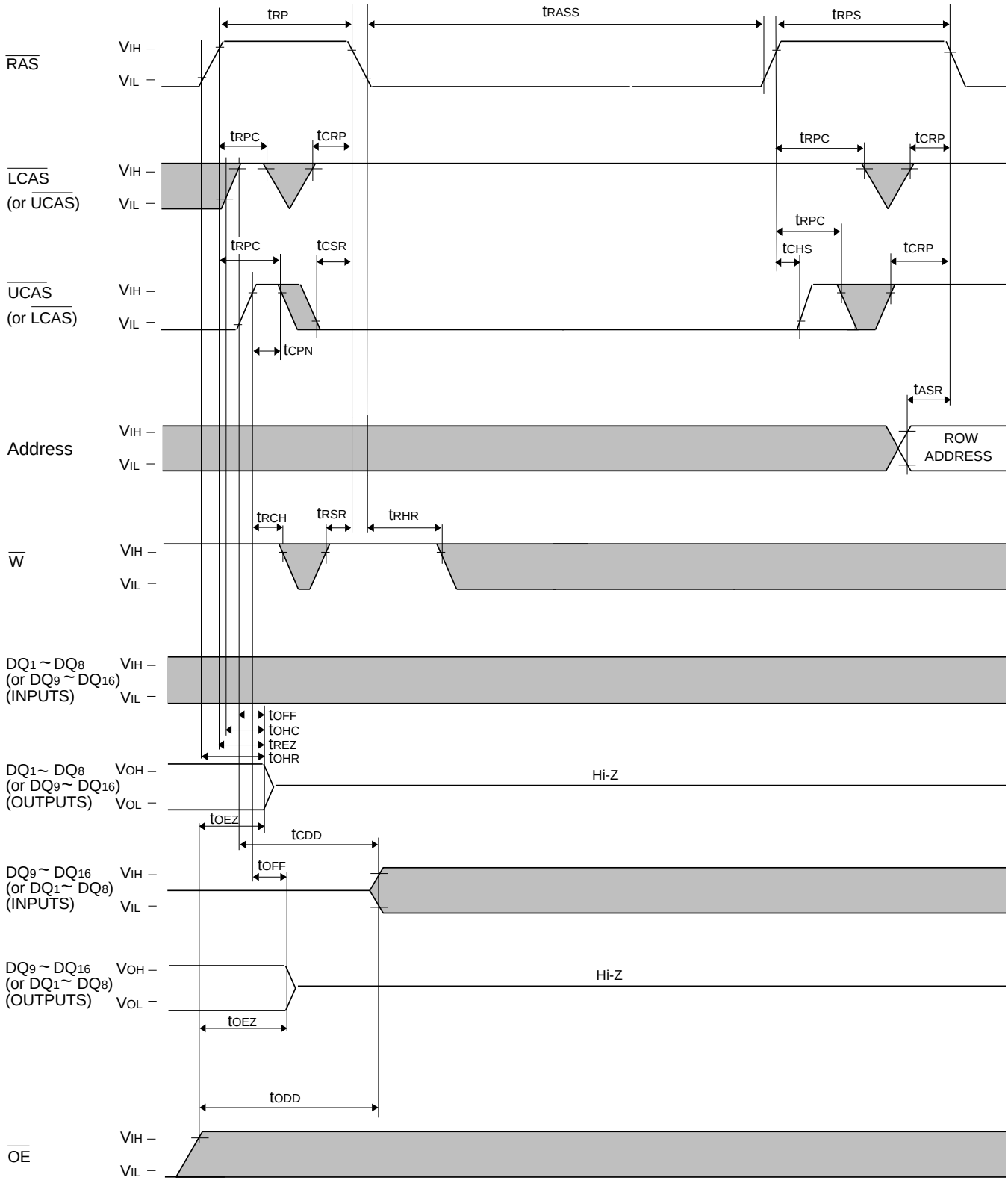
Upper / (Lower) $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle
(at M5M465165Dxx only)



Upper / (Lower) Hidden Refresh Cycle (Byte Read) (Note 31)
(at M5M465165Dxx only)



Byte Self Refresh Cycle
(at M5M465165Dxx only)



M5M467405/465405DJ,DTP -5,-6,-5S,-6S
M5M467805/465805DJ,DTP -5,-6,-5S,-6S
M5M465165DJ,DTP -5,-6,-5S,-6S

EDO MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
EDO MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

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