N25S818HA

256 kb Low Power Serial SRAMs

32 k x 8 Bit Organization

Introduction

The ON Semiconductor serial SRAM family includes several integrated memory devices including this 256 kb serially accessed Static Random Access Memory, internally organized as 32 k words by 8 bits. The devices are designed and fabricated using ON Semiconductor's advanced CMOS technology to provide both high−speed performance and low power. The devices operate with a single chip select ($\overline{\text{CS}}$) input and use a simple Serial Peripheral Interface (SPI) serial bus. A single data in and data out line is used along with a clock to access data within the devices. The N25S818HA devices include a $\overline{\text{HOLD}}$ pin that allows communication to the device to be paused. While paused, input transitions will be ignored. The devices can operate over a wide temperature range of −40°C to +85°C and can be available in several standard package offerings.

Features

- **Power Supply Range:** 1.7 to 1.95 V
- **Very Low Standby Current:** Typical Isb as low as 200 nA
- **Very Low Operating Current:** As low as 3 mA
- **Simple Memory Control:**
  Single chip select ($\overline{\text{CS}}$)
  Serial input (SI) and serial output (SO)
- **Flexible Operating Modes:**
  Word read and write
  Page mode (32 word page)
  Burst mode (full array)
- **Organization:** 32 k x 8 bit
- **Self Timed Write Cycles**
- **Built−in Write Protection ($\overline{\text{CS}}$ High)**
- **$\overline{\text{HOLD}}$ Pin for Pausing Communication**
- **High Reliability:** Unlimited write cycles
- Green SOIC and TSSOP
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

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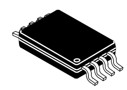
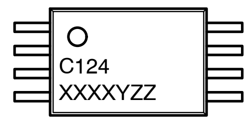
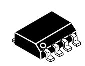
MARKING DIAGRAMS

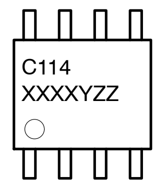


TSSOP−8
T SUFFIX
CASE 948AL





SOIC−8
S SUFFIX
CASE 751BD



XXXX	=	Date Code
Y	=	Assembly Code
ZZ	=	Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
N25S818HAS21I	SOIC−8 (Pb−Free)	100 Units / Tube
N25S818HAT21I	TSSOP−8 (Pb−Free)	100 Units / Tube
N25S818HAS21IT	SOIC−8 (Pb−Free)	3000 / Tape & Reel
N25S818HAT21IT	TSSOP−8 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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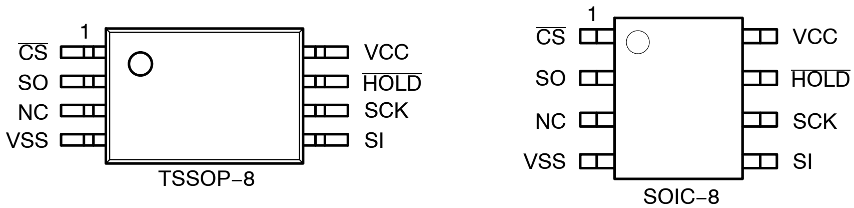


Figure 1. Pin Connections
(Top View)

Table 1. DEVICE OPTIONS

Part Number	Density	Power Supply (V)	Speed (MHz)	Package	Typical Standby Current	Read/Write Operating Current
N25S818HAS2	256 Kb	1.8	16	SOIC	200 nA	3 mA @ 1 Mhz
N25S818HAT2				TSSOP		

Table 2. PIN NAMES

Pin Name	Pin Function
$\overline{CS}$	Chip Select Input
SCK	Serial Clock Input
SI	Serial Data Input
SO	Serial Data Output
$\overline{HOLD}$	Hold Input
NC	No Connect
V_{CC}	Power
V_{SS}	Ground

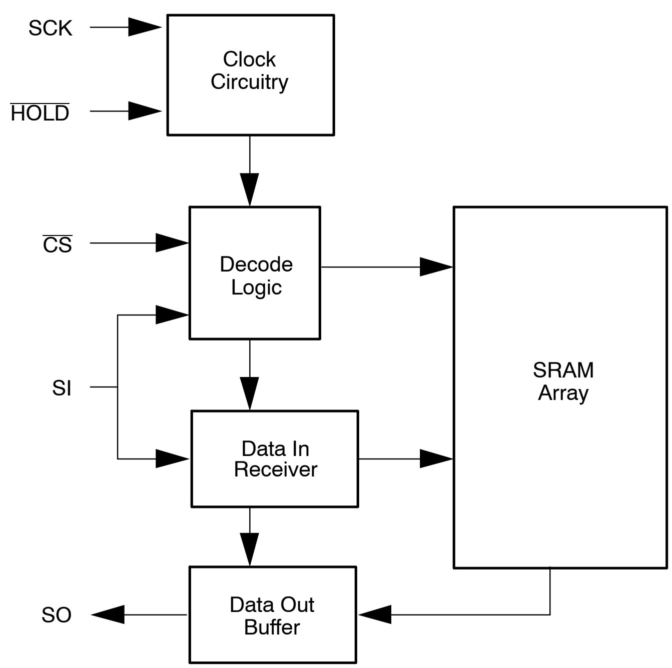


Figure 2. Functional Block Diagram

Table 3. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	–0.3 to V_{CC} + 0.3	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	–0.3 to 4.5	V
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	–40 to 125	°C
Operating Temperature	T_A	–40 to +85	°C
Soldering Temperature and Time	T_{SOLDER}	260°C, 10 sec	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 4. OPERATING CHARACTERISTICS (Over Specified Temperature Range)

Item	Symbol	Test Conditions	Min	Typ (Note 1)	Max	Unit
Supply Voltage	V_{CC}	1.8 V Device	1.7		1.95	V
Input High Voltage	V_{IH}		0.7 x V_{CC}		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}		–0.3		0.8	V
Output High Voltage	V_{OH}	I_{OH} = –0.4 mA	V_{CC} – 0.5			V
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.2	V
Input Leakage Current	I_{LI}	$\overline{CS}$ = V_{CC}, V_{IN} = 0 to V_{CC}			0.5	μA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{CC}, V_{OUT} = 0 to V_{CC}			0.5	μA
Read/Write Operating Current	I_{CC1}	F = 1 MHz, I_{OUT} = 0			3	mA
	I_{CC2}	F = 10 MHz, I_{OUT} = 0			6	mA
	I_{CC3}	F = fCLK MAX, I_{OUT} = 0			10	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}		200	500	nA

1. Typical values are measured at Vcc = Vcc Typ., T_A = 25°C and are not 100% tested.

Table 5. CAPACITANCE (Note 2)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V, f = 1 MHz, T_A = 25°C		7	pF
I/O Capacitance	$C_{I/O}$	V_{IN} = 0 V, f = 1 MHz, T_A = 25°C		7	pF

2. These parameters are verified in device characterization and are not 100% tested

Table 6. TIMING TEST CONDITIONS

Item	
Input Pulse Level	0.1 V_{CC} to 0.9 V_{CC}
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	0.5 V_{CC}
Output Load	CL = 100 pF
Operating Temperature	−40 to +85°C

Table 7. TIMING

Item	Symbol	Min	Max	Units
Clock Frequency	f_{CLK}		16	MHz
Clock Rise Time	t_R		2	μs
Clock Fall Time	t_F		2	μs
Clock High Time	t_{HI}	32		ns
Clock Low Time	t_{LO}	32		ns
Clock Delay Time	t_{CLD}	32		ns
$\overline{CS}$ Setup Time	t_{CSS}	32		ns
$\overline{CS}$ Hold Time	t_{CSH}	50		ns
$\overline{CS}$ Disable Time	t_{CSD}	32		ns
SCK to $\overline{CS}$	t_{SCS}	5		ns
Data Setup Time	t_{SU}	10		ns
Data Hold Time	t_{HD}	10		ns
Output Valid From Clock Low	t_V		32	ns
Output Hold Time	t_{HO}	0		ns
Output Disable Time	t_{DIS}		20	ns
$\overline{HOLD}$ Setup Time	t_{HS}	10		ns
$\overline{HOLD}$ Hold Time	t_{HH}	10		ns
$\overline{HOLD}$ Low to Output High−Z	t_{HZ}	10		ns
$\overline{HOLD}$ High to Output Valid	t_{HV}		50	ns

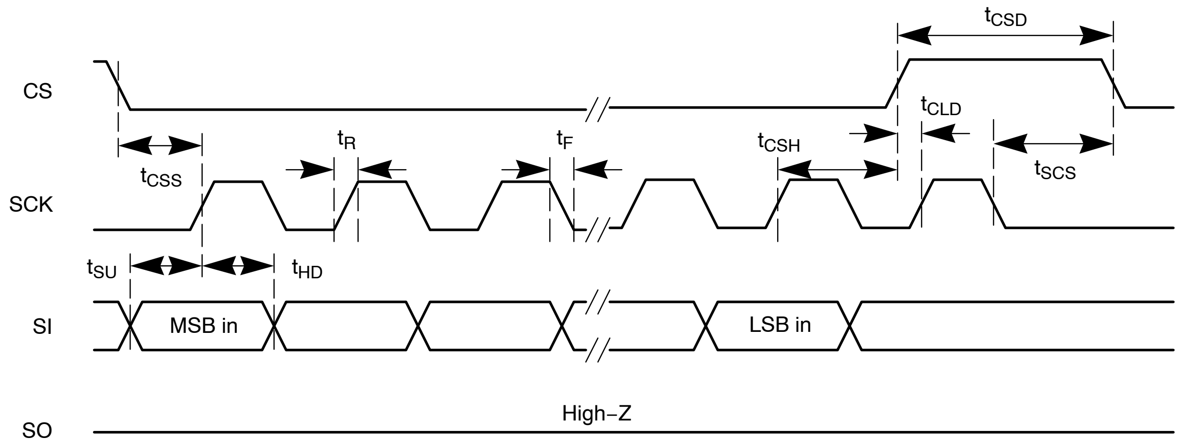


Figure 3. Serial Input Timing

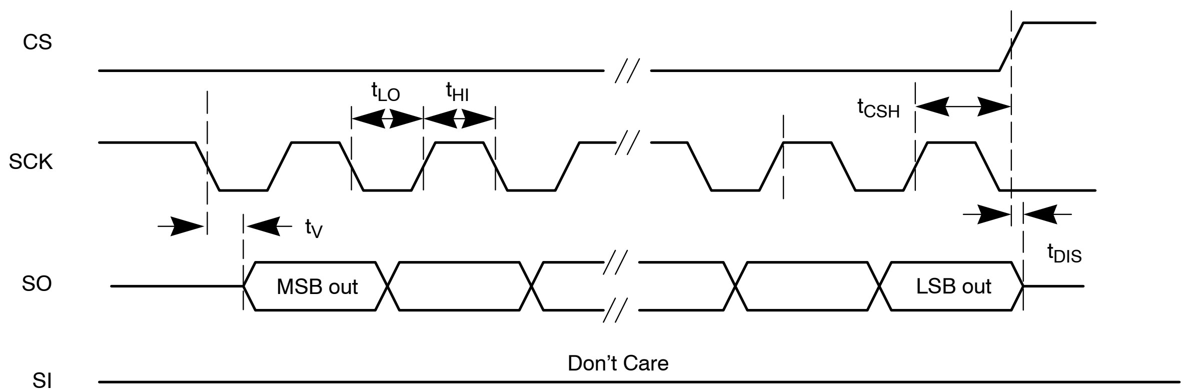


Figure 4. Serial Output Timing

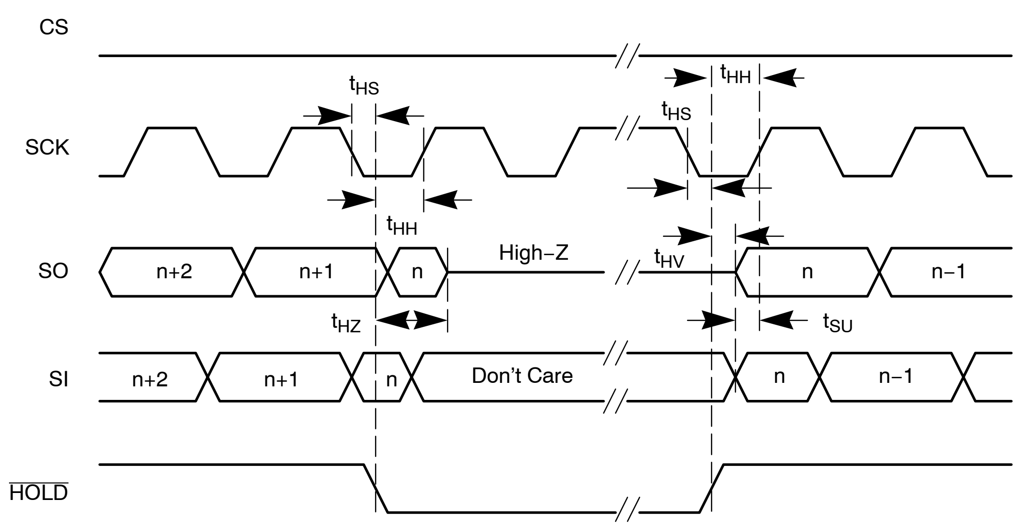


Figure 5. Hold Timing

Table 8. CONTROL SIGNAL DESCRIPTIONS

Signal	Name	I/O	Description
$\overline{\text{CS}}$	Chip Select	I	A low level selects the device and a high level puts the device in standby mode. If $\overline{\text{CS}}$ is brought high during a program cycle, the cycle will complete and then the device will enter standby mode. When $\overline{\text{CS}}$ is high, SO is in high−Z. $\overline{\text{CS}}$ must be driven low after power−up prior to any sequence being started.
SCK	Serial Clock	I	Synchronizes all activities between the memory and controller. All incoming addresses, data and instructions are latched on the rising edge of SCK. Data out is updated on SO after the falling edge of SCK.
SI	Serial Data In	I	Receives instructions, addresses and data on the rising edge of SCK.
SO	Serial Data Out	O	Data is transferred out after the falling edge of SCK.
$\overline{\text{HOLD}}$	Hold	I	A high level is required for normal operation. Once the device is selected and a serial sequence is started, this input may be taken low to pause serial communication without resetting the serial sequence. The pin must be brought low while SCK is low for immediate use. If SCK is not low, the Hold function will not be invoked until the next SCK high to low transition. The device must remain selected during this sequence. SO is high−Z during the Hold time and SI and SCK are inputs are ignored. To resume operations, $\overline{\text{HOLD}}$ must be pulled high while the SCK pin is low. Lowering the $\overline{\text{HOLD}}$ input at any time will take to SO output to High−Z.

Functional Operation

Basic Operation

The 256 Kb serial SRAM is designed to interface directly with a standard Serial Peripheral Interface (SPI) common on many standard micro−controllers. It may also interface with other non−SPI ports by programming discrete I/O lines to operate the device.

The serial SRAM contains an 8−bit instruction register and is accessed via the SI pin. The $\overline{\text{CS}}$ pin must be low and the $\overline{\text{HOLD}}$ pin must be high for the entire operation. Data is sampled on the first rising edge of SCK after $\overline{\text{CS}}$ goes low. If the clock line is shared, the user can assert the $\overline{\text{HOLD}}$ input and place the device into a Hold mode. After releasing the $\overline{\text{HOLD}}$ pin, the operation will resume from the point where it was held.

The following table contains the possible instructions and formats. All instructions, addresses and data are transferred MSB first and LSB last.

Table 9. INSTRUCTION SET

Instruction	Instruction Format	Description
READ	0000 0011	Read data from memory starting at selected address
WRITE	0000 0010	Write data to memory starting at selected address
RDSR	0000 0101	Read status register
WRSR	0000 0001	Write status register

READ Operations

The serial SRAM READ is selected by enabling $\overline{\text{CS}}$ low. First, the 8−bit READ instruction is transmitted to the device followed by the 16−bit address with the MSB being a don’t care. After the READ instruction and addresses are sent, the data stored at that address in memory is shifted out on the SO pin after the output valid time from the clock edge.

If operating in page mode, after the initial word of data is shifted out, the data stored at the next memory location on the page can be read sequentially by continuing to provide clock pulses. The internal address pointer is automatically incremented to the next higher address on the page after each word of data is read out. This can be continued for the entire page length of 32 words long. At the end of the page, the addresses pointer will be wrapped to the 0 word address within the page and the operation can be continuously looped over the 32 words of the same page.

If operating in burst mode, after the initial word of data is shifted out, the data stored at the next memory location can be read sequentially by continuing to provide clock pulses. The internal address pointer is automatically incremented to the next higher address after each word of data is read out. This can be continued for the entire array and when the highest address is reached (7FFFh), the address counter wraps to the address 0000h. This allows the burst read cycle to be continued indefinitely.

All READ operations are terminated by pulling $\overline{\text{CS}}$ high.

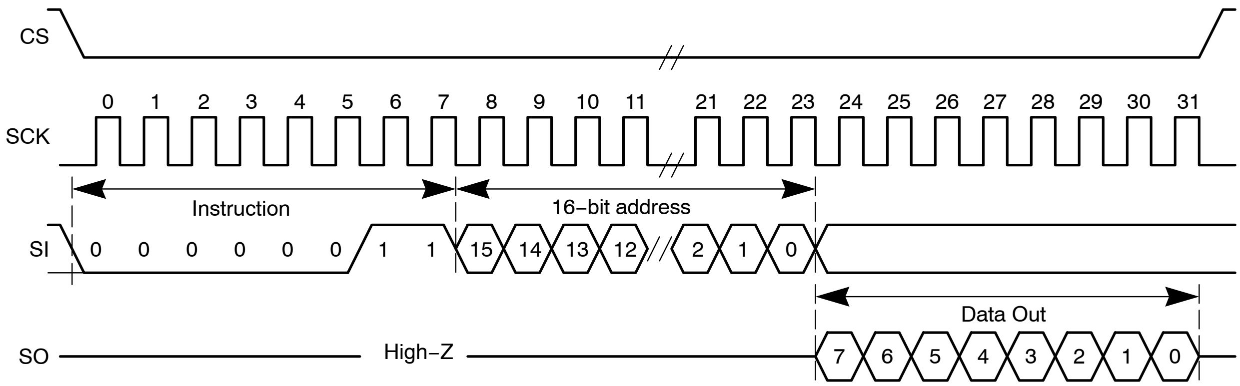


Figure 6. Word READ Sequence

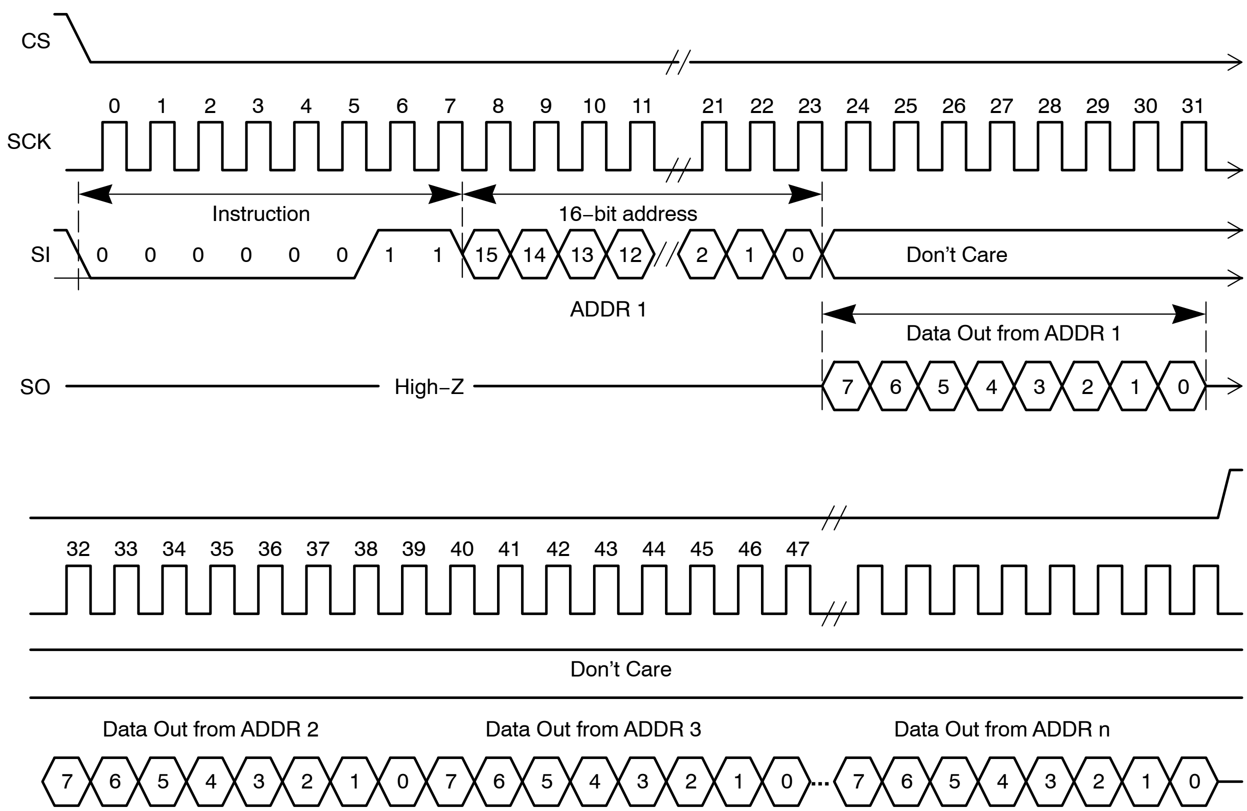


Figure 7. Page and Burst READ Sequence

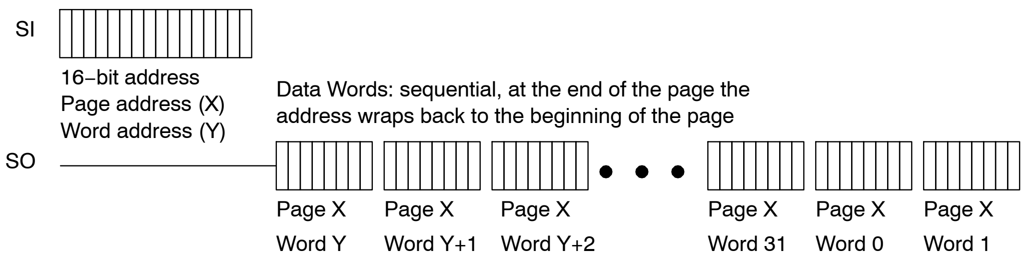


Figure 8. Page READ Sequence

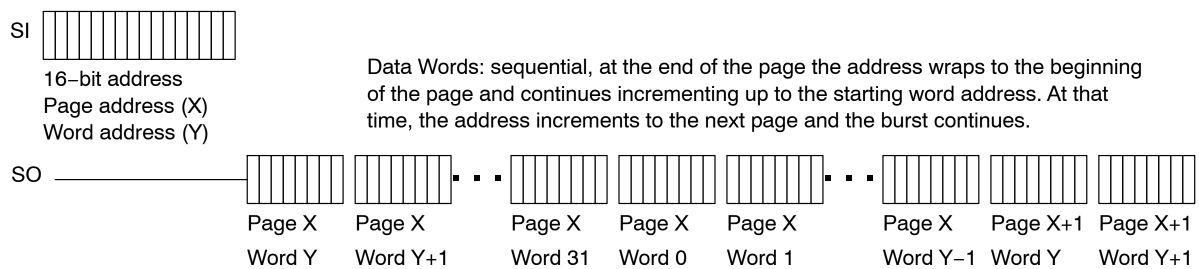


Figure 9. Burst READ Sequence

WRITE Operations

The serial SRAM WRITE is selected by enabling $\overline{CS}$ low. First, the 8−bit WRITE instruction is transmitted to the device followed by the 16−bit address with the MSB being a don’t care. After the WRITE instruction and addresses are sent, the data to be stored in memory is shifted in on the SI pin.

If operating in page mode, after the initial word of data is shifted in, additional data words can be written as long as the address requested is sequential on the same page. Simply write the data on SI pin and continue to provide clock pulses. The internal address pointer is automatically incremented to the next higher address on the page after each word of data is written in. This can be continued for the entire page length of 32 words long. At the end of the page, the addresses pointer will be wrapped to the 0 word address within the page and the operation can be continuously looped over the 32 words of the same page. The new data will replace data already stored in the memory locations.

If operating in burst mode, after the initial word of data is shifted in, additional data words can be written to the next sequential memory locations by continuing to provide clock pulses. The internal address pointer is automatically incremented to the next higher address after each word of data is read out. This can be continued for the entire array and when the highest address is reached (7FFFh), the address counter wraps to the address 0000h. This allows the burst write cycle to be continued indefinitely. Again, the new data will replace data already stored in the memory locations.

All WRITE operations are terminated by pulling $\overline{CS}$ high.

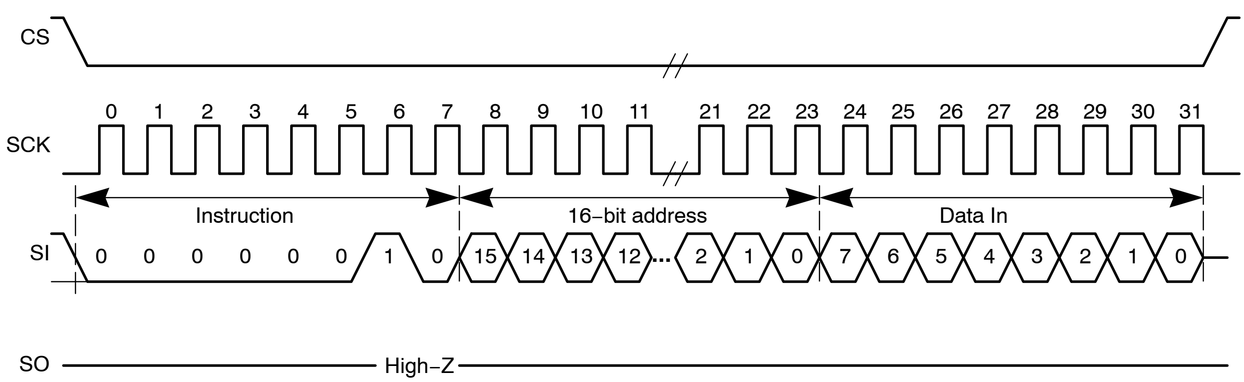


Figure 10. Word WRITE Sequence

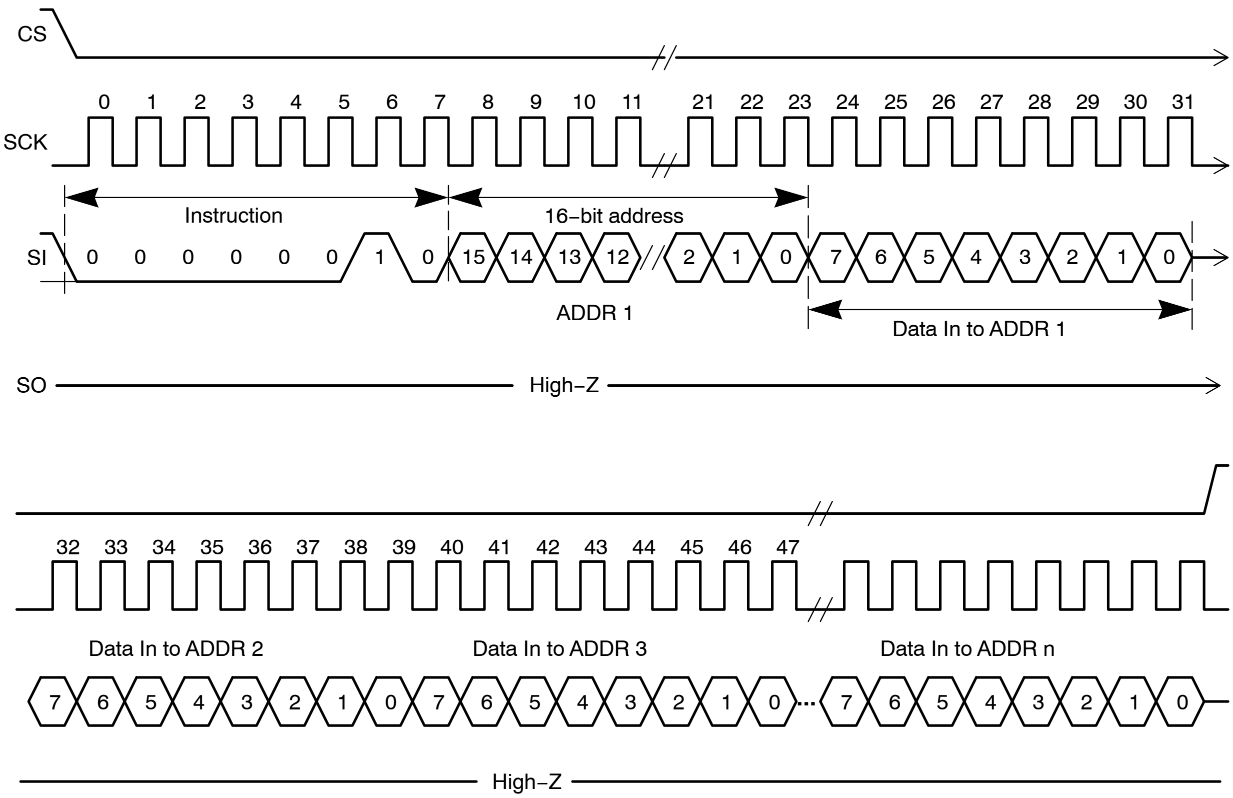


Figure 11. Page and Burst WRITE Sequence

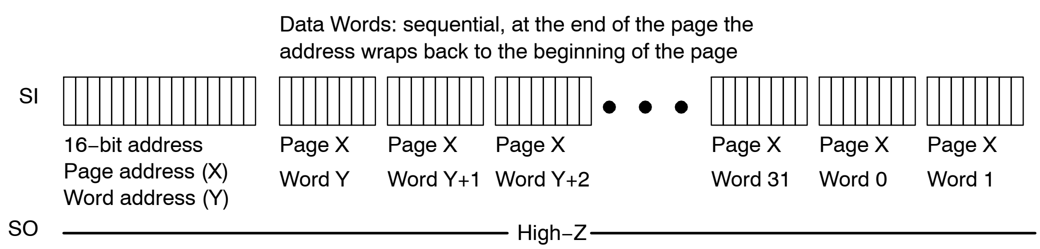


Figure 12. Page WRITE Sequence

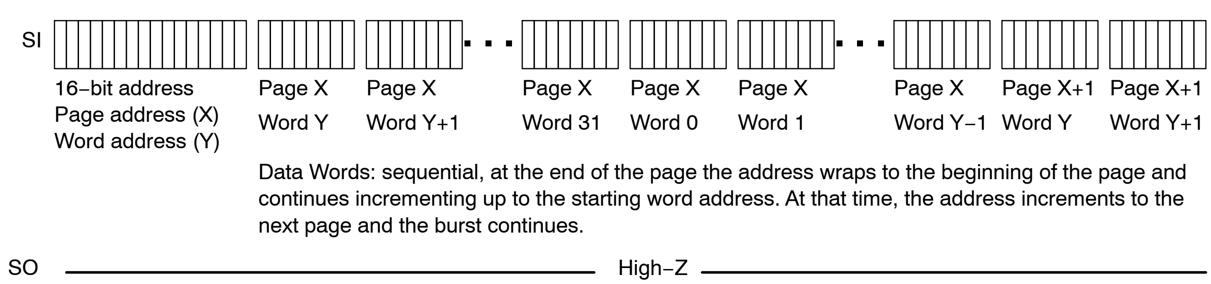


Figure 13. Burst WRITE Sequence

WRITE Status Register Instruction (WRSR)

This instruction provides the ability to write the status register and select among several operating modes. Several of the register bits must be set to a low ‘0’ if any of the other bits are written. The timing sequence to write to the status register is shown below, followed by the organization of the status register.

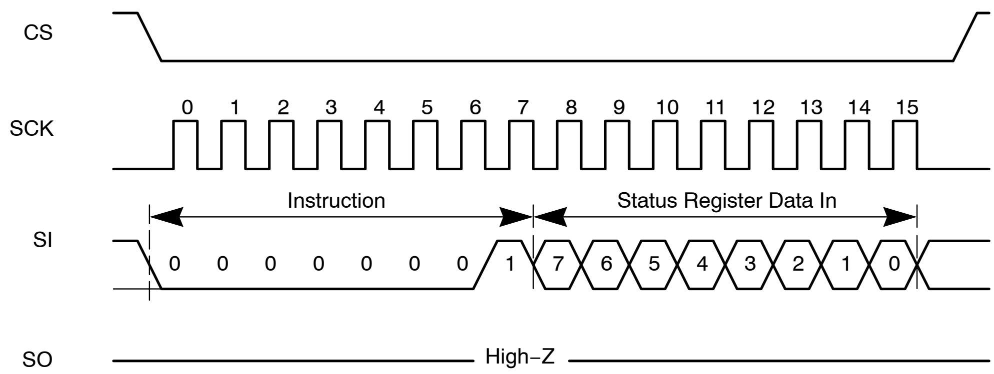


Figure 14. WRITE Status Register Sequence

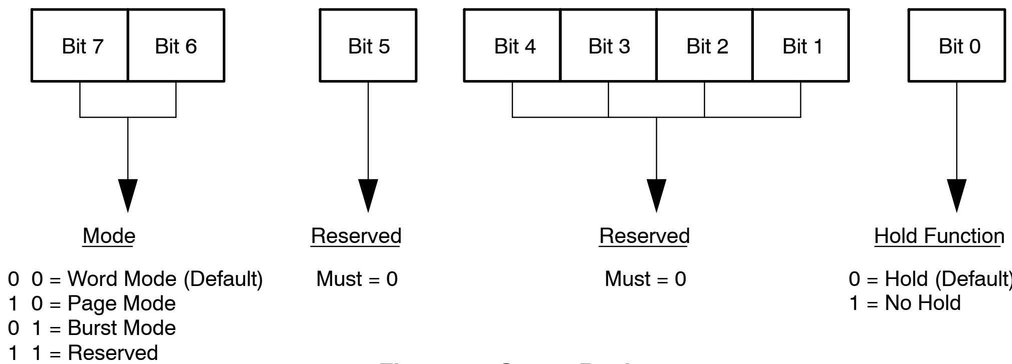


Figure 15. Status Register

READ Status Register Instruction (RDSR)

This instruction provides the ability to read the Status register. The register may be read at any time by performing the following timing sequence.

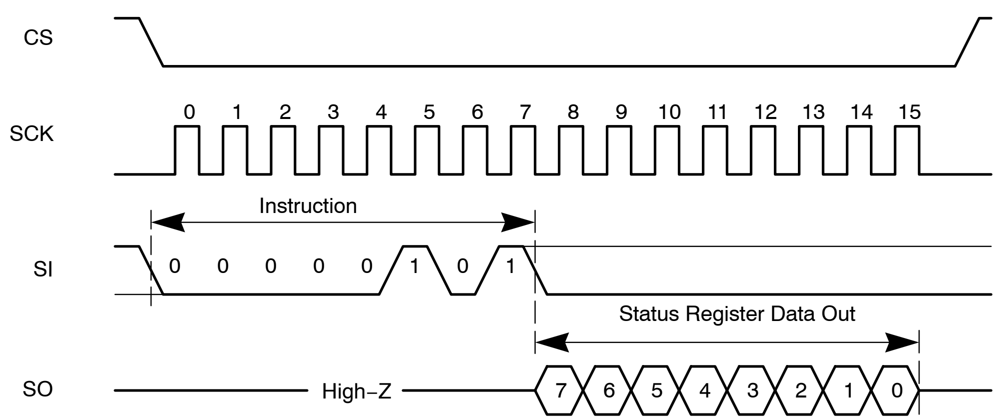


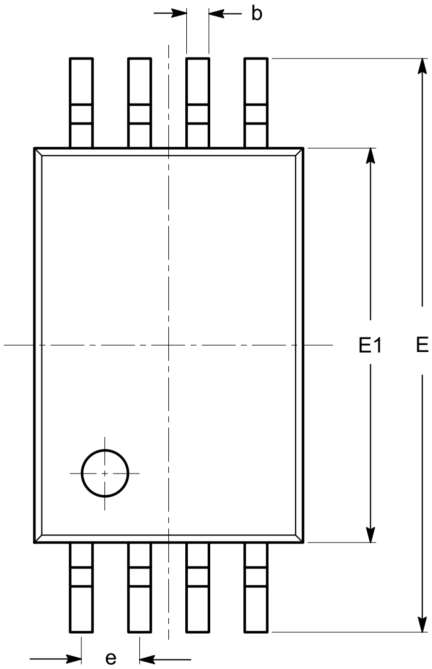
Figure 16. READ Status Register Instruction (RDSR)

Power−Up State

The serial SRAM enters a know state at power−up time. The device is in low−power standby state with $\overline{CS}$ = 1. A low level on $\overline{CS}$ is required to enter an active state.

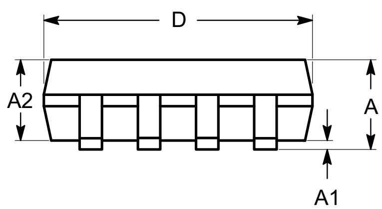
PACKAGE DIMENSIONS

TSSOP8, 4.4x3
CASE 948AL−01
ISSUE O

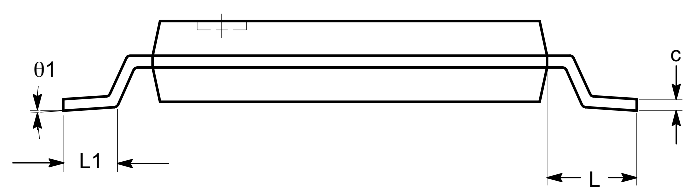


SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0º		8º

TOP VIEW



SIDE VIEW



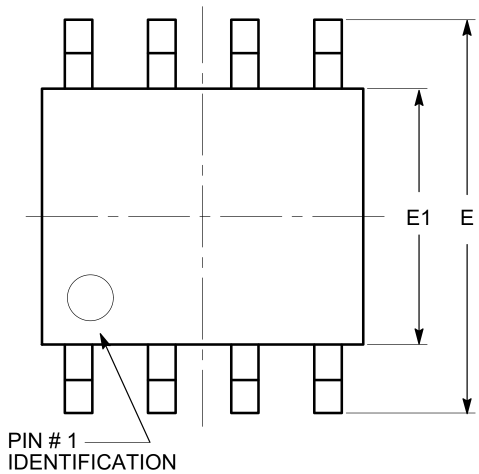
END VIEW

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

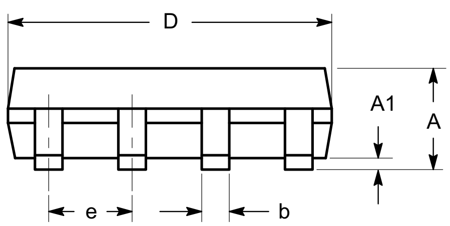
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

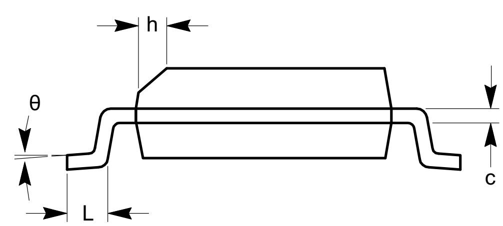


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
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