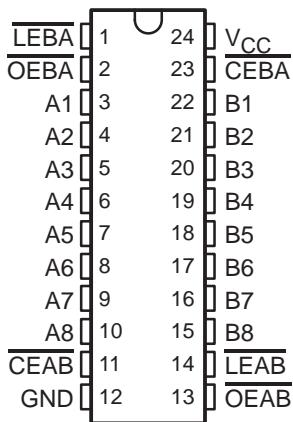


**SN54LVTH543, SN74LVTH543**  
**3.3-V ABT OCTAL REGISTERED TRANSCEIVERS**  
**WITH 3-STATE OUTPUTS**

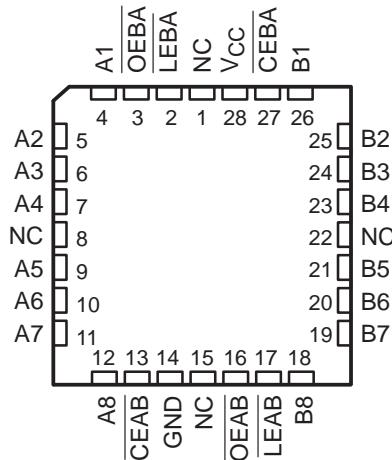
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- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V<sub>CC</sub>)
- Typical V<sub>OLP</sub> (Output Ground Bounce) <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Support Unregulated Battery Operation Down to 2.7 V
- I<sub>off</sub> and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

SN54LVTH543 . . . JT OR W PACKAGE  
 SN74LVTH543 . . . DB, DGV, DW, NS, OR PW PACKAGE  
 (TOP VIEW)



SN54LVTH543 . . . FK PACKAGE  
 (TOP VIEW)



NC – No internal connection

### description/ordering information

These octal transceivers are designed specifically for low-voltage (3.3-V) V<sub>CC</sub> operation, but with the capability to provide a TTL interface to a 5-V system environment.

### ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube	SN74LVTH543DW	LVTH543
		Tape and reel	SN74LVTH543DWR	
	SOP – NS	Tape and reel	SN74LVTH543NSR	LVTH543
	SSOP – DB	Tape and reel	SN74LVTH543DBR	LXH543
	TSSOP – PW	Tube	SN74LVTH543PW	LXH543
		Tape and reel	SN74LVTH543PWR	
	TVSOP – DGV	Tape and reel	SN74LVTH543DGVR	LXH543
–55°C to 125°C	CDIP – JT	Tube	SNJ54LVTH543JT	SNJ54LVTH543JT
	CFP – W	Tube	SNJ54LVTH543W	SNJ54LVTH543W
	LCCC – FK	Tube	SNJ54LVTH543FK	SNJ54LVTH543FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

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**description/ordering information (continued)**

The 'LVTH543 devices contain two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable (LEAB or LEBA) and output-enable (OEAB or OEBA) inputs are provided for each register, to permit independent control in either direction of data flow.

The A-to-B enable (CEAB) input must be low to enter data from A or to output data from B. If CEAB is low and LEAB is low, the A-to-B latches are transparent; a subsequent low-to-high transition of LEAB puts the A latches in the storage mode. With CEAB and OEAB both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the CEBA, LEBA, and OEBA inputs.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When  $V_{CC}$  is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, OE should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

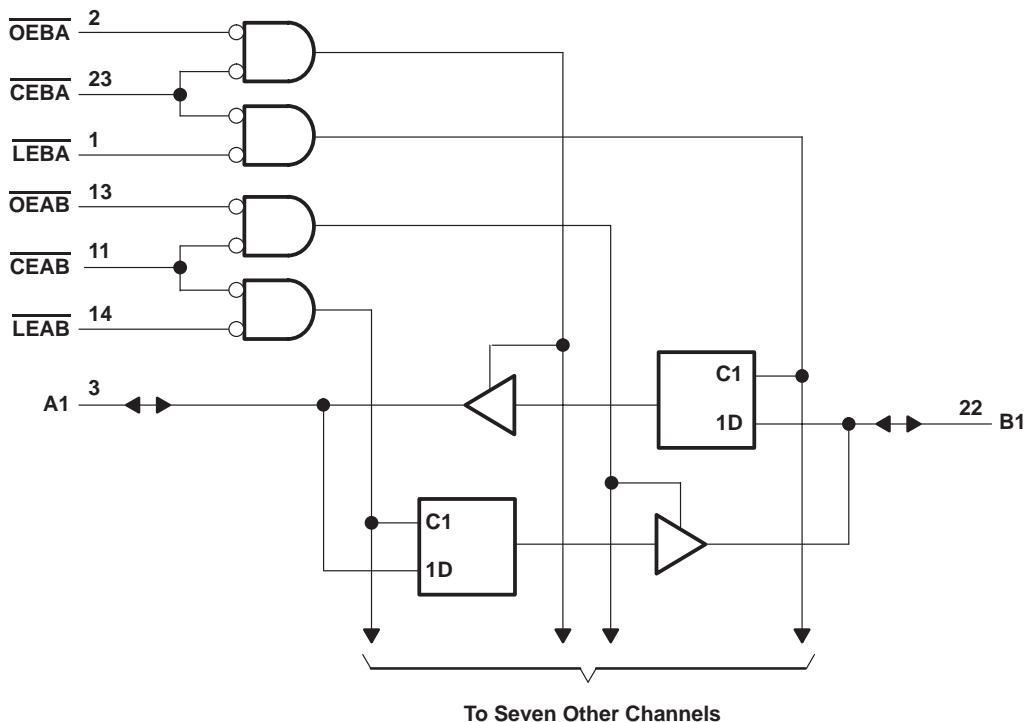
FUNCTION TABLE†

INPUTS				OUTPUT B
<u>CEAB</u>	<u>LEAB</u>	<u>OEAB</u>	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	$B_0^{\ddagger}$
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same, except that it uses CEBA, LEBA, and OEBA.

‡ Output level before the indicated steady-state input conditions were established

## logic diagram (positive logic)



Pin numbers shown are for the DB, DGV, DW, JT, NS, PW, and W packages.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 4.6 V	
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V	
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) .....	-0.5 V to 7 V	
Voltage range applied to any output in the high state, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V	
Current into any output in the low state, $I_O$ : SN54LVTH543 .....	96 mA	
	SN74LVTH543 .....	128 mA
Current into any output in the high state, $I_O$ (see Note 2): SN54LVTH543 .....	48 mA	
	SN74LVTH543 .....	64 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA	
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA	
Package thermal impedance, $\theta_{JA}$ (see Note 3): DB package .....	63°C/W	
	DGV package .....	86°C/W
	DW package .....	46°C/W
	NS package .....	65°C/W
	PW package .....	88°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C	

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .  
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

# SN54LVTH543, SN74LVTH543

## 3.3-V ABT OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS704F – AUGUST 1997 – REVISED OCTOBER 2003

### recommended operating conditions (see Note 4)

		SN54LVTH543		SN74LVTH543		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	2.7	3.6	2.7	3.6	V
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V
V <sub>I</sub>	Input voltage		5.5		5.5	V
I <sub>OH</sub>	High-level output current		-24		-32	mA
I <sub>OL</sub>	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
Δt/ΔV <sub>CC</sub>	Power-up ramp rate		200		200	μs/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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SN54LVTH543, SN74LVTH543  
**3.3-V ABT OCTAL REGISTERED TRANSCEIVERS**  
**WITH 3-STATE OUTPUTS**

SCBS704F – AUGUST 1997 – REVISED OCTOBER 2003

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN54LVTH543			SN74LVTH543			UNIT	
		MIN	TYP†	MAX	MIN	TYP†	MAX		
$V_{IK}$	$V_{CC} = 2.7 \text{ V}$ , $I_I = -18 \text{ mA}$			-1.2			-1.2	V	
$V_{OH}$	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ , $I_{OH} = -100 \mu\text{A}$	$V_{CC} - 0.2$			$V_{CC} - 0.2$			V	
	$V_{CC} = 2.7 \text{ V}$ , $I_{OH} = -8 \text{ mA}$	2.4			2.4				
	$V_{CC} = 3 \text{ V}$	$I_{OH} = -24 \text{ mA}$	2						
		$I_{OH} = -32 \text{ mA}$			2				
$V_{OL}$	$V_{CC} = 2.7 \text{ V}$	$I_{OL} = 100 \mu\text{A}$		0.2		0.2		V	
		$I_{OL} = 24 \text{ mA}$		0.5		0.5			
	$V_{CC} = 3 \text{ V}$	$I_{OL} = 16 \text{ mA}$		0.4		0.4			
		$I_{OL} = 32 \text{ mA}$		0.5		0.5			
		$I_{OL} = 48 \text{ mA}$		0.55					
		$I_{OL} = 64 \text{ mA}$				0.55			
$I_I$	Control inputs	$V_{CC} = 3.6 \text{ V}$ , $V_I = V_{CC}$ or GND		$\pm 1$		$\pm 1$		$\mu\text{A}$	
		$V_{CC} = 0$ or $3.6 \text{ V}$ , $V_I = 5.5 \text{ V}$		10		10			
	A or B ports‡	$V_{CC} = 3.6 \text{ V}$	$V_I = 5.5 \text{ V}$		20		20		
			$V_I = V_{CC}$		1		1		
			$V_I = 0$		-5		-5		
$I_{off}$	$V_{CC} = 0$ , $V_I$ or $V_O = 0$ to $4.5 \text{ V}$					$\pm 100$		$\mu\text{A}$	
$I_I(\text{hold})$	A or B ports	$V_{CC} = 3 \text{ V}$	$V_I = 0.8 \text{ V}$	75		75		$\mu\text{A}$	
			$V_I = 2 \text{ V}$	-75		-75			
		$V_{CC} = 3.6 \text{ V} \S$	$V_I = 0$ to $3.6 \text{ V}$			$\pm 500$			
$I_{OZPU}$		$V_{CC} = 0$ to $1.5 \text{ V}$ , $V_O = 0.5$ to $3 \text{ V}$ , $OE = \text{don't care}$			$\pm 100^*$		$\pm 100$	$\mu\text{A}$	
$I_{OZPD}$		$V_{CC} = 1.5 \text{ V}$ to $0$ , $V_O = 0.5$ to $3 \text{ V}$ , $OE = \text{don't care}$			$\pm 100^*$		$\pm 100$	$\mu\text{A}$	
$I_{CC}$		$V_{CC} = 3.6 \text{ V}$ , $I_O = 0$ , $V_I = V_{CC}$ or GND	Outputs high		0.19		0.19	$\text{mA}$	
			Outputs low		5		5		
			Outputs disabled		0.19		0.19		
$\Delta I_{CC} \ddagger$		$V_{CC} = 3 \text{ V}$ to $3.6 \text{ V}$ , One input at $V_{CC} - 0.6 \text{ V}$ , Other inputs at $V_{CC}$ or GND			0.2		0.2	$\text{mA}$	
$C_I$	$V_I = 3 \text{ V}$ or $0$			4		4		$\text{pF}$	
$C_{IO}$	$V_O = 3 \text{ V}$ or $0$			9		9		$\text{pF}$	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Unused terminals are at  $V_{CC}$  or GND.

§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

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**SN54LVTH543, SN74LVTH543****3.3-V ABT OCTAL REGISTERED TRANSCEIVERS  
WITH 3-STATE OUTPUTS**

SCBS704F – AUGUST 1997 – REVISED OCTOBER 2003

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

			SN54LVTH543				SN74LVTH543				UNIT	
			V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V			
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t <sub>W</sub>	Pulse duration, LEAB or LEBA low			3.3	3.3	3.3	3.3	3.3	3.3	ns		
t <sub>SU</sub>	Setup time	A or B before LEAB or LEBA↑	Data high	0.4	0.4	0.4	0.4	0.4	0.4	ns		
			Data low	1	1.5	1	1.5	1	1.5			
		A or B before CEAB or CEBA↑	Data high	0.2	0.2	0.2	0.2	0.2	0.2			
			Data low	0.7	1.2	0.7	1.2	0.7	1.2			
t <sub>H</sub>	Hold time	A or B after LEAB or LEBA↑	Data high	1.5	0.6	1.5	0.6	1.5	0.6	ns		
			Data low	1.3	1.5	1.3	1.5	1.3	1.5			
		A or B after CEAB or CEBA↑	Data high	1.6	0.5	1.6	0.5	1.6	0.5			
			Data low	1.4	1.6	1.4	1.6	1.4	1.6			

**switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF  
(unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH543				SN74LVTH543				UNIT	
			V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V			
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		
t <sub>PLH</sub>	A or B	B or A	1.2	3.9	4.5	1.3	2.5	3.7	4.3	ns		
t <sub>PHL</sub>			1.2	3.9	4.5	1.3	2.5	3.7	4.3			
t <sub>PLH</sub>	LE	A or B	1.2	5.1	6.1	1.3	2.9	4.7	5.9	ns		
t <sub>PHL</sub>			1.2	5.1	6.1	1.3	2.9	4.7	5.9			
t <sub>PZH</sub>	OE	A or B	1	5.1	6.4	1.1	2.9	4.9	6.2	ns		
t <sub>PZL</sub>			1	5.1	6.4	1.1	3.2	4.9	6.2			
t <sub>PHZ</sub>	OE	A or B	1.9	5.6	6.2	2	3.4	5.3	5.9	ns		
t <sub>PLZ</sub>			1.9	5.6	6.2	2	3.7	5.3	5.9			
t <sub>PZH</sub>	CE	A or B	1.2	5.5	7	1.3	3.2	5.3	6.8	ns		
t <sub>PZL</sub>			1.2	5.5	7	1.3	3.5	5.3	6.8			
t <sub>PHZ</sub>	CE	A or B	2.2	5.7	6.2	2.3	3.8	5.4	5.9	ns		
t <sub>PLZ</sub>			2.2	5.7	5.9	2.3	3.9	5.4	5.6			

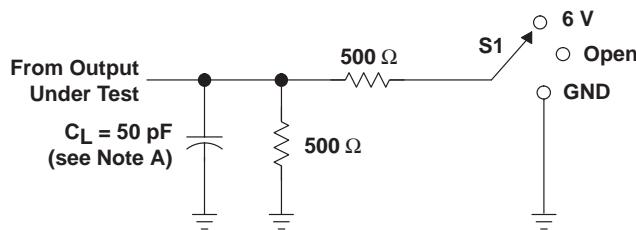
† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

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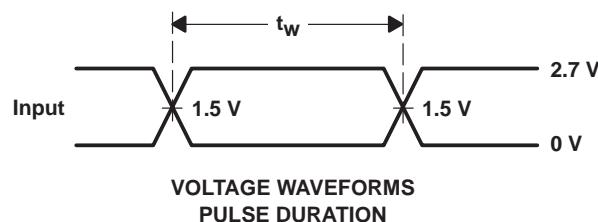


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**PARAMETER MEASUREMENT INFORMATION**

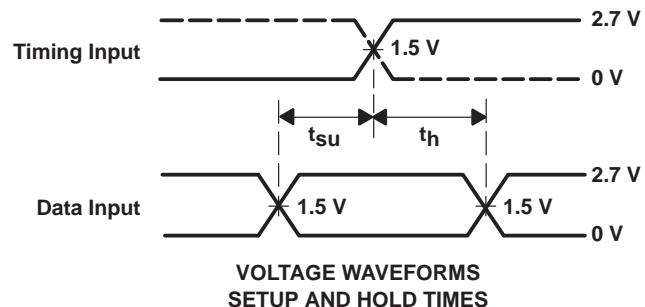


LOAD CIRCUIT

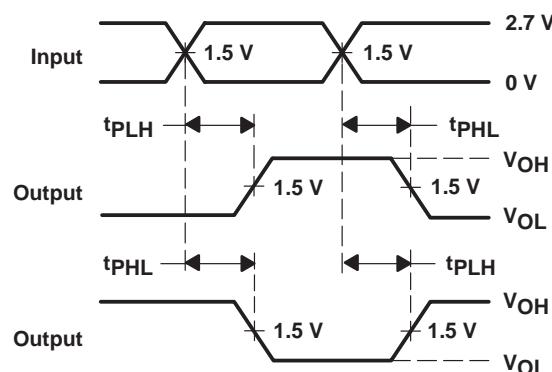


VOLTAGE WAVEFORMS  
 PULSE DURATION

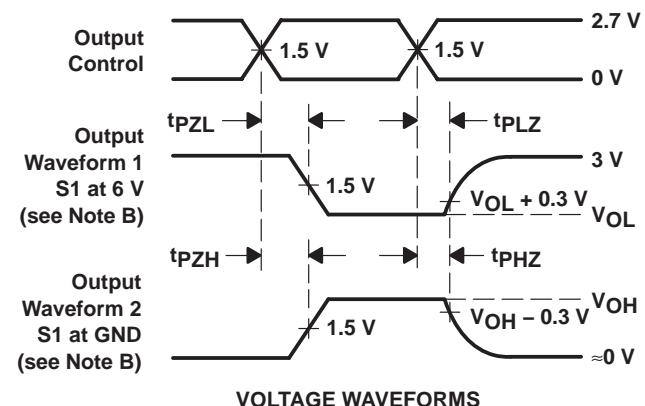
TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	6 V
tPHZ/tPZH	GND



VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES  
 INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES  
 LOW- AND HIGH-LEVEL ENABLING

NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
- Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVTH543DBLE	OBsolete	SSOP	DB	24		TBD	Call TI	Call TI	-40 to 85		
SN74LVTH543DBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH543	Samples
SN74LVTH543DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH543	Samples
SN74LVTH543DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH543	Samples
SN74LVTH543PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH543	Samples
SN74LVTH543PWLE	OBsolete	TSSOP	PW	24		TBD	Call TI	Call TI	-40 to 85		
SN74LVTH543PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH543	Samples
SN74LVTH543PWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH543	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74LVTH543 :**

- Enhanced Product: [SN74LVTH543-EP](#)

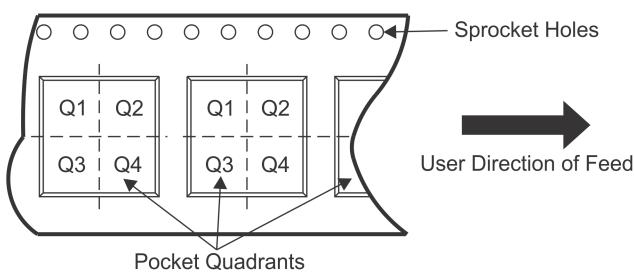
NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVTH543DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74LVTH543DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVTH543PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

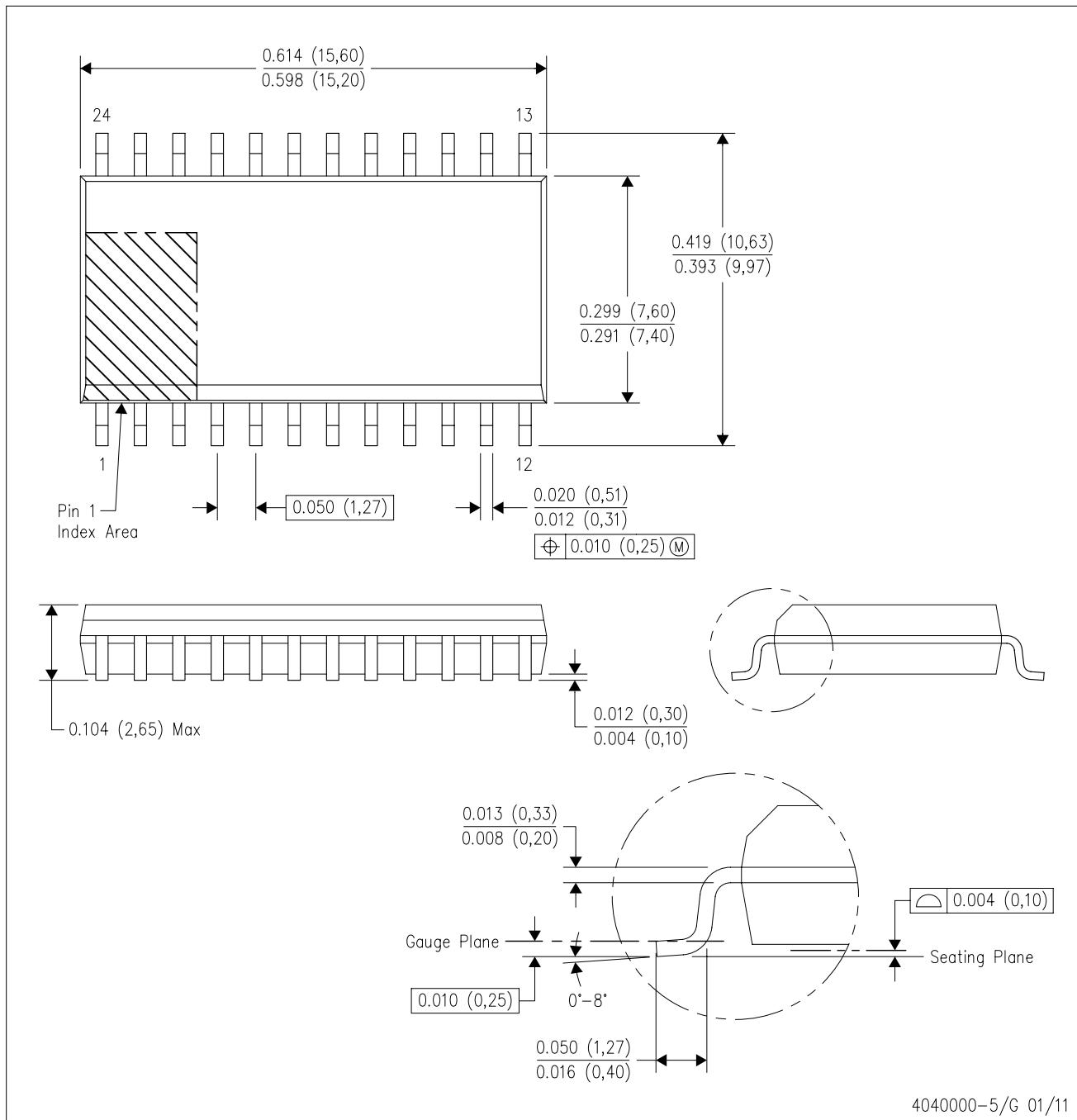
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVTH543DBR	SSOP	DB	24	2000	367.0	367.0	38.0
SN74LVTH543DWR	SOIC	DW	24	2000	367.0	367.0	45.0
SN74LVTH543PWR	TSSOP	PW	24	2000	367.0	367.0	38.0

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

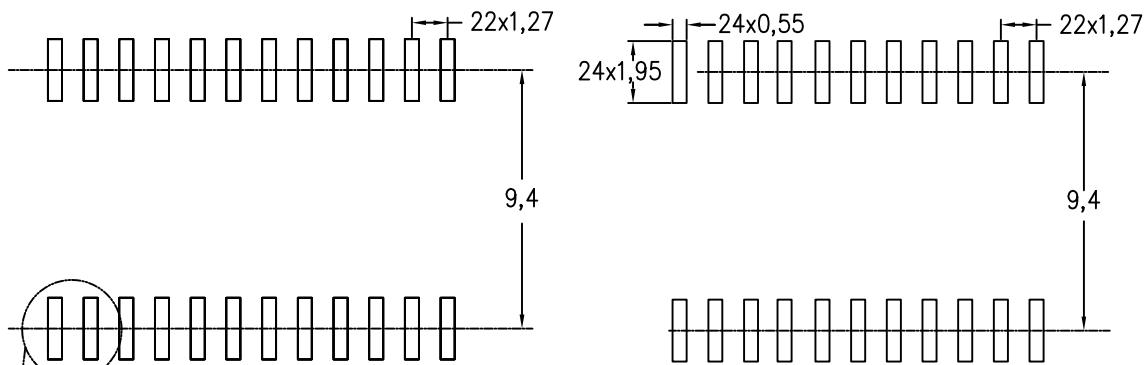


NOTES:

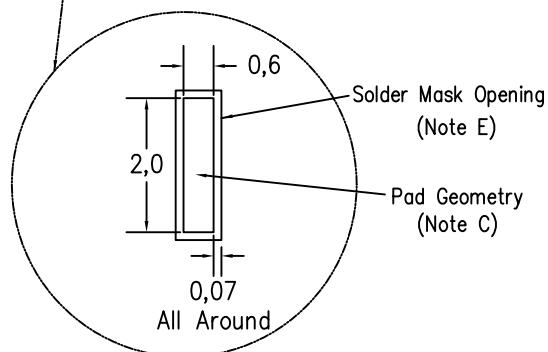
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MS-013 variation AD.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)

Non Solder Mask Define Pad



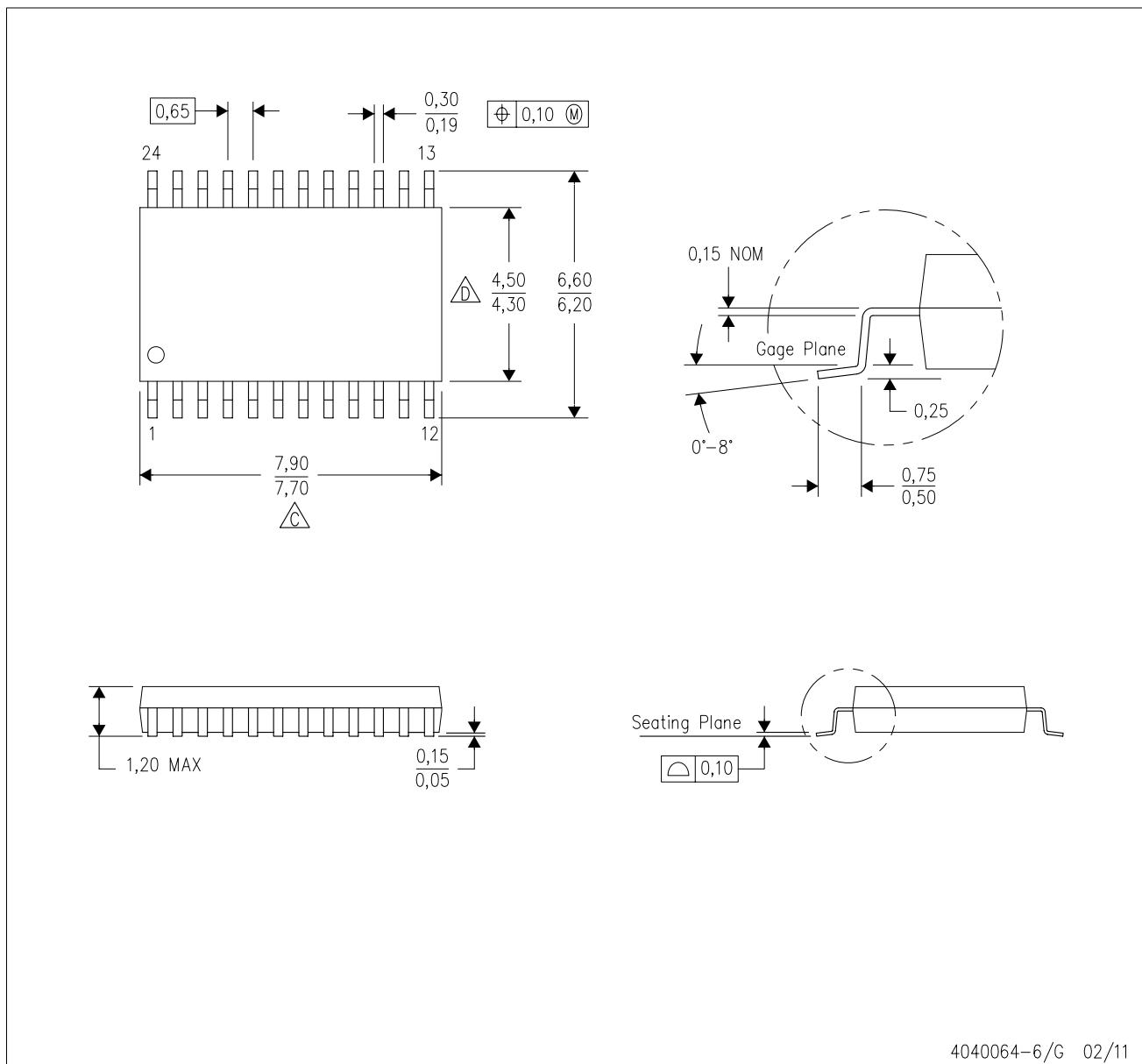
4209202-5/F 08/13

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Refer to IPC7351 for alternate board design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



4040064-6/G 02/11

NOTES:

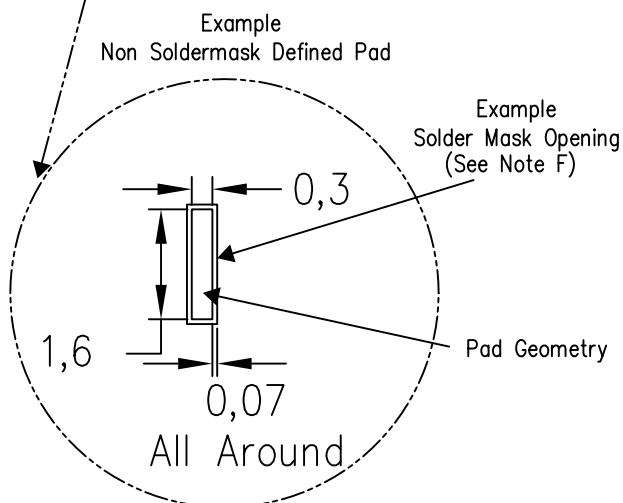
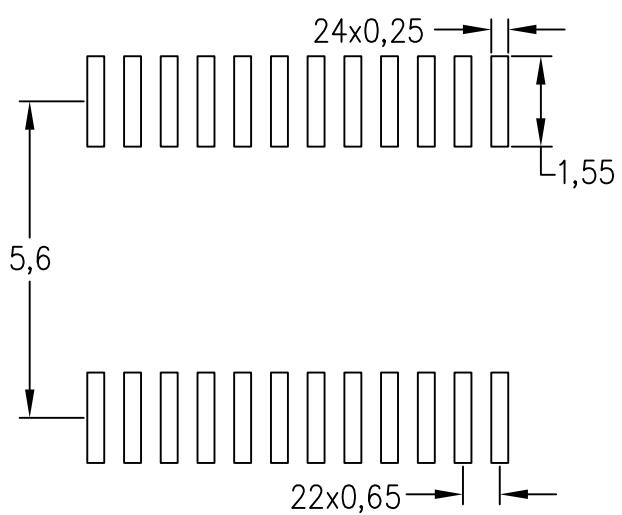
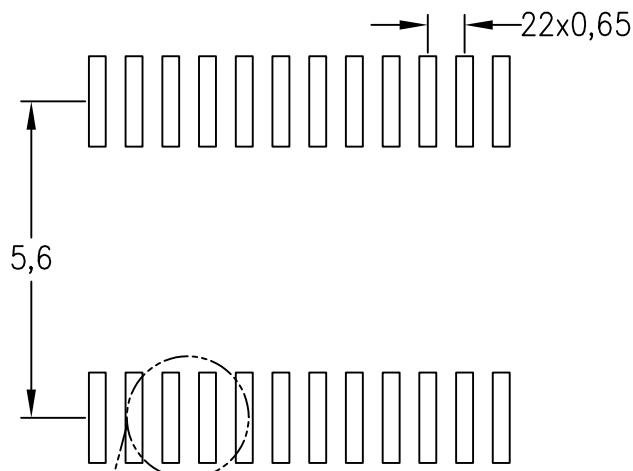
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153

## PW (R-PDSO-G24)

## PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings  
Based on a stencil thickness  
of .127mm (.005inch).



4211284-4/F 12/12

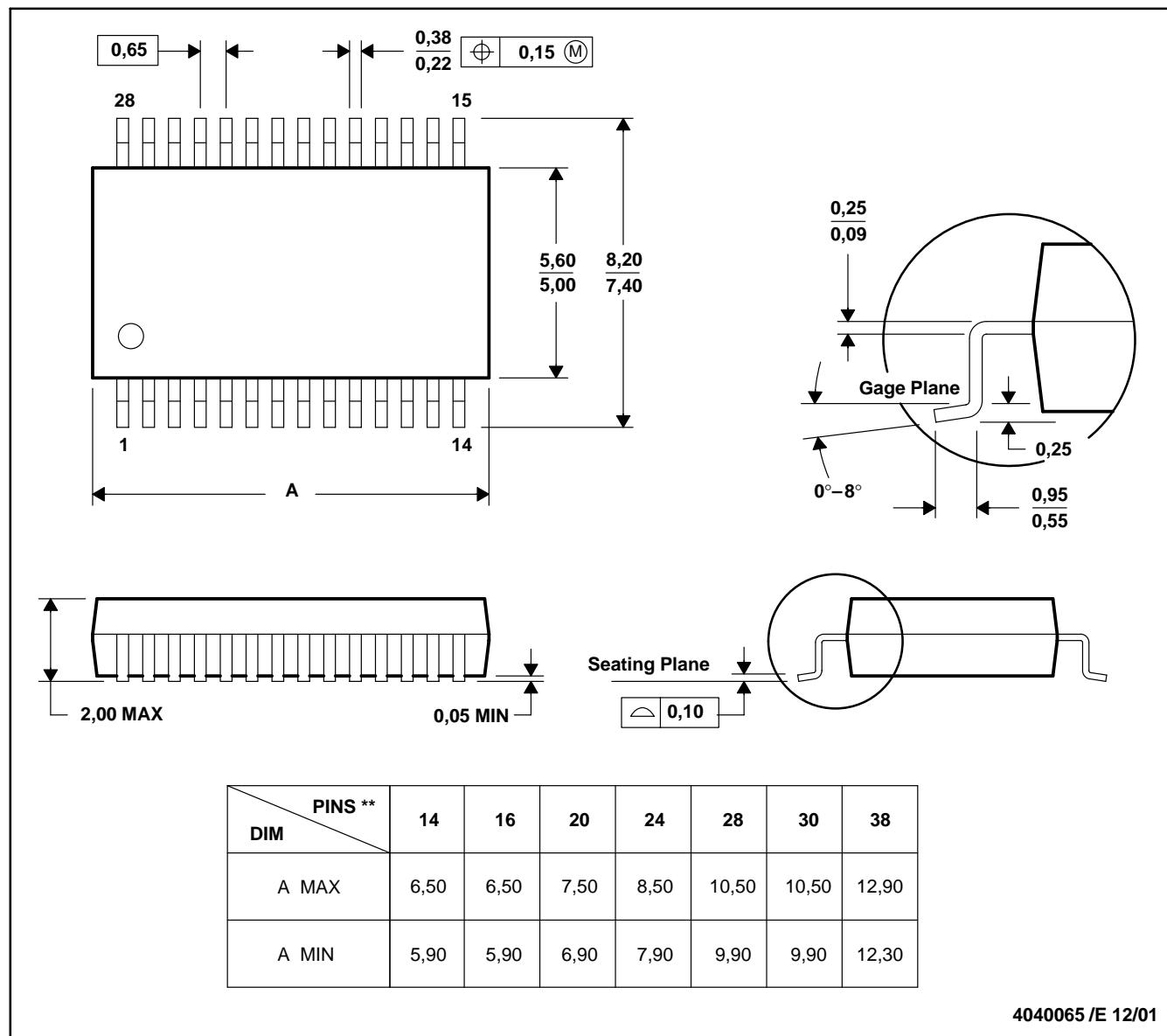
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
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Interface	<a href="http://interface.ti.com">interface.ti.com</a>
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