SCLS134B - DECEMBER 1982 - REVISED MAY 1997

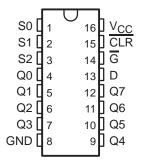
- 8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion With Storage
- Asynchronous Parallel Clear
- Active-High Decoder
- Enable Input Simplifies Expansion
- Expandable for n-Bit Applications
- Four Distinct Functional Modes
- Package Options Include Plastic Small-Outline (D), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

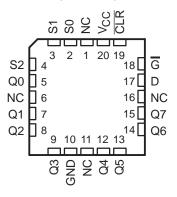
These 8-bit addressable latches are designed for general-purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

Four distinct modes of operation are selectable by controlling the clear (\overline{CLR}) and enable (\overline{G}) inputs. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch follows the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, \overline{G} should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output follows the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

SN54HC259 . . . J OR W PACKAGE SN74HC259 . . . D, N, OR PW PACKAGE (TOP VIEW)



SN54HC259 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

The SN54HC259 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC259 is characterized for operation from –40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



Function Tables

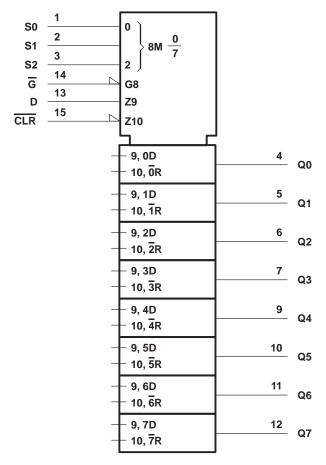
FUNCTION

INPL	JTS	OUTPUT OF ADDRESSED	EACH OTHER	EUNCTION			
CLR	G	LATCH	OUTPUT	FUNCTION			
Н	L	D	Q _{iO}	Addressable latch			
Н	Н	Q _{iO}	Q_{iO}	Memory			
L	L	D	L	8-line demultiplexer			
L	Н	L	L	Clear			

LATCH SELECTION

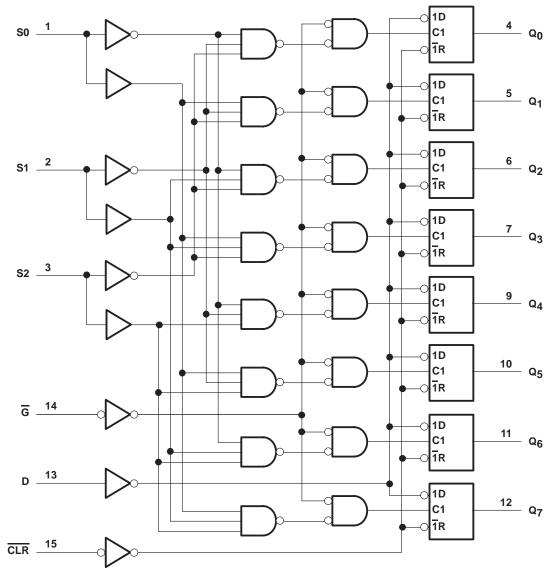
SEL	ECT INF	LATCH	
S2	S 1	S0	ADDRESSED
L	L	L	0
L	L	Н	1
L	Н	L	2
L	Н	Н	3
Н	L	L	4
Н	L	Н	5
Н	Н	L	6
Н	Н	Н	7

logic symbol†



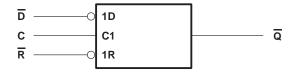
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, N, PW, and W packages.

logic diagram (positive logic)

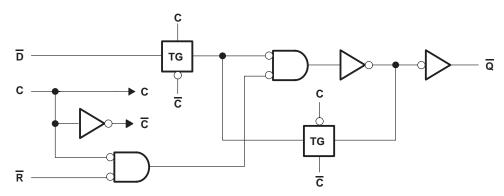


Pin numbers shown are for the D, J, N, PW, and W packages.

logic symbol, each internal latch



logic diagram, each internal latch (positive logic)



absolute maximum ratings over operating free-air temperature range[†]

Supply voltage range, V _{CC}		–0.5 V to	o 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see	ee Note 1)	±20	0 mA
Output clamp current, IOK (VO < 0 or VO > VCO	c) (see Note 1)	±20	0 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})		±2	5 mA
Continuous current through V _{CC} or GND		±50	0 mA
Package thermal impedance, θ _{JA} (see Note 2):			
•	N package		°C/W
	PW package		°C/W
Storage temperature range, T _{stq}		–65°C to 1	50°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

SN54HC259, SN74HC259 8-BIT ADDRESSABLE LATCHES

SCLS134B - DECEMBER 1982 - REVISED MAY 1997

recommended operating conditions

			SI	N54HC25	59	SN74HC259		59	LINIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		2	5	6	2	5	6	V
		V _{CC} = 2 V	1.5			1.5			
V_{IH}	High-level input voltage	V _{CC} = 4.5 V	3.15			3.15			V
		VCC = 6 V	4.2			4.2		MAX	
	Input voltage	V _{CC} = 2 V	0		0.5	0		0.5	
V_{IL}		V _{CC} = 4.5 V	0		1.35	0		1.35	V
		VCC = 6 V	0		1.8	0		0.5 1.35 1.8 VCC VCC 1000 500 400	
VI	Input voltage		0		VCC	0		VCC	V
VO	Output voltage		0		VCC	0		VCC	V
		V _{CC} = 2 V	0		1000	0		1000	
t _t	Input transition (rise and fall) time	$V_{CC} = 4.5 \text{ V}$	0		500	0		500	ns
		V _{CC} = 6 V	0	2 5 6 2 5 6 1.5 1.5 3.15 3.15 4.2 4.2 0 0.5 0 0.5 0 1.35 0 1.35 0 1.8 0 1.8 0 VCC 0 VCC 0 VCC 0 VCC 0 1000 0 1000 0 500 0 500 0 400 0 400					
TA	Operating free-air temperature		-55		125	-40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS		V	T _A = 25°C		SN54HC259		SN74HC259		UNIT	
PARAMETER	l lEST CC	SNOTHONS	vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
			2 V	1.9	1.998		1.9		1.9		
		I _{OH} = -20 μA	4.5 V	4.4	4.499		4.4		4.4		
Voн	VI = VIH or VIL		6 V	5.9	5.999		5.9		5.9		V
		$I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.3		3.7		3.84		
		$I_{OH} = -5.2 \text{ mA}$	6 V	5.48	5.8		5.2		5.34		
	VI = VIH or VIL	I _{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	
			4.5 V		0.001	0.1		0.1		0.1	
VOL			6 V		0.001	0.1		0.1		0.1	V
		I _{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I _{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
lį	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
Icc	$V_I = V_{CC}$ or 0,	I _O = 0	6 V			8		160		80	μΑ
C _i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			Vac		25°C	SN54F	IC259	SN74H	IC259	UNIT
			vcc	MIN	MAX	MIN	MAX	MIN	MAX	UNII
t _W Pulse duration			2 V	80		120		100		
		CLR low	4.5 V	16		24		20		
	Dulgo duration		6 V	14		20		17		
	ruise duration		2 V	80		120		100		ns
		G low	4.5 V	16		24		20		
			6 V	14		20		17		
		•		75		115		95		
t _{su}	Setup time, data or address before $\overline{G}\!\!\uparrow$		4.5 V	15		23		19		ns
			6 V	13		20		16		
			2 V	5		5		5		ns
th	Hold time, data or address after $\overline{G} \!\!\uparrow$		4.5 V	5		5		5		
			6 V	5		5		5		

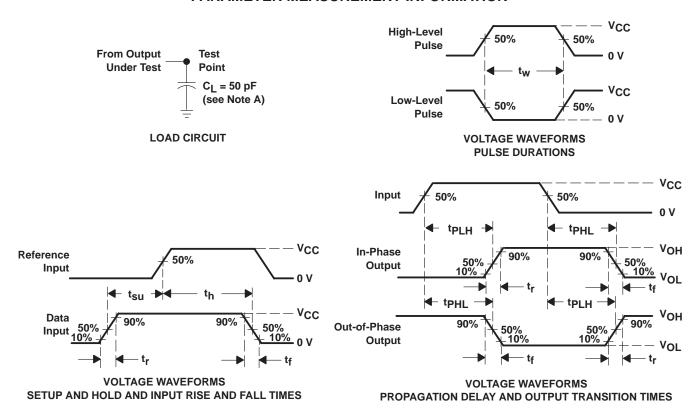
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	Vaa	T,	ղ = 25°C	;	SN54H	IC259	SN74H	IC259	LINIT						
PARAMETER	(INPUT)	(OUTPUT)	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT						
			2 V		60	150		225		190							
t _{PHL}	CLR	Any Q	4.5 V		18	30		45		38	ns						
			6 V		14	26		38		32							
			2 V		56	130		195		165							
	Data Any Q	Any Q	4.5 V		17	26		39		33							
			6 V		13	22		33		28							
		Any Q	2 V		74	200		300		250							
^t pd	Address		4.5 V		21	40		60		50	ns						
			6 V		17	34		51		43]						
		Any Q	2 V		66	170		255		215							
	G		4.5 V		20	34		51		43							
			6 V		16	29		43		37							
			2 V		28	75		110		95							
t _t		Any	Any	Any	Any	Any	Any	Any	4.5 V		8	15		22		19	ns
			6 V		6	13		19		16							

operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per latch	No load	33	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.

- B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \ \Omega$, $t_r = 6 \ ns$, $t_f = 6 \ ns$.
- C. The outputs are measured one at a time with one input transition per measurement.
- D. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 1998, Texas Instruments Incorporated