International
IOR Rectifier

Data Sheet No. PD60347A

IRS26310DJPbF

HIGH VOLTAGE 3 PHASE GATE DRIVER IC WITH DC BUS OVER –VOLTAGE PROTECTION

Features

- Drives up to six IGBT/MOSFET power devices
- Gate drive supplies up to 20 V per channel
- Integrated bootstrap functionality
- DC bus sensing with Over Voltage protection
- Over-current protection
- Over-temperature shutdown input
- Advanced input filter
- Integrated deadtime protection
- Shoot-through (cross-conduction) protection
- Under voltage lockout for V_{CC} & V_{BS}
- Enable/disable input and fault reporting
- Adjustable fault clear timing
- Separate logic and power grounds
- 3.3 V input logic compatible
- Tolerant to negative transient voltage
- Designed for use with bootstrap power supplies
- Matched propagation delays for all channels
- -40 °C to 125 °C operating range
- RoHS compliant

Typical Applications

- Permanent magnet motor drives for appliances
- Industrial drives
- Micro inverter drives

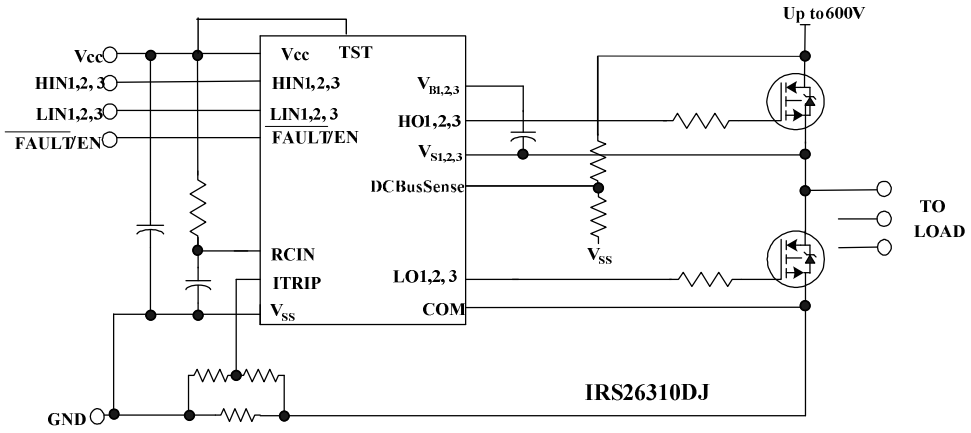
Product Summary

Topology	3 Phase
V_{OFFSET}	≤ 600 V
V_{OUT}	12 V – 20 V
I_{o+} & I_{o-} (typical)	200 mA & 350 mA
t_{ON} & t_{OFF} (typical)	530 ns & 530 ns
Deadtime (typical)	290 ns

Package Options

44-Lead PLCC (without 12 leads)

Typical Connection Diagram



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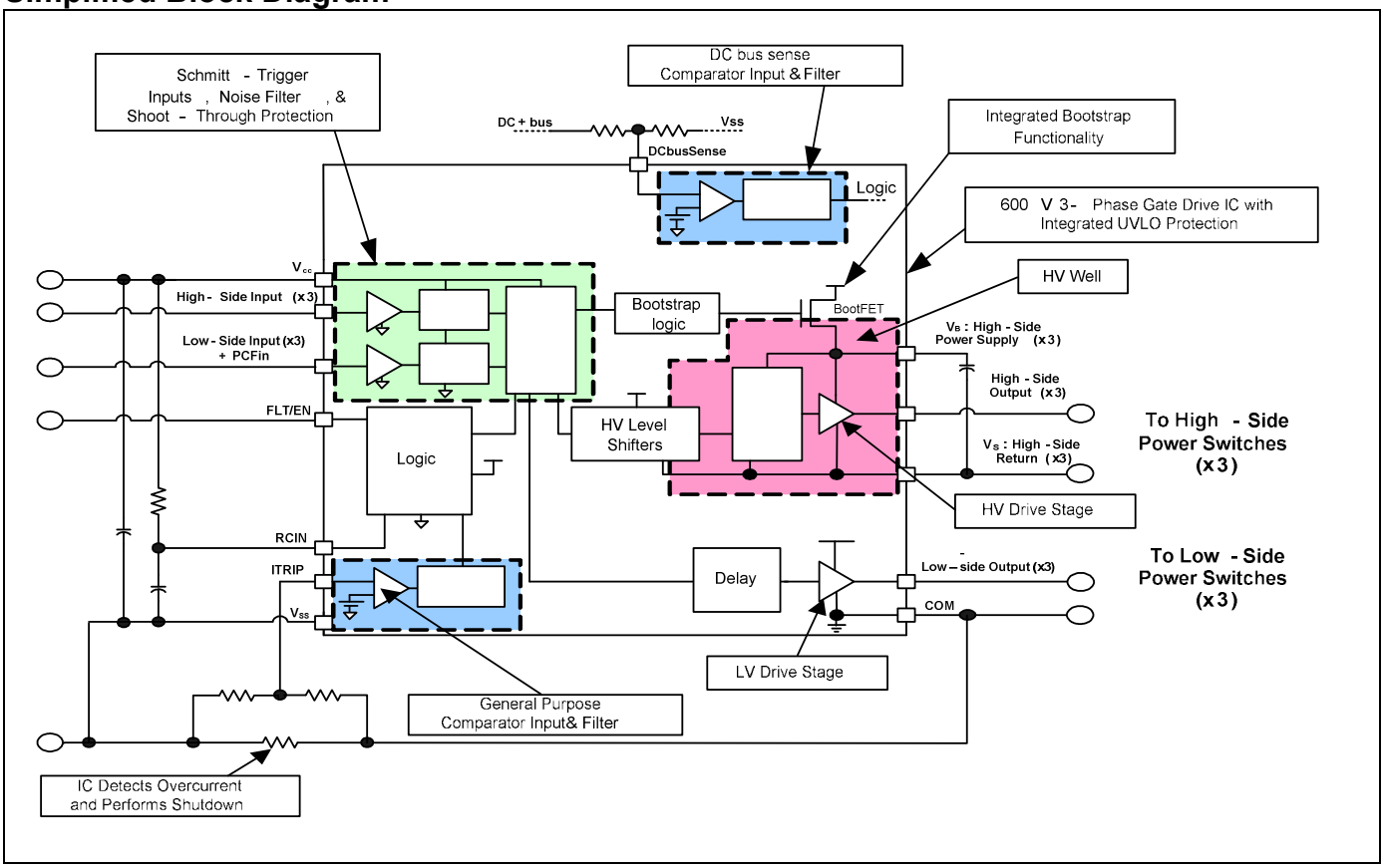
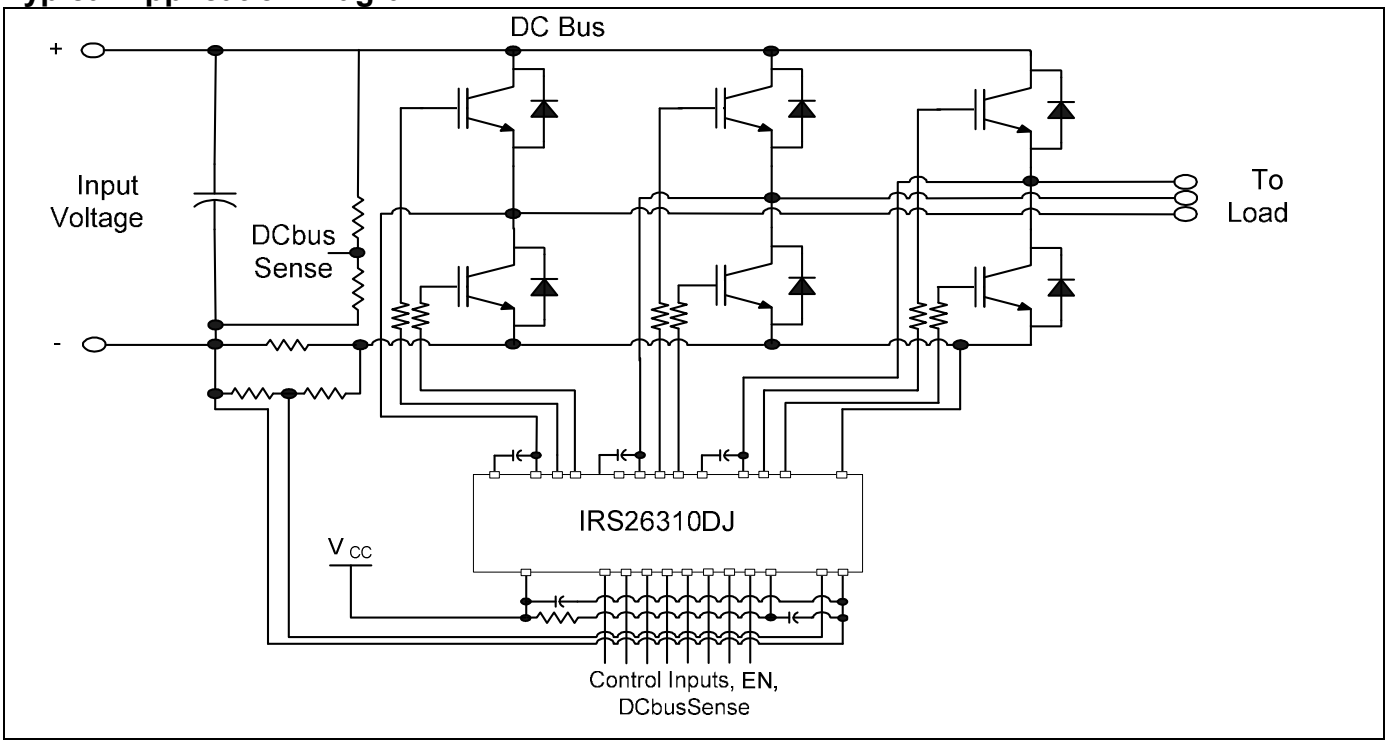
Description

The IRS26310DJPBF is a high voltage, high speed power MOSFET and IGBT driver with three independent high and low side referenced output channels for 3-phase applications. This IC is designed to be used with low-cost bootstrap power supplies; the bootstrap diode functionality has been integrated into this device to reduce the component count and the PCB size. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 3.3V logic. A current trip function which terminates all six outputs can be derived from an external current sense resistor. An enable function is available to terminate all six outputs simultaneously. An open-drain FAULT signal is provided to indicate that an overcurrent or a VCC undervoltage shutdown has occurred. Overcurrent fault conditions are cleared automatically after a delay programmed externally via an RC network connected to the RCIN input. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 600 V. A DCbus sensing is provided using an external divider. Over Voltage DCbus protection is activate when DCbus exceed an externally adjustable threshold, activating zero-vector braking mode (all Low side output turn-on, all High side output-turn-off).

Simplified Block Diagram



Typical Application Diagram



Qualification Information†

Qualification Level		Industrial††	
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level		PLCC44	MSL3††† , 245°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class B (per JEDEC standard JESD22-A114)	
	Human Body Model	Class 2 (per EIA/JEDEC standard EIA/JESD22-A115)	
	Charged Device Model	Class IV (per JEDEC standard JESD22-C101)	
IC Latch-Up Test		Class I, Level A (per JESD78)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to V_{SS} unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Voltage clamps are included between V_{CC} & COM (25 V), V_{CC} & V_{SS} (20 V), and V_B & V_S (20 V).

Symbol	Definition	Min.	Max.	Units
V_S	High side offset voltage	V_B - 20†	V_B + 0.3	V
V_{TST}	TST Voltage	-0.3	20	
V_B	High side floating supply voltage	-0.3	620	
V_{HO}	High side floating output voltage	V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage	-0.3	20	
V_{SS}	Logic ground	V_{CC} - 20	V_{CC} + 0.3	
$V_{LO1,2,3}$	Low side output voltage	-0.3	V_{CC} + 0.3	
V_{IN}	Input voltage LIN, HIN, ITRIP, EN, RCIN	V_{SS} -0.3	V_{CC} + 0.3	
V_{FLT}	FAULT output voltage	V_{SS} -0.3	V_{CC} + 0.3	
$V_{DCBusSense}$	Input sensing for DC_{BUS} voltage	V_{SS} -0.3	V_{CC} + 0.3	
dV/dt	Allowable offset voltage slew rate	—	50	V/ns
P_D	Package power dissipation @ TA ≤ +25°C	—	2	W
Rth_{JA}	Thermal resistance, junction to ambient	—	63	°C/W
T_J	Junction temperature	—	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

† All supplies are fully tested at 25 V. An internal 20 V clamp exists for each supply.

Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to V_{SS} unless otherwise stated in the table. The offset rating is tested with supplies of (V_{CC}-COM) = (V_B-V_S) = 15 V.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply voltage	V_S +12	V_S + 20	V
V_S	High side floating supply voltage†	COM-8	600	
$V_S(t)$	Transient high-side floating supply voltage††	-50	600	
V_{TST}	TST Voltage	12	20	
V_{CC}	Low side supply voltage	12	20	
V_{HO}	High side output voltage	V_S	V_B	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{SS}	Logic ground	-5	5	
V_{FLT}	FAULT output voltage	V_{SS}	V_{CC}	
V_{RCIN}	RCIN input voltage	V_{SS}	V_{CC}	
V_{ITRIP}	ITRIP input voltage	V_{SS}	$V_{SS\ +\ 5}$	
V_{IN}	Logic input voltage LIN, HIN, EN	V_{SS}	$V_{SS\ +\ 5}$	
$V_{DCBusSense}$	Input sensing for DCbus voltage†††	V_{SS}	V_{CC}	
T_A	Ambient temperature	-40	125	°C

† Logic operation for V_S of –8 V to 600 V. Logic state held for V_S of –8 V to $–V_{BS}$. Please refer to Design Tip DT97-3 for more details.

†† Operational for transient negative V_S of V_{SS} - 50 V with a 50 ns pulse width. Guaranteed by design. Refer to the Application Information section of this datasheet for more details.

††† DCBusSense pin is internally clamped with a 10.4 V zener diode.

Static Electrical Characteristics

(V_{CC}-COM) = (V_B-V_S) = 15 V. T_A = 25 °C unless otherwise specified. The V_{IN} ,V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels. The V_O and I_O parameters are referenced to respective V_S and COM and are applicable to the respective output leads HO or LO. The V_{CCUV} parameters are referenced to V_{SS}. The V_{BSUV} parameters are referenced to V_S.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input	2.5	—	—	V	
V_{IL}	Logic "0" input	—	—	0.8		
$V_{IN,TH+}$	Input positive going threshold	—	1.9	—		
$V_{IN,TH-}$	Input negative going threshold	—	1	—		
$V_{EN,TH+}$	Enable positive going threshold	—	—	2.5		
$V_{EN,TH-}$	Enable negative going threshold	0.8	—	—		
$V_{IT,TH+}$	ITRIP positive going threshold	0.37	0.46	0.55		
$V_{IT,HYS}$	ITRIP hysteresis	0.05	0.07	—		
$V_{RCIN,\ TH+}$	RCIN positive going threshold	—	8	—		
$V_{RCIN,\ HYS}$	RCIN hysteresis	—	3	—		
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	—	1.12	1.74		I_O = 20 mA
V_{OL}	Low level output voltage, V_O	—	0.4	0.6		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	10.4	11.1	11.6		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	10.2	10.9	11.4		
$V_{CCUVHYS}$	V_{CC} supply undervoltage hysteresis	0.17	0.2	—		
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	10.4	11.1	11.6		
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	10.2	10.9	11.4		
V_{BSUVHY}	V_{BS} supply undervoltage hysteresis	0.17	0.2	—		
$V_{DCBUSSTH+}$	Over voltage DCBusSense positive going threshold	3.86	4.20	4.54		Note 1
$V_{DCBUSSTH-}$	Over voltage DCBusSense negative going threshold	3.70	4.03	4.35		
$V_{DCBUSSHYS}$	Over voltage DCBusSense hysteresis	0.14	0.17	—		
I_{LK}	Offset supply leakage current	—	3	50		V_B =V_S = 600 V
I_{QBS}	Quiescent V_{BS} supply current	—	50	120		All inputs @ logic 0 value
I_{QCC}	Quiescent V_{CC} supply current	—	3	4	mA	
I_{IN+}	Input bias current (Lo or Ho= High)	—	100	150	uA	V_{IN} = 3.3 V
I_{IN-}	Input bias current (Lo or Ho = Low)	-1	0	—		V_{IN} = 0 V
I_{ITRIP+}	"High" ITRIP input bias current	—	5	40		V_{ITRIP} = 5 V
I_{ITRIP-}	"Low" ITRIP input bias current	-1	0	—		V_{ITRIP} = 0 V
$I_{FLT/EN+}$	"High" FLT/ENABLE input bias current	—	0	1		$V_{FLT/EN}$ = 3.3 V
$I_{FLT/EN-}$	"Low" FLT/ENABLE input bias current	-1	0	—		$V_{FLT/EN}$ = 0 V
$I_{DCBUSSENSE+}$	"High" DCBusSense input bias current	—	0	1		$V_{DCBSENSE}$ = 5 V
$I_{DCBUSSENSE-}$	"Low" DCBusSense input bias current	-1	0	—		$V_{DCBSENSE}$ = 0 V

Note 1: Guaranteed by design over a temperature range of 0ºC to 110ºC

Static Electrical Characteristics (continued)

(V_{CC}-COM) = (V_B-V_S) = 15 V. T_A = 25 °C unless otherwise specified. The V_{IN} ,V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels. The V_O and I_O parameters are referenced to respective V_S and COM and are applicable to the respective output leads HO or LO. The V_{CCUV} parameters are referenced to V_{SS}. The V_{BSUV} parameters are referenced to V_S.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
I_{RCIN+}	"High" RCIN input bias current	—	0	1	uA	V_{RCIN} = 15 V
I_{RCIN-}	"Low" RCIN input bias current	-1	0	—		V_{RCIN} = 0 V
Io+	Output high short circuit pulsed current	120	200	—	mA	Vo = 0 V, PW ≤ 10 µs
Io-	Output low short circuit pulsed current	250	350	—		Vo = 15 V, PW ≤ 10 µs
R_{on_RCIN}	RCIN low on resistance	—	50	100	Ω	I = 1.5 mA
$R_{on\_FAULTEN}$	FAULT low on resistance	—	50	100		
R_{BS}	Internal bootstrap diode Ron	—	200	400		

Dynamic Electrical Characteristics

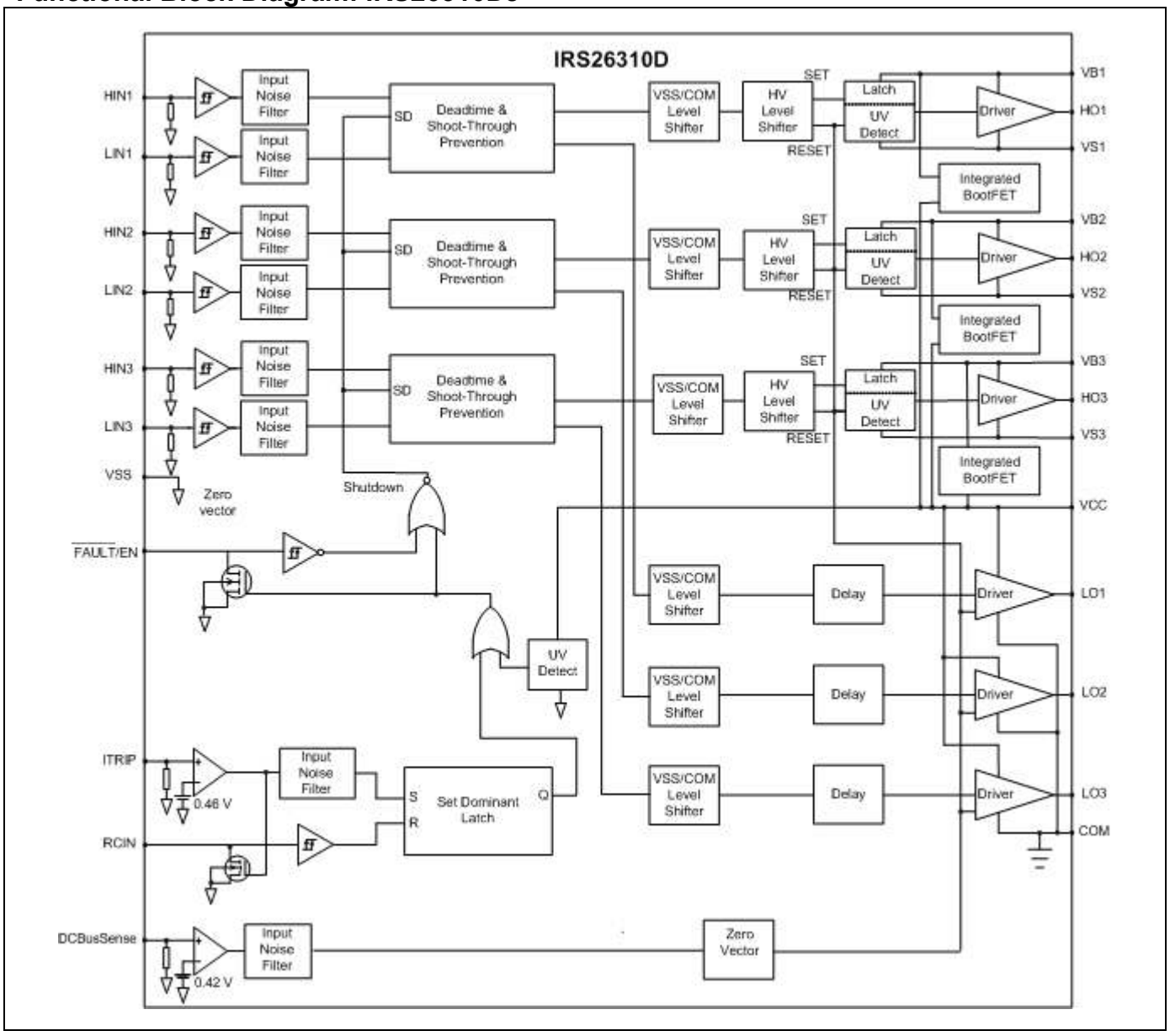
V_{CC}= V_B = 15 V, V_S = V_{SS} = COM, T_A = 25 °C, and C_L = 1000 pF unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	400	530	750	ns	V_{IN} = 0V & 5V
t_{off}	Turn-off propagation delay	400	530	750		
t_r	Turn-on rise time	—	125	190		
t_f	Turn-off fall time	—	50	75		
t_{ITRIP}	ITRIP to output shutdown propagation delay	500	750	1200		V_{ITRIP} = 5V
t_{ITRIP_blk}	ITRIP blanking time	—	500	750		V_{IN} = 0V & 5V V_{ITRIP} = 5V
t_{FLT}	ITRIP to FAULT propagation delay	400	600	950		
t_{ENOUT}	ENABLE high to output propagation delay	350	460	650		V_{IN} = 0V & 5V V_{EN} = 0V & 3.3V
t_{SDOUT}	ENABLE low to output shutdown propagation delay	350	460	650		
$t_{ZV\_DCBS\_LOon}$	DCBusSense entering Over voltage to LO turn on	310	460	730		$V_{DCBSENSE}$ = 0V & 5V
$t_{ZV\_DCBS\_HOoff}$	DCBusSense entering Over voltage to HO turn off	310	460	730		
$t_{ZV\_DCBS\_HOon}$	DCBusSense exiting Over voltage to HO turn on	270	380	590		
$t_{ZV\_DCBS\_LOoff}$	DCBusSense exiting Over voltage to LO turn off	300	450	720		
$t_{ZV\_DCBS\_flt\_LO}$	DCBusSense input filter time on LO	140	250	420		
$t_{ZV\_DCBS\_flt\_HO}$	$DC_{BUS}S_{ENSE}$ input filter time on HO	140	250	420		
t_{FILIN}	Input filter time (HIN, LIN) †	200	350	510	ns	V_{IN} = 0V & 5V
$t_{FILTEREN}$	Enable input filter time	100	200	—		
DT	Deadtime	190	290	420		V_{IN} = 0V & 5V External dead time 0s
MT	Ton, Toff matching time (on all six channels)	—	—	50		
MDT	DT matching (HIN->LO & LO->HIN on all channels)	—	—	60		
PM	Pulse width distortion ††	—	—	75		PW input =10µs
t_{FLTCLR}	FAULT clear time RCIN: R = 2 meg, C = 1nF	1.3	1.65	2	ms	V_{IN} = 0V or 5V V_{ITRIP} = 0V

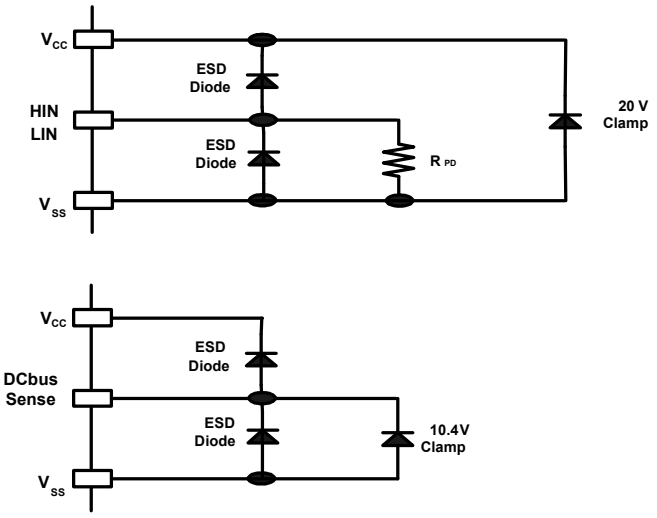
† The minimum width of the input pulse is recommended to exceed 500 ns to ensure the filtering time of the input filter is exceeded.

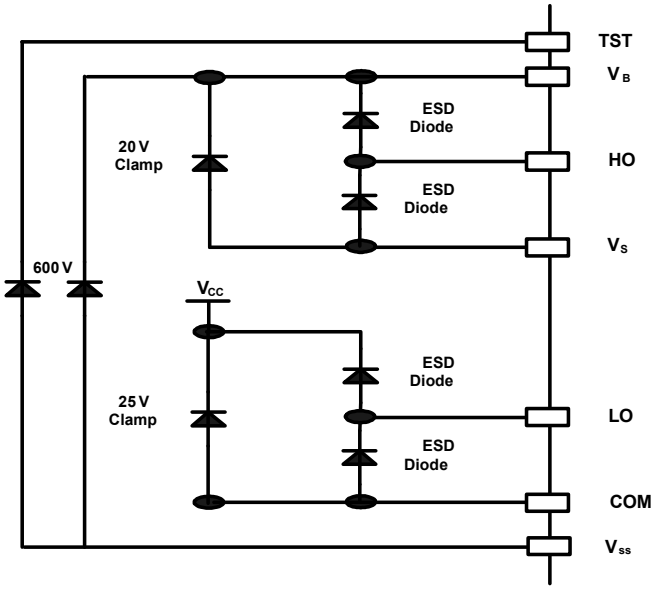
†† PM is defined as PW_{IN} - PW_{OUT}.

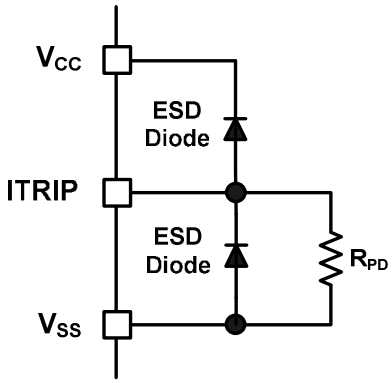
Functional Block Diagram: IRS26310DJ

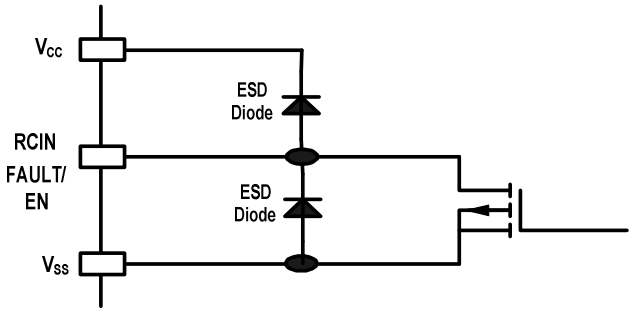


Input/Output Pin Equivalent Circuit Diagrams: IRS26310D





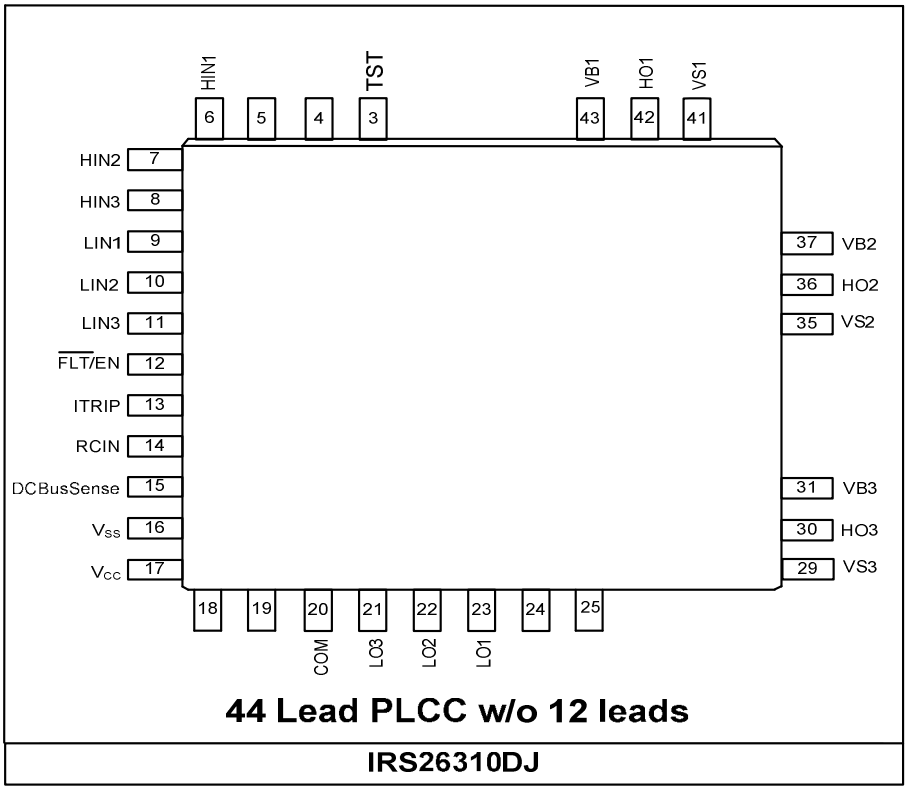




Lead Definitions: IRS26310DJ

Symbol	Description
VCC	Low-side supply voltage
VSS	Logic ground
TST	TST to be shorted to VCC
VB1	High-side gate drive floating supply (phase 1)
VB2	High-side gate drive floating supply (phase 2)
VB3	High-side gate drive floating supply (phase 3)
VS1	High voltage floating supply return (phase 1)
VS2	High voltage floating supply return (phase 2)
VS3	High voltage floating supply return (phase 3)
HIN1	Logic inputs for high-side gate driver outputs (phase 1)
HIN2	Logic inputs for high-side gate driver outputs (phase 2)
HIN3	Logic inputs for high-side gate driver outputs (phase 3
LIN1	Logic inputs for low-side gate driver outputs (phase 1)
LIN2	Logic inputs for low-side gate driver outputs (phase 2)
LIN3	Logic inputs for low-side gate driver outputs (phase 3)
HO1	High-side driver outputs (phase 1)
HO2	High-side driver outputs (phase 2)
HO3	High-side driver outputs (phase 3)
LO1	Low-side driver outputs (phase 1)
LO2	Low-side driver outputs (phase 2)
LO3	Low-side driver outputs (phase 3)
COM	Low-side gate drive return
FAULT/N EN	Indicates over-current, over-temperature (ITRIP), or low-side undervoltage lockout has occurred. This pin has negative logic and an open-drain output. The use of over-current and over-temperature protection requires the use of external components. Logic input to shutdown functionality. Logic functions when EN is high (i.e., positive logic). No effect on FAULT and not latched.
ITRIP	Analog input for over-current shutdown. When active, ITRIP shuts down outputs and activates FAULT and RCIN low. When ITRIP becomes inactive, FAULT stays active low for an externally set time t_{FLTCLR}, then automatically becomes inactive (open-drain high impedance).
DCbusSense	Analog input for DCbus sensing
RCIN	An external RC network input used to define the FAULT CLEAR delay (t_{FLTCLR}) approximately equal to R*C. When RCIN > 8 V, the FAULT pin goes back into an open-drain high-impedance state.

Lead Assignments



44 Lead PLCC w/o 12 leads

IRS26310DJ

Application Information and Additional Details

Informations regarding the following topics are included as subsections within this section of the datasheet.

- IGBT/MOSFET Gate Drive
- Switching and Timing Relationships
- Deadtime
- Matched Propagation Delays
- Input Logic Compatibility
- Undervoltage Lockout Protection
- Shoot-Through Protection
- Enable Input
- Fault Reporting and Programmable Fault Clear Timer
- Over-Current Protection
- Over-Temperature Shutdown Protection
- DC bus over-voltage Protection
- Truth Table: Undervoltage lockout, ITRIP, and ENABLE
- Advanced Input Filter
- Short-Pulse / Noise Rejection
- Integrated Bootstrap Functionality
- Bootstrap Power Supply Design
- Separate Logic and Power Grounds
- Tolerant to Negative V_S Transients
- PCB Layout Tips
- Bootstrap FET limitation
- Additional Documentation

IGBT/MOSFET Gate Drive

The IRS26310D HVIC is designed to drive up to six MOSFET or IGBT power devices. Figures 1 and 2 illustrate several parameters associated with the gate drive functionality of the HVIC. The output current of the HVIC, used to drive the gate of the power switch, is defined as I_O. The voltage that drives the gate of the external power switch is defined as V_{HO} for the high-side power switch and V_{LO} for the low-side power switch; this parameter is sometimes generically called V_{OUT} and in this case does not differentiate between the high-side or low-side output voltage.

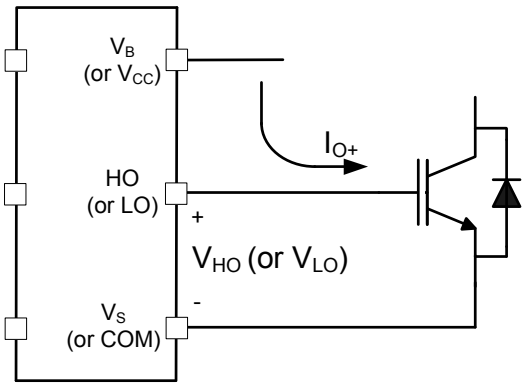


Figure 1: HVIC sourcing current

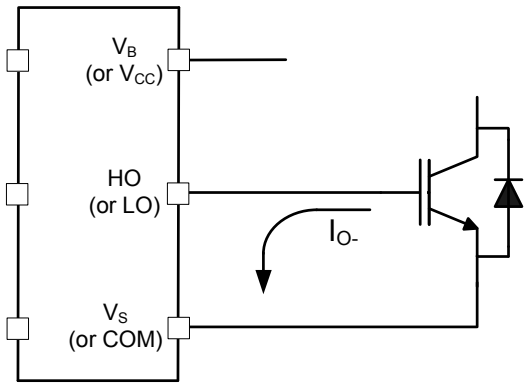


Figure 2: HVIC sinking current

Switching and Timing Relationships

The relationship between the input and output signals of the IRS26310D is illustrated below in Figures 3. From this figure, we can see the definitions of several timing parameters (i.e., PW_{IN}, PW_{OUT}, t_{ON}, t_{OFF}, t_R, and t_F) associated with this device.

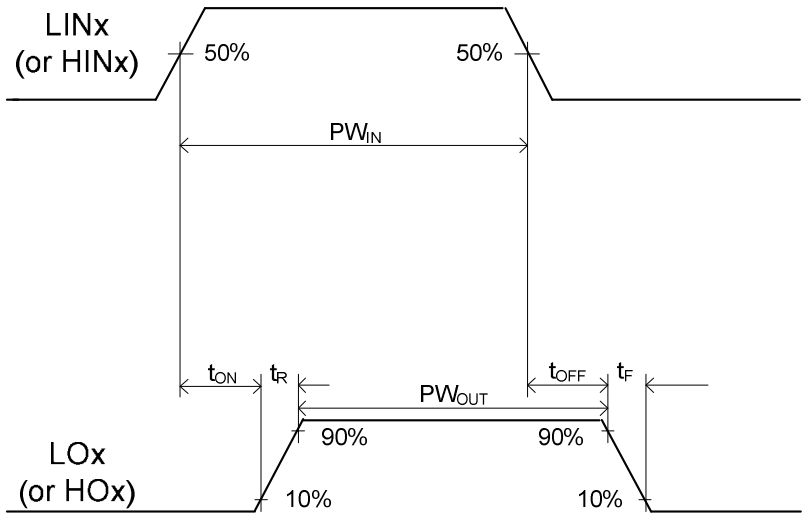


Figure 3: Switching time waveforms

The following two figures illustrate the timing relationships of some of the functionality of the IRS26310D; this functionality is described in further detail later in this document.

During interval A of Figure 4, the HVIC has received the command to turn-on both the high- and low-side switches at the same time; as a result, the shoot-through protection of the HVIC has prevented this condition and both the high- and low-side output are held in the off state.

Interval B of Figures 4 and 5 shows that the signal on the ITRIP input pin has gone from a low to a high state; as a result, all of the gate drive outputs have been disabled (i.e., see that HOx has returned to the low state; LOx is also held low), the voltage on the RCIN pin has been pulled to 0 V, and a fault is reported by the FAULT output transitioning to the low state. Once the ITRIP input has returned to the low state, the output will remain disabled and the fault condition reported until the voltage on the RCIN pin charges up to $V_{RCIN,TH}$ (see interval C in Figure 6); the charging characteristics are dictated by the RC network attached to the RCIN pin.

During intervals D and E of Figure 4, we can see that the enable (EN) pin has been pulled low (as is the case when the driver IC has received a command from the control IC to shutdown); this results in the outputs (HOx and LOx) being held in the low state until the enable pin is pulled high.

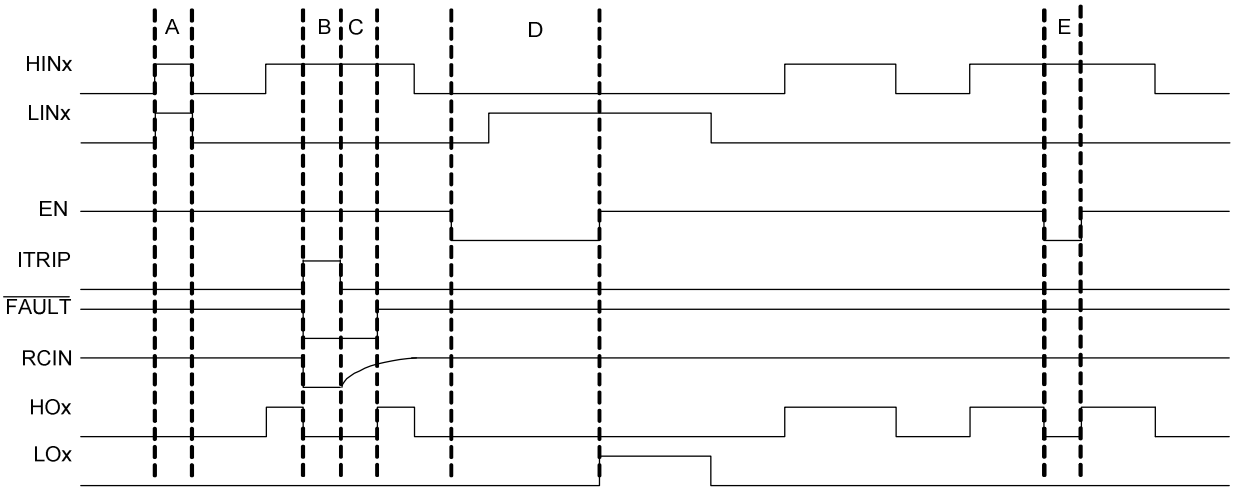


Figure 4: Input/output timing diagram

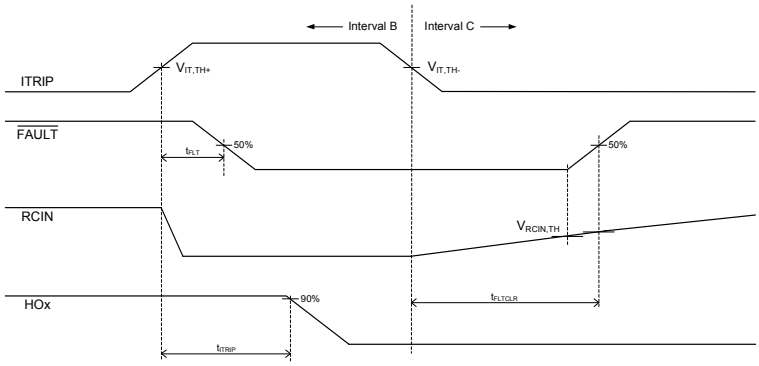


Figure 5: Detailed view of B & C intervals

Deadtime

This family of HVICs features integrated deadtime protection circuitry. The deadtime for these ICs is fixed; other ICs within IR's HVIC portfolio feature programmable deadtime for greater design flexibility. The deadtime feature inserts a time period (a minimum deadtime) in which both the high- and low-side power switches are held off; this is done to ensure that the power switch being turned off has fully turned off before the second power switch is turned on. This minimum deadtime is automatically inserter whenever the external deadtime is shorter than DT; external deadtimes larger than DT are not modified by the gate driver. Figure 6 illustrates the deadtime period and the relationship between the output gate signals.

The deadtime circuitry of the IRS26310D is matched with respect to the high- and low-side outputs of a given channel; additionally, the deadtimes of each of the three channels are matched. Figure 6 defines the two deadtime parameters (i.e., DT_1 and DT_2) of a specific channel; the deadtime matching parameter (MDT) associated with the IRS26310D specifies the maximum difference between DT_1 and DT_2. The MDT parameter also applies when comparing the DT of one channel of the IRS26310D to that of another.

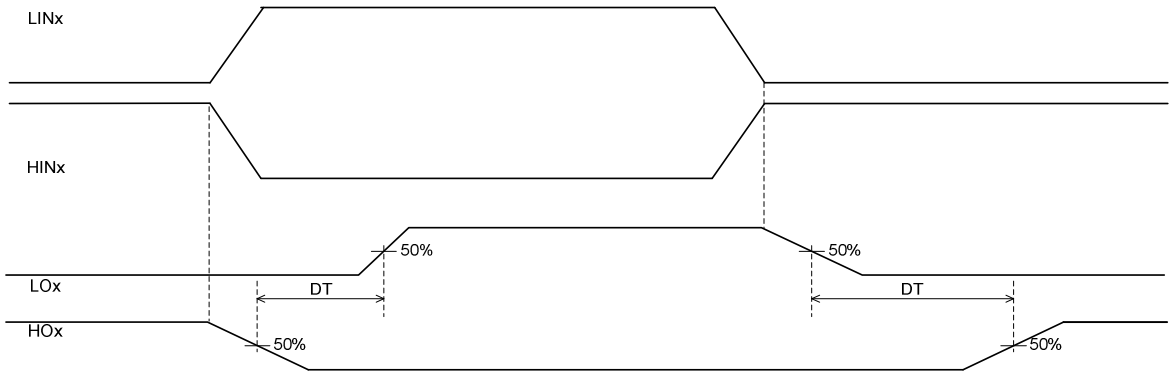


Figure 6: Illustration of deadtime

Matched Propagation Delays

The IRS26310D family of HVICs is designed with propagation delay matching circuitry. With this feature, the IC's response at the output to a signal at the input requires approximately the same time duration (i.e., t_{ON}, t_{OFF}) for both the low-side channels and the high-side channels; the maximum difference is specified by the delay matching parameter (MT). Additionally, the propagation delay for each low-side channel is matched when compared to the other low-side channels and the propagation delays of the high-side channels are matched with each other; the MT specification applies as well. The propagation turn-on delay (t_{ON}) of the IRS26310D is matched to the propagation turn-on delay (t_{OFF}).

Input Logic Compatibility

The inputs of this IC are compatible with standard CMOS and TTL outputs. The IRS26310D has been designed to be compatible with 3.3 V and 5 V logic-level signals. Figure 7 illustrates an input signal to the IRS26310D, its input threshold values, and the logic state of the IC as a result of the input signal.

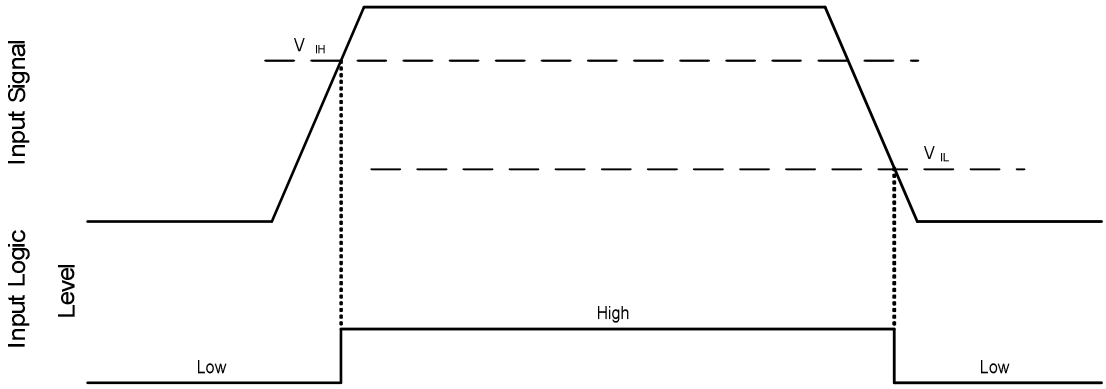


Figure 7: HIN & LIN input thresholds

Undervoltage Lockout Protection

This family of ICs provides undervoltage lockout protection on both the V_{CC} (logic and low-side circuitry) power supply and the V_{BS} (high-side circuitry) power supply. Figure 8 is used to illustrate this concept; V_{CC} (or V_{BS}) is plotted over time and as the waveform crosses the UVLO threshold ($V_{CCUV+/-}$ or $V_{BSUV+/-}$) the undervoltage protection is enabled or disabled.

Upon power-up, should the V_{CC} voltage fail to reach the V_{CCUV+} threshold, the IC will not turn-on. Additionally, if the V_{CC} voltage decreases below the V_{CCUV-} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition and shutdown the high- and low-side gate drive outputs, and the FAULT pin will transition to the low state to inform the controller of the fault condition.

Upon power-up, should the V_{BS} voltage fail to reach the V_{BSUV} threshold, the IC will not turn-on. Additionally, if the V_{BS} voltage decreases below the V_{BSUV} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition, and shutdown the high-side gate drive outputs of the IC.

The UVLO protection ensures that the IC drives the external power devices only when the gate supply voltage is sufficient to fully enhance the power devices. Without this feature, the gates of the external power switch could be driven with a low voltage, resulting in the power switch conducting current while the channel impedance is high; this could result in very high conduction losses within the power device and could lead to power device failure.

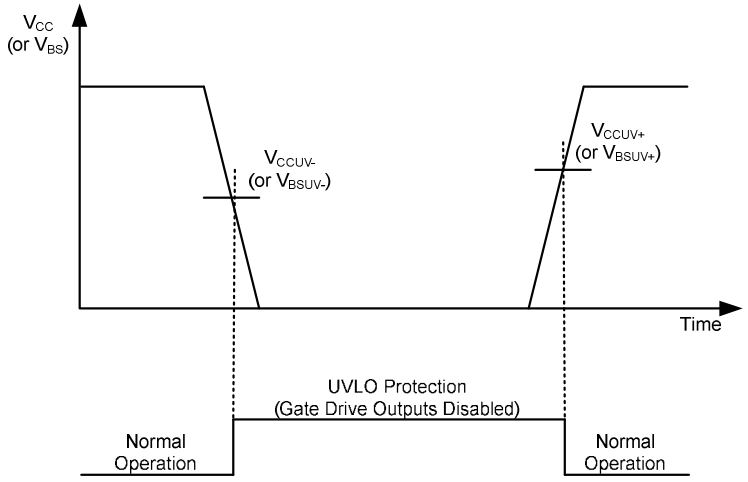


Figure 8: UVLO protection

Shoot-Through Protection

The IRS26310D is equipped with shoot-through protection circuitry (also known as cross-conduction prevention circuitry). Figure 9 shows how this protection circuitry prevents both the high- and low-side switches from conducting at the same time. Table 1 illustrates the input/output relationship of the devices in the form of a truth table. Note that the IRS26310D has non-inverting inputs (the output is in-phase with its respective input).

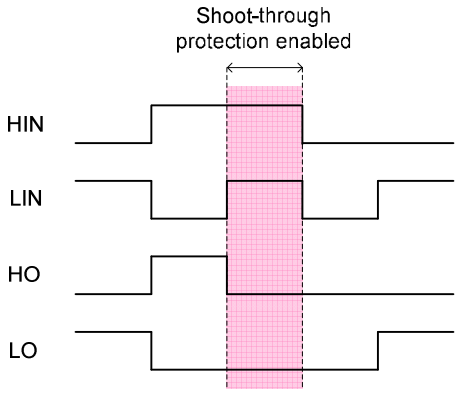


Figure 9: Illustration of shoot-through protection circuitry

IRS26310DJ			
HIN	**LIN**	**HO**	**LO**
0	0	0	0
0	1	0	1
1	0	1	0
1	1	0	0

Table 1: Input/output truth table

Enable Input

The IRS26310D is equipped with an enable input pin that is used to shutdown or enable the HVIC. When the EN pin is in the high state the HVIC is able to operate normally (assuming no other fault conditions). When a condition occurs that should shutdown the HVIC, the EN pin should see a low logic state. The enable circuitry of the IRS26310D features an input filter; the minimum input duration is specified by $t_{FILTER,EN}$. Please refer to the EN pin parameters $V_{EN,TH+}$, $V_{EN,TH-}$, and I_{EN} for the details of its use. Table 2 gives a summary of this pin's functionality and Figure 10 illustrates the outputs' response to a shutdown command.

Enable Input	
Enable input high	Outputs enabled*
Enable input low	Outputs disabled

Table 2: Enable functionality truth table
(*assumes no other fault condition)

Figure 10: Output enable/disable timing waveform

Fault Reporting and Programmable Fault Clear Timer

The IRS26310D family provides an integrated fault reporting output and an adjustable fault clear timer. There are two situations that would cause the HVIC to report a fault via the FAULT pin. The first is an undervoltage condition of V_{CC} and the second is if the ITRIP pin recognizes a fault. Once the fault condition occurs, the FAULT pin is internally pulled to V_{SS} and the fault clear timer is activated. The fault output stays in the low state until the fault condition has been removed and the fault clear timer expires; once the fault clear timer expires, the voltage on the FAULT pin will return to V_{CC}.

The length of the fault clear time period (t_{FLTCLR}) is determined by exponential charging characteristics of the capacitor where the time constant is set by R_{RCIN} and C_{RCIN}. In Figure 11 where we see that a fault condition has occurred (UVLO or ITRIP), RCIN and FAULT are pulled to V_{SS}, and once the fault has been removed, the fault clear timer begins. Figure 12 shows that R_{RCIN} is connected between the V_{CC} and the RCIN pin, while C_{RCIN} is placed between the RCIN and V_{SS} pins.

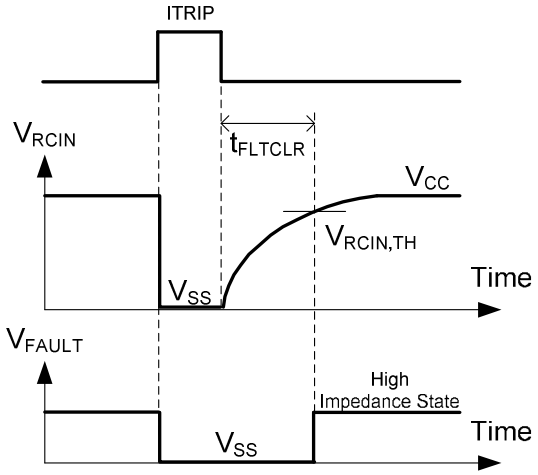


Figure 11: RCIN and FAULT pin waveforms

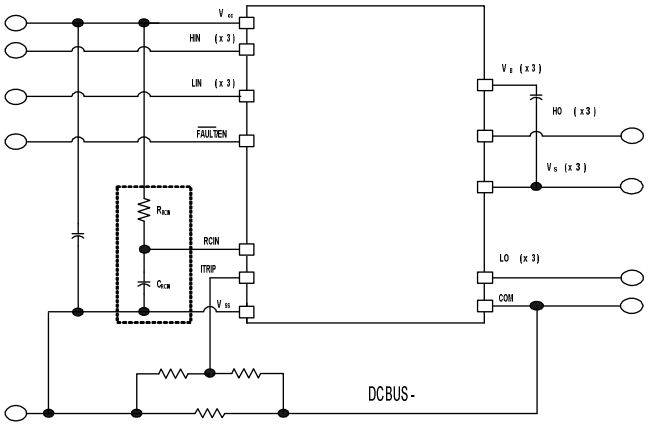


Figure 12: Programming the fault clear timer

The design guidelines for this network are shown in Table 3.

C_{RCIN}	≤1 nF
	Ceramic
R_{RCIN}	0.5 MΩ to 2 MΩ
	>> $R_{ON,RCIN}$

Table 3: Design guidelines

The length of the fault clear time period can be determined by using the formula below.

$$v_C(t) = V_f(1-e^{-t/RC})$$

$$t_{FLTCLR} = -(R_{RCIN}C_{RCIN})\ln(1-V_{RCIN,TH}/V_{CC})$$

Over-Current Protection

The IRS26310D HVICs are equipped with an ITRIP input pin. This functionality can be used to detect over-current events in the DC- bus. Once the HVIC detects an over-current event through the ITRIP pin, the outputs are shutdown, a fault is reported through the FAULT pin, and RCIN is pulled to V_{SS}.

The level of current at which the over-current protection is initiated is determined by the resistor network (i.e., R_0, R_1, and R_2) connected to ITRIP as shown in Figure 14, and the ITRIP threshold ($V_{IT,TH+}$). The circuit designer will need to determine the maximum allowable level of current in the DC- bus and select R_0, R_1, and R_2 such that the voltage at node V_X reaches the over-current threshold ($V_{IT,TH+}$) at that current level.

$$V_{IT,TH+} = R_0 I_{DC-}(R_1/(R_1+R_2))$$

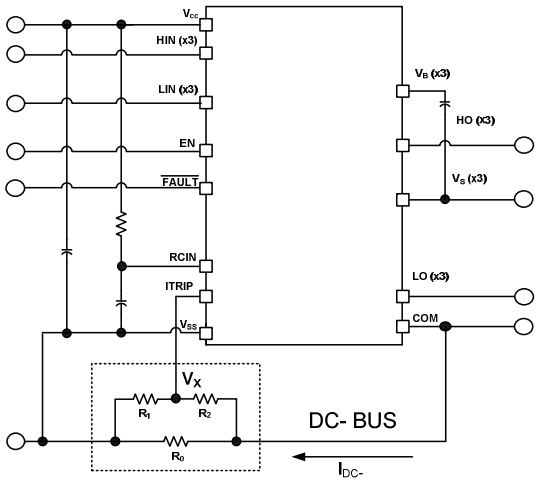


Figure 13: Programming the over-current protection

For example, a typical value for resistor R_0 could be 50 mΩ. The voltage of the ITRIP pin should not be allowed to exceed 5 V; if necessary, an external voltage clamp may be used.

Over-Temperature Shutdown Protection

The ITRIP input of the IRS26310D can also be used to detect over-temperature events in the system and initiate a shutdown of the HVIC (and power switches) at that time. In order to use this functionality, the circuit designer will need to design the resistor network as shown in Figure 14 and select the maximum allowable temperature.

This network consists of a thermistor and two standard resistors R_3 and R_4. As the temperature changes, the resistance of the thermistor will change; this will result in a change of voltage at node V_X. The resistor values should be selected such the voltage V_X should reach the threshold voltage ($V_{IT,TH+}$) of the ITRIP functionality by the time that the maximum allowable temperature is reached. The voltage of the ITRIP pin should not be allowed to exceed 5 V.

When using both the over-current protection and over-temperature protection with the ITRIP input, OR-ing diodes (e.g., DL4148) can be used. This network is shown in Figure 15; the OR-ing diodes have been labeled D_1 and D_2.

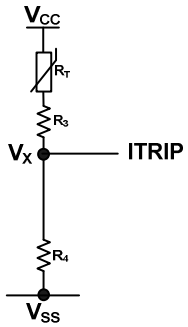


Figure 14: Programming over-temperature protection

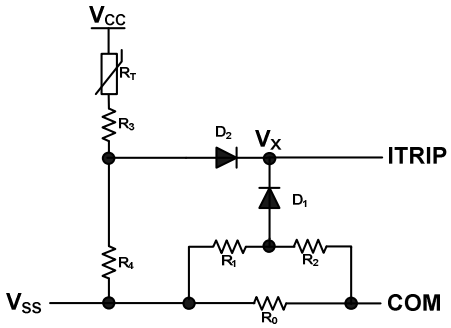


Figure 15: Using over-current protection and over-temperature protection

DC bus Over-Voltage Protection

When driving permanent magnet ac motors there is a potential to regenerate some of the motor mechanical energy back onto the dc bus. “Zero vector braking” prevents charging of the dc bus capacitor by shorting all three motor terminals to a common rail to dissipate this mechanical energy in the motor windings. The dc bus over-voltage protection feature on the IC initiates zero vector braking when the dc bus voltage goes above some critical voltage level to prevent damage to dc bus components. Zero vector braking should only be used when the motor winding inductance is sufficient to limit the motor short circuit current to a safe level. Dc bus protection operates even when all PWM inputs are disabled so will protect the motor when operating in high speed field weakening mode.

The IRS26310D ICs have a DCbusSense input pin to detect over-voltage events on the DC bus. Once the IC detects an over-voltage event, zero vector mode braking is forced (all Low side output turn-on, all High side output-turn-off) overriding the PWM signals coming from the controller. A fault is not reported on the FAULT pin for this condition because the power inverter is still active. DC bus over-voltage protection is not latched and so the zero vector mode is released when DCbusSense pin is lower than $O_{VDCBUSVTH-}$.

The level of voltage at which the over-voltage protection is initiated is determined by the resistor divider (i.e., R_0 and R_1) connected to DCbusSense as shown in Figure 16, and the DCbusSense threshold ($O_{VDCBUSVTH+}$). The circuit designer will need to determine the maximum allowable level of DC bus voltage and select R_0 and R_1 such that the voltage at node V_X reaches the over-voltage threshold ($O_{VDCBUSVTH+}$).

$$O_{VDCBUSVTH+} = R_1 V_{DCBUS}/(R_0+R_1)$$

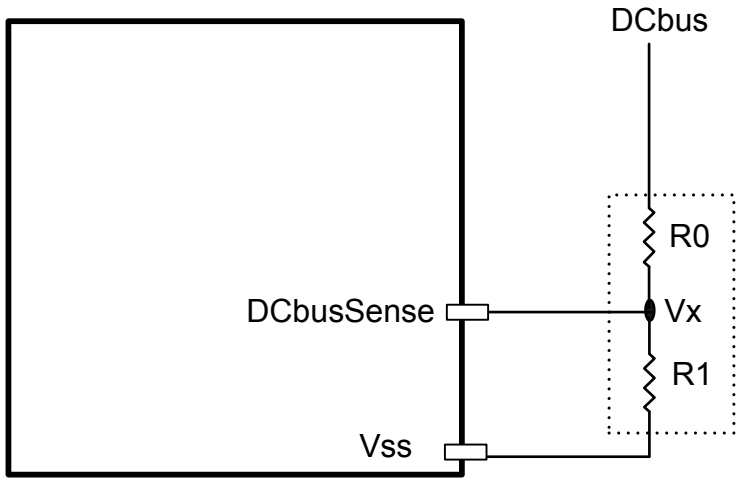


Figure 16: Programming the DC bus over-voltage protection

Truth Table: Undervoltage lockout, ITRIP, and ENABLE

Table 4 provides the truth table for the IRS26310D. The first line shows that the UVLO for V_{CC} has been tripped; the FAULT output has gone low and the gate drive outputs have been disabled. V_{CCUV} is not latched in this case and when V_{CC} is greater than V_{CCUV}, the FAULT output returns to the high impedance state. The second case shows that DCbus OV has been tripped and that the zero vector mode has been activated.

The third case shows that the UVLO for V_{BS} has been tripped and that the high-side gate drive output has been disabled. After V_{BS} exceeds the V_{BSUV} threshold, HO will stay low until the HVIC input receives a new or rising transition of HIN. The fourth case illustrates that the ITRIP trip threshold has been reached and that the gate drive outputs have been disabled and a fault has been reported through the fault pin (When ITRIP< V_{ITRIP} FAULT returns to High impedance after RCIN pin becomes greater than 8V). In the fifth case, the HVIC has received a command through the EN input to shutdown; as a result, the gate drive outputs have been disabled. The last case shows the normal operation of the HVIC (a shoot-through protection prevention logic prevent LO1,2,3 and HO1,2,3 for each channel turn on simultaneously).

	VCC	DCbus sense	VBS	ITRIP	EN	RCIN	FAULT	LO	HO
UVLO V_{CC}	$<V_{CCUV}$	---	---	---	---	High	0	0	0
DCbus OV	15 V	>OVdcbus	---	---	---	High	High Z	1	0
UVLO V_{BS}	15 V	<OVdcbus	$<V_{BSUV}$	0 V	5 V	High	High Z	LIN	0
ITRIP fault	15 V	<OVdcbus	15 V	$>V_{ITRIP}$	5 V	Low	0	0	0
EN command	15 V	<OVdcbus	15 V	0 V	0 V	High	High Z	0	0
Normal operation	15 V	<OVdcbus	15 V	0 V	5 V	High	High Z	LIN	HIN

Table 4: DCbus OV, UVLO, ITRIP, EN, RCIN, & FAULT truth table

Advanced Input Filter

The advanced input filter allows an improvement in the input/output pulse symmetry of the HVIC and helps to reject noise spikes and short pulses. This input filter has been applied to the HIN, LIN, and EN inputs. The working principle of the new filter is shown in Figures 17 and 18.

Figure 17 shows a typical input filter and the asymmetry of the input and output. The upper pair of waveforms (Example 1) show an input signal with a duration much longer then $t_{FIL,IN}$; the resulting output is approximately the difference between the input signal and $t_{FIL,IN}$. The lower pair of waveforms (Example 2) show an input signal with a duration slightly longer then $t_{FIL,IN}$; the resulting output is approximately the difference between the input signal and $t_{FIL,IN}$.

Figure 18 shows the advanced input filter and the symmetry between the input and output. The upper pair of waveforms (Example 1) show an input signal with a duration much longer then $t_{FIL,IN}$; the resulting output is approximately the same duration as the input signal. The lower pair of waveforms (Example 2) show an input signal with a duration slightly longer then $t_{FIL,IN}$; the resulting output is approximately the same duration as the input signal.

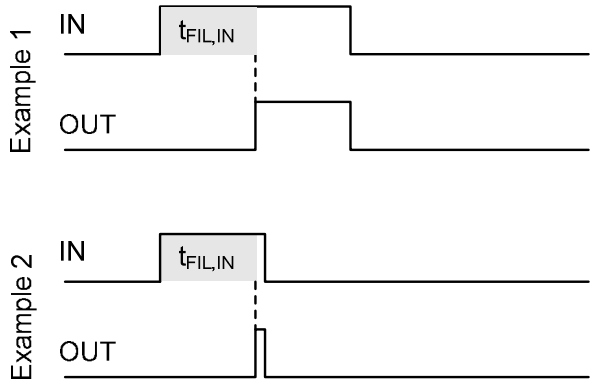


Figure 17: Typical input filter

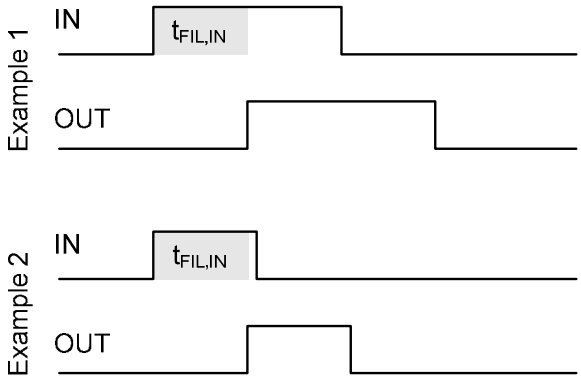


Figure 18: Advanced input filter

Short-Pulse / Noise Rejection

This device's input filter provides protection against short-pulses (e.g., noise) on the input lines. If the duration of the input signal is less than $t_{FIL,IN}$, the output will not change states. Example 1 of Figure 19 shows the input and output in the low state with positive noise spikes of durations less than $t_{FIL,IN}$; the output does not change states. Example 2 of Figure 19 shows the input and output in the high state with negative noise spikes of durations less than $t_{FIL,IN}$; the output does not change states.

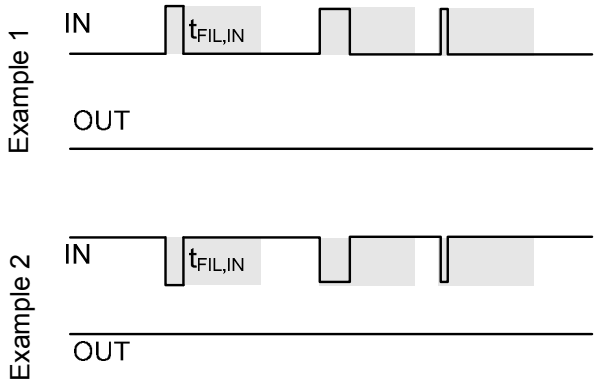


Figure 19: Noise rejecting input filters

Figures 20 and 21 present lab data that illustrates the characteristics of the input filters while receiving ON and OFF pulses.

The input filter characteristic is shown in Figure 20; the left side illustrates the narrow pulse ON (short positive pulse) characteristic while the left shows the narrow pulse OFF (short negative pulse) characteristic. The x-axis of Figure 20 shows the duration of PW_{IN}, while the y-axis shows the resulting PW_{OUT} duration. It can be seen that for a PW_{IN} duration less than $t_{FIL,IN}$, that the resulting PW_{OUT} duration is zero (e.g., the filter rejects the input signal/noise). We also see that once the PW_{IN} duration exceed $t_{FIL,IN}$, that the PW_{OUT} durations mimic the PW_{IN} durations very well over this interval with the symmetry improving as the duration increases. To ensure proper operation of the HVIC, it is suggested that the input pulse width for the high-side inputs be ≥ 500 ns.

The difference between the PW_{OUT} and PW_{IN} signals of both the narrow ON and narrow OFF cases is shown in Figure 21; the careful reader will note the scale of the y-axis. The x-axis of Figure 21 shows the duration of PW_{IN}, while the y-axis shows the resulting PW_{OUT}–PW_{IN} duration. This data illustrates the performance and near symmetry of this input filter.

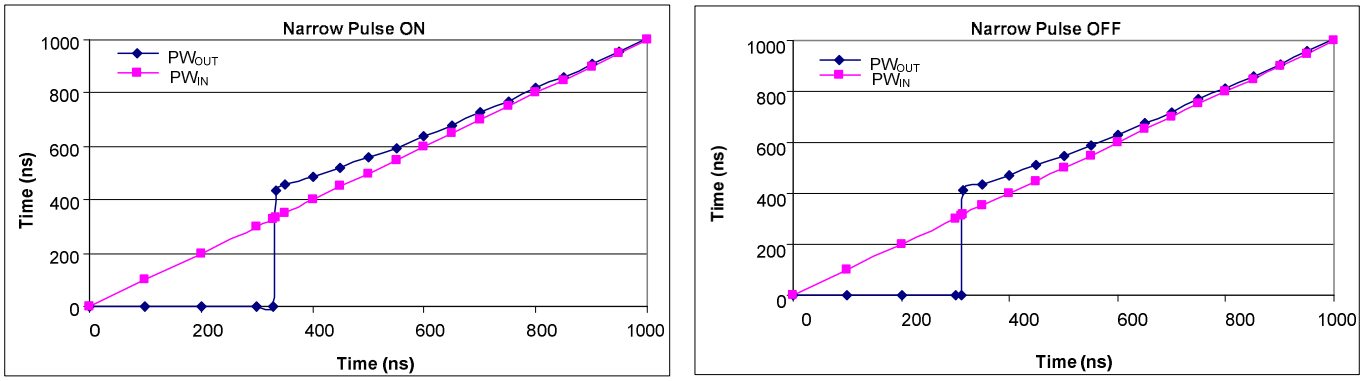


Figure 20: Input filter characteristic

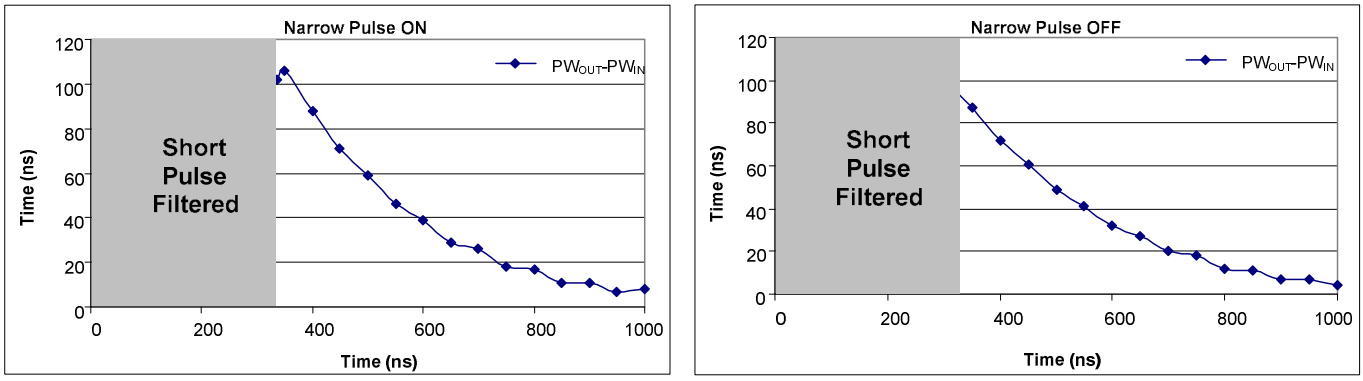


Figure 21: Difference between the input pulse and the output pulse

Integrated Bootstrap Functionality

The new IRS26310D family features integrated high-voltage bootstrap MOSFETs that eliminate the need of the external bootstrap diodes and resistors in many applications.

There is one bootstrap MOSFET for each high-side output channel and it is connected between the V_{CC} supply and its respective floating supply (i.e., V_{B1}, V_{B2}, V_{B3}); see Figure 22 for an illustration of this internal connection.

The integrated bootstrap MOSFET is turned on only during the time when LO is 'high', and it has a limited source current due to R_{BS}. The V_{BS} voltage will be charged each cycle depending on the on-time of LO and the value of the C_{BS} capacitor, the drain-source (collector-emitter) drop of the external IGBT (or MOSFET), and the low-side free-wheeling diode drop.

The bootstrap MOSFET of each channel follows the state of the respective low-side output stage (i.e., the bootstrap MOSFET is ON when LO is high, it is OFF when LO is low), unless the V_B voltage is higher than approximately 110% of V_{CC}. In that case, the bootstrap MOSFET is designed to remain off until V_B returns below that threshold; this concept is illustrated in Figure 23.

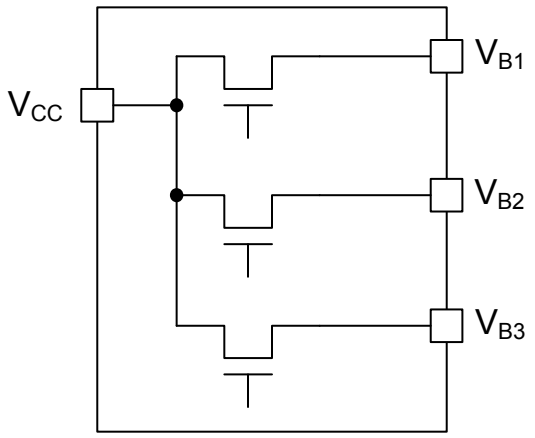


Figure 22: Internal bootstrap MOSFET connection

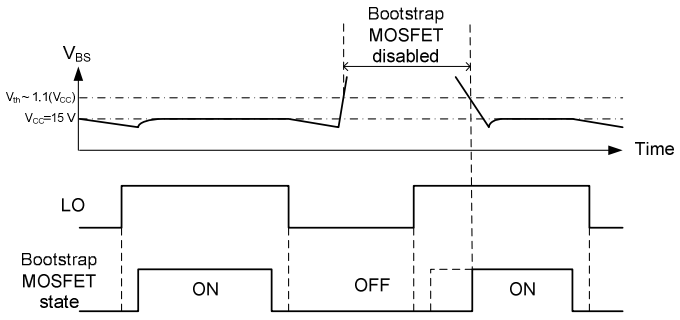


Figure 23: Bootstrap MOSFET state diagram

A bootstrap MOSFET is suitable for most of the PWM modulation schemes and can be used either in parallel with the external bootstrap network (i.e., diode and resistor) or as a replacement of it. The use of the integrated bootstrap as a replacement of the external bootstrap network may have some limitations. An example of this limitation may arise when this functionality is used in non-complementary PWM schemes (typically 6-step modulations) and at very high

PWM duty cycle. In these cases, superior performances can be achieved by using an external bootstrap diode in parallel with the internal bootstrap network.

Bootstrap Power Supply Design

For information related to the design of the bootstrap power supply while using the integrated bootstrap functionality of the IRS26310, please refer to Application Note 1123 (AN-1123) entitled "Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality." This application note is available at www.irf.com.

For information related to the design of a standard bootstrap power supply (i.e., using an external discrete diode) please refer to Design Tip 04-4 (DT04-4) entitled "Using Monolithic High Voltage Gate Drivers." This design tip is available at www.irf.com.

Separate Logic and Power Grounds

The IRS26310D has separate logic and power ground pin (V_{SS} and COM respectively) to eliminate some of the noise problems that can occur in power conversion applications. Current sensing shunts are commonly used in many applications for power inverter protection (i.e., over-current protection), and in the case of motor drive applications, for motor current measurements. In these situations, it is often beneficial to separate the logic and power grounds.

Figure 24 shows a HVIC with separate V_{SS} and COM pins and how these two grounds are used in the system. The V_{SS} is used as the reference point for the logic and over-current circuitry; V_X in the figure is the voltage between the ITRIP pin and the V_{SS} pin. Alternatively, the COM pin is the reference point for the low-side gate drive circuitry. The output voltage used to drive the low-side gate is V_{LO}-COM; the gate-emitter voltage (V_{GE}) of the low-side switch is the output voltage of the driver minus the drop across $R_{G,LO}$.

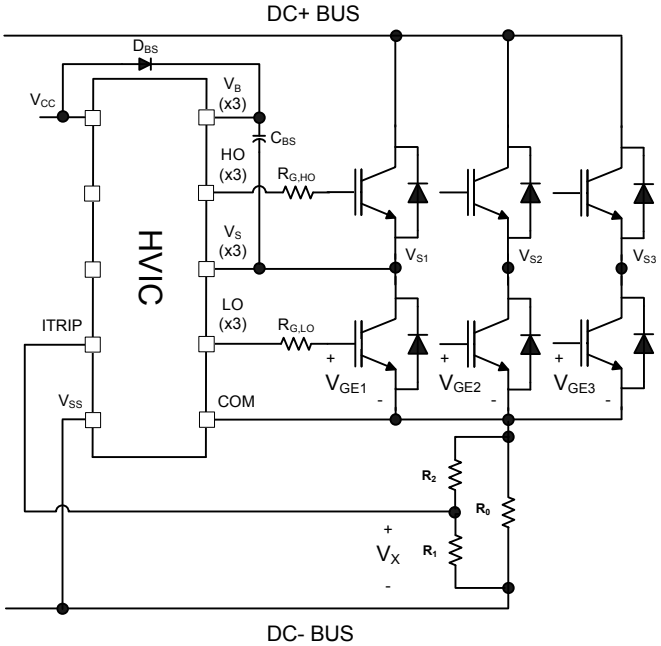


Figure 24: Separate V_{SS} and COM pins

Tolerant to Negative V_S Transients

A common problem in today's high-power switching converters is the transient response of the switch node's voltage as the power switches transition on and off quickly while carrying a large current. A typical 3-phase inverter circuit is shown in Figure 25; here we define the power switches and diodes of the inverter.

If the high-side switch (e.g., the IGBT Q1 in Figures 26 and 27) switches off, while the U phase current is flowing to an inductive load, a current commutation occurs from high-side switch (Q1) to the diode (D2) in parallel with the low-side switch of the same inverter leg. At the same instance, the voltage node V_{S1}, swings from the positive DC bus voltage to the negative DC bus voltage.

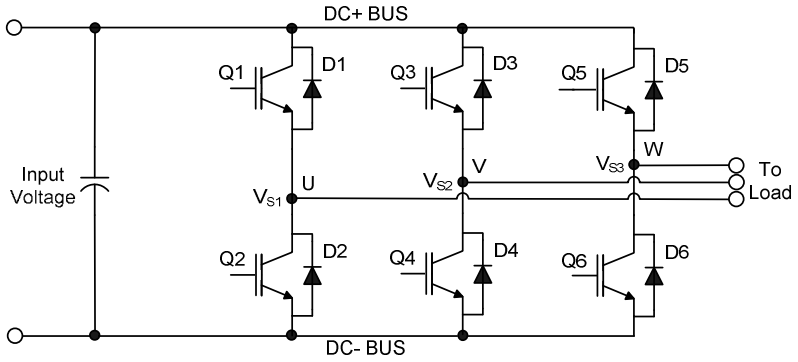


Figure 25: Three phase inverter

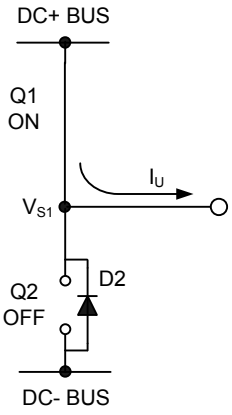


Figure 26: Q1 conducting

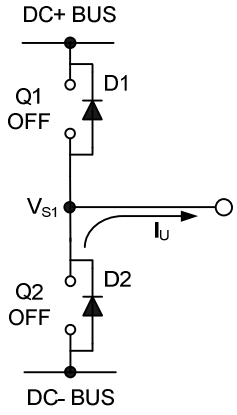


Figure 27: D2 conducting

Also when the V phase current flows from the inductive load back to the inverter (see Figures 28 and 29), and Q4 IGBT switches on, the current commutation occurs from D3 to Q4. At the same instance, the voltage node, V_{S2}, swings from the positive DC bus voltage to the negative DC bus voltage.

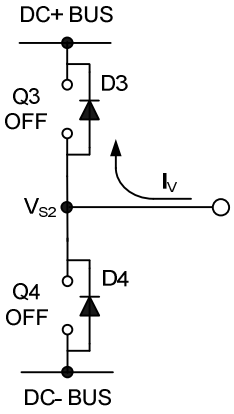


Figure 28: D3 conducting

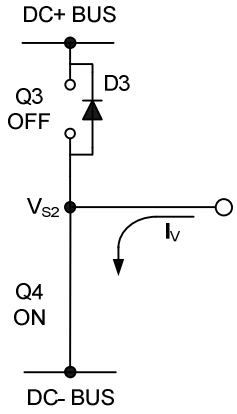


Figure 29: Q4 conducting

However, in a real inverter circuit, the V_S voltage swing does not stop at the level of the negative DC bus, rather it swings below the level of the negative DC bus. This undershoot voltage is called "negative V_S transient".

The circuit shown in Figure 30 depicts one leg of the three phase inverter; Figures 31 and 32 show a simplified illustration of the commutation of the current between Q1 and D2. The parasitic inductances in the power circuit from the die bonding to the PCB tracks are lumped together in L_C and L_E for each IGBT. When the high-side switch is on, V_{S1} is below the DC+ voltage by the voltage drops associated with the power switch and the parasitic elements of the circuit. When the high-side power switch turns off, the load current momentarily flows in the low-side freewheeling diode due to the inductive load connected to V_{S1} (the load is not shown in these figures). This current flows from the DC- bus (which is connected to the COM pin of the HVIC) to the load and a negative voltage between V_{S1} and the DC- Bus is induced (i.e., the COM pin of the HVIC is at a higher potential than the V_S pin).

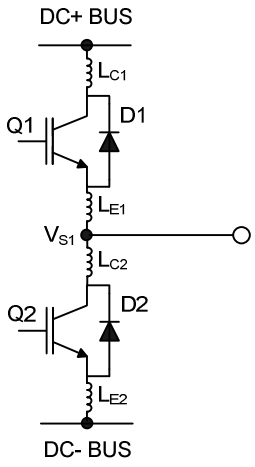


Figure 30: Parasitic Elements

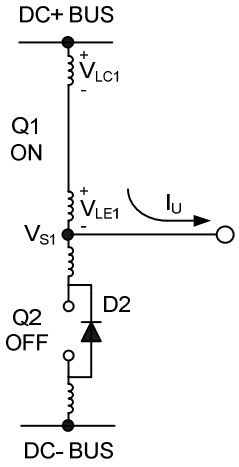


Figure 31: V_S positive

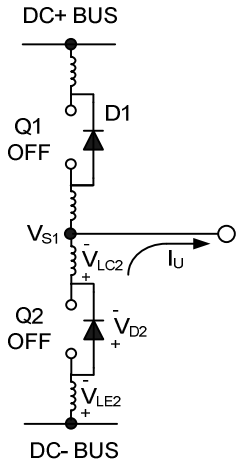


Figure 32: V_S negative

In a typical motor drive system, dV/dt is typically designed to be in the range of 3-5 V/ns. The negative V_S transient voltage can exceed this range during some events such as short circuit and over-current shutdown, when di/dt is greater than in normal operation.

International Rectifier's HVICs have been designed for the robustness required in many of today's demanding applications. The IRS26310D has been seen to withstand large negative V_S transient conditions on the order of -50 V for a period of 50 ns. An illustration of the IRS26310D's performance can be seen in Figure 33. This experiment was conducted using various loads to create this condition; the curve shown in this figure illustrates the successful operation of the IRS26310D under these stressful conditions.

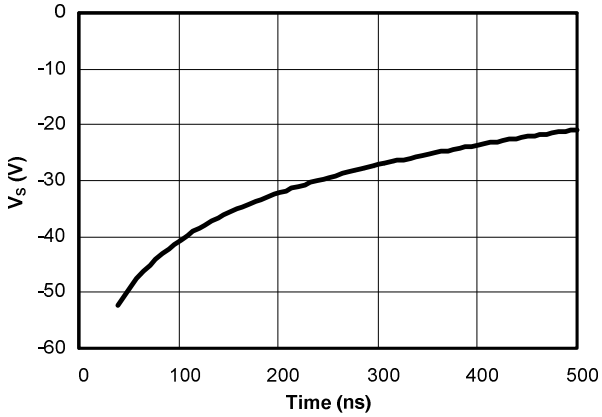


Figure 33: Negative V_S transient results for an International Rectifier HVIC

Even though the IRS26310D has been shown able to handle these large negative V_S transient conditions, it is highly recommended that the circuit designer always limit the negative V_S transients as much as possible by careful PCB layout and component use.

PCB Layout Tips

Distance between high and low voltage components: It's strongly recommended to place the components tied to the floating voltage pins (V_B and V_S) near the respective high voltage portions of the device. The IRS26310D in the PLCC44 package has had some unused pins removed in order to maximize the distance between the high voltage and low voltage pins. Please see the Case Outline PLCC44 information in this datasheet for the details.

Ground Plane: In order to minimize noise coupling, the ground plane should not be placed under or near the high voltage floating side.

Gate Drive Loops: Current loops behave like antennas and are able to receive and transmit EM noise (see Figure 34). In order to reduce the EM coupling and improve the power switch turn on/off performance, the gate drive loops must be reduced as much as possible. Moreover, current can be injected inside the gate drive loop via the IGBT collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes to developing a voltage across the gate-emitter, thus increasing the possibility of a self turn-on effect.

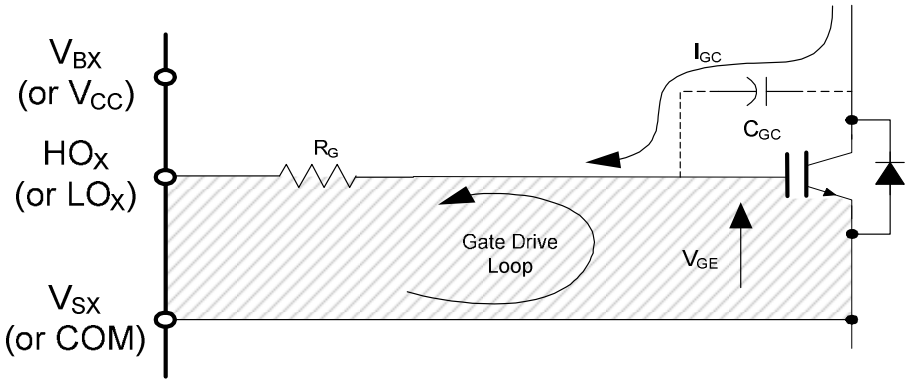


Figure 34: Antenna Loops

Supply Capacitor: It is recommended to place a bypass capacitor (C_{IN}) between the V_{CC} and V_{SS} pins. This connection is shown in Figure 35. A ceramic 1 µF ceramic capacitor is suitable for most applications. This component should be placed as close as possible to the pins in order to reduce parasitic elements.

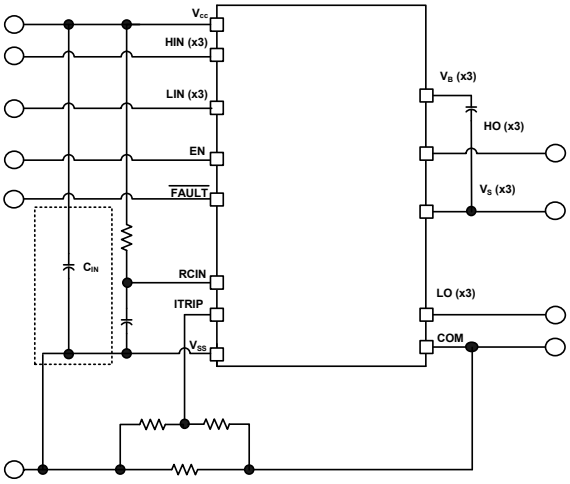


Figure 35: Supply capacitor

Routing and Placement: Power stage PCB parasitic elements can contribute to large negative voltage transients at the switch node; it is recommended to limit the phase voltage negative transients. In order to avoid such conditions, it is recommended to 1) minimize the high-side emitter to low-side collector distance, and 2) minimize the low-side emitter to negative bus rail stray inductance. However, where negative V_S spikes remain excessive, further steps may be taken to reduce the spike. This includes placing a resistor (5 Ω or less) between the V_S pin and the switch node (see Figure 36), and in some cases using a clamping diode between V_{SS} and V_S (see Figure 37). See DT04-4 at www.irf.com for more detailed information.

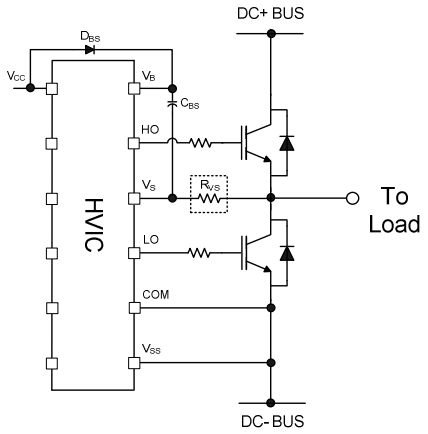


Figure 36: V_S resistor

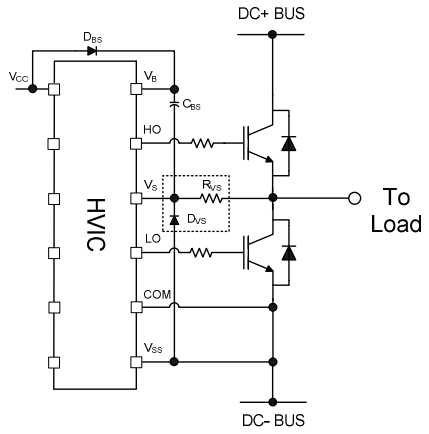


Figure 37: V_S clamping diode

Integrated Bootstrap FET limitation

The integrated Bootstrap FET functionality has an operational limitation under the following bias conditions applied to the HVIC:

- **VCC pin voltage = 0V AND**
- **VS or VB pin voltage > 0**

In the absence of a VCC bias, the integrated bootstrap FET voltage blocking capability is compromised and a current conduction path is created between VCC & VB pins, as illustrated in Fig.38 below, resulting in power loss and possible damage to the HVIC.

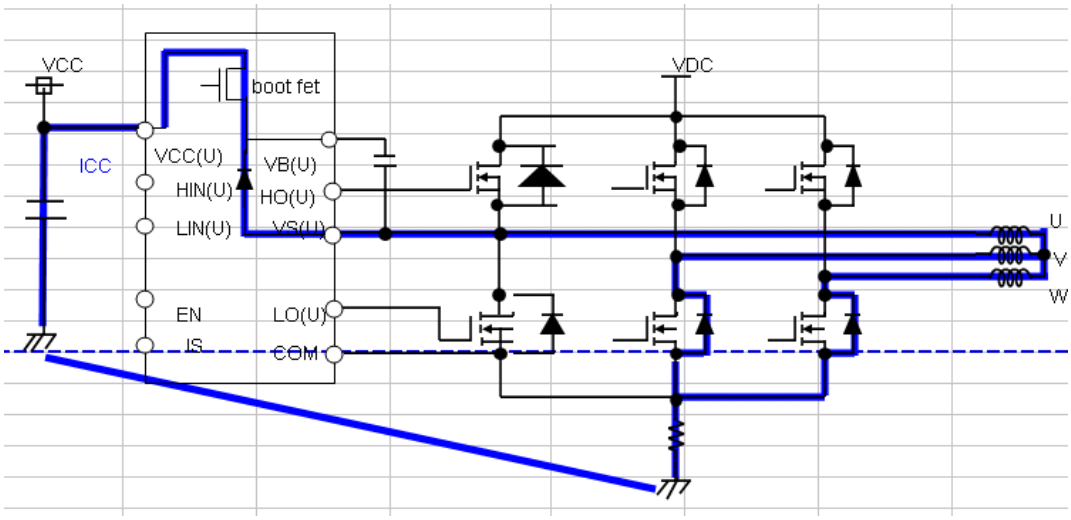


Figure 38: Current conduction path between VCC and VB pin

Relevant Application Situations:

The above mentioned bias condition may be encountered under the following situations:

- In a motor control application, a permanent magnet motor naturally rotating while VCC power is OFF. In this condition, Back EMF is generated at a motor terminal which causes high voltage bias on VS nodes resulting unwanted current flow to VCC.
- Potential situations in other applications where VS/VB node voltage potential increases before the VCC voltage is available (for example due to sequencing delays in SMPS supplying VCC bias)

Application Workaround:

Insertion of a standard p-n junction diode between VCC pin of IC and positive terminal of VCC capacitors (as illustrated in Fig.39) prevents current conduction “out-of” VCC pin of gate driver IC. It is important not to connect the VCC capacitor directly to pin of IC. Diode selection is based on 25V rating or above & current capability aligned to ICC consumption of IC - 100mA should cover most application situations. As an example, Part number # LL4154 from Diodes Inc (25V/150mA standard diode) can be used.

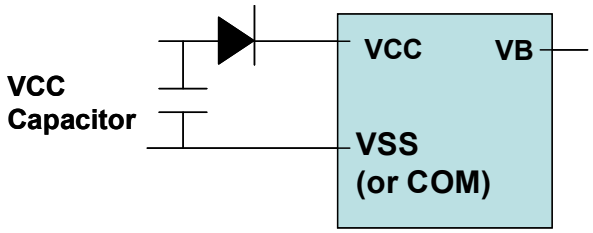


Figure 39: Diode insertion between VCC pin and VCC capacitor

Note that the forward voltage drop on the diode (V_F) must be taken into account when biasing the VCC pin of the IC to meet UVLO requirements. *VCC pin Bias = VCC Supply Voltage – V_F of Diode*.

Additional Documentation

Several technical documents related to the use of HVICs are available at www.irf.com; use the Site Search function and the document number to quickly locate them. Below is a short list of some of these documents.

DT97-3: Managing Transients in Control IC Driven Power Stages
AN-1123: Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality
DT04-4: Using Monolithic High Voltage Gate Drivers
AN-978: HV Floating MOS-Gate Driver ICs

Parameter Temperature Trends

Figures 40-60 provide information on the experimental performance of the IRS26310D HVIC. The line plotted in each figure is generated from actual lab data. A small number of individual samples were tested at three temperatures (-40 ºC, 25 ºC, and 125 ºC) in order to generate the experimental (Exp.) curve. The line labeled Exp. consist of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood temperature trend. The individual data points on the curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).

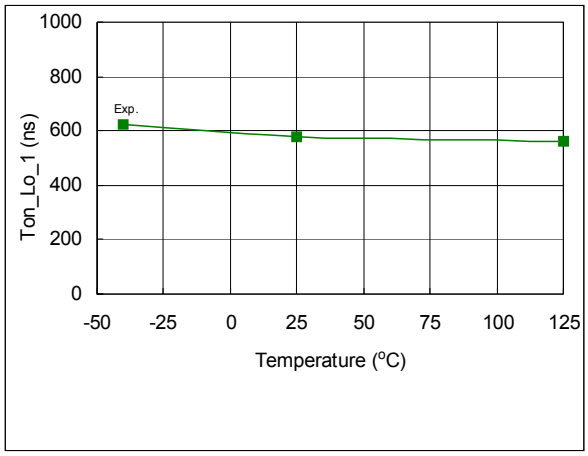


Figure 40: t_{ON} vs. temperature

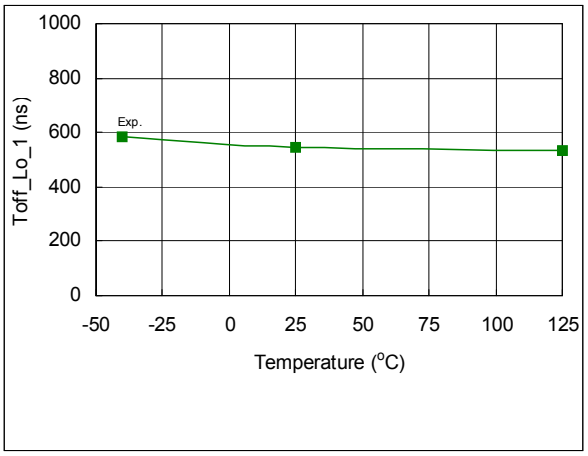


Figure 41: t_{OFF} vs. temperature

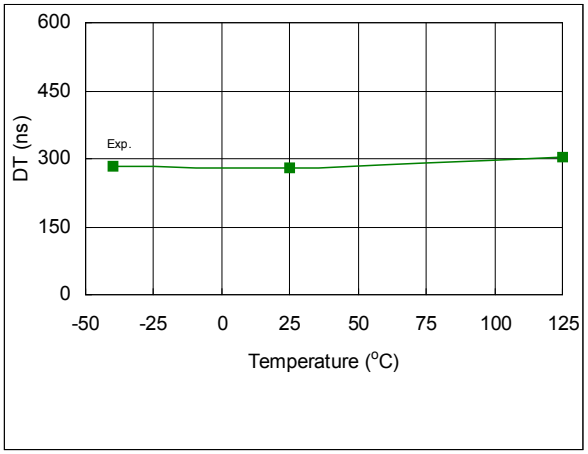


Figure 42: DT vs. temperature

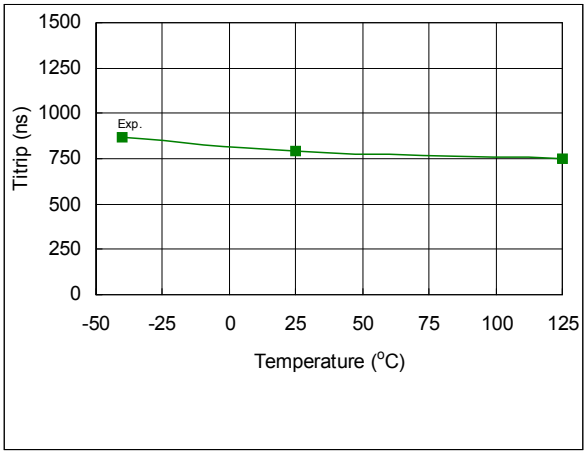


Figure 43: t_{ITRIP} vs. temperature

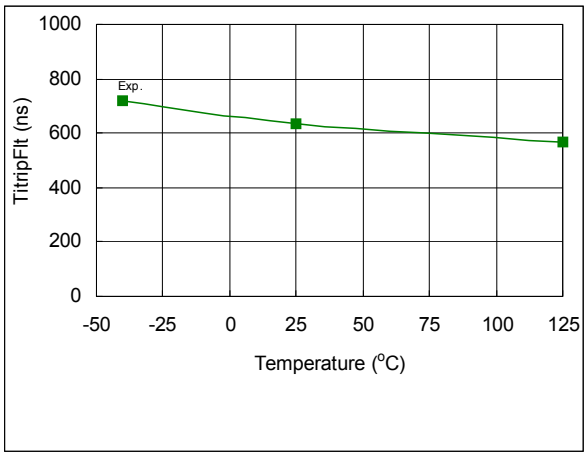


Figure 44: t_{FLT} vs. temperature

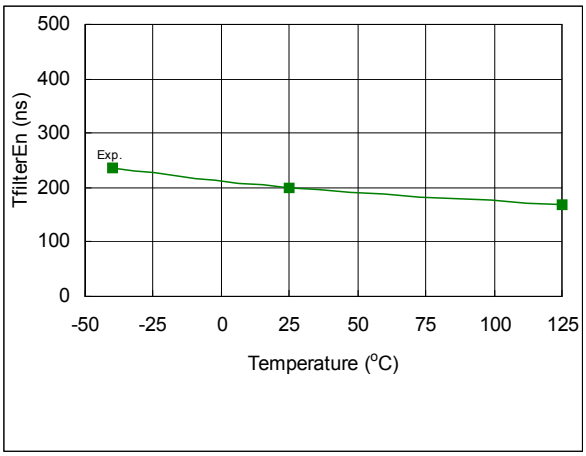


Figure 45 t_{EN} vs. temperature

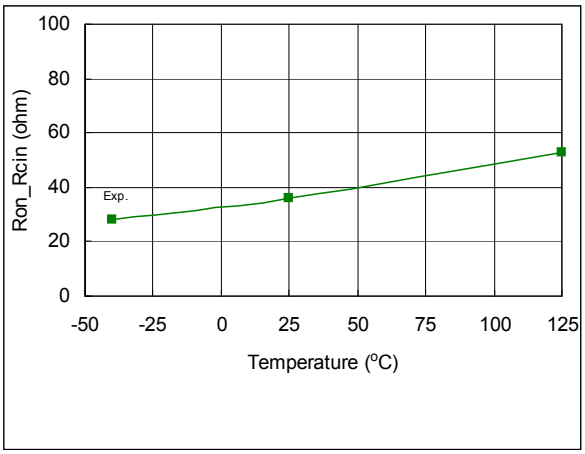


Figure 46: $R_{ON,RCIN}$ vs. temperature

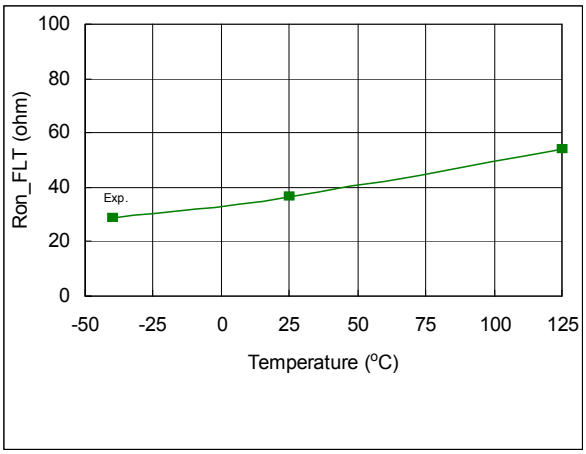


Figure 47: $R_{ON,FLT}$ vs. temperature

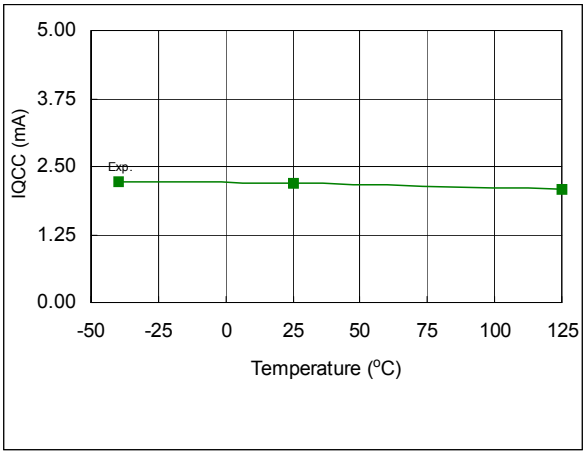


Figure 48: I_{QCC} vs. temperature

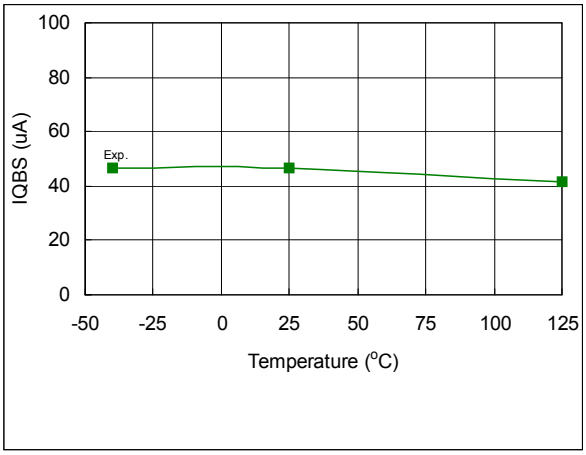


Figure 49: I_{QBS} vs. temperature

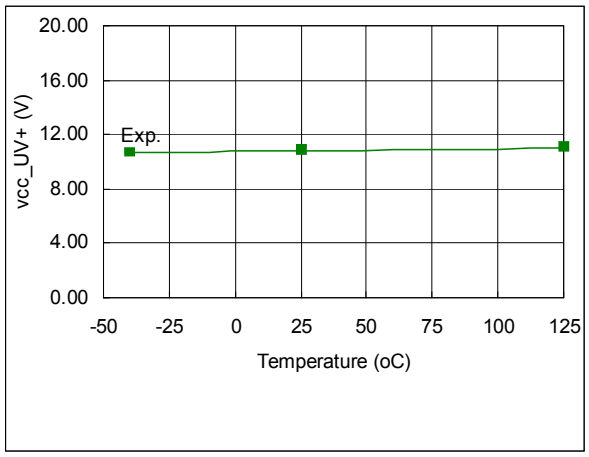


Figure 50: V_{CCUV+} vs. temperature

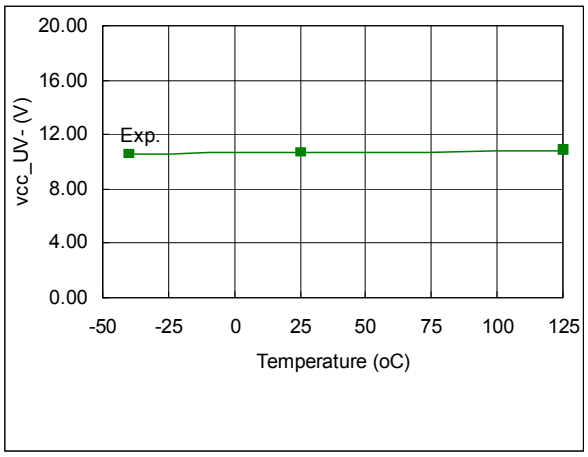


Figure 51: V_{CCUV-} vs. temperature

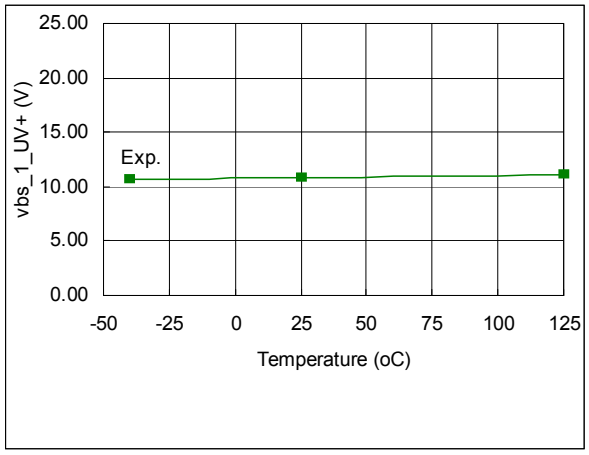


Figure 52: V_{BSUV+} vs. temperature

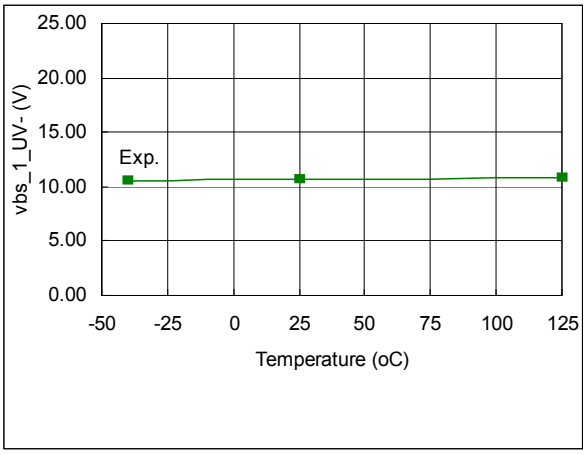


Figure 53: V_{BSUV-} vs. temperature

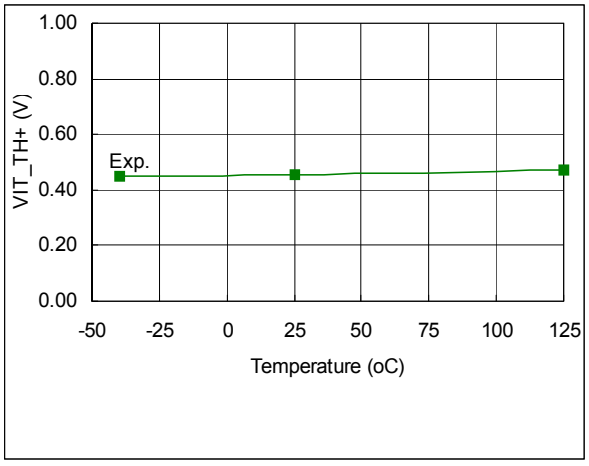


Figure 54: $V_{IT,TH+}$ vs. temperature

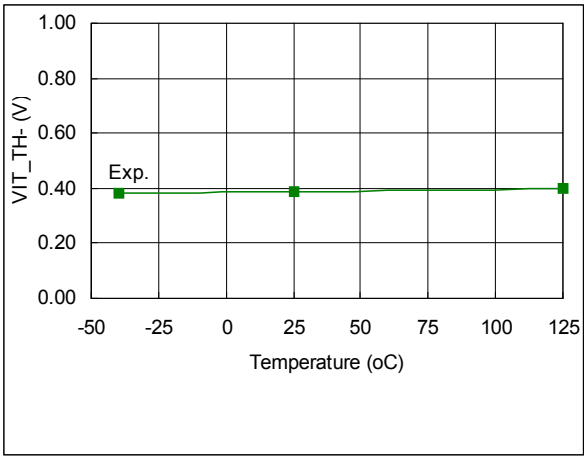


Figure 55: $V_{IT,TH-}$ vs. temperature

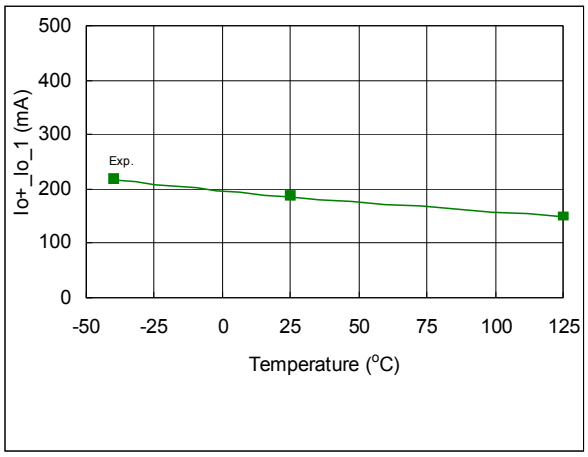


Figure 56: I_{O+} vs. temperature

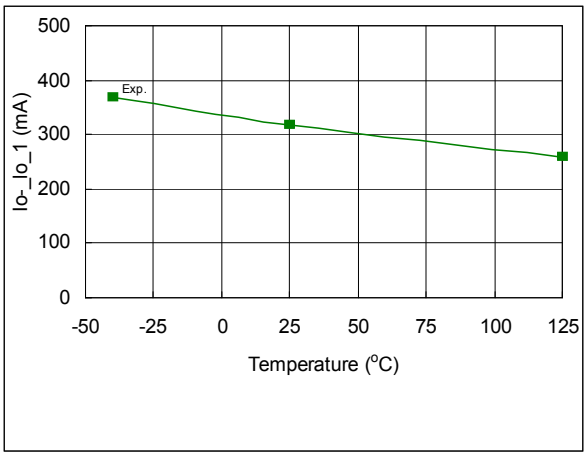


Figure 57: I_{O-} vs. temperature

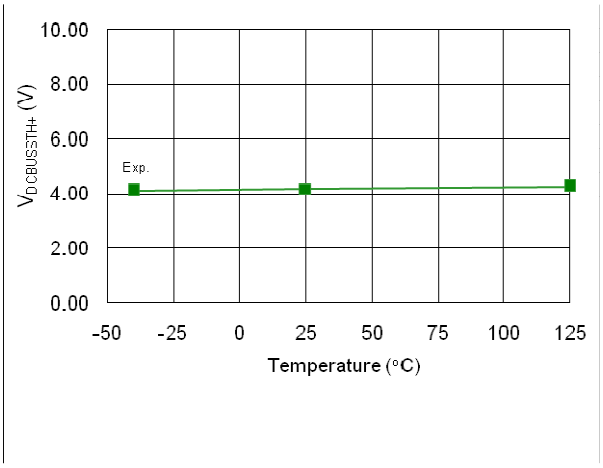


Figure 58: $V_{DCBUSSTH+}$ vs. temperature

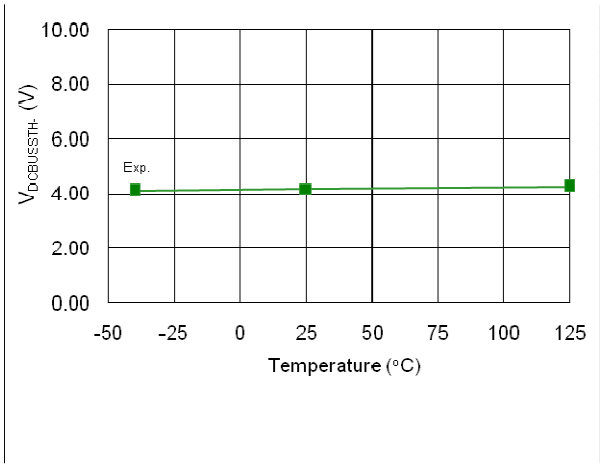


Figure 59: $V_{DCBUSSTH-}$ vs. temperature

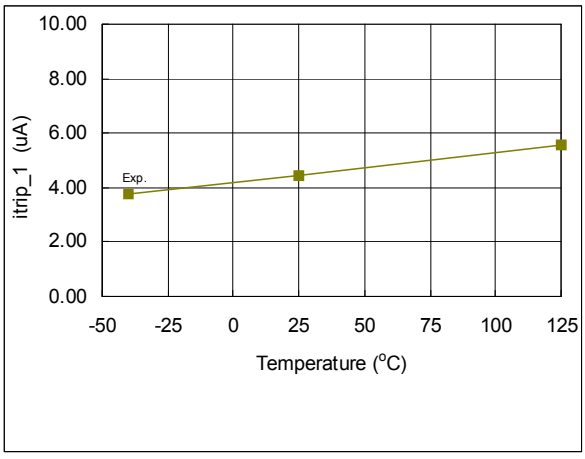
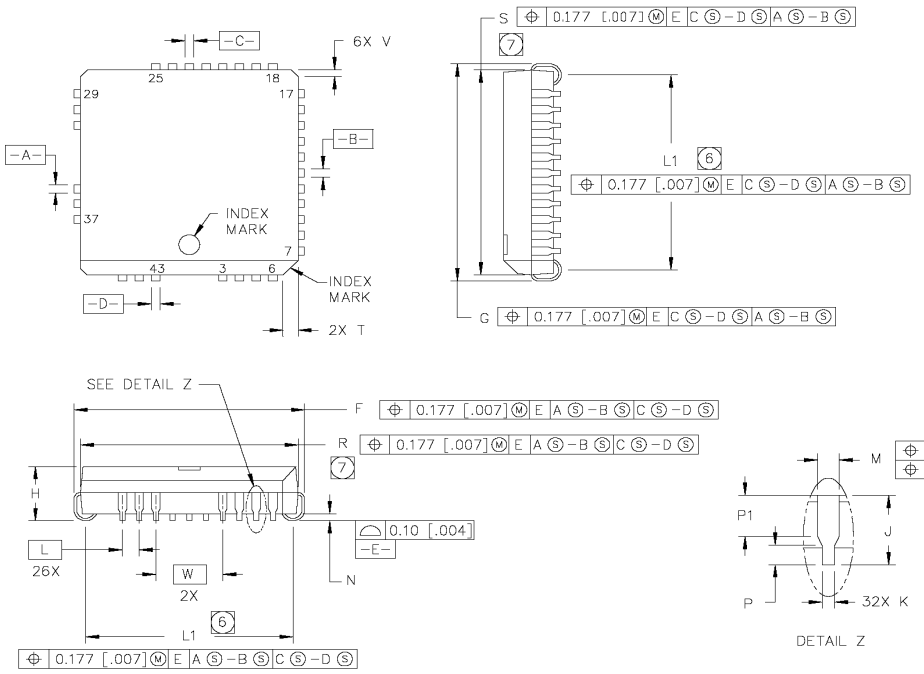


Figure 60: I_{ITRIP+} vs. temperature

Package Details: PLCC44



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F	17.40	17.65	.685	.695
G	17.40	17.65	.685	.695
H	4.20	4.57	.165	.180
J	2.29	3.04	.090	.120
K	0.33	0.48	.013	.019
L	1.27 BSC		.050 BSC	
M	0.66	0.81	.026	.032
N	0.51	——	.020	——
P	0.64	——	.025	——
R	16.51	16.66	.650	.656
S	16.51	16.66	.650	.656
T	1.07	1.21	.042	.048
V	——	0.50	——	.020
W	5.08 BSC		.200 BSC	
L1	15.50	16.00	.610	.630
P1	1.53	——	.060	——

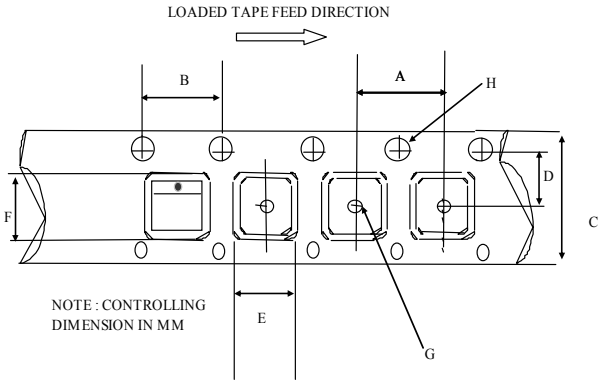
NOTES

1. DIMENSIONING & TOLERENCING PER ANSI Y14.5M–1982.
2. DIMENSIONS SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE MS–018AC.
5. DATUMS –A–, –B–, –C–, & –D– ARE DETERMINED BY WHERE THE TOP OF THE LEADS EXIT PLASTIC BODY AT MOLD PARTING LINE.
6. TO BE MEASURED AT –E– SEATING PLANE.
7. DIMENSIONS DO NOT INCLUDE MOLD FLASH, ALLOWABLE FLASH IS 0.254 [.010].

44-Lead PLCC w/o 12 leads

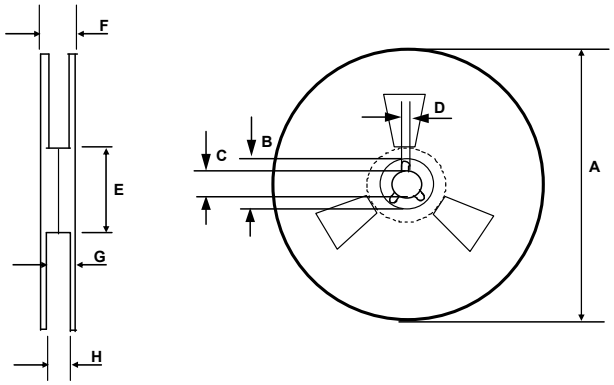
01-6009 00
01-3004 02(mod.) (MS-018AC)

Tape and Reel Details: PLCC44



CARRIER TAPE DIMENSION FOR 44PLCC

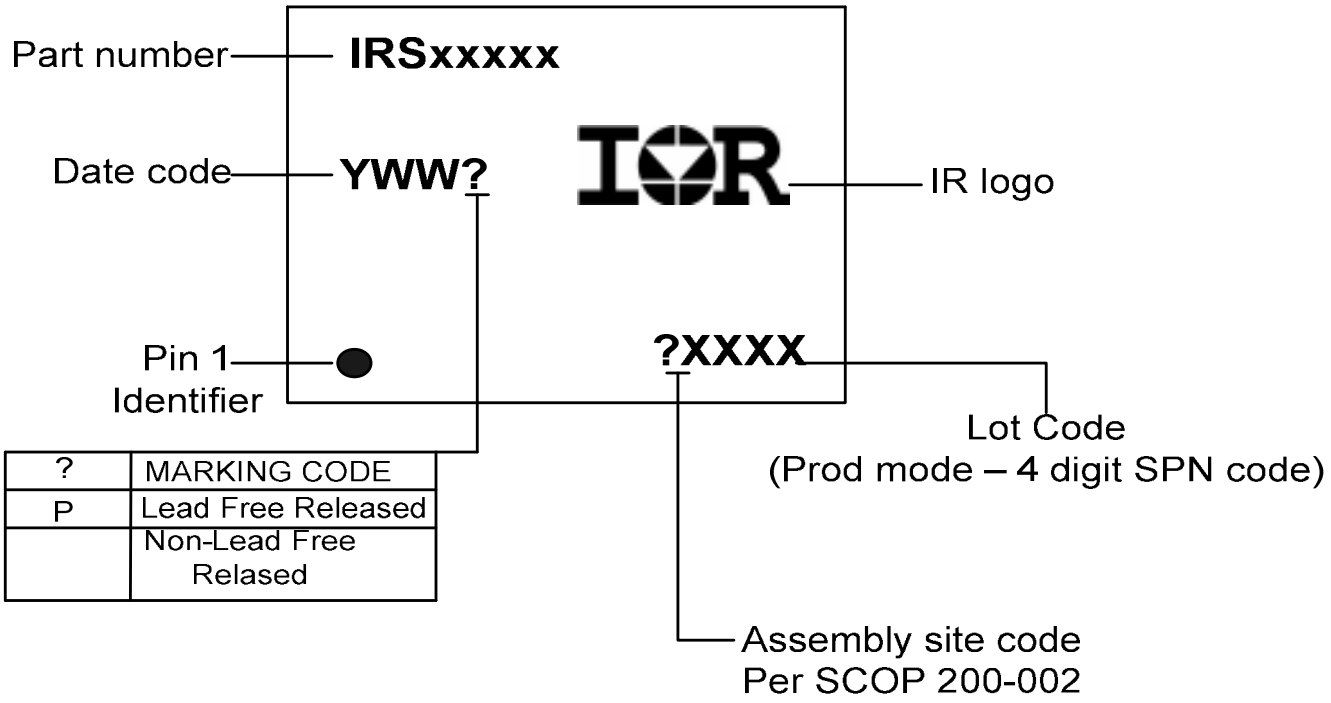
Code	Metric		Imperial	
	Min	Max	Min	Max
A	23.90	24.10	0.94	0.948
B	3.90	4.10	0.153	0.161
C	31.70	32.30	1.248	1.271
D	14.10	14.30	0.555	0.562
E	17.90	18.10	0.704	0.712
F	17.90	18.10	0.704	0.712
G	2.00	n/a	0.078	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 44PLCC

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	38.4	n/a	1.511
G	34.7	35.8	1.366	1.409
H	32.6	33.1	1.283	1.303

Part Marking Information



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Relased

Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRS26310D	PLCC44	Tube/Bulk	27	IRS26310DJPBF
		Tape and Reel	500	IRS26310DJTRPBF

For technical support, please contact IR's Technical Assistance Center
http://www.irf.com/technical-info/

WORLD HEADQUARTERS:
233 Kansas St., El Segundo, California 90245
Tel: (310) 252-7105

Revision History

Revision	Date	Change comments
1.6	04-17-08	Corrected unit for deadtime from “uS” to “nS”
1.7	04-18-08	Updated Qualification information table per new IR standard
1.8	06-01-11	Add bootstrap FET limitation