MMFT2N02EL

Preferred Device

Power MOSFET
2 Amps, 20 Volts
N–Channel SOT–223

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. This device is also designed with a low threshold voltage so it is fully enhanced with 5 Volts. This new energy efficient device also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, dc–dc converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients. The device is housed in the SOT–223 package which is designed for medium power surface mount applications.

- Silicon Gate for Fast Switching Speeds
- Low Drive Requirement to Interface Power Loads to Logic Level ICs, $V_{GS(th)}$ = 2 Volts Max
- The SOT–223 Package can be Soldered Using Wave or Reflow. The Formed Leads Absorb Thermal Stress During Soldering, Eliminating the Possibility of Damage to the Die

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DS}	20	Vdc
Gate–to–Source Voltage – Continuous	V_{GS}	±15	Vdc
Drain Current – Continuous – Pulsed	I_D I_{DM}	1.6 6.4	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D (Note 1.)	0.8 6.4	Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–65 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy – Starting T_J = 25°C (V_{DD} = 10 V, V_{GS} = 5 V, Peak I_L = 2 A, L = 0.2 mH, R_G = 25 Ω)	E_{AS}	66	mJ

THERMAL CHARACTERISTICS

Thermal Resistance – Junction–to–Ambient (surface mounted)	$R_{\theta JA}$	156	°C/W
Maximum Temperature for Soldering Purposes, Time in Solder Bath	T_L	260 10	°C Sec

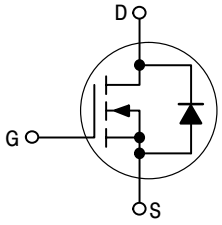
1. Power rating when mounted on FR–4 glass epoxy printed circuit board using recommended footprint.

ON Semiconductor™

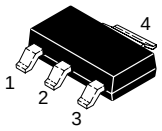
http://onsemi.com

2 AMPERES
20 VOLTS
$R_{DS(on)}$ = 150 mΩ

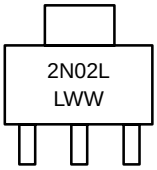
N–Channel



MARKING DIAGRAM

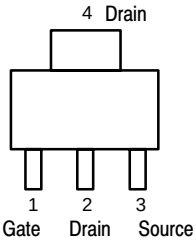


TO–261AA
CASE 318E
STYLE 3



L = Location Code
WW = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
MMFT2N02ELT1	SOT–223	1000 Tape & Reel

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage, (V_{GS} = 0, I_D = 250 μA)		$V_{(BR)DSS}$	20	–	–	Vdc
Zero Gate Voltage Drain Current, (V_{DS} = 20 V, V_{GS} = 0)		I_{DSS}	–	–	10	μAdc
Gate–Body Leakage Current, (V_{GS} = 15 V, V_{DS} = 0)		I_{GSS}	–	–	100	nAdc
ON CHARACTERISTICS						
Gate Threshold Voltage, (V_{DS} = V_{GS}, I_D = 1 mA)		$V_{GS(th)}$	1	–	2	Vdc
Static Drain–to–Source On–Resistance, (V_{GS} = 5 V, I_D = 0.8 A)		$R_{DS(on)}$	–	–	0.15	Ohms
Drain–to–Source On–Voltage, (V_{GS} = 5 V, I_D = 1.6 A)		$V_{DS(on)}$	–	–	0.32	Vdc
Forward Transconductance, (V_{DS} = 10 V, I_D = 0.8 A)		g_{FS}	–	2.6	–	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 15 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	–	580	–	pF
Output Capacitance		C_{oss}	–	430	–	
Reverse Transfer Capacitance		C_{rss}	–	250	–	
SWITCHING CHARACTERISTICS						
Turn–On Delay Time	(V_{DD} = 15 V, I_D = 1.6 A V_{GS} = 5 V, R_G = 50 ohms, R_{GS} = 25 ohms)	$t_{d(on)}$	–	16	–	ns
Rise Time		t_r	–	73	–	
Turn–Off Delay Time		$t_{d(off)}$	–	77	–	
Fall Time		t_f	–	107	–	
Total Gate Charge	(V_{DS} = 16 V, I_D = 1.6 A, V_{GS} = 5 Vdc) See Figures 15 and 16	Q_g	–	20	–	nC
Gate–Source Charge		Q_{gs}	–	1.7	–	
Gate–Drain Charge		Q_{gd}	–	6	–	
SOURCE DRAIN DIODE CHARACTERISTICS (Note 2.)						
Forward On–Voltage	I_S = 1.6 A, V_{GS} = 0	V_{SD}	–	0.9	–	Vdc
Forward Turn–On Time	I_S = 1.6 A, V_{GS} = 0, dI_S/dt = 400 A/μs, V_R = 16 V	t_{on}	Limited by stray inductance			
Reverse Recovery Time		t_{rr}	–	55	–	ns

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%

TYPICAL ELECTRICAL CHARACTERISTICS

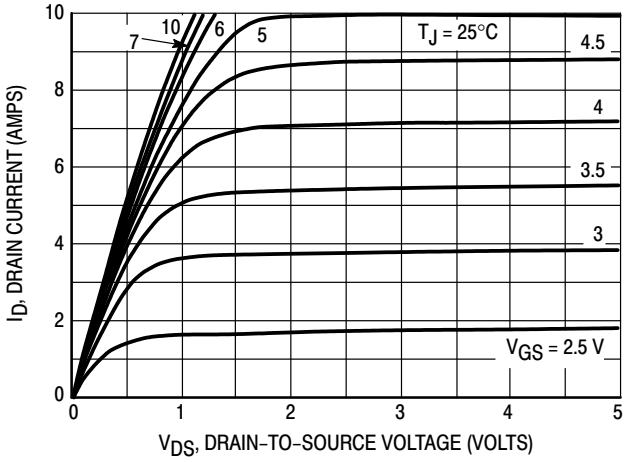


Figure 1. On Region Characteristics

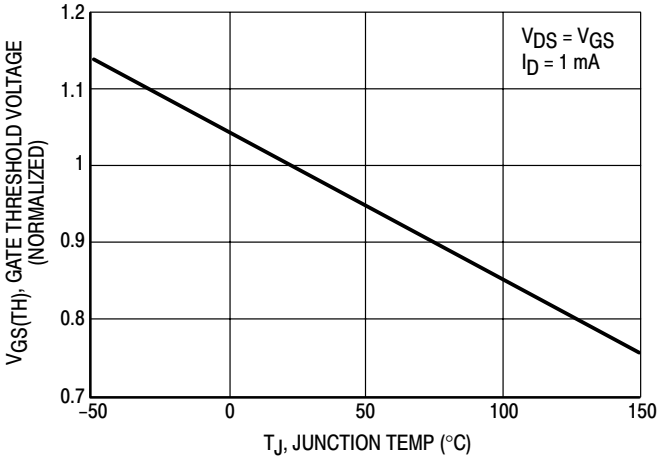


Figure 2. Gate−Threshold Voltage Variation With Temperature

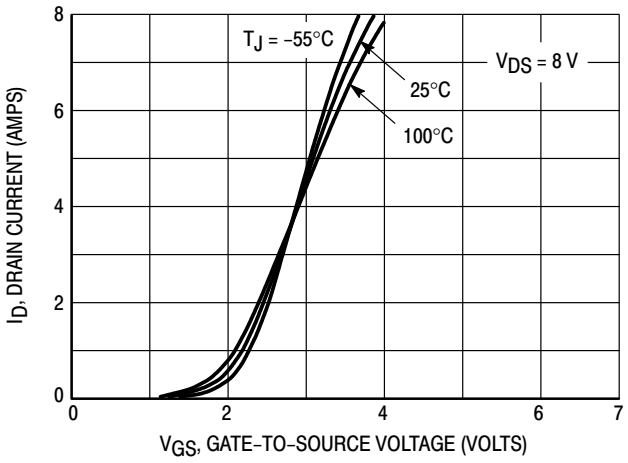


Figure 3. Transfer Characteristics

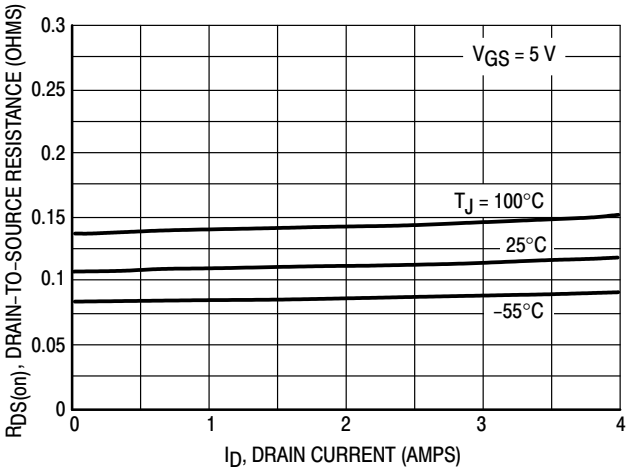


Figure 4. On−Resistance versus Drain Current

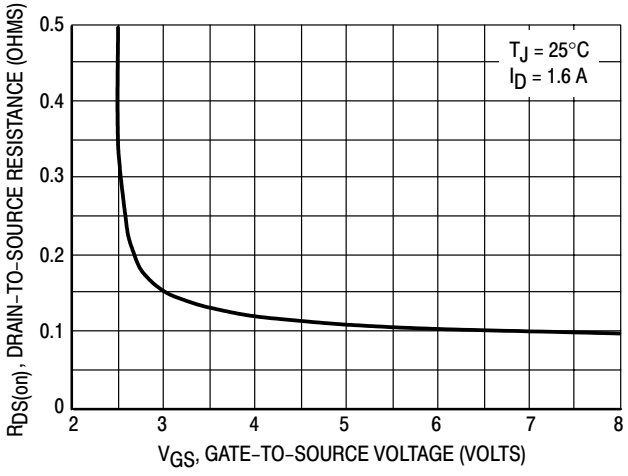


Figure 5. On−Resistance versus Gate−to−Source Voltage

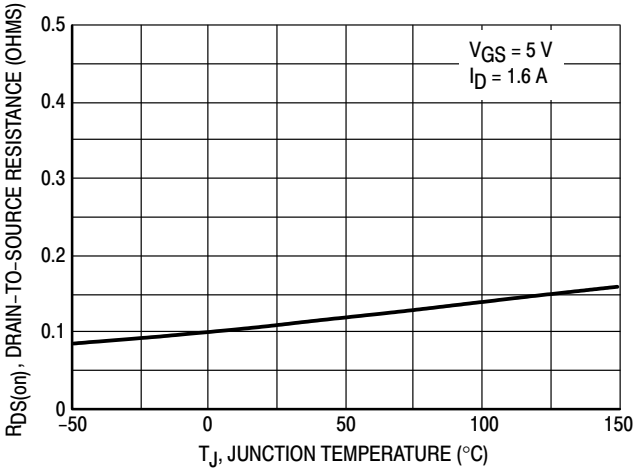


Figure 6. On−Resistance versus Junction Temperature

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain–to–source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on an ambient temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various ambient temperatures can be determined by using the thermal response curves. ON Semiconductor Application Note, AN569, “Transient Thermal Resistance–General Data and Its Use” provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, BV_{DSS}. The switching SOA is applicable for both turn–on and turn–off of the devices for switching times less than one microsecond.

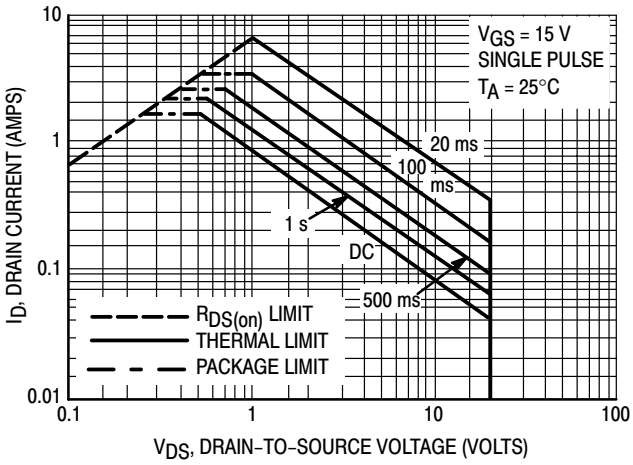


Figure 7. Maximum Rated Forward Biased Safe Operating Area

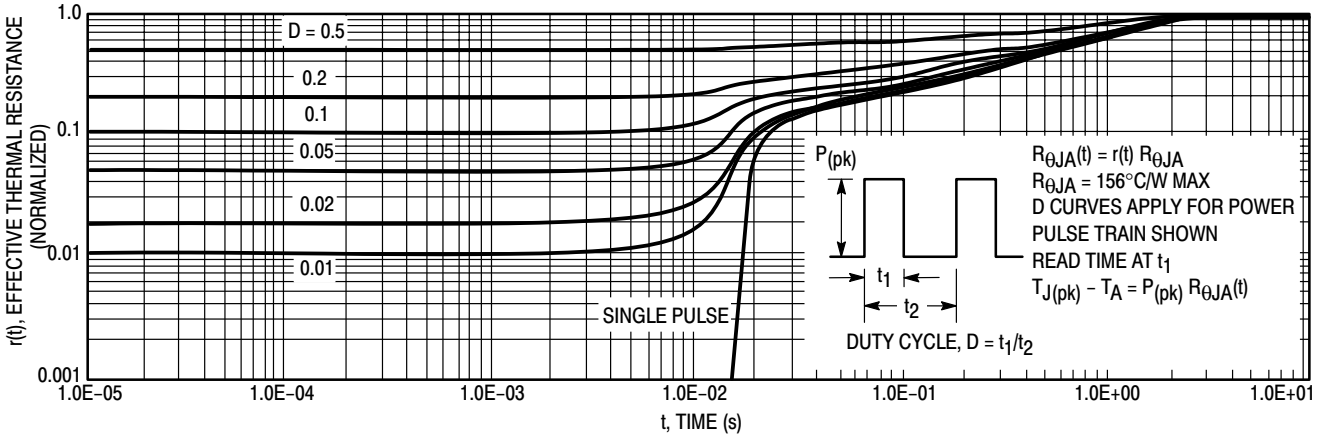


Figure 8. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 10 defines the limits of safe operation for commutated source–drain current versus re–applied drain voltage when the source–drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 9 are present. Full or half–bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so dI_S/dt is specified with a maximum value. Higher values of dI_S/dt require an appropriate derating of I_{FM}, peak V_{DS} or both. Ultimately dI_S/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain–to–source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source–drain diode current just prior to the onset of commutation.

V_R is specified at 80% rated BV_{DSS} to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in ON Semiconductor’s test circuit are assumed to be practical minimums. dVDS/dt in excess of 10 V/ns was attained with dI_S/dt of 400 A/μs.

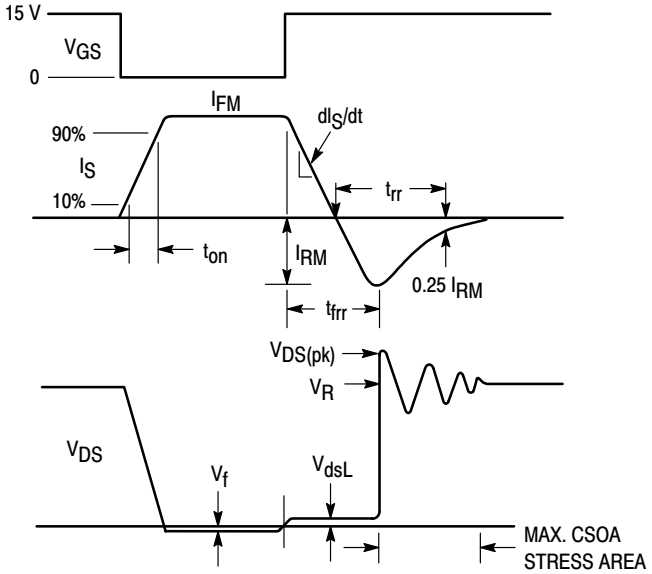


Figure 9. Commutating Waveforms

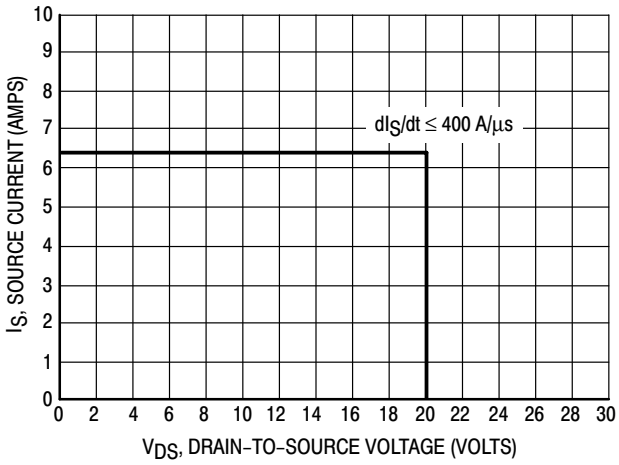


Figure 10. Commutating Safe Operating Area (CSOA)

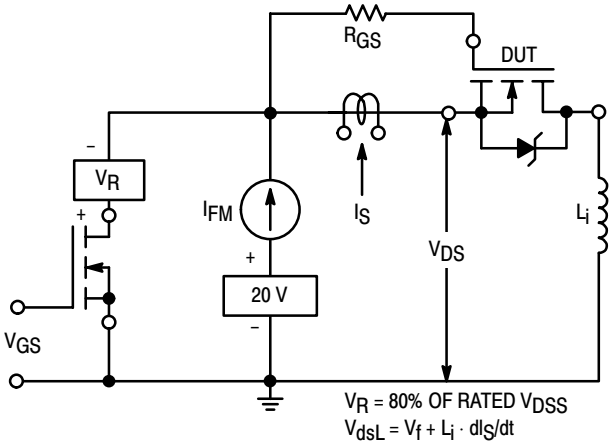


Figure 11. Commutating Safe Operating Area Test Circuit

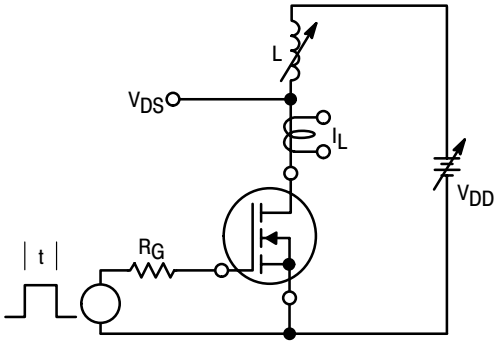


Figure 12. Unclamped Inductive Switching Test Circuit

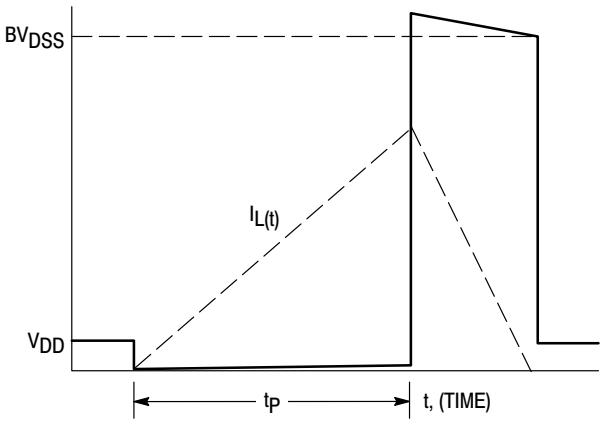


Figure 13. Unclamped Inductive Switching Waveforms

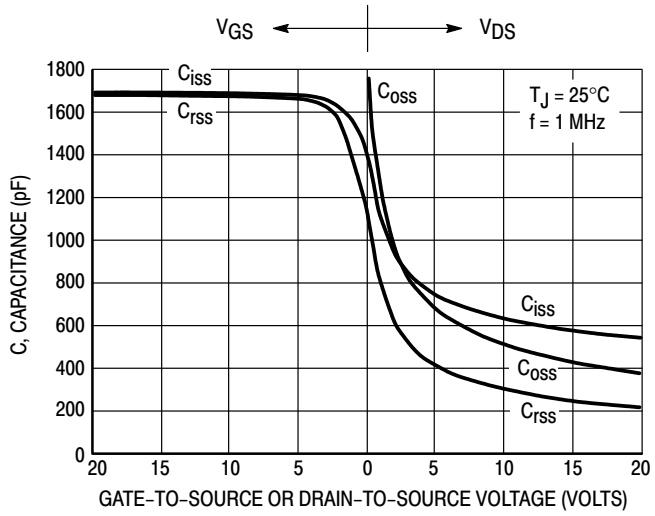


Figure 14. Capacitance Variation With Voltage

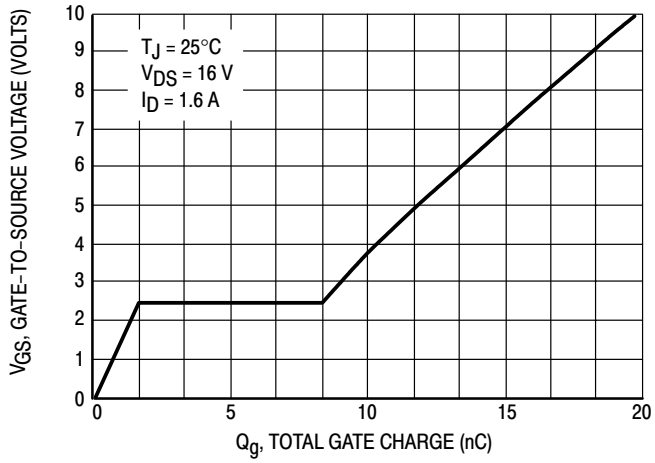
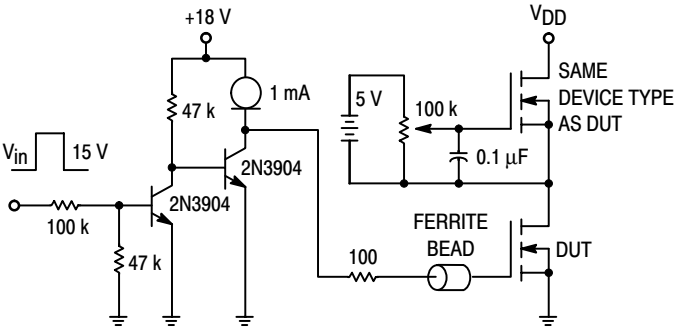


Figure 15. Gate Charge versus Gate–To–Source Voltage



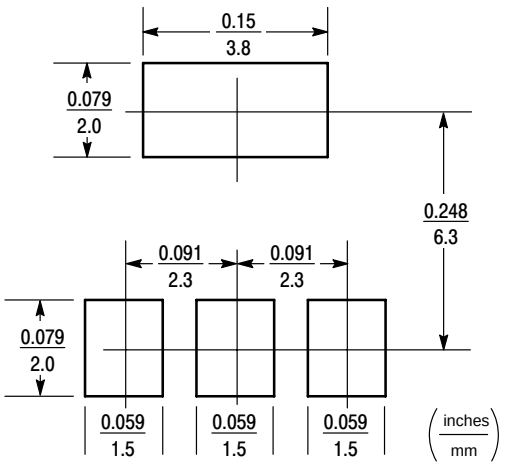
V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%.

Figure 16. Gate Charge Test Circuit

INFORMATION FOR USING THE SOT–223 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT–223 POWER DISSIPATION

The power dissipation of the SOT–223 is a function of the drain pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet for the SOT–223 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 800 milliwatts.

$$P_D = \frac{150°C - 25°C}{156°C/W} = 800 \text{ milliwatts}$$

The 156°C/W for the SOT–223 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 800 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–223 package. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. A graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 17.

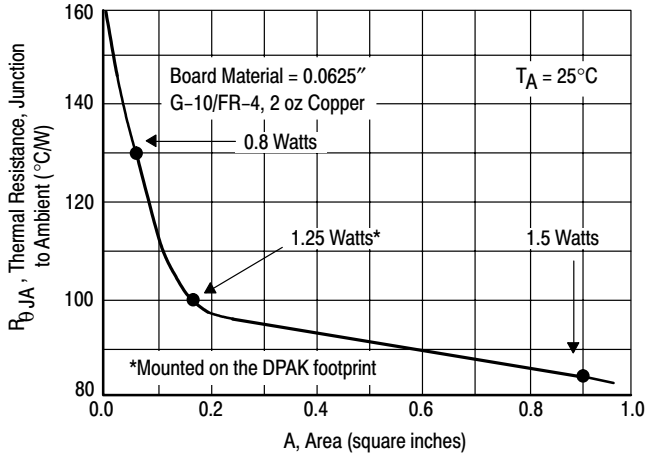


Figure 17. Thermal Resistance versus Drain Pad Area for the SOT–223 Package (Typical)

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. A solder stencil is required to screen the optimum amount of solder paste onto the footprint. The stencil is made of brass or stainless steel with a typical thickness of 0.008 inches. The stencil opening size for the SOT–223 package should be the same as the pad size on the printed circuit board, i.e., a 1:1 registration.

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 18 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

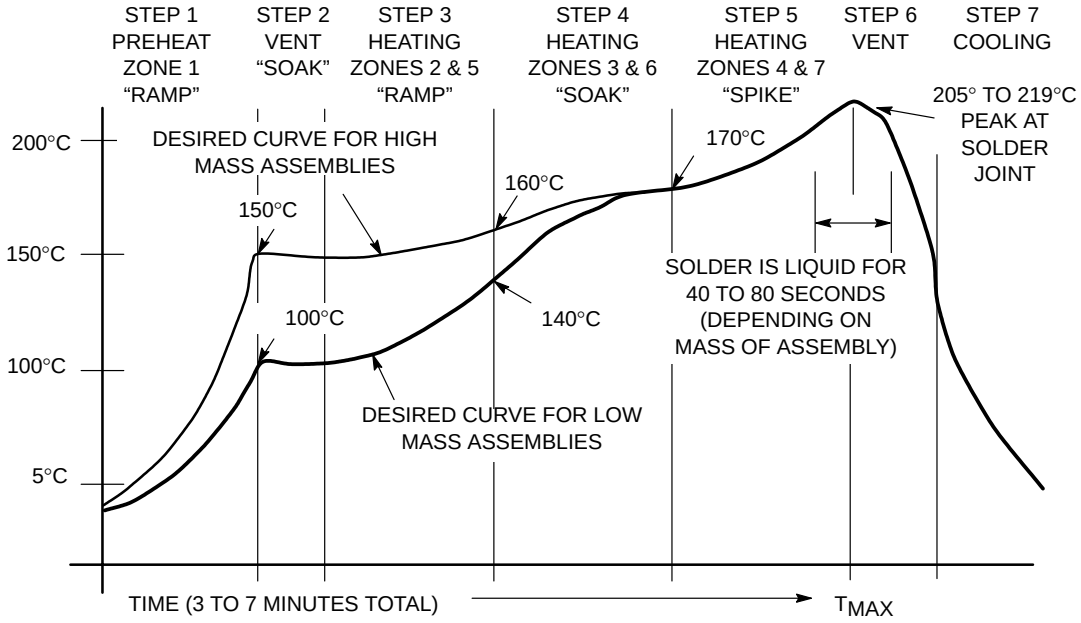
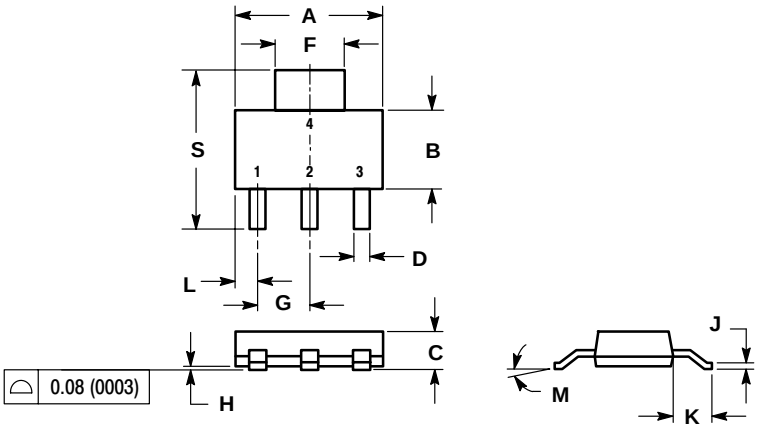


Figure 18. Typical Solder Heating Profile

PACKAGE DIMENSIONS

SOT–223 (TO–261)
CASE 318E–04
ISSUE K



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.249	0.263	6.30	6.70
B	0.130	0.145	3.30	3.70
C	0.060	0.068	1.50	1.75
D	0.024	0.035	0.60	0.89
F	0.115	0.126	2.90	3.20
G	0.087	0.094	2.20	2.40
H	0.0008	0.0040	0.020	0.100
J	0.009	0.014	0.24	0.35
K	0.060	0.078	1.50	2.00
L	0.033	0.041	0.85	1.05
M	0 °	10 °	0 °	10 °
S	0.264	0.287	6.70	7.30

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

Notes

Thermal Clad is a registered trademark of the Bergquist Company.

PUBLICATION ORDERING INFORMATION

NORTH AMERICA Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com
Fax Response Line: 303–675–2167 or 800–344–3810 Toll Free USA/Canada

N. American Technical Support: 800–282–9855 Toll Free USA/Canada

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ON Semiconductor Website: http://onsemi.com

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